



TaichuPix-3 test

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Flex test overview

Effect of power voltage

Digital power voltage: 1.75 V-1.95 V

Effect of readout CLK frequency

> 20 MHz, 15.625 MHz

Effect of interposer board

All tests performed with 2-layer flex





Performance with different power setup



- > OCT success rate = number of valid output/ number of sample times
- > OCT bit error rate = number of error pixel address/number of data



Note: Success rate (>80%) is larger than the one in previous tests (~10%), reason was not understood well

Increasing power voltage does not benefit the success rate/error rate

Performance with different readout frequency

FlexV1p3-F: chip U7 test in the OCT mode



Decreasing readout frequency benefit the success rate/error rate

Effect of different readout frequency



- > Minimum ITHR=96 for readout clk of 20 MHz/15.625 MHz
- > NO 'ghost' spot with readout clk 15.625 MHz for different ITHR



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2-layer flex test results

FlexV1p3-H: chip U10 & U9

- > Minimum ITHR: 64 for U10, 96 for U9
- Laser test for both of U10 & U9:
 - 'ghost' spot observed with readout clk of 20 MHz, efficiency less than 100%
 - No 'ghost' spot with readout clk of 15.625 MHz, efficiency ~100%



Effect of interposer board



- The interposer board has obvious effect on the noise level of chip
 - > Different minimum ITHR obtained for chip U7 with different interposer boards
 - Interposer v1: minimum ITHR =96 (clk 20M/15.625M)
 - Interposer v2 No.1: minimum ITHR =160 (clk 20M/15.625M)
 - Interposer v2 No.2: minimum ITHR =224 (clk 20MHz), ITHR=96 (clk 15.625MHz)



Summary



- Preliminary results indicate chip closer to the power socket has lower noise → lower threshold can be set
- No 'ghost' spot and count lost observed on the 2-layer flex when decrease the readout frequency to be 15.625 MHz

Next step:

- > Test multiple chips working on the same ladder
- > Test different chip with worse power supply on the same flex
 - Chip U5/6 needed to be bonded on FlexV1p3-H and FlexV1p4-A