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TaichuPix-3 test

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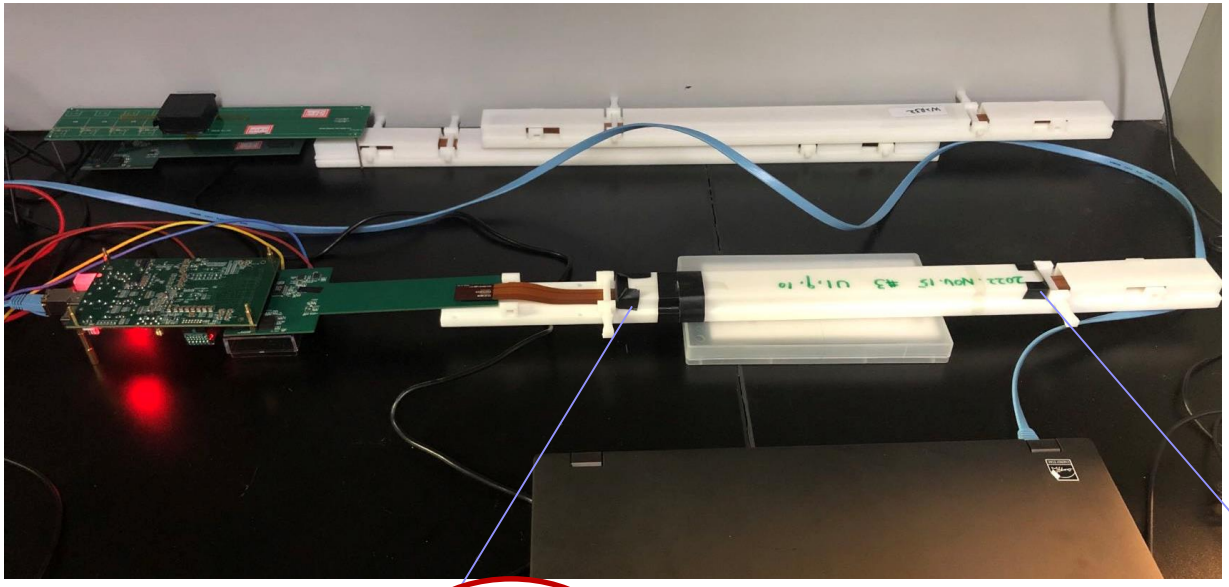
Flex test overview

- **Tests of the 2-layer flex with two chips working simultaneously**
  - Config both U10 & U9, analog power changed before&after, digital power do not

- **Test of the 4-layer flex with two chips working simultaneously**

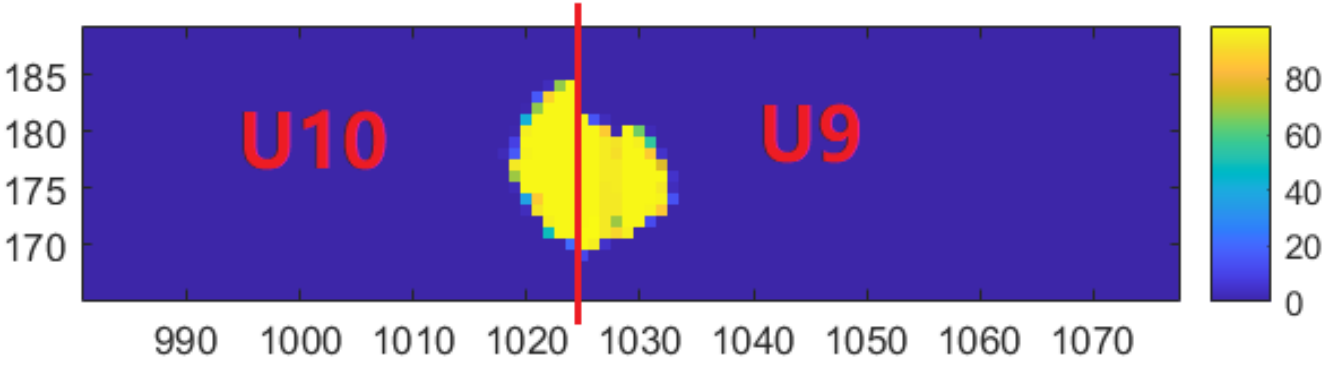


U10	**U9**	U8	**U7**	U6	U5	**U4**	U3	U2	**U1**

2-layer flex test result

- **FlexV1p3-H: chip U10 & U9**
  - Config U9/U10 respectively: minimum ITHR is 64 for U9/U10 (no power current overload)
  - Config U9 and U10 simultaneously, minimum ITHR is 128 → noise increased
  - Laser test: U9 and U10 can work simultaneously, NO error code/cross-talk found

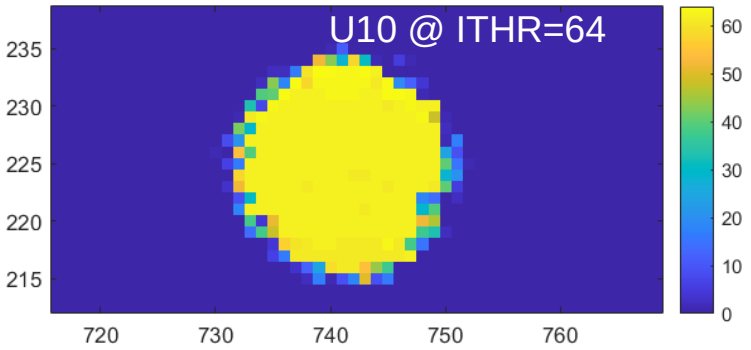
Gap between two chips NOT shown

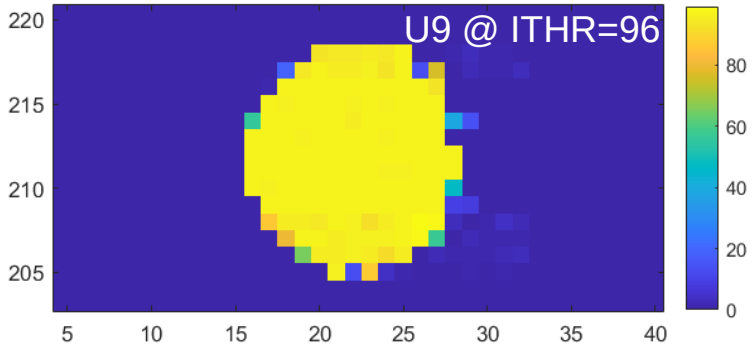


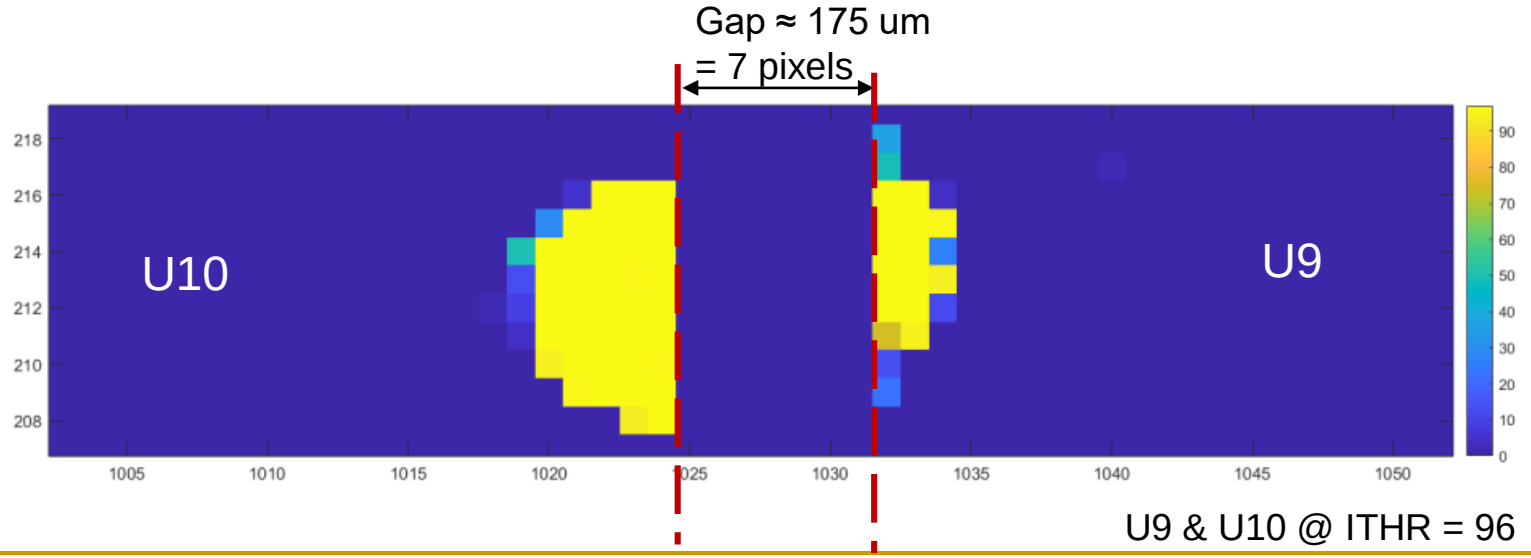
U9 & U10 @ ITHR= 128

4-layer flex test result

- **FlexV1p4-B: chip U10 & U9**
  - Config U9/U10 respectively: minimum ITHR is 64 for U10, 96 for U9
  - Laser test: U9 and U10 can work simultaneously, NO error code/cross-talk found

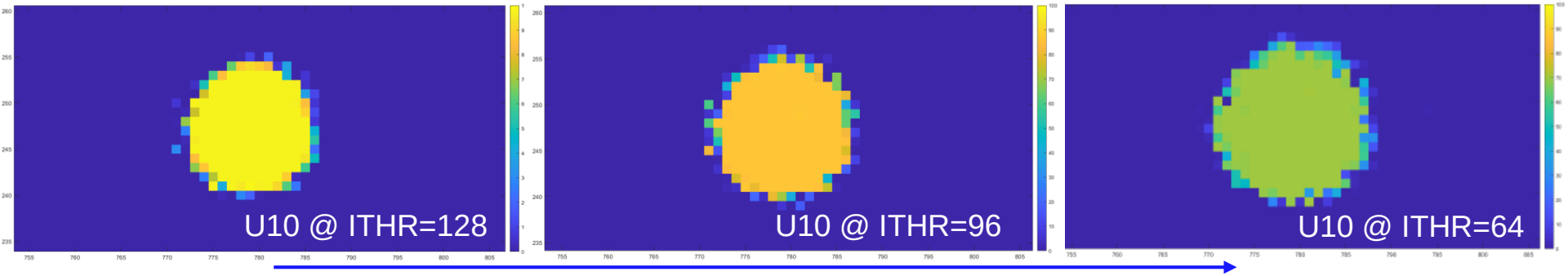




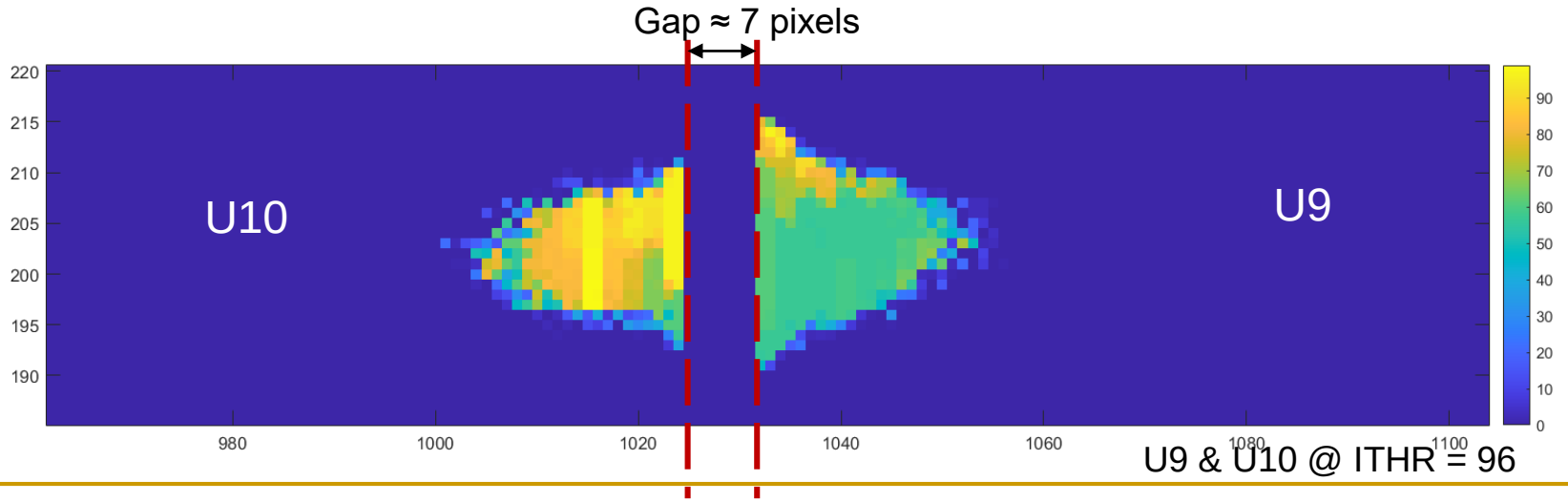


4-layer flex test result

- **FlexV1p4-C: chip U10 & U9**
  - Config U9/U10 respectively: minimum ITHR is 64 for U10, 96 for U9
  - Laser test: U9 and U10 can work simultaneously, NO error code/cross-talk found



Count efficiency decreasing with ITHR decreasing ??



Status of flex boards

- **Four 4-layer flex bonding with U9 & U10**
  - One flex short after U9 bonding: FlexV1p4-A → need to be repaired
  - Two work normally: FlexV1p4-B, FlexV1p4-C
  - One untested: FlexV1p4-D

- **One 2-layer flex bonding with U9 & U10**
  - Works normally in the beginning, to be problematic during test after plug for several times → damage of socket is under suspicion

- **Eight bare 4-layer flex ready for chip bonding (socket welded)**