



山东高等技术研究院

SHANDONG INSTITUTE

OF ADVANCED TECHNOLOGY

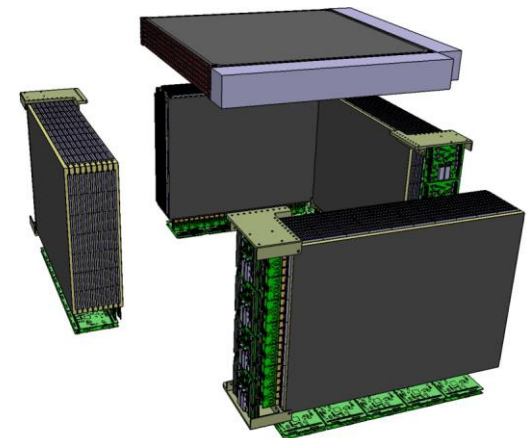
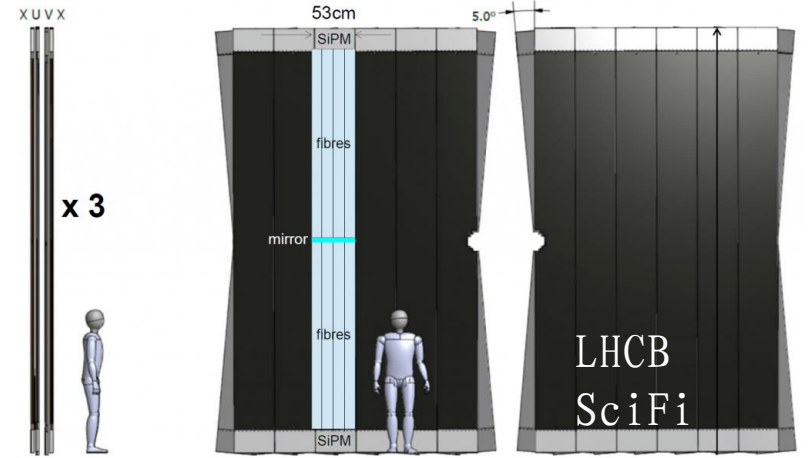
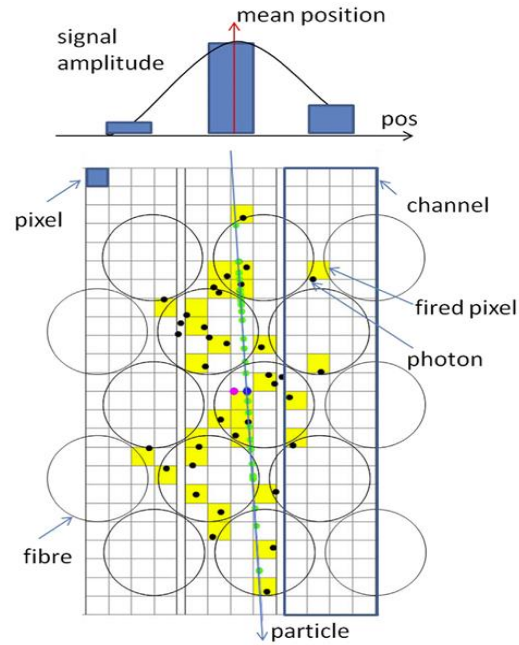
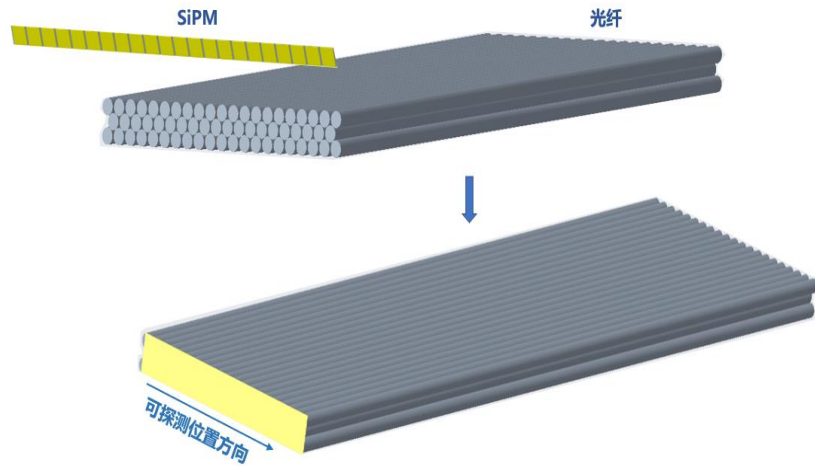
基于Citiroc1A的多通道SiPM 信号读出电子学

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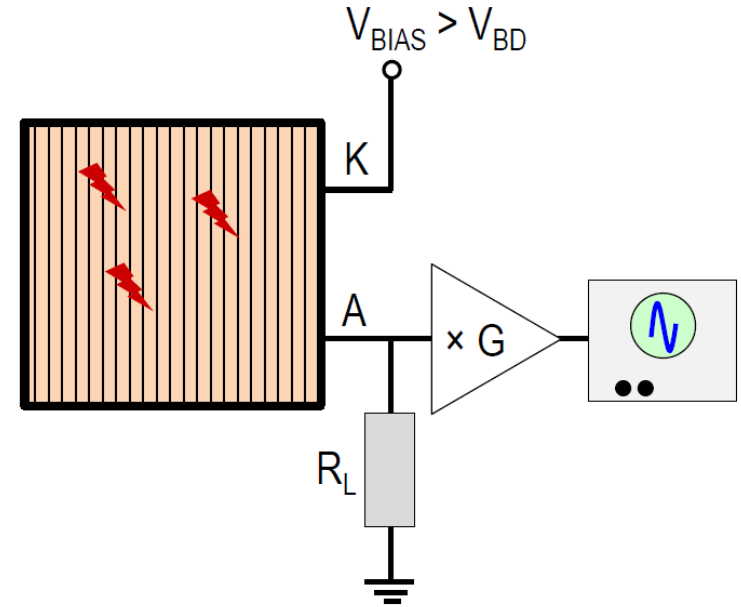
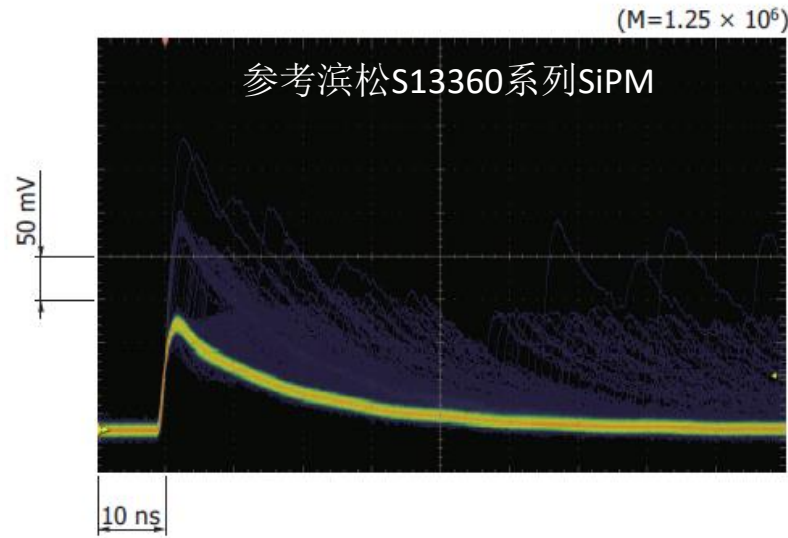
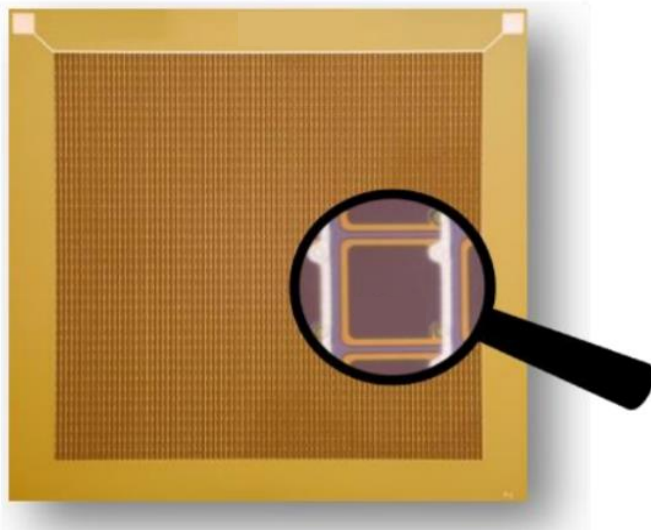
塑料闪烁光纤探测器

位置灵敏探测器



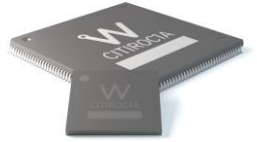
- 探测器结构：塑料闪烁光纤探测主体和1维SiPM光电转换器件
- 最小塑闪光纤直径可低至 $125\mu\text{m}$ ，比传统塑料闪烁体条探测器具有更高的颗粒度和位置分辨能力，同时导致读出通道数增多

硅光倍增器SiPM



- 单个SiPM由多个工作在Geiger模式下的SPAD并联组成
- 结构紧凑，尺寸灵活，对磁场不敏感，可响应单光子水平的信号
- 工作所需反向偏压低（几十伏），增益可达 10^5-10^6
- 良好的单光子时间分辨（ $<100\text{ps}$ ）

多通道SiPM信号读出



Citiroc1A ASIC

- 32通道SiPM信号放大和积分
- 高增益和低增益两种信号输出，动态范围0-400pC (10⁶增益下2500pe)
- 积分成形电路可调达峰时间12.5-87.5ns，满足闪烁光信号时间尺度
- 对单光子信号灵敏，可触发1/3 pe

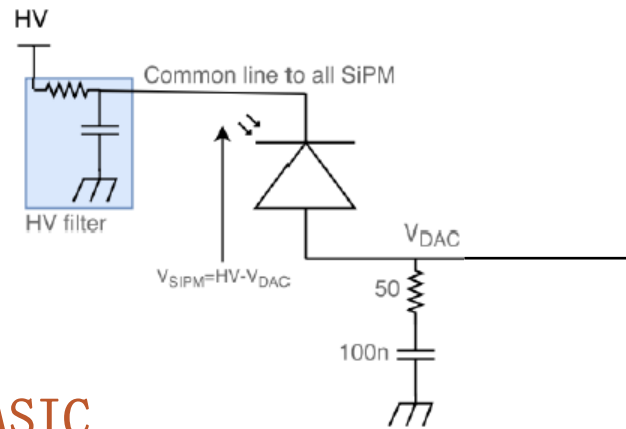
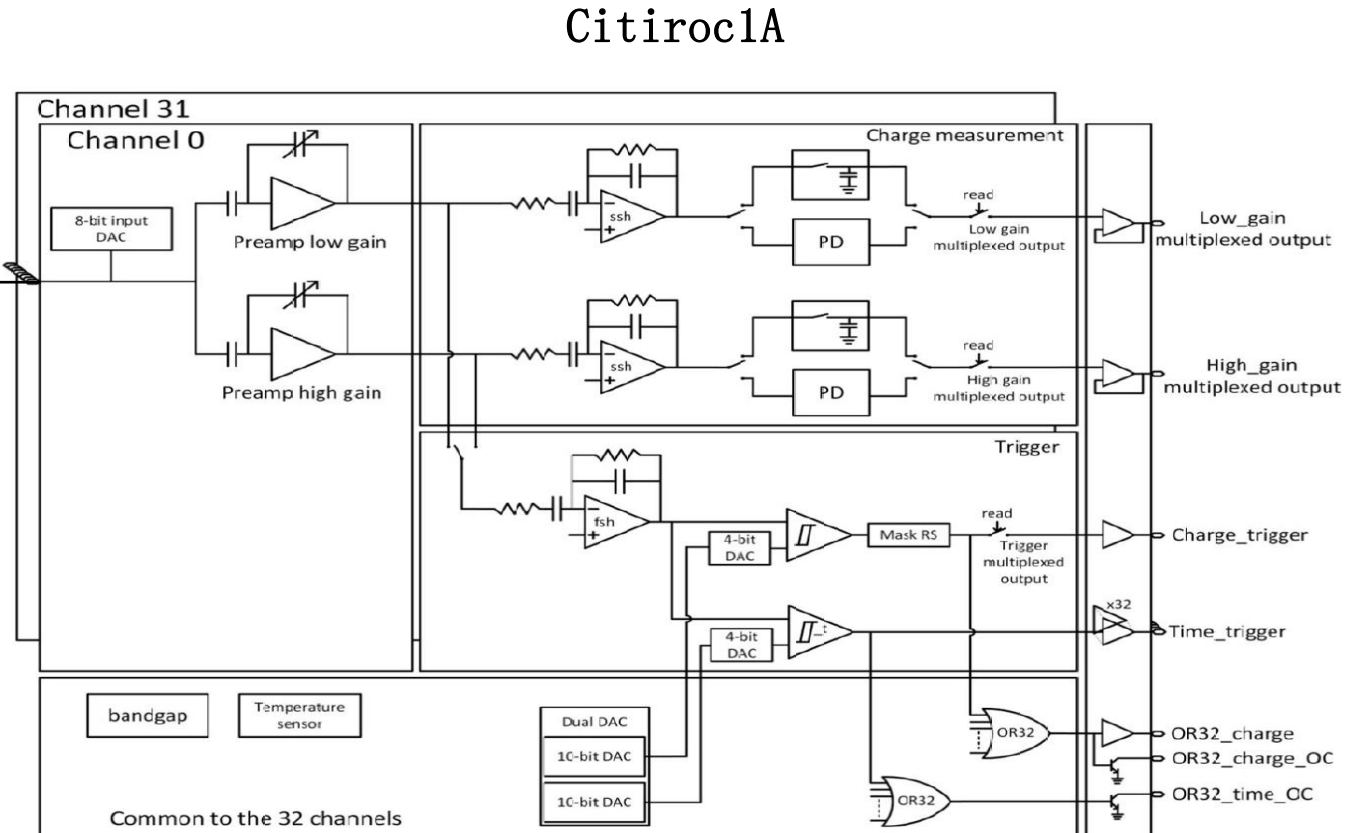
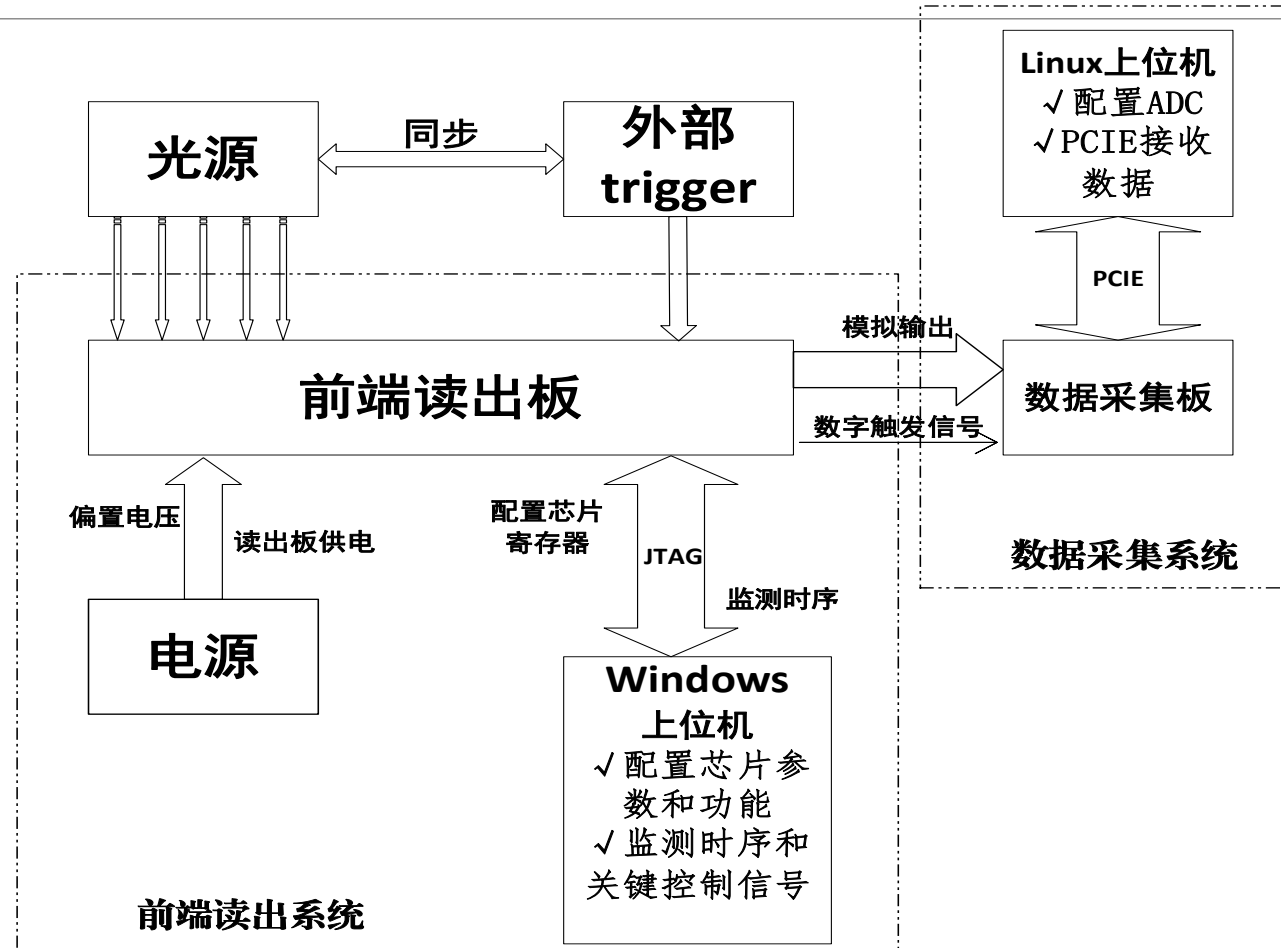


Figure 1 - General ASIC block scheme



电子学总体设计考虑

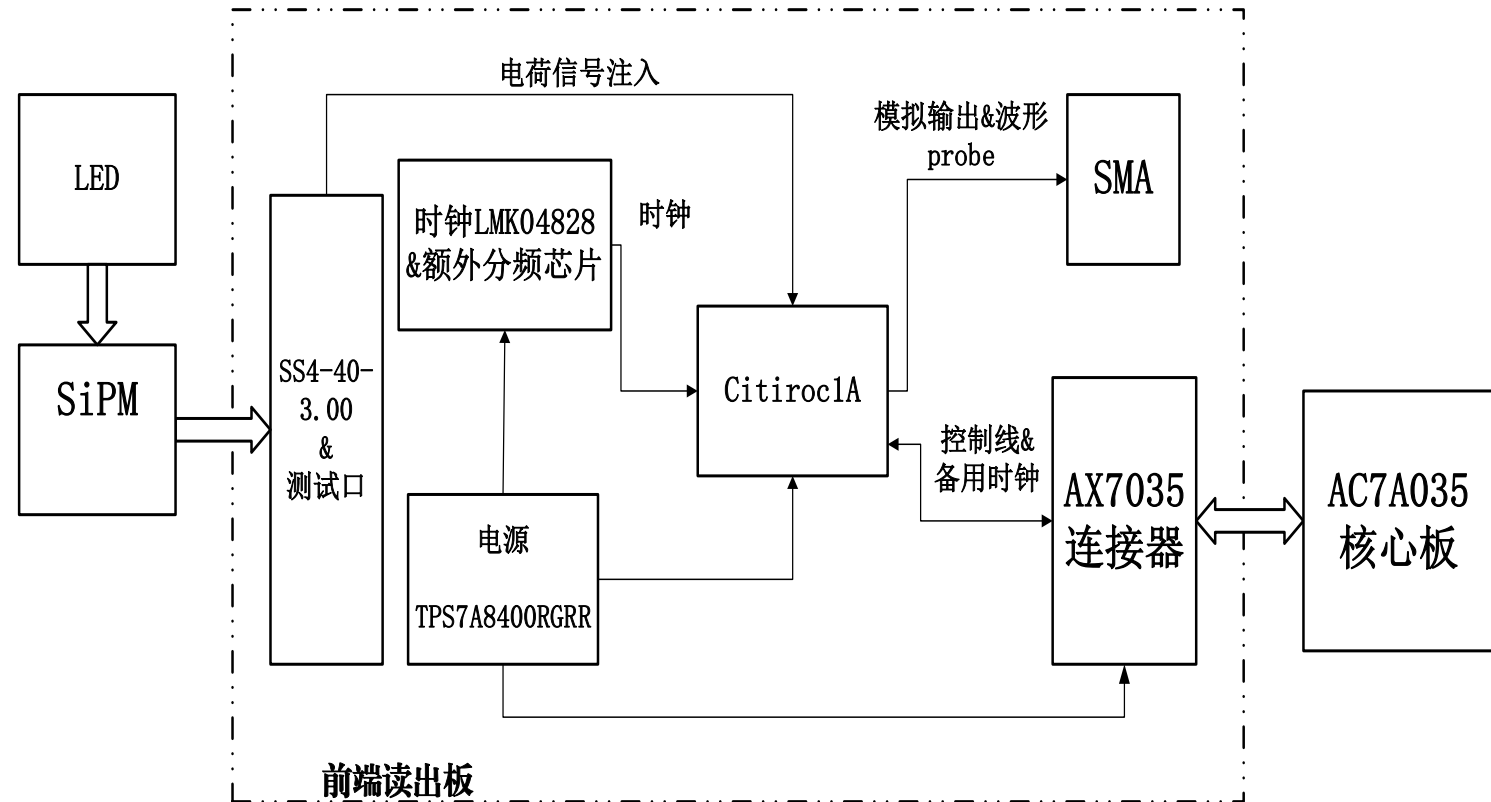
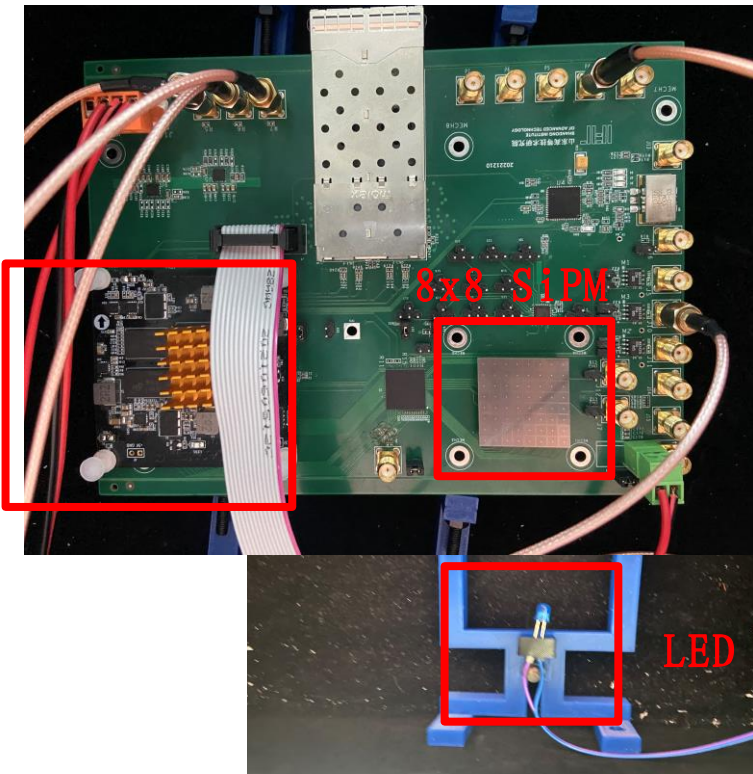
全局框图 →



电子学总体设计考虑

前端读出系统

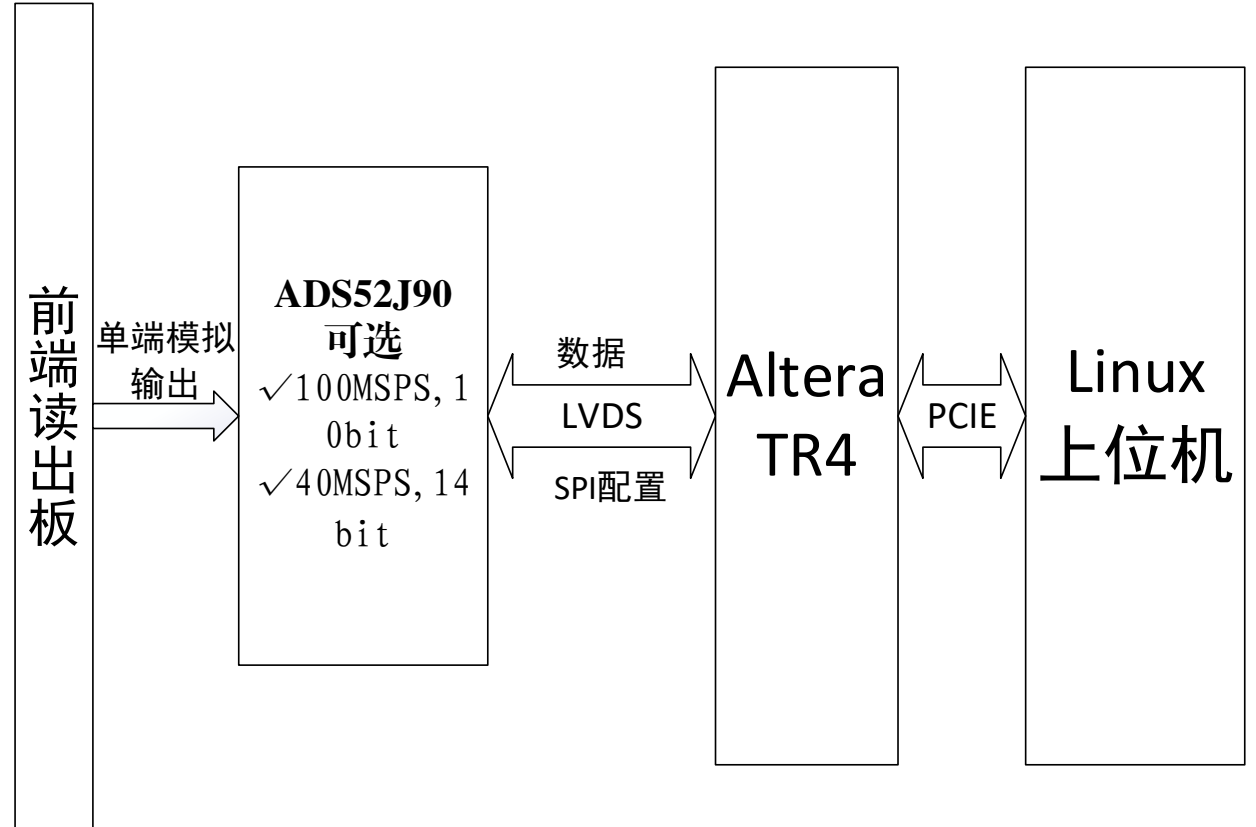
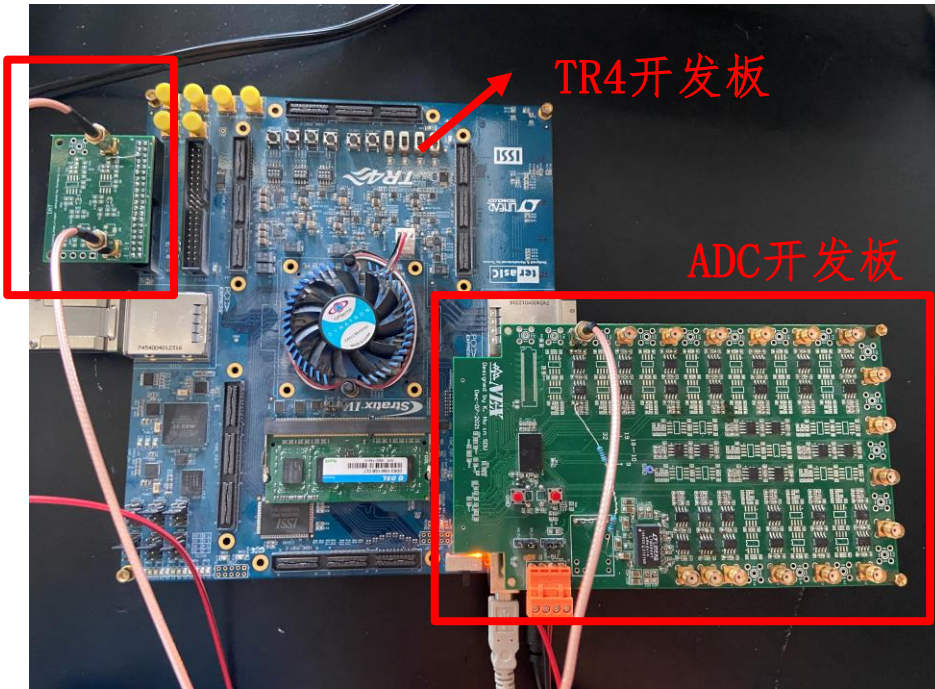
核心板



电子学总体设计考虑

数据采集系统

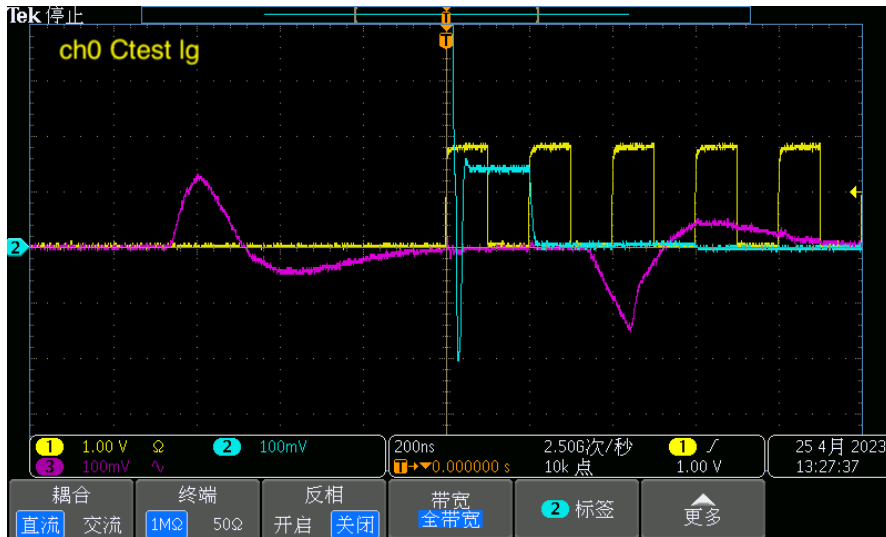
数据采集触发



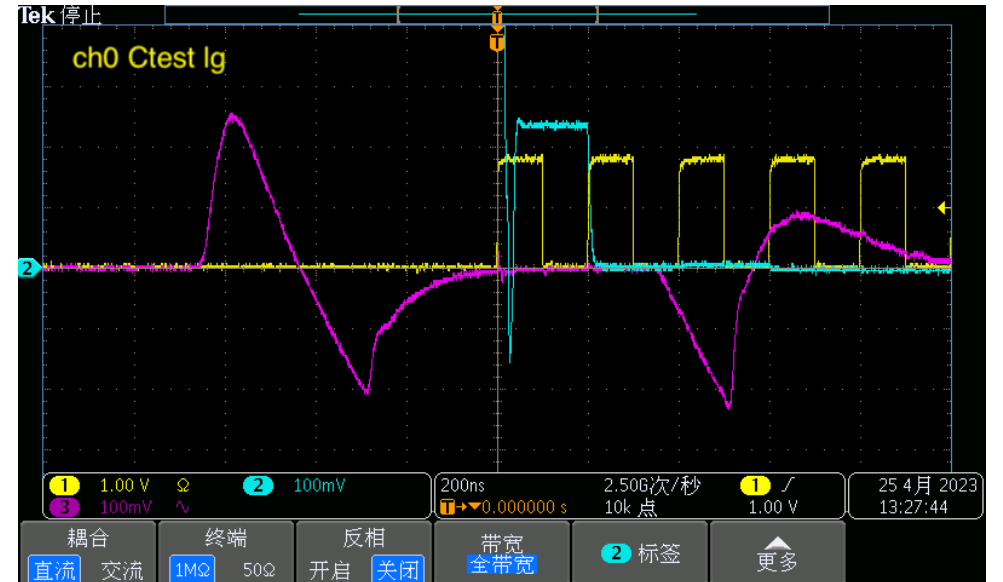
前端读出系统功能调试

测试条件:

- 从in_calib管脚进行信号注入
- 信号发生器设置5ns上升沿, 100ns下降沿、200mV-500mV, 1us脉宽的脉冲信号
- 电荷注入板, 100pF
- 读出时钟5Mhz (芯片支持最高的频率)



示波器观测模拟输出
功能验证



模拟信号输出结果图, 蓝色为low gain模拟输出, 紫色为low gain通道的slow shaper输出, 黄色为读出时钟

SiPM联合测试

实验条件

- 信号发生器控制led灯→光照
- 笔记本→前端读出系统上位机
- 台式机→数据获取系统上位机
- 8x8 SiPM or 单点SiPM →输入
- 台式电源 or 高压模块→偏置
- 80cm x 80cm x 40cm 金属暗箱

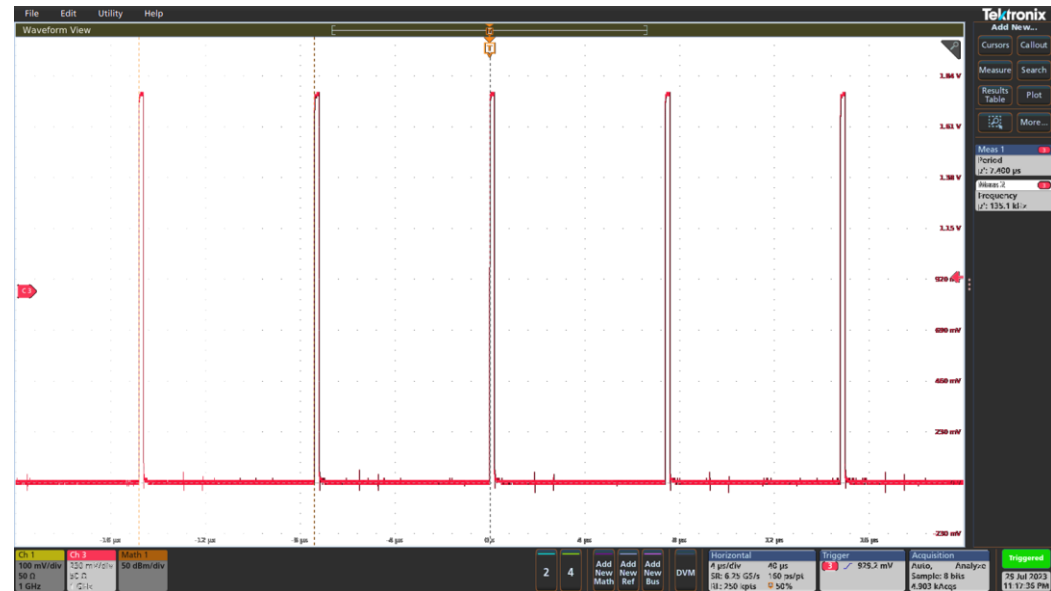
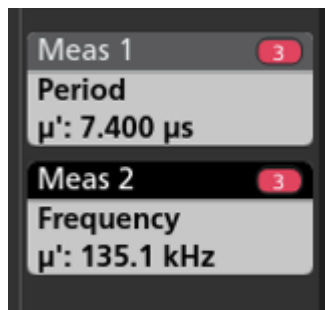


基本性能

死时间和最大频率

➤ 7.4us, 即最高约135kHz

事例率读出



- 阈值设置使得基线触发
- 开启一个通道的hit multiplexer
- 示波器测量频率

基本性能

噪声水平

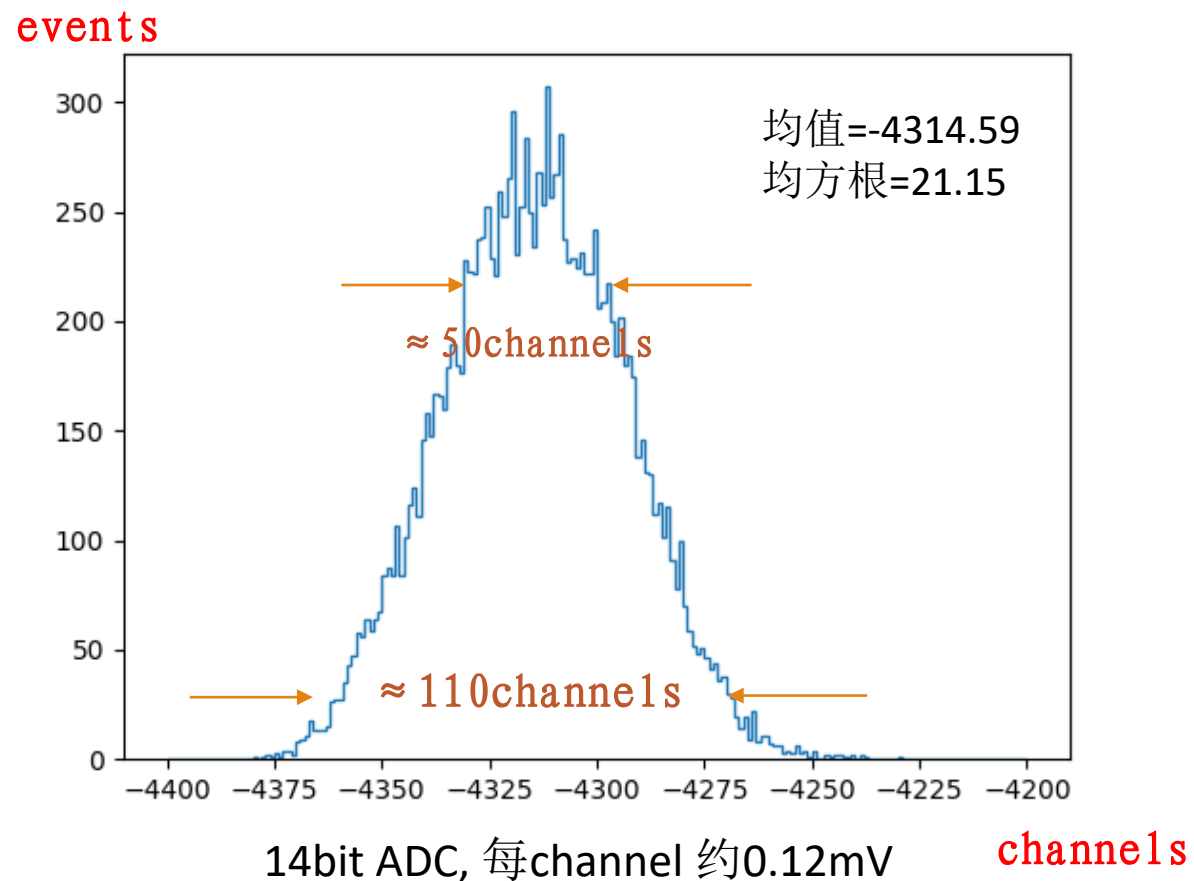
➤ 基线能谱

➤ Low Gain通道输出

➤ preamp gain = 4.62V/V

➤ peaking time = 50ns

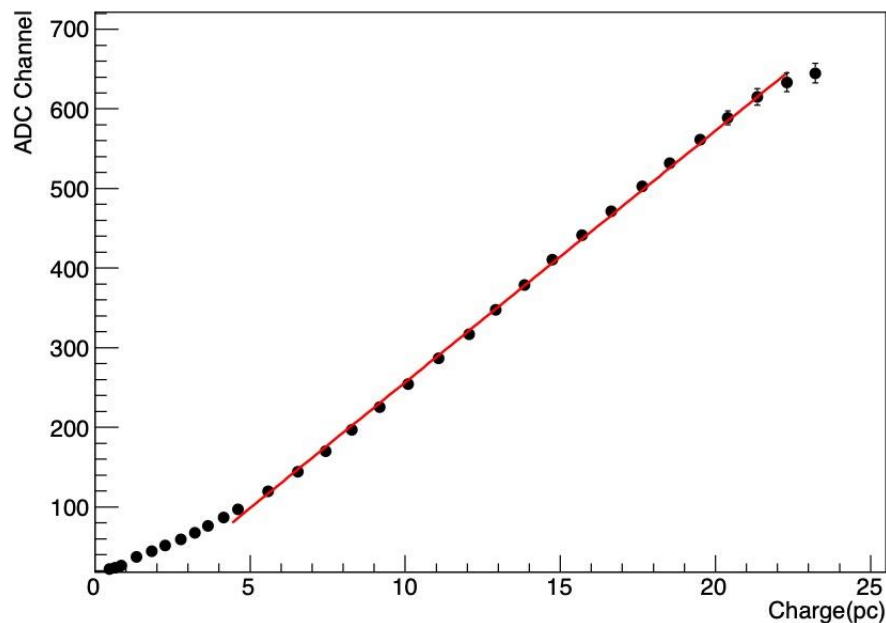
➤ 已连接单点SiPM, 偏置 $\approx 55.8V$



基本性能

芯片动态范围

Citiroc1A_High_Gain

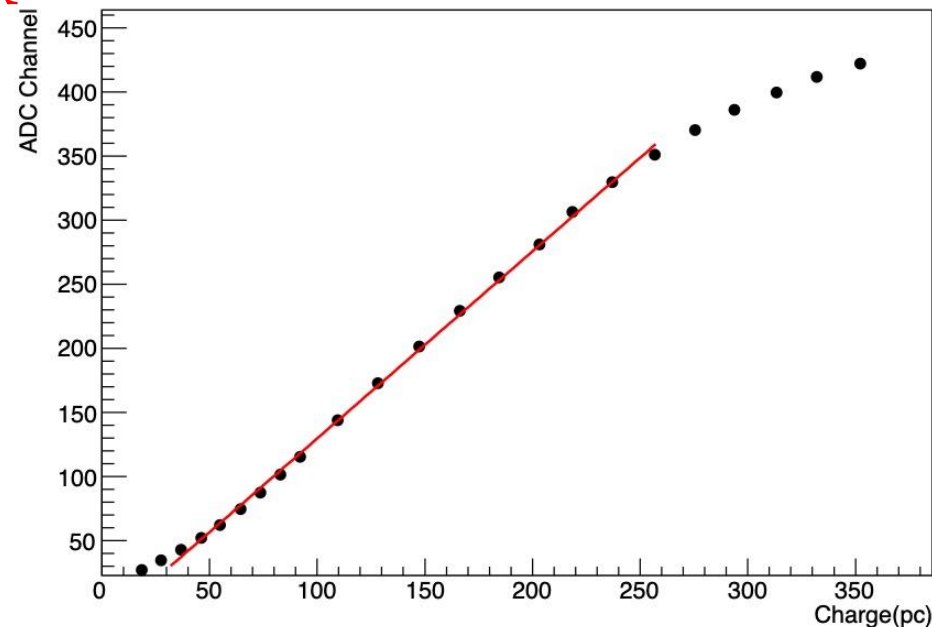


10bit ADC, preamp gain = 46.15V/V,
peaking time = 25ns

测量方式：电荷注入

HG和LG在各自的高电荷量和低电荷量区间都出现了非线性现象

Citiroc1A_Low_Gain



10bit ADC, preamp gain = 1.94V/V,
peaking time = 25ns

基本性能

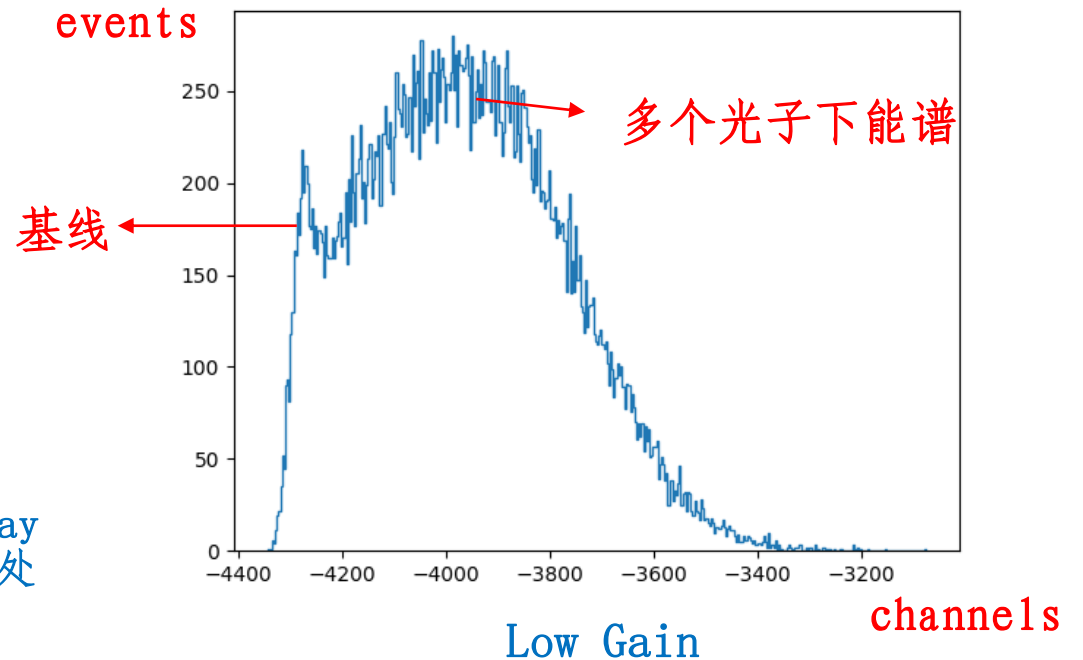
能谱与增益

- 偏置: 55.8V
- 增益: 4.62V/V x 10
- peaking time : 50ns
- hold delay > 200ns
- 光强: 3.2V, 35ns宽度的脉冲→LED
- 14bit 40MSPS ADC采集

可能原因: 前端读出板的板级噪声较高

已排除原因: ADC位数 (10bit换成14bit)、hold delay (60ns→大于200ns)、光强 (在商用板验证)、数据处理方式、ADC板级噪声 (±10channel)、注入板噪声 (更换为8x8 SiPM后, 直接插在电路板上)

看不到单光子峰、无法区分相邻光子峰

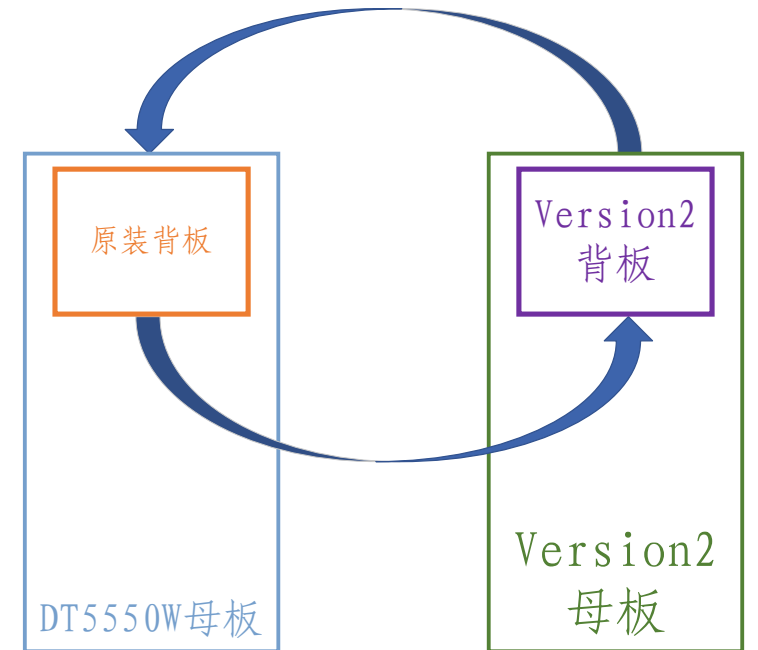


未来计划

电路板改版：

- 将所有功能模块划分到背板与母板上，减少接口和连接器的使用，提高集成度
- 子板包含Citiroc1A、LDO电源、SiPM放置、偏置补偿（可选）
- 母板包含ADC、FPGA、时钟芯片、开关电源、光纤通信模块、高压模块
- 用DT5550W实现交互验证

优化测试流程，提高软件使用效率



小结

- 前端读出板设计开发
- 前端读出系统的功能验证
- 前端读出系统、数据采集系统以及SiPM的联合测试
- 基本性能测试：噪声、死时间、动态范围
- 能谱：无法区分增益、看不到单光子峰
- 进行下一版改版设计

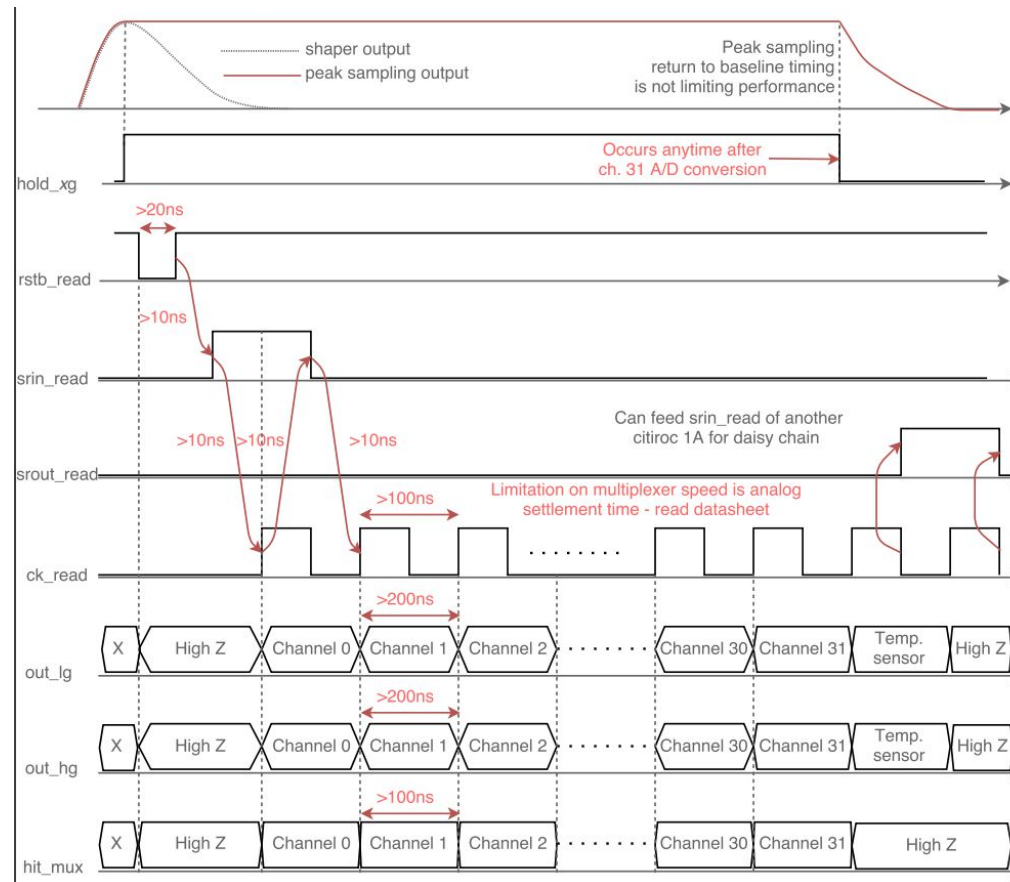
谢谢大家，敬请指正！

Backup

Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 100 ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SiPM gain
Packaging & Dimension	TQFP 160 – TFBGA353
Power Consumption	225mW – Supply voltage : 3.3V
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	32 trigger outputs 2 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger output (Trigger OR)
Internal Programmable Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment (10bits), channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor

Table 1 – ASIC main parameters

Backup



Backup

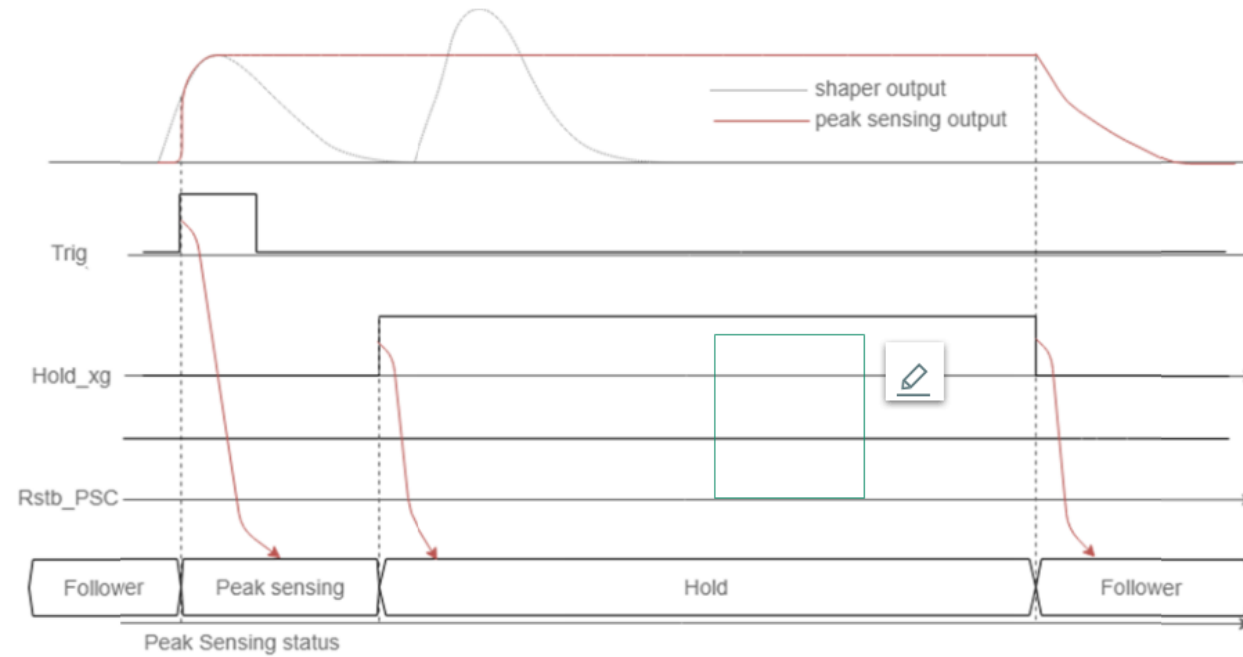


Figure 14 - Peak detector chronogram

Backup

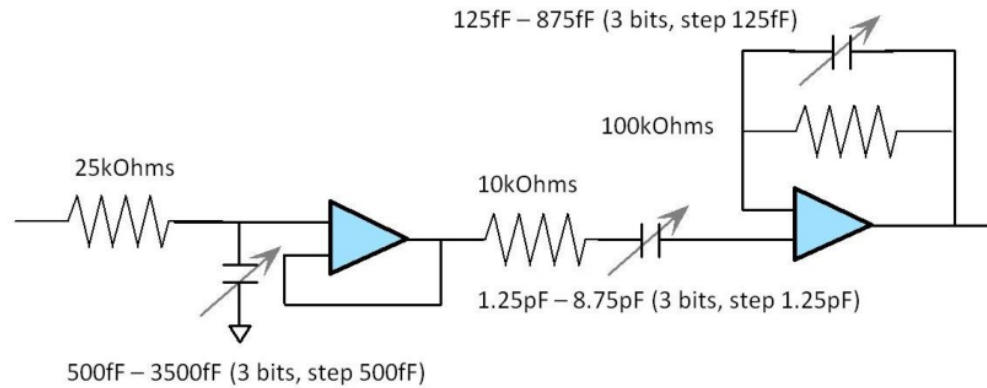


Figure 10 - Slow shaper schematic

Slow control value	Peaking time value
6 (110)	12.5 ns
5 (101)	25.0 ns
4 (100)	37.5 ns
3 (011)	50.0 ns
2 (010)	62.5 ns
1 (001)	75.0 ns
0 (000)	87.5 ns

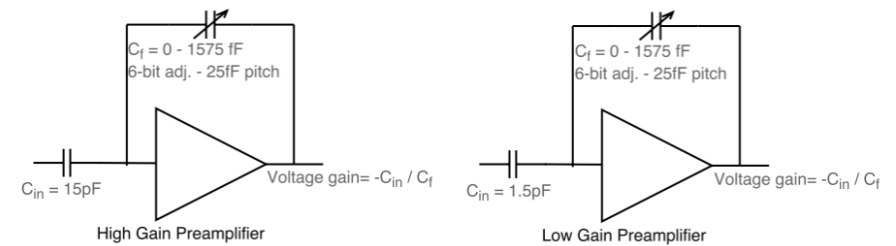


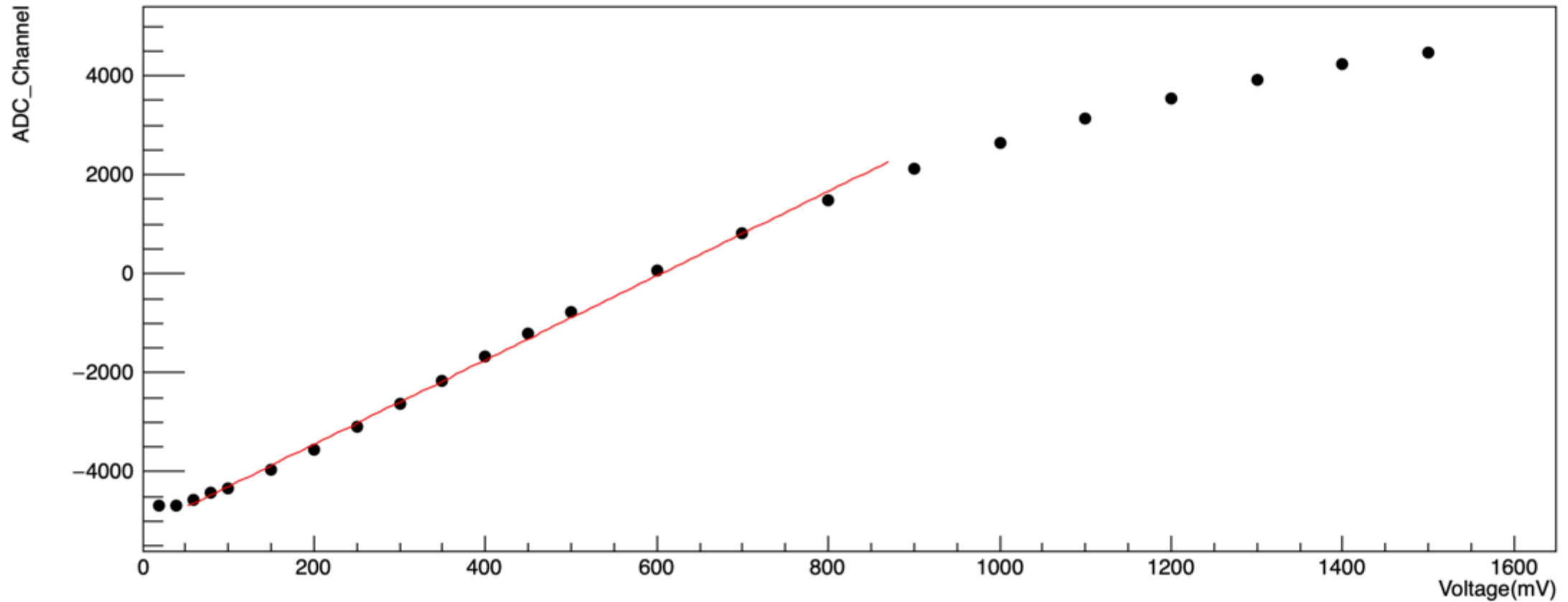
Figure 8 - High gain and low gain voltage sensitive preamplifier

6-bit feedback config	Feedback capacitance	Low gain preamp gain	High gain preamp gain
111110 [62]	25 fF	60 V/V	600 V/V
111101 [61]	50 fF	30 V/V	300 V/V
....			
011111 [31]	800 fF	1.875 V/V	18.75 V/V
....			
000001 [1]	1550 fF	0.97 V/V	9.7 V/V
000000 [0]	1575 fF	0.95 V/V	9.5 V/V

Table 3 - Preamplifier Gain versus slow control program

Backup

Charge_Low_Gain



14bit ADC, Gain = 50, peaking time = 50ns