基于高压 CMOS 的 LHCb 上游径迹探测器升级

李一鸣
中国科学院高能物理研究所
代表 LHCb U2UT 团队

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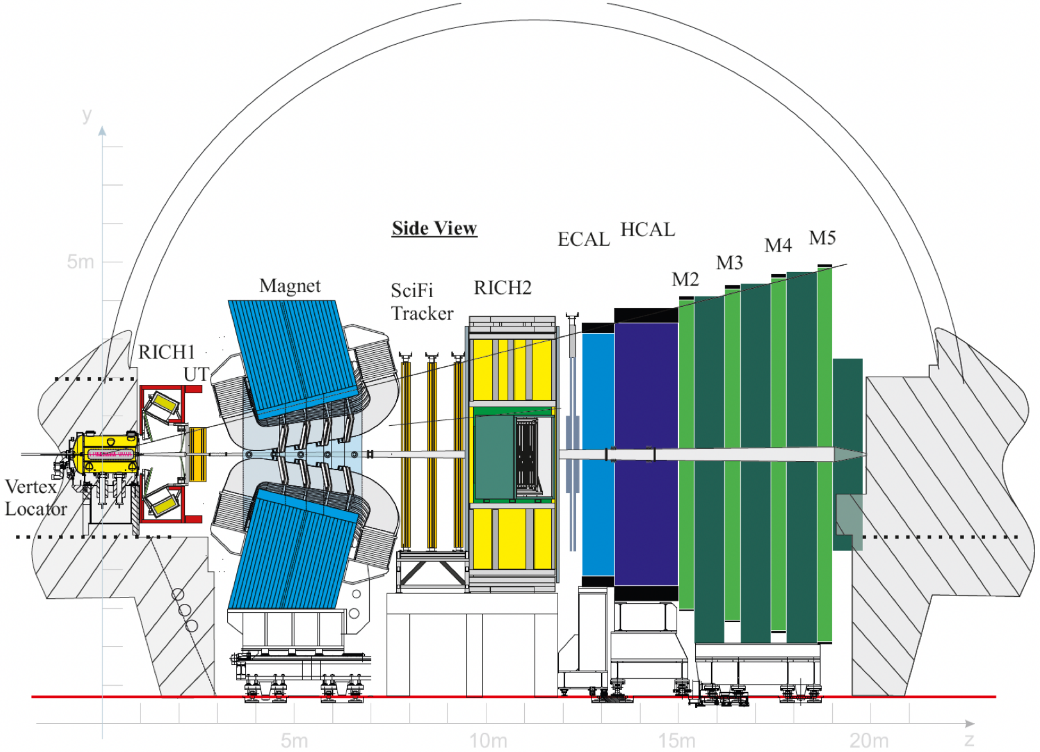
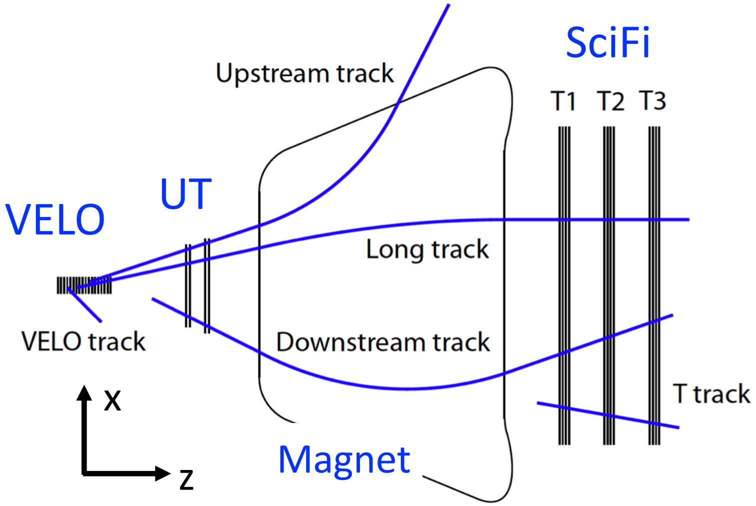
LHCb 径迹探测系统

- LHCb: LHC上为重味物理设计的单臂前向探测器实验
- 2023 年 3月完成一期升级，开始 Run3 运行
  - 瞬时亮度提高至 $2\times10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - 移除硬件触发

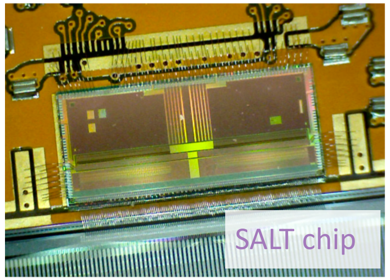




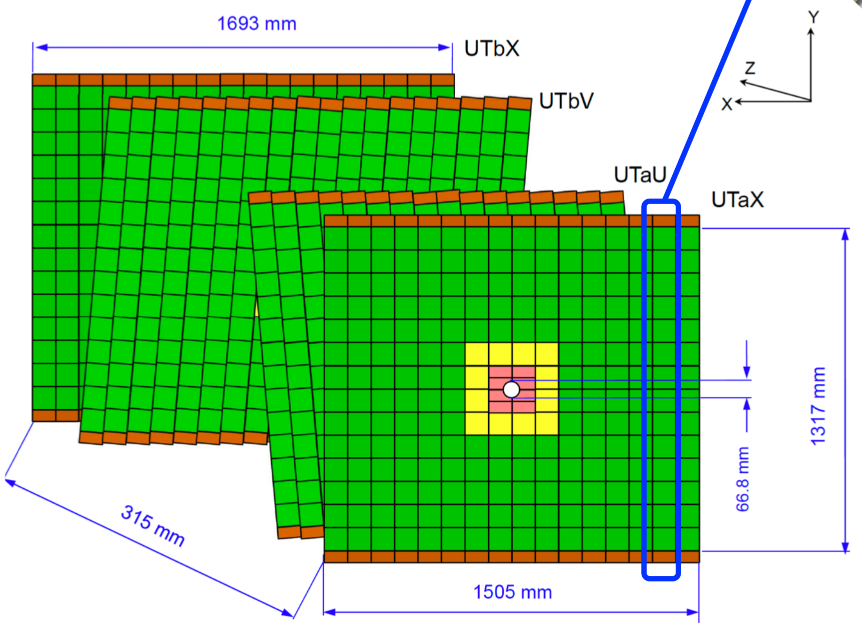
- 上游径迹探测探测器 Upstream Tracker (UT) 是径迹重建系统中重要一环:
  - 有助于长寿命粒子重建
  - 加快 VELO-SciFi 匹配，有助于在线实时重建

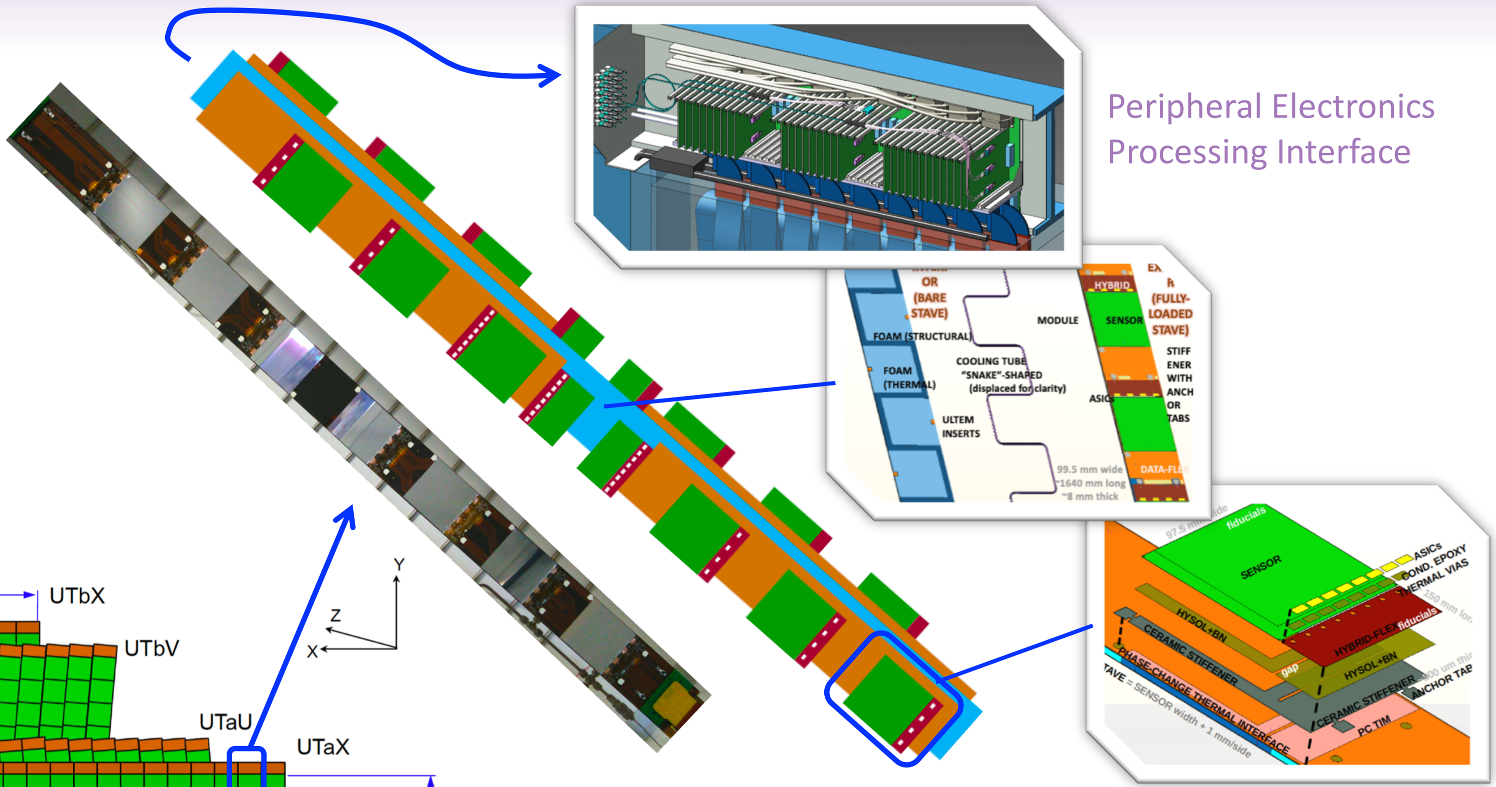
现有 UT 探测器

- 四层硅微条探测器
- 靠近束流颗粒度更高
- SALT：专用前端读出芯片



Sensor	A	B	C	D
Type	p-in-n	n-in-p	n-in-p	n-in-p
Thickness(μm)	320	250	250	250
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16





- Stave: Cooling tube (CO_2) embedded in foam core + CFRP face sheets
- Stave readout at both ends:
  - data formatting, timing distribution, control and optical conversion

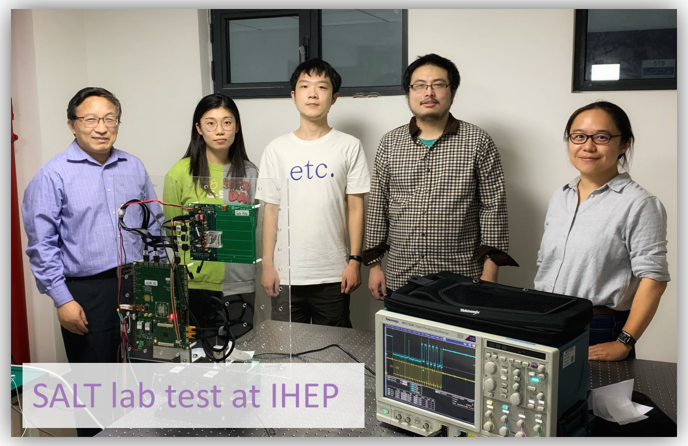
LHCb 中国组贡献

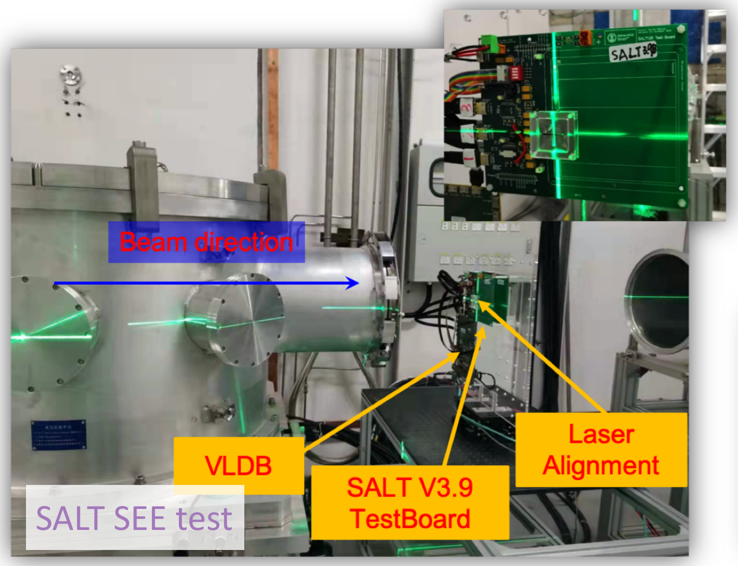
- 中国组在 UT 测试、安装中起骨干作用
  - 利用散裂中子源等国内设施开展 SALT 芯片抗辐照性能研究
  - 在 CERN 参与 UT 整体安装调试

Supported by NSFC project 11961141015
"LHCb升级中径迹探测器和数据获取系统的研究"


A-side installation complete


C-side installation complete


SALT lab test at IHEP



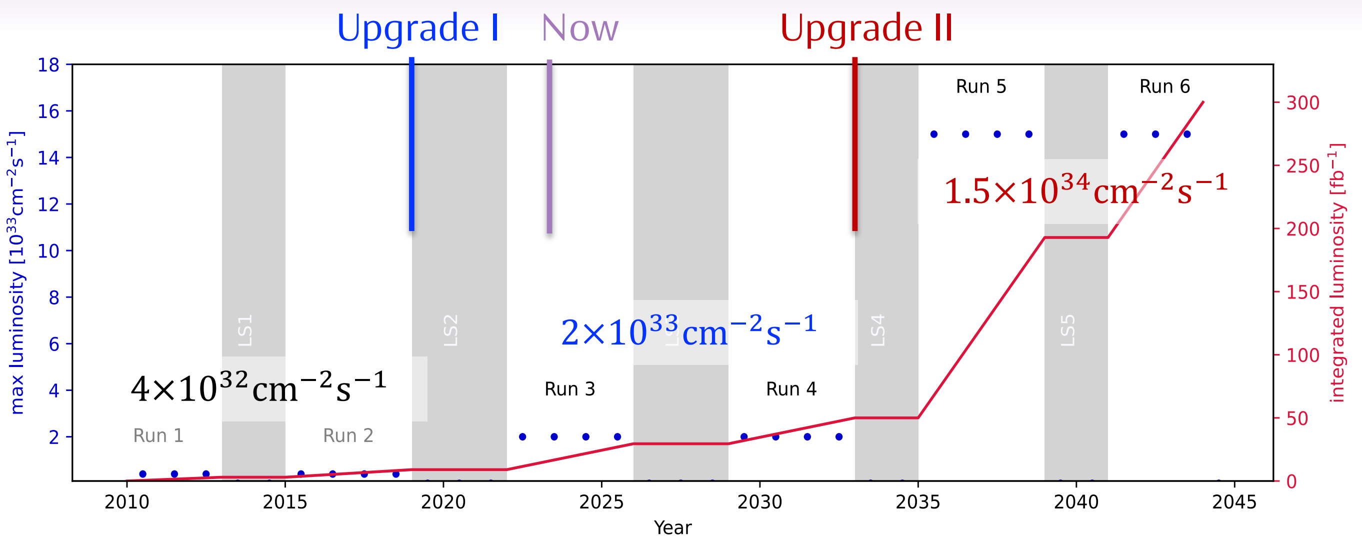
SALT SEE test

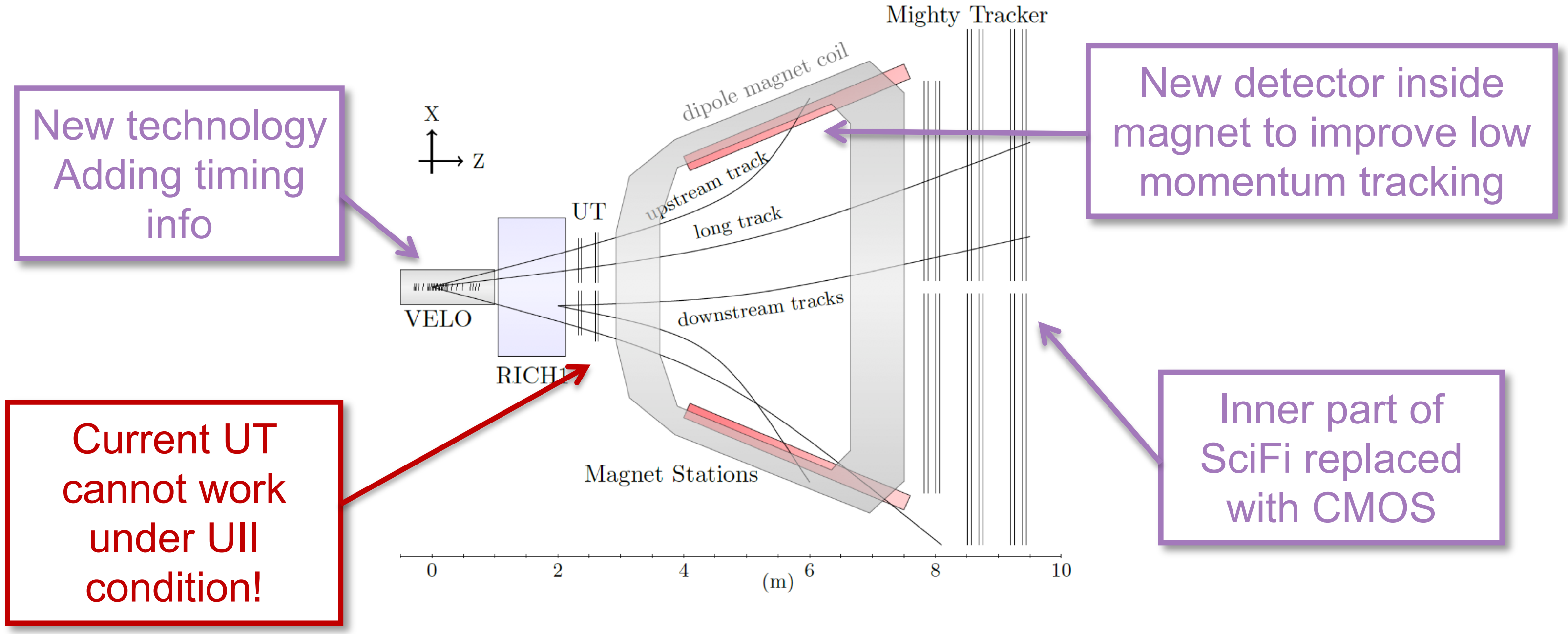

SALT SEE Test at CSNS

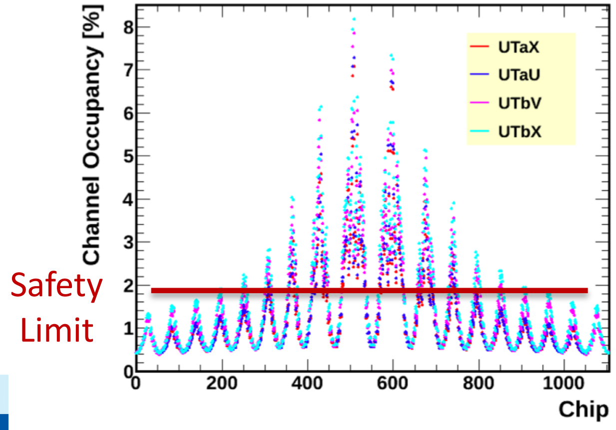

SALT SEE Test at CIAE

LHCb 二期升级

- LHCb 计划在 2032 年后进行二期升级，充分发掘 HL-LHC 味物理潜力
- 瞬时亮度提升至 $1.5\times10^{34}\ \mathrm{cm^{-2}s^{-1}}$ 并在LHC全周期采集 $\mathcal{L}_{int}\sim 300\ \mathrm{fb^{-1}}$
- 高亮度，新挑战:
  - 事例堆积变多: $\mu\sim 1\rightarrow 5\ (\mathrm{UI})\rightarrow 40\ (\mathrm{UII})$
  - 探测器占用率增加
  - 辐照损伤更严重
  - 实时径迹重建至关重要



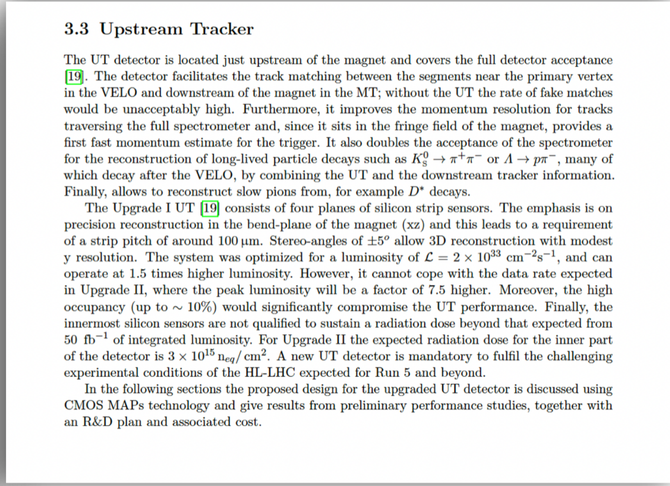




UT 升级计划

- 二期升级中 UT 将全面升级
  - 硅微条替换为基于 CMOS 的硅像素探测器
  - 颗粒度更高、抗辐照性能更好
- 中国为核心的 U2UT 团队自 2021年起提出初步升级方案并开展预研

LHCb Upgrade II TDR, CERN-LHCC-2021-012;
Y. Li, Nucl. Inst. Meth. A 1032 (2022) 166629



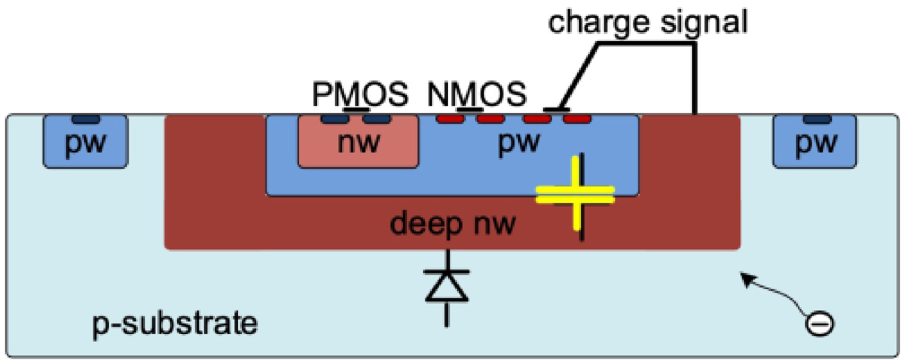
3.3 Upstream Tracker

The UT detector is located just upstream of the magnet and covers the full detector acceptance [19]. The detector facilitates the track matching between the segments near the primary vertex in the VELO and downstream of the magnet in the MT; without the UT the rate of fake matches would be unacceptably high. Furthermore, it improves the momentum resolution for tracks traversing the full spectrometer and, since it sits in the fringe field of the magnet, provides a first fast momentum estimate for the trigger. It also doubles the acceptance of the spectrometer for the reconstruction of long-lived particle decays such as $K^0_S \to \pi^+\pi^-$ or $\Lambda \to p\pi^-$, many of which decay after the VELO, by combining the UT and the downstream tracker information. Finally, allows to reconstruct slow pions from, for example D^* decays.

The Upgrade I UT [19] consists of four planes of silicon strip sensors. The emphasis is on precision reconstruction in the bend-plane of the magnet (xz) and this leads to a requirement of a strip pitch of around 100 µm. Stereo-angles of $\pm5^o$ allow 3D reconstruction with modest y resolution. The system was optimized for a luminosity of $\mathcal{L} = 2 \times 10^{33}$ cm^{-2}s^{-1}, and can operate at 1.5 times higher luminosity. However, it cannot cope with the data rate expected in Upgrade II, where the peak luminosity will be a factor of 7.5 higher. Moreover, the high occupancy (up to $\sim 10\%$) would significantly compromise the UT performance. Finally, the innermost silicon sensors are not qualified to sustain a radiation dose beyond that expected from 50 fb^{-1} of integrated luminosity. For Upgrade II the expected radiation dose for the inner part of the detector is 3×10^{15} n$_{eq}$/cm^2. A new UT detector is mandatory to fulfil the challenging experimental conditions of the HL-LHC expected for Run 5 and beyond.

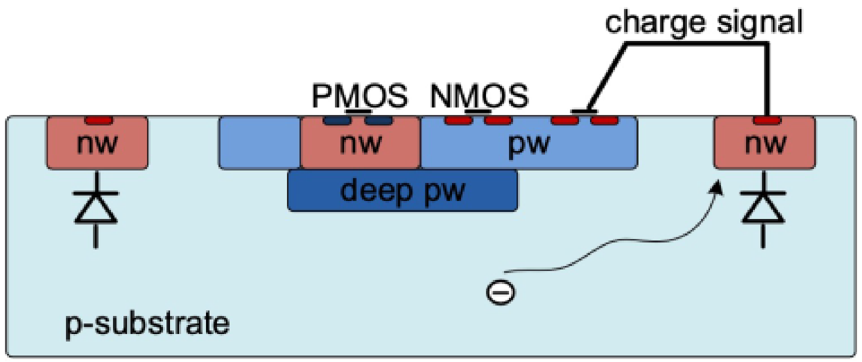
In the following sections the proposed design for the upgraded UT detector is discussed using CMOS MAPs technology and give results from preliminary performance studies, together with an R&D plan and associated cost.

传感器技术选项



High Voltage CMOS

- Circuitry inside the charge collection well
- Large uniform electric field
- On average shorter drift path
- Better radiation hardness (less trapping)
- HV-CMOS process commercially available
- Large sensor capacitance (pw and dnw)
- Foundries: TSI-180, Lfoundry-150, ···



CMOS with small electrode

- Circuitry outside the charge collection well
- Optimization of little low-field regions
- On average longer drift path
- Radiation hardness needs process modifications
- Very small sensor capacitance
- Foundries: Towerjazz-180, TPSCo-65···

传感器设计指标

Characteristics	LV-CMOS	HV-CMOS
Chip size	3.5×3.5 cm^2	2.0×2.0 cm^2
Pixel size	30×30 um^2	50×150 um^2
Chip thickness	~ 100 um	
Position resolution	5-10 um	15, 40 um
Time resolution	O (1) ns	
Power consumption	100 – 300 mW/cm^2	
Radiation dose	3×10^{15} n_{eq}/cm^2, or 240 MRad TID	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s

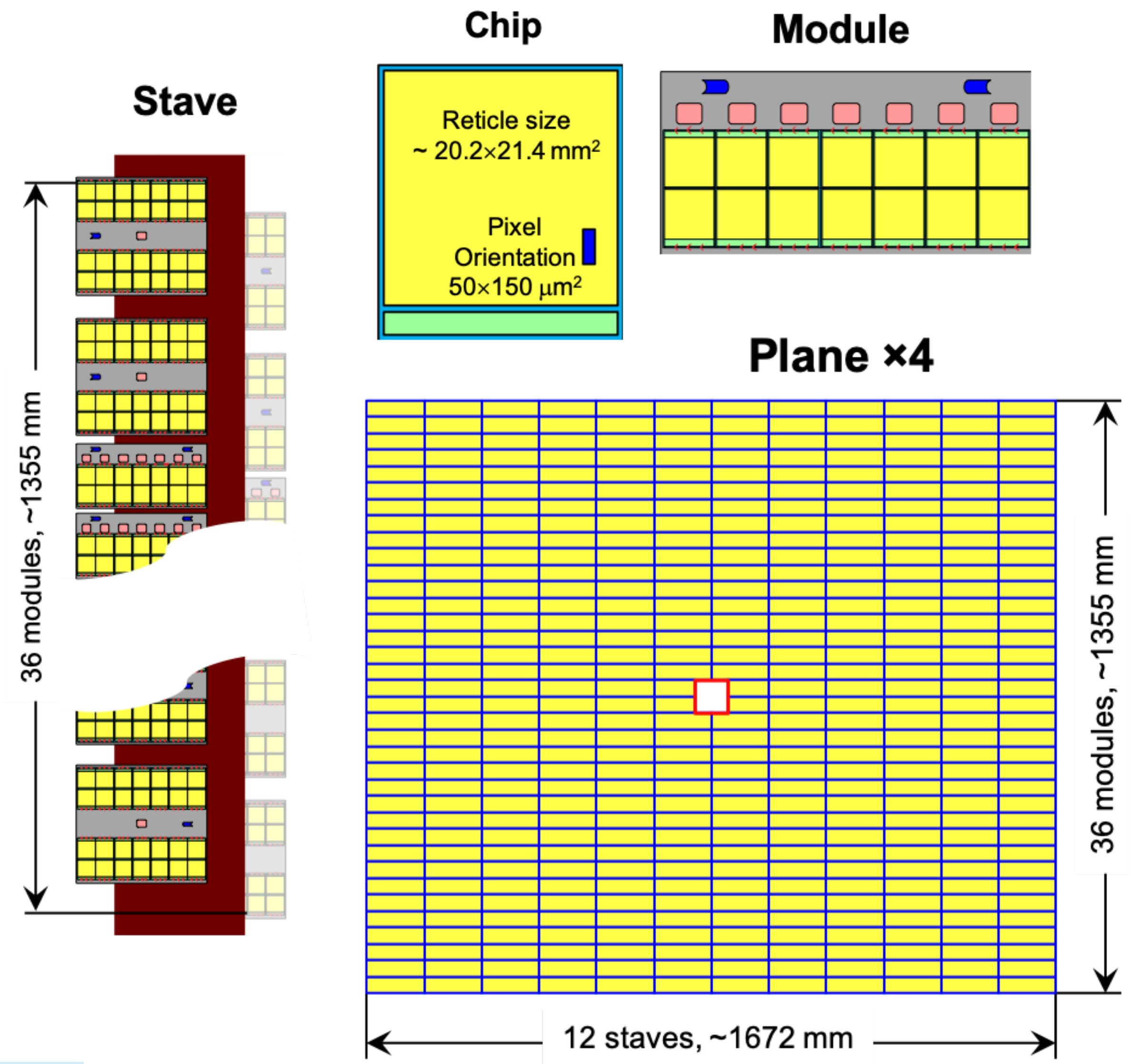
Capable of distinguishing 25ns bunch crossing

Depends on timing resolution

Affects cooling requirements

Achievable by HV-CMOS

基于 HVCMOS 的系统设计

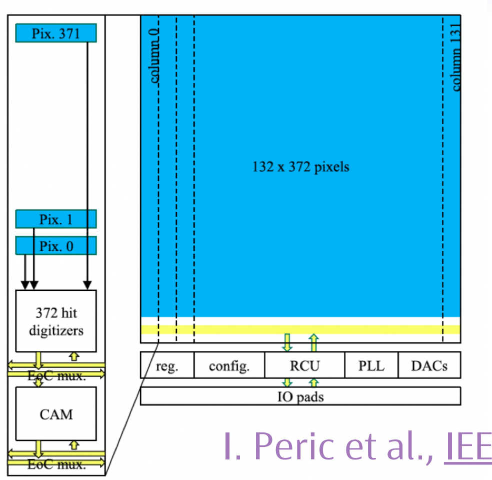


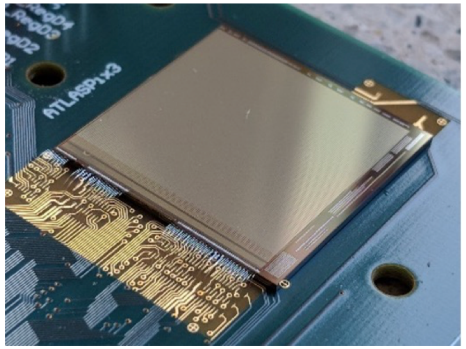
- 保留现有 UT 部分特点和机械结构
  - 纵向板条
  - 竖直方向磁场： 水平方向空间分辨率更高
- 光电转换在模块级别完成

Ring	5	4	3	2	1
e-links / chip	1	1	1	1-3	2-7
Gbps / e-link	0.32	0.64	1.28	1.28	1.28
lpGBT / module	0.5	1	2	7	14/10
Num of modules	1312	240	80	64	32
Num of lpGPTs	656	240	160	448	384

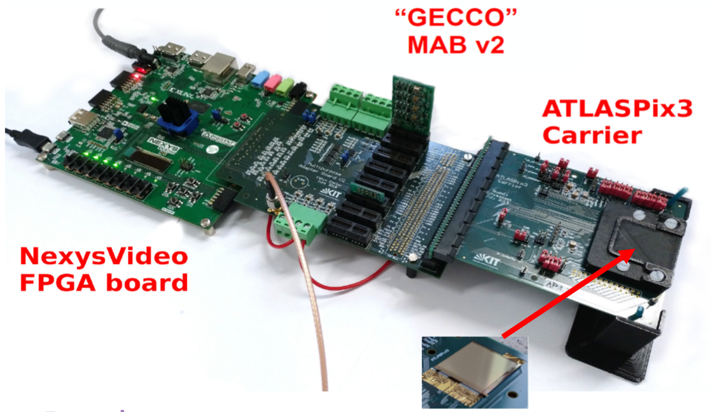
HVCMOS 芯片选项: ATLASPix3

- ATLASPix3 原为 ATLAS实验升级设计
  - TSI 180nm HV process on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 132 columns × 372 rows (20.2 × 21 mm^2 chip)
  - Functioning after ~10^{15} n_{eq}/cm^2
  - Power consumption ~160 mW/cm^2
- 高能所等团队对其开展充分测试，以此主要性能为基础形成 U2UT 初版设计

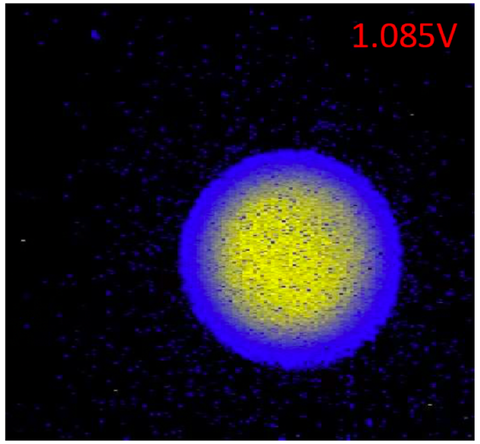




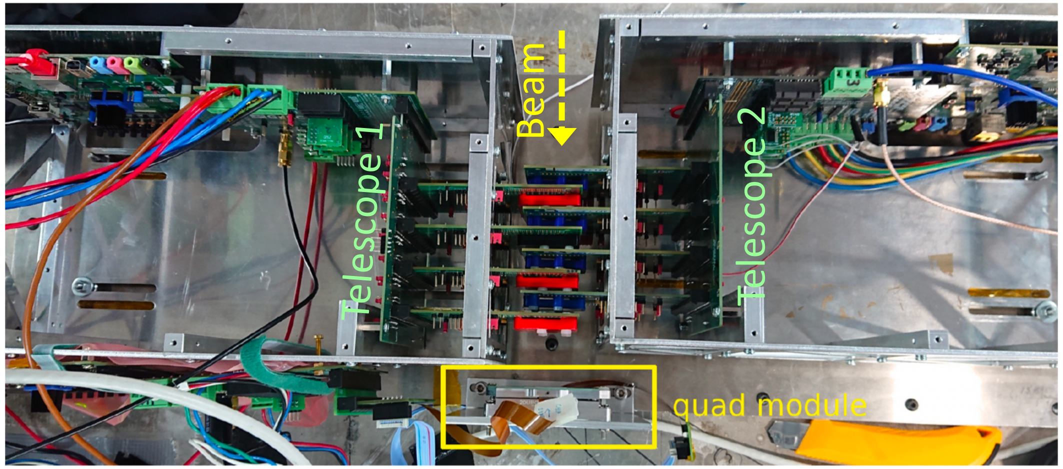
I. Peric et al., IEEE JSSC, Vol 56, No.8, Aug. 2021



Readout setup



Hitmap with Fe55 source



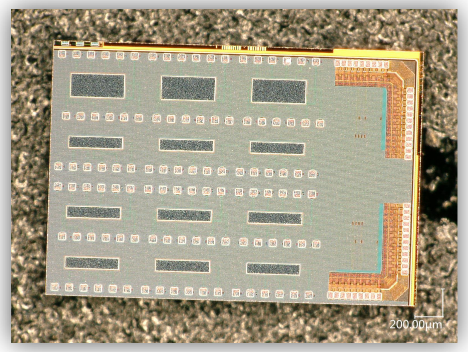
Test beam at DESY in 2022

先进工艺的高压CMOS探索

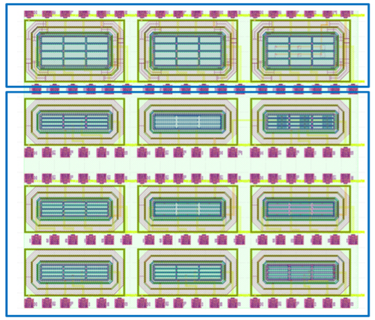
- 探索更先进制程的高压CMOS工艺，有助于集成更丰富功能，降低系统功耗
- SMIC 55nm CMOS 是有希望的技术选项

- 2022年利用 SMIC 55nm LL提交MPW
  - 验证sensor diode 特性
  - IV显示击穿电压约 -10V，像素电容200 fF以内

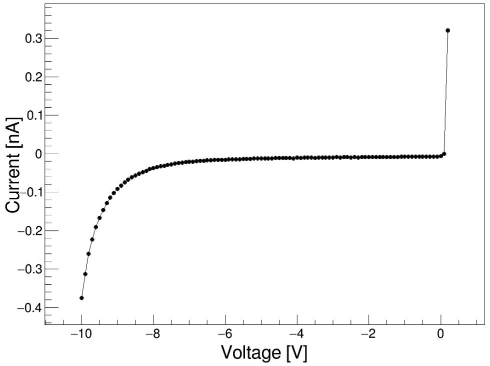
- 今年8月计划利用 SMIC 55nm HV 再次提交MPW
  - 可选择1k/2kOhm cm的高阻值衬底
  - 预期击穿电压将显著提高
  - 加入前端放大电路和数字电路验证

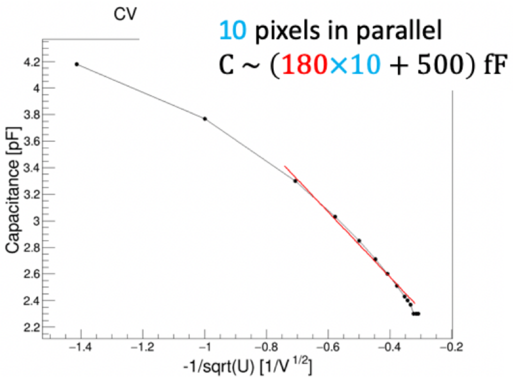


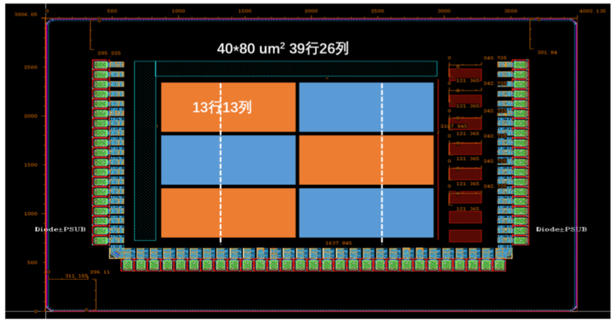
Pixel size:50x150um



Pixel size:25x150um



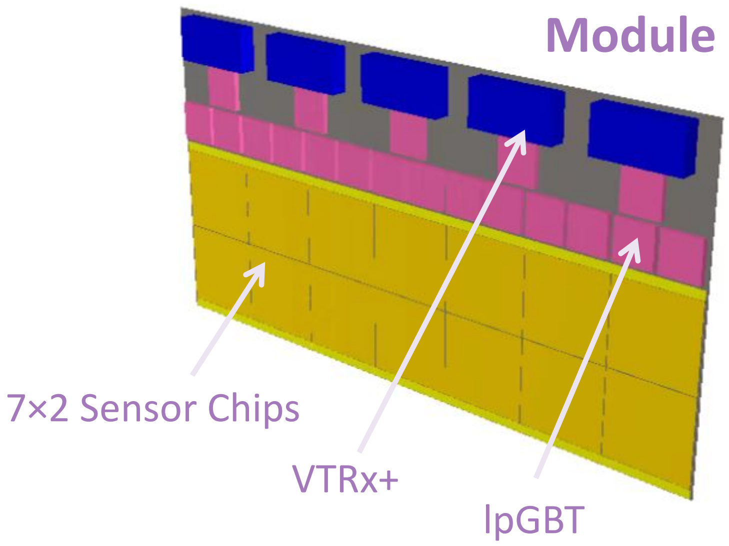


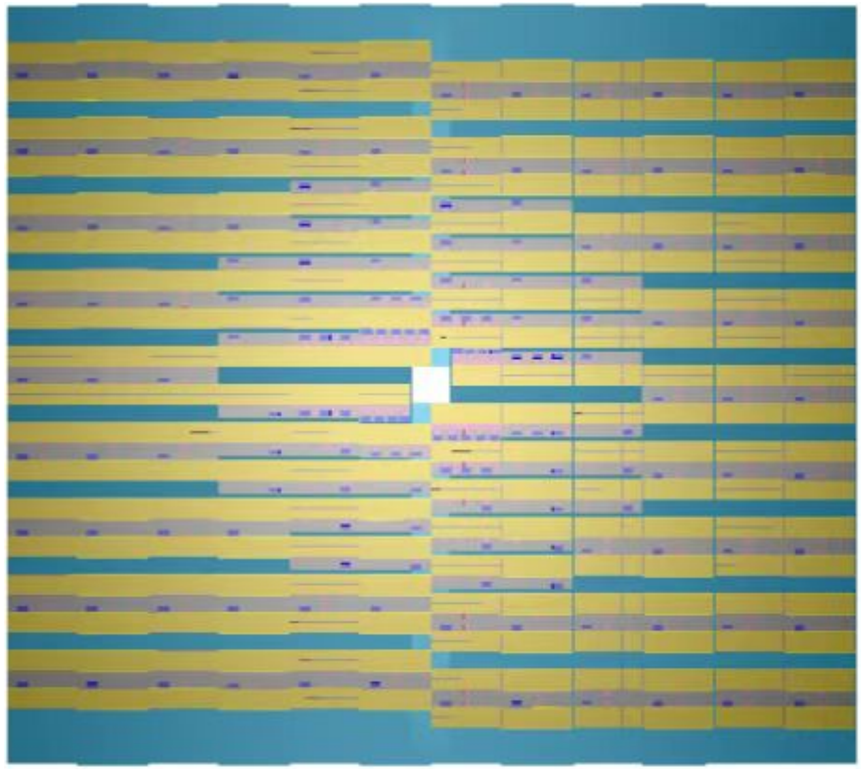


注：仅作为资源利用参考，不代表最终结构

探测器软件建模

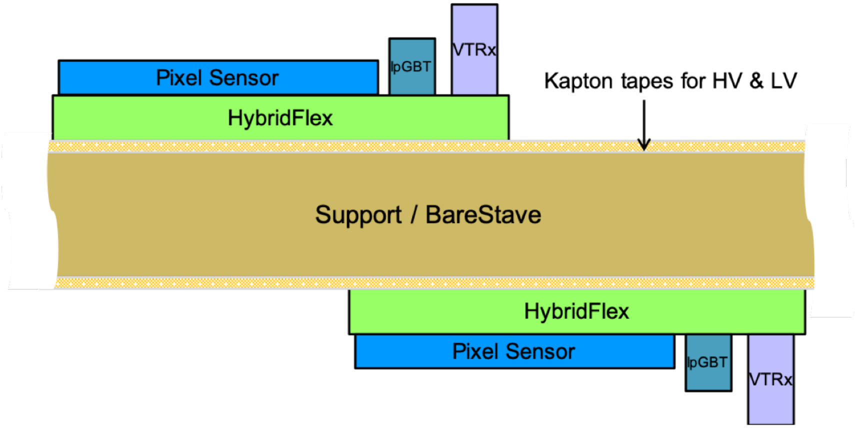
- 探测器设计方案已在LHCb软件框架下完成建模
- 全模拟的第一步，探测器优化的必须
  - Created in both DDDB and DD4HEP format
  - Integration into LHCb simulation and reconstruction software framework ongoing



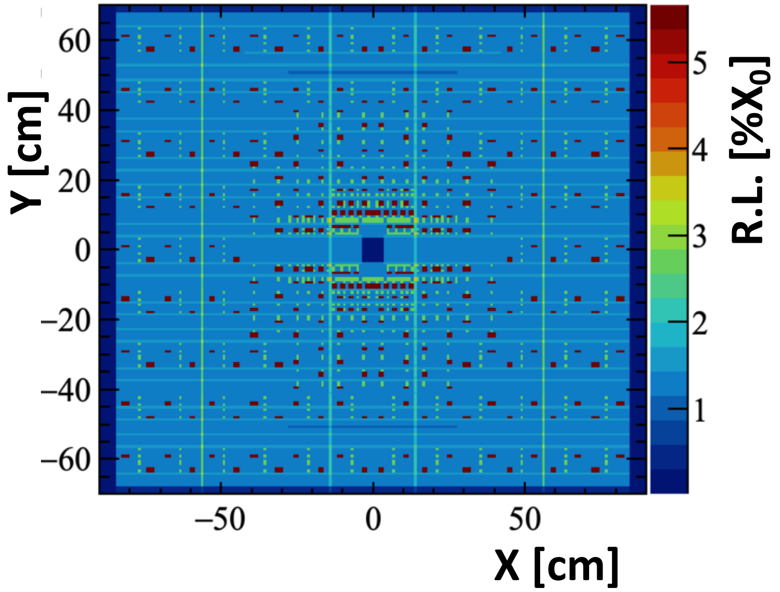


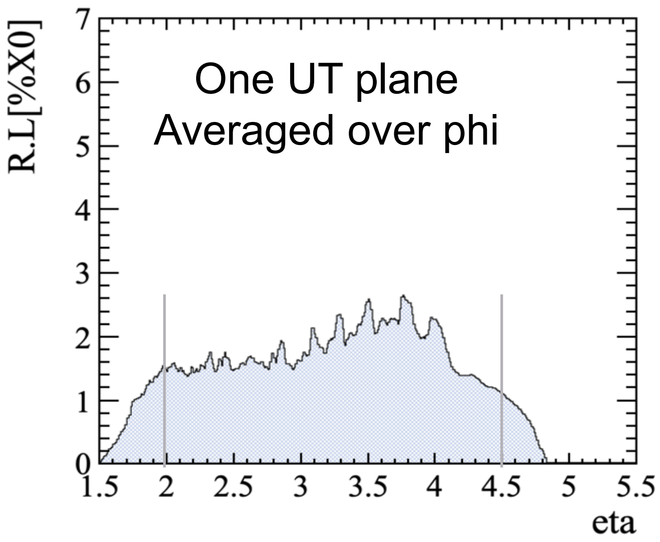
物质量扫描

- 基于目前探测器建模开展物质量扫描，有针对性开展减薄
  - VTRx+ 和 lpGBT 等器件数量尚未确定
  - 但已构成探测器优化的起点



(Preliminary)	Thickness [mm]	RL (2<h<4.5) [% X_0]
Pixel Sensor	0.200	0.24
lpGBT	1.250	0.25
VTRx+	4.000	0.27
HybridFlex	0.300	0.42
Kapton Tape	0.100	0.14
BareStave	4.000	0.21
One plane	**-**	**1.54**





总结

- LHCb上游径迹探测器 UT 已完成安装，开始运行调试
- 面向十年后的 LHCb 二期升级，UT 需要全新设计
  - 高压CMOS是有希望的传感器技术选项之一
  - 针对U2UT的传感器/系统设计/探测器模拟已开始
- LHCb中国组在U2UT中起到核心领导作用

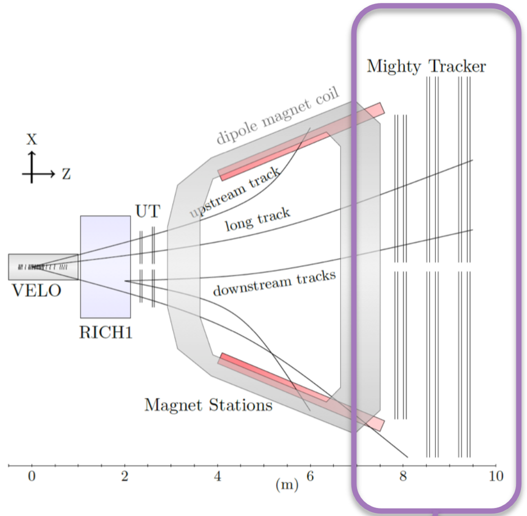
感谢聆听，欢迎关注！

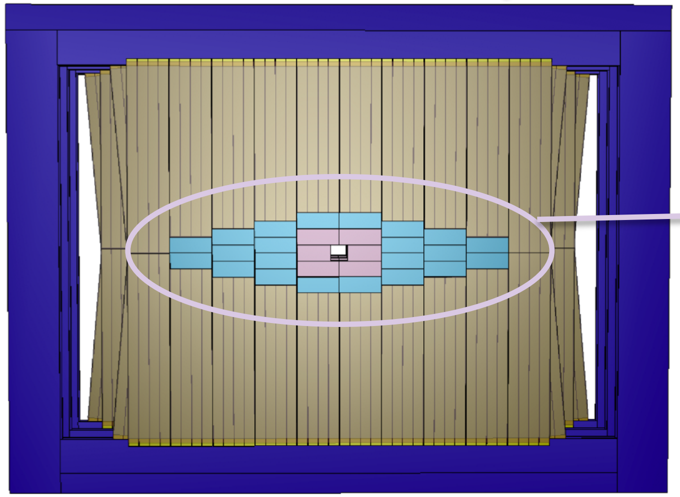
邮箱: liyiming@ihep.ac.cn

电话：18618321243

BACK UP

Synergy with Mighty Tracker





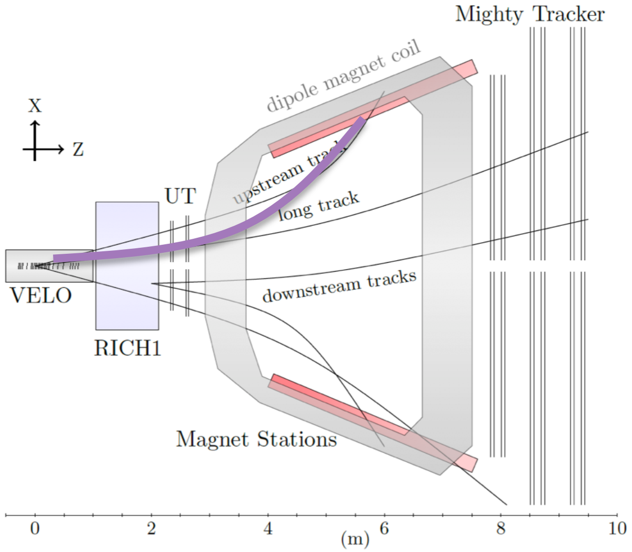
- Innermost region of SciFi will be replace by CMOS tracker
- Less radiation; more complex integration and more pressing timeline
- R&D based on HV-CMOS
  - Tests with ATLASPix3
  - Dedicated MightyPix1 on TSI 180nm received recently
- Synergy with UT under discussion

Pixel size	< 100 μm x 300 μm
In-time efficiency	> 99% within 25 ns window
Timing resolution	~ 3 ns within 25 ns window
Radiation tolerance	6 x 10^{14} 1 MeV n_{eq}/cm^2
Power consumption	< 150 mW/cm^2
Data transmission	4 links of 1.28 Gb/s each
Compatibility with the LHCb readout system	

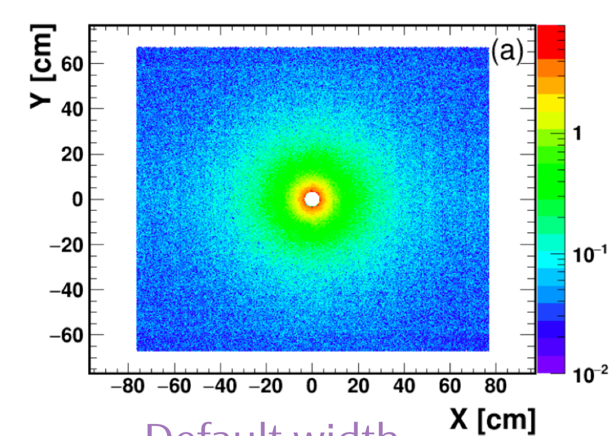
MightyPix1 floorplan
¼ of a full matrix size

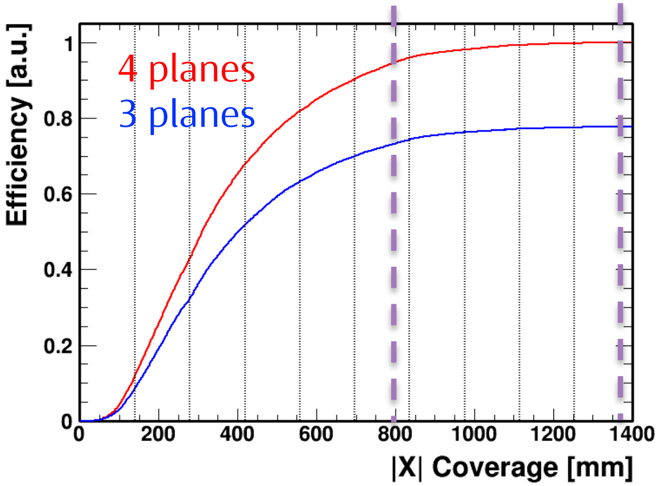
Detector Optimisation

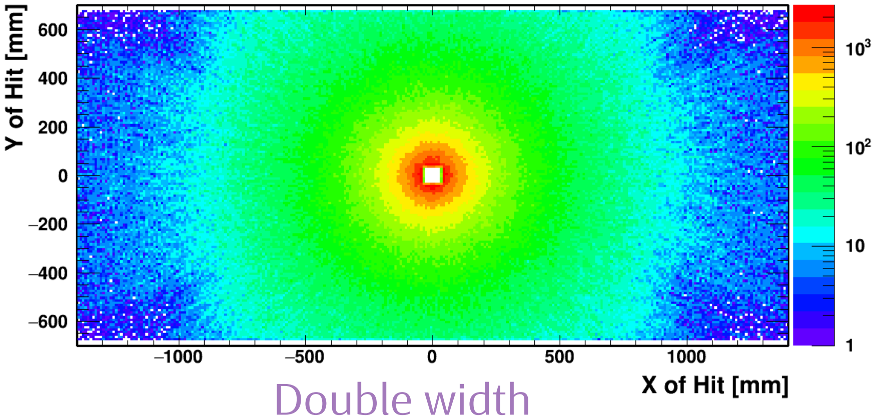
- Detailed studies foreseen to define / to optimise the UT design
  - Impact on tracking performance of VELO-UT(-MS)
  - Detector acceptance optimization associated with magnet station
  - Optimisation on number and layout of layers (3 vs. 4)
  - Estimation of material budget and cooling options
  - Effect of a possible additional timing layer with different technology
  - …



Default width Double width







Default width

Double width