CEPC顶点探测器研制进展

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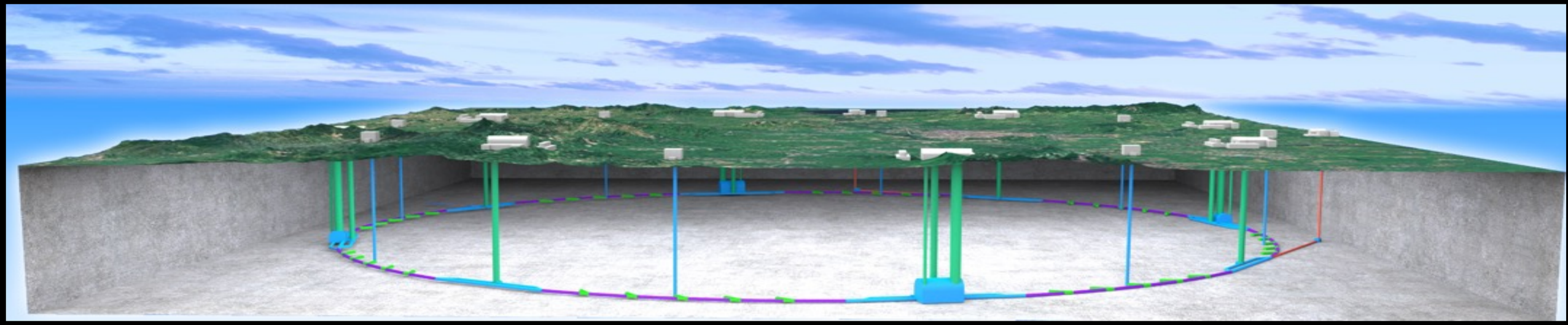
CEPC项目简介

2012年希格斯粒子发现后，中国科学家提出粒子物理发展路线：CEPC

- 100公里周长的双环正负电子对撞机
- **250GeV：大量产生希格斯粒子(4×10^6个)**
- **在90GeV：产生Z玻色子(>4×10^{12}个)**
- **在160GeV：产生W玻色子(>10^8个)**
- **预计今年完成加速器TDR设计**

CEPC Operation mode		ZH	Z	W^+W^-	ttbar
$\sqrt{s}$ [GeV]		~ 240	~ 91.2	~ 160	~ 360
Run time [years]		7	2	1	-
CDR (30MW)	L / IP [$\times10^{34}$ $cm^{-2}s^{-1}$]	3	32	10	-
	$\int L\,dt$ [ab^{-1}, 2 IPs]	5.6	16	2.6	-
	Event yields [2 IPs]	1×10^6	7×10^{11}	2×10^7	-
Run time [years]		10	2	1	5
Latest TDR (50MW)	L / IP [$\times10^{34}$ $cm^{-2}s^{-1}$]	8.3	191.7	26.6	0.8
	$\int L\,dt$ [ab^{-1}, 2 IPs]	20	96	7	1
	Event yields [2 IPs]	4×10^6	4×10^{12}	5×10^7	5×10^5



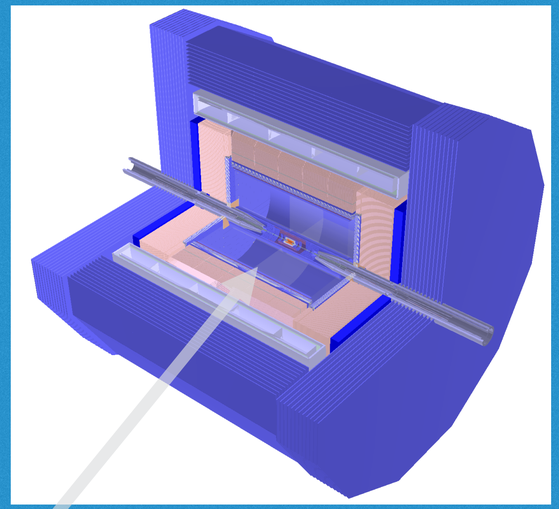
CEPC的4个探测器概念

CEPC plans for 2 interaction points

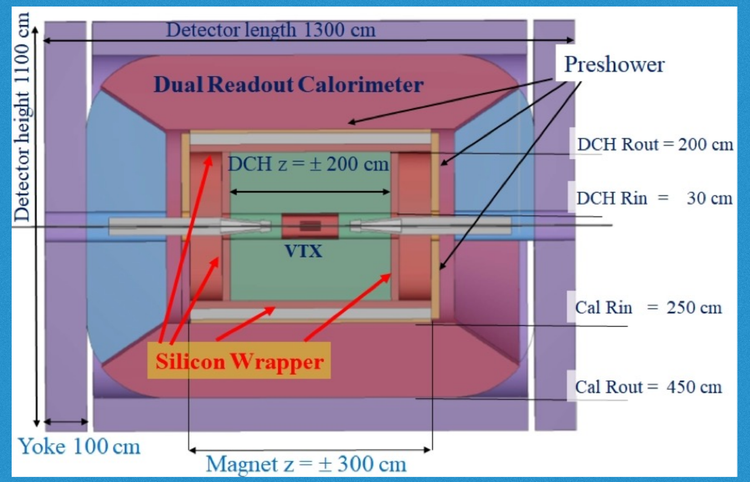
- 基于时间投影室与高颗粒度量能器的ILD-like
- 基于全硅径迹探测器（full-silicon） 概念
- 基于漂移室与双读出量能器 的IDEA概念
- 基于漂移室与4D晶体量能器的概念设计

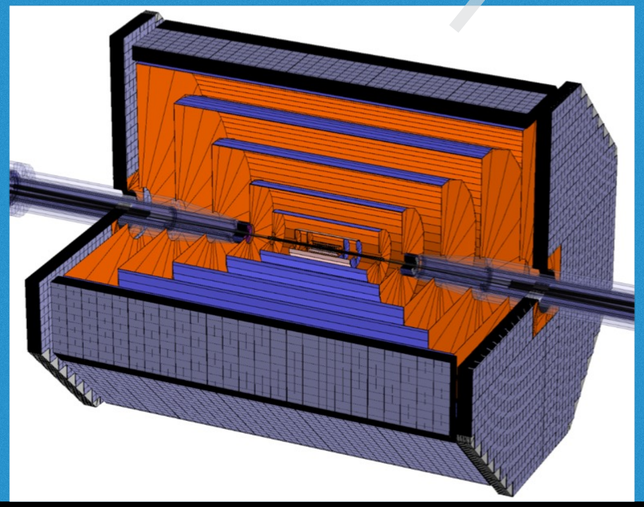
→ 4个探测器概念中都需要高精度的硅顶点探测器

ILD-like detector (3 Tesla)



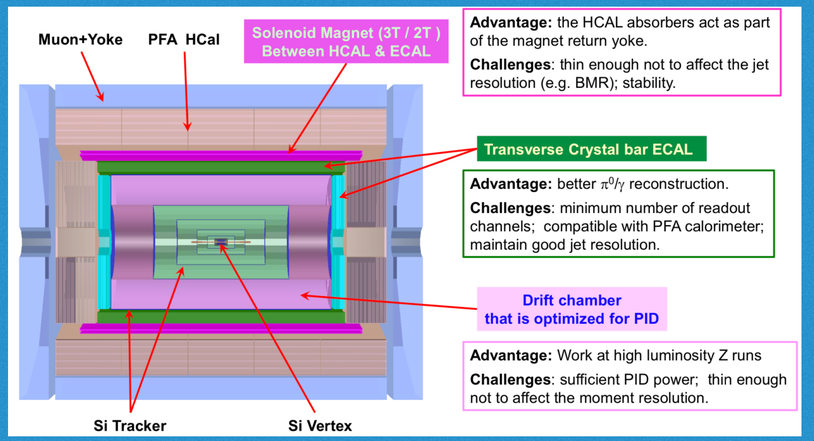
Low magnetic field concept (2 Tesla)





Full silicon tracker concept

4th concept



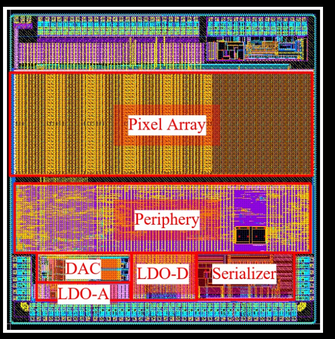
CEPC的科技部国家重点研发项目： 顶点探测器课题

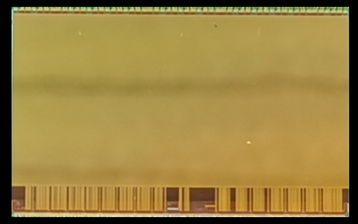
经费: 1200万
2018-2023年

参与单位	承担任务
IHEP（高能所）	**Full CMOS chip modeling, Pixel Analog, PLL block** **Detector module (ladder) prototyping** **Data acquisition system R & D** **Vertex detector assembly and commissioning**
西北工大	**CMOS sensor chip: Periphery Logic, LDO**
山大	**CMOS sensor chip: Bias generation, TCAD simulation** **Sensor test board design**
南大	**Irradiation, test beam organization**
华中师大/西班牙**IFAE**研究所	**CMOS sensor chip: Pixel Digital**

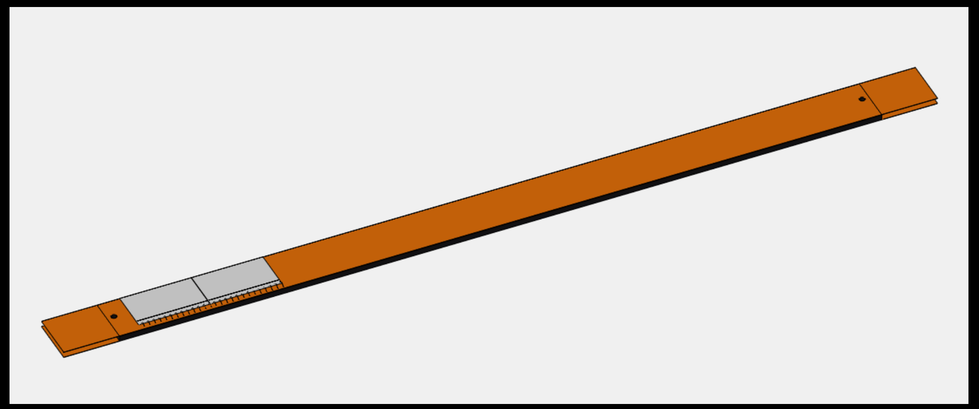
CEPC顶点探测器样机项目

CMOS 图像传感器芯片设计

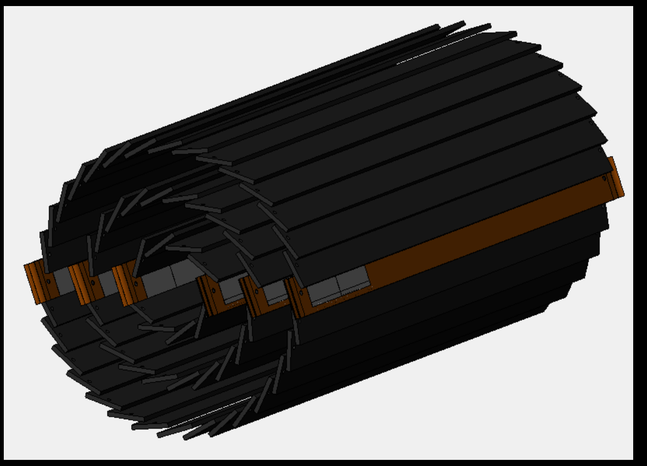


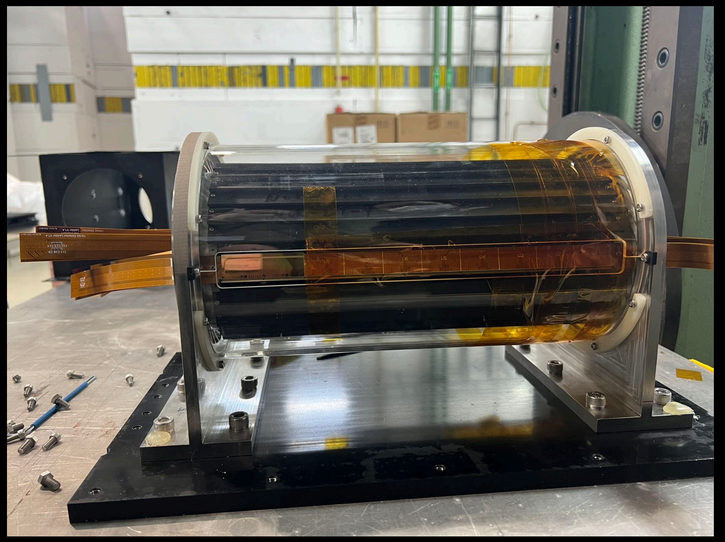


探测器模块组装



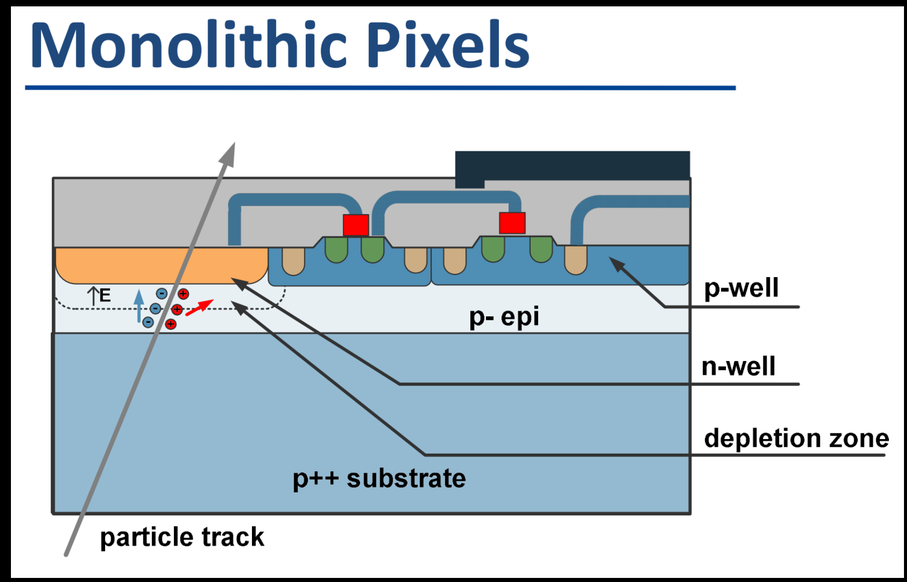
顶点探测器样机整机组装





CMOS 像素传感器芯片设计的挑战

- 现有的单片集成型CMOS 传感器芯片不能满足CEPC要求
  - 像素尺寸小→ high resolution (3-5 μm)
  - **抗辐照能力: >1 Mrad (per year)**
  - 高计数率-> CEPC Z pole 高亮度运行 (40MHz 的对撞频率)

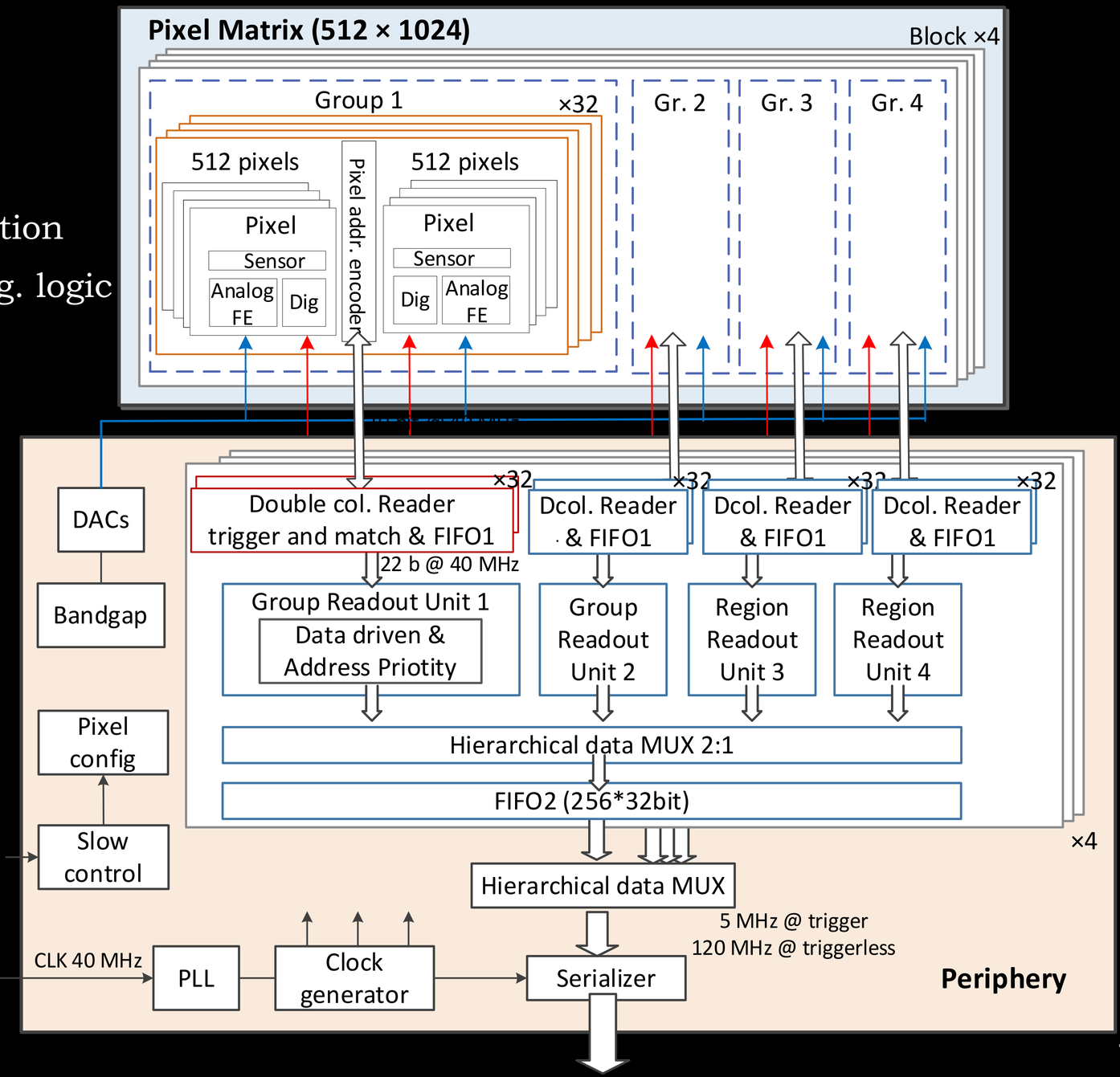


	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

TaichuPix（太初）芯片的读出架构

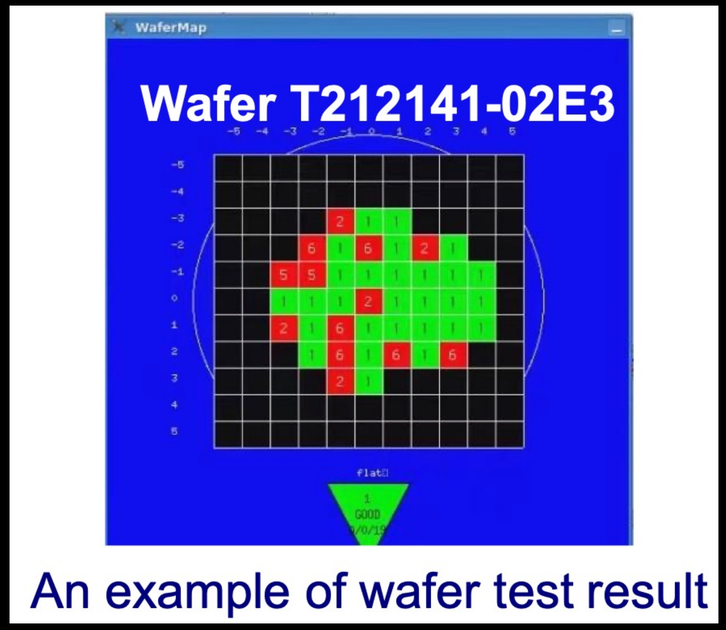
- 数据驱动的列基读出架构
- 实现CPEC需要的高空间分辨与高速读出

- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Readout time: 50 ns for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

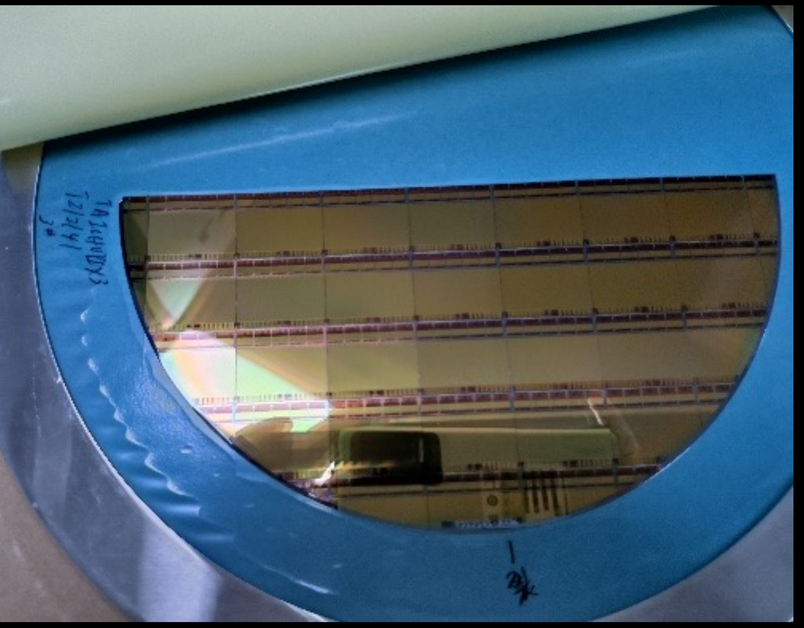


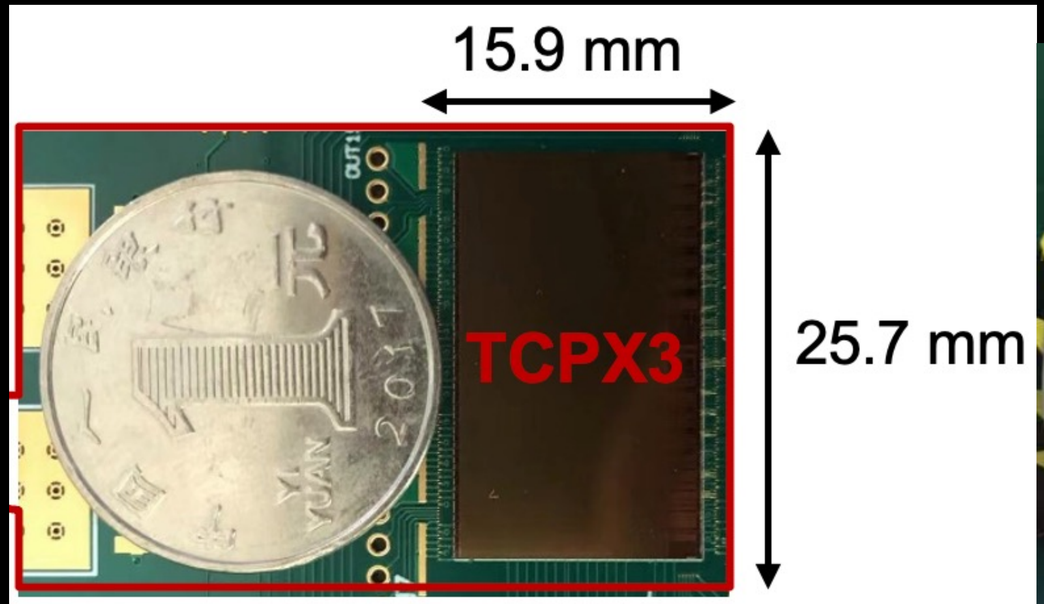
TaichuPix3（太初3） 芯片工程批流片

- 经过三次流片实现了全功能全尺寸太初芯片
- **CEPC首个全尺寸、全功能的像素探测器芯片**
  - **1024×512 像素，芯片尺寸：15.9×25.7mm**
    - **25μm×25μm 像素尺寸**
    - **工艺: Towerjazz 180nm CIS process**
  - 晶圆级探针卡测试也验证了成品率

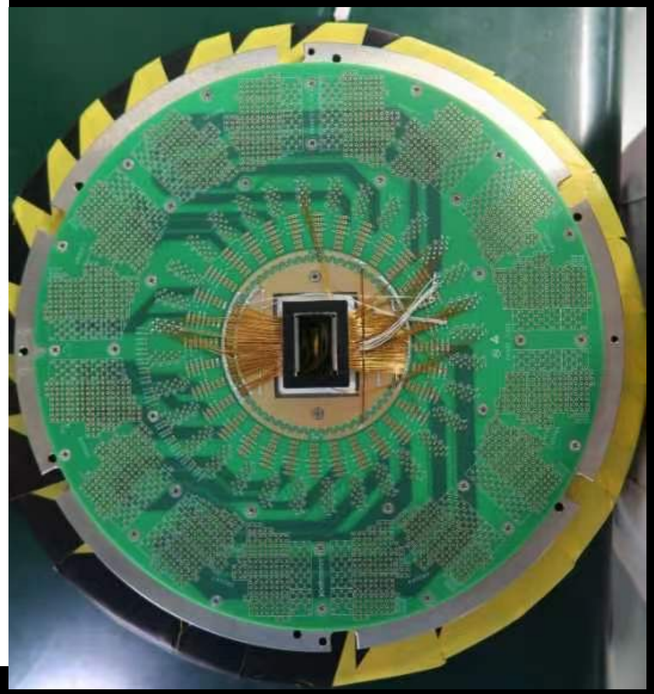


An example of wafer test result



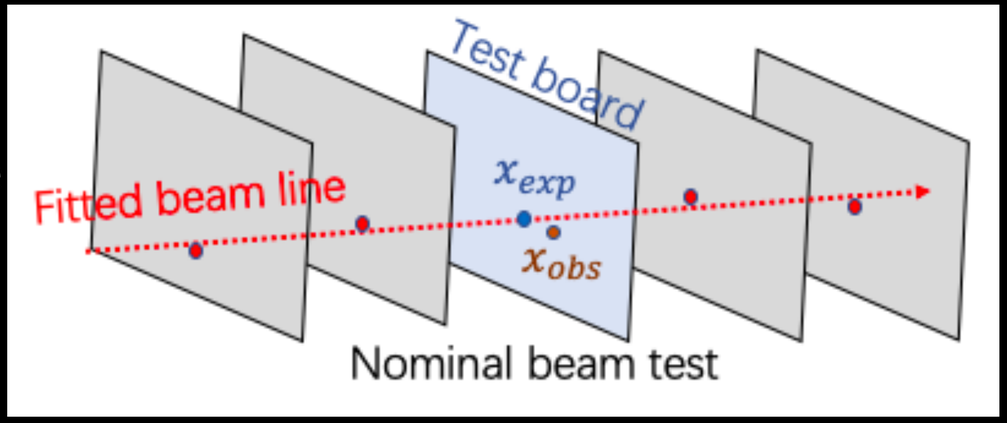


TaichuPix-3 chip vs. coin

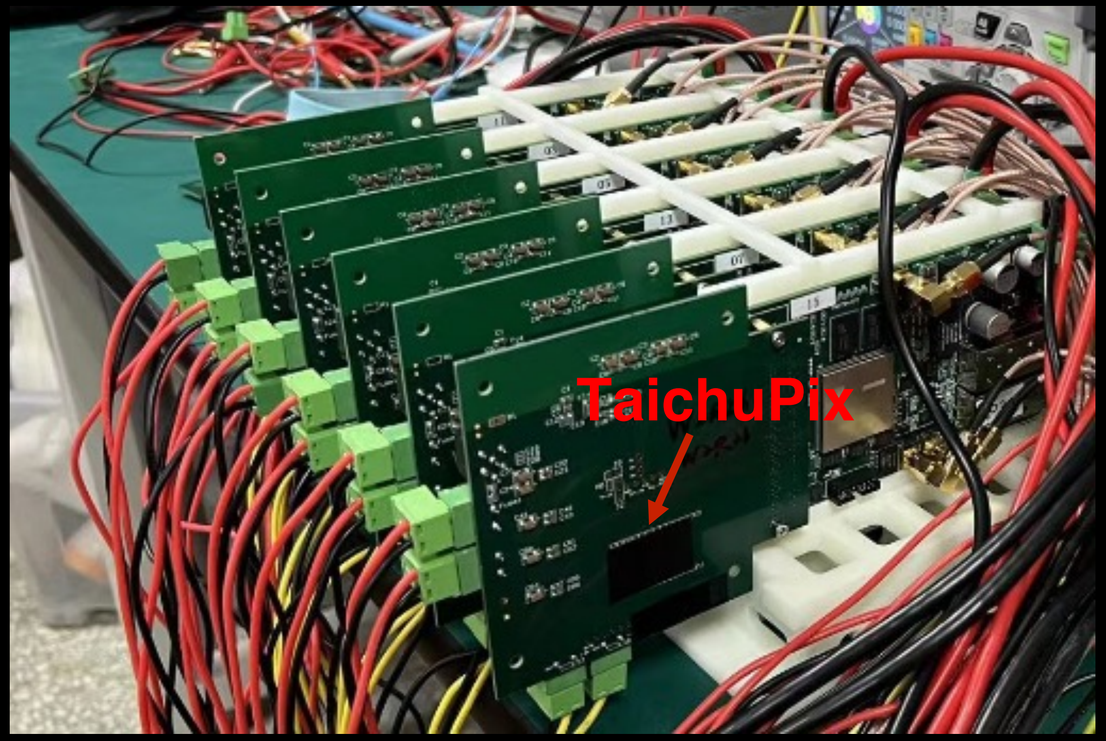


束流测试中空间分辨率的测量

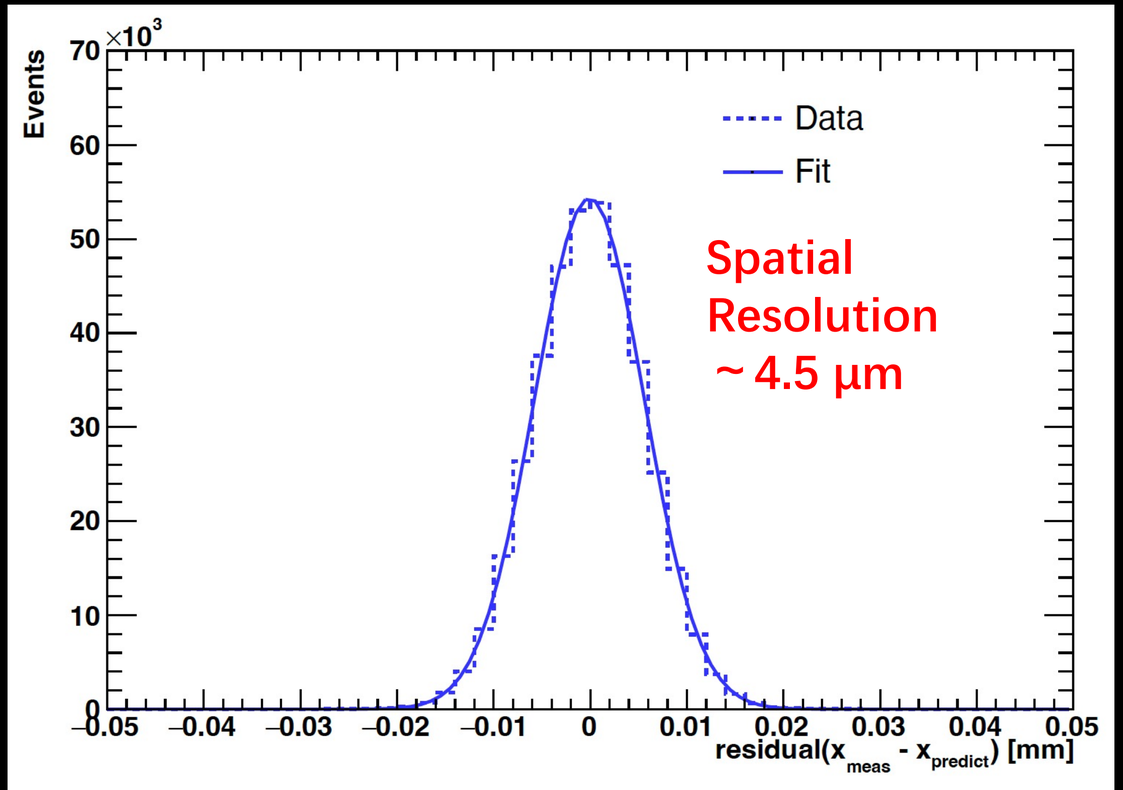
- 用6个太初3芯片研制了束流望远镜。
  - 在德国DESY进行束流测试（4-5 GeV 电子束），1kHz rate
  - 用其中5层太初芯片作为束流望远镜
  - 其中一层为待测探测器（DUT）
  - 空间分辨率达到4.5 μm



太初芯片组成的束流望远镜。

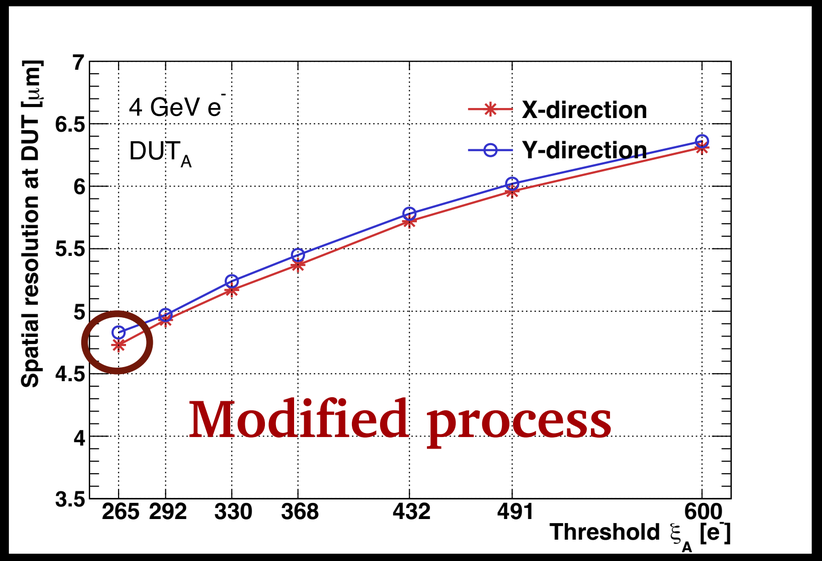


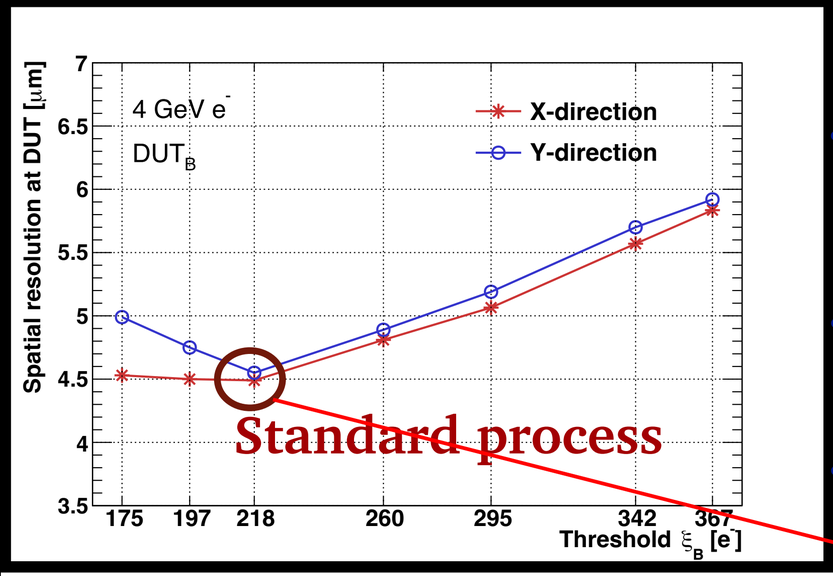
DUT测量位置与望远镜径迹预测位置的残差



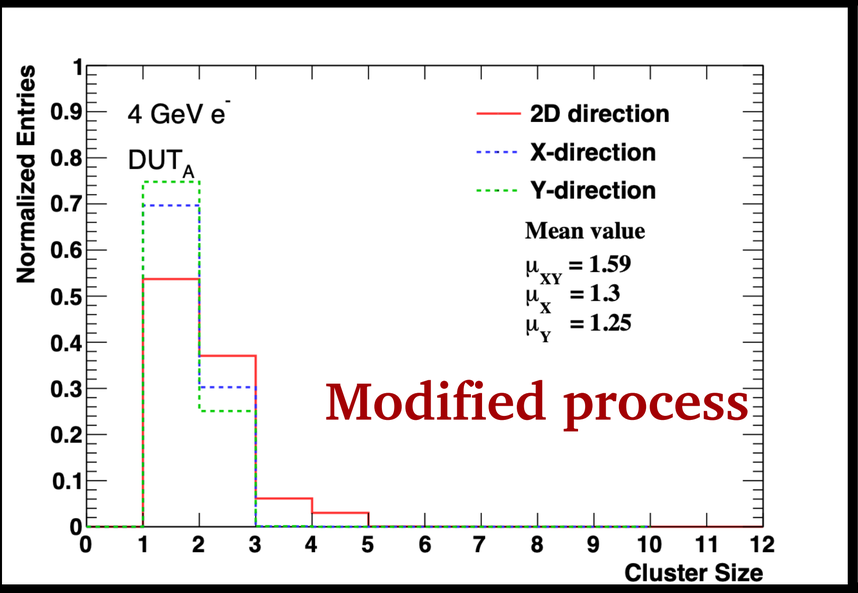
太初芯片的空间分辨率 Vs 阈值

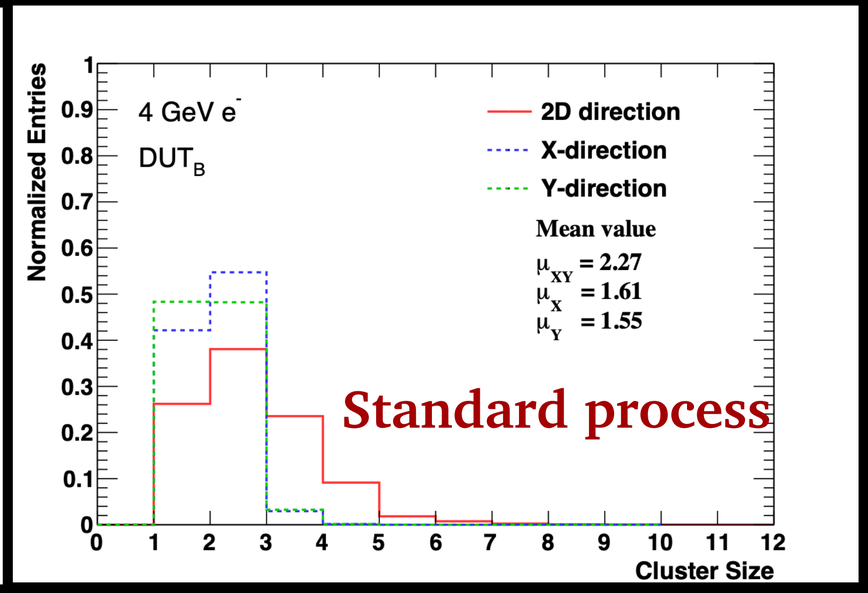
- 在优化芯片阈值后，探测效率可以达到4.5 微米
  - 低阈值情况下，charge sharing多，空间分辨率提高

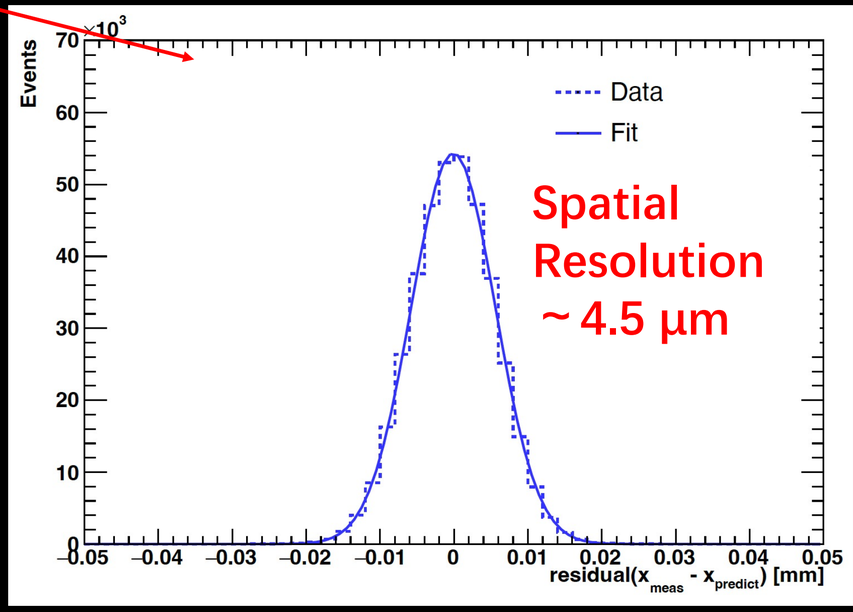




- Less charge sharing effects in modified process with full depletion
- If lowering the threshold, cluster size will be dominated by noise
-



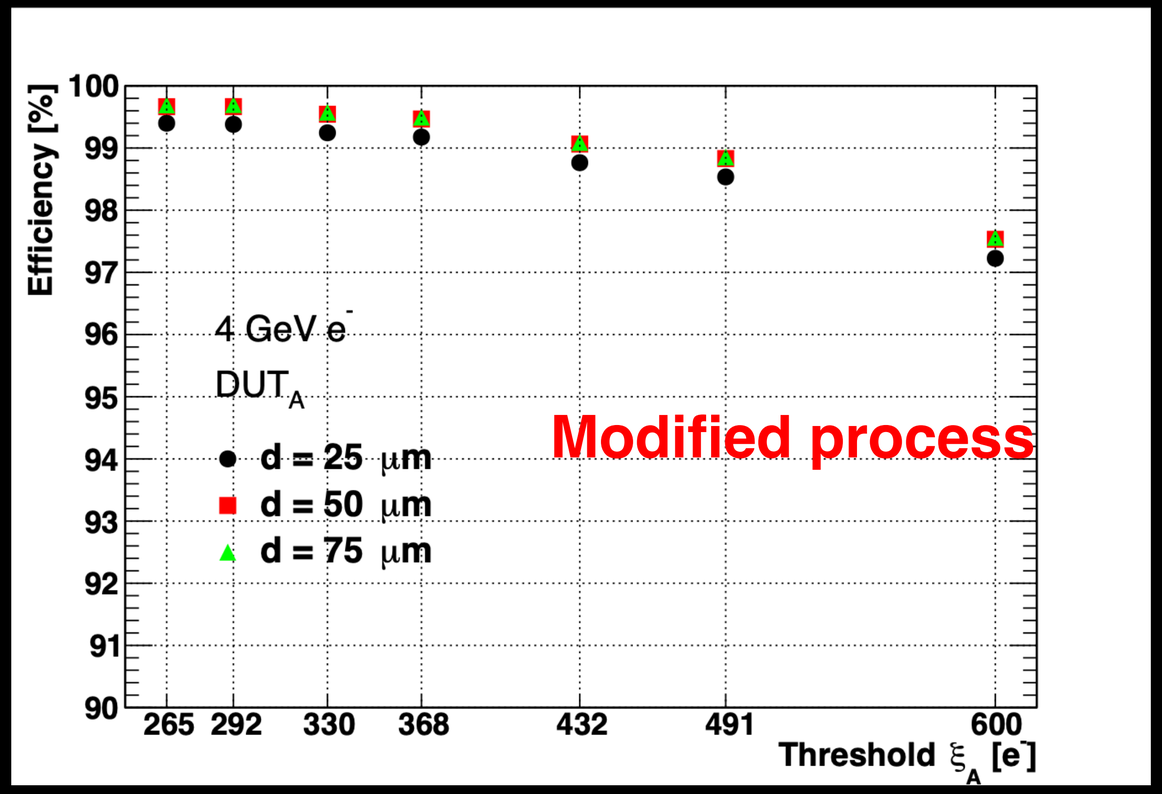


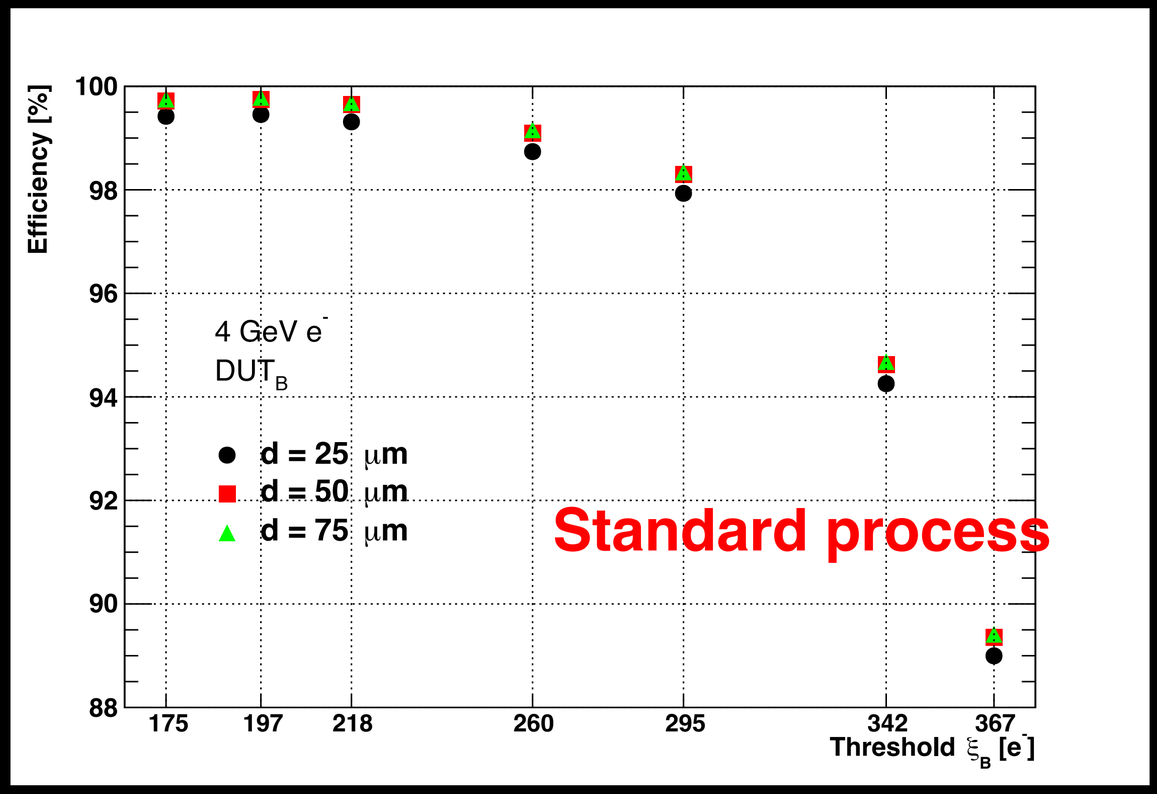


探测效率与阈值的关系

$$\epsilon = \frac{N^{matched\ Tracks}_{|x_{meas},y_{meas}-x_{pre},y_{pre}|<d}}{N^{Tracks}_{tel}}$$

- 在优化芯片阈值后，探测效率可以达到99.4%
- Modified工艺比标准工艺探测效率稍高，由于耗尽层厚度增加

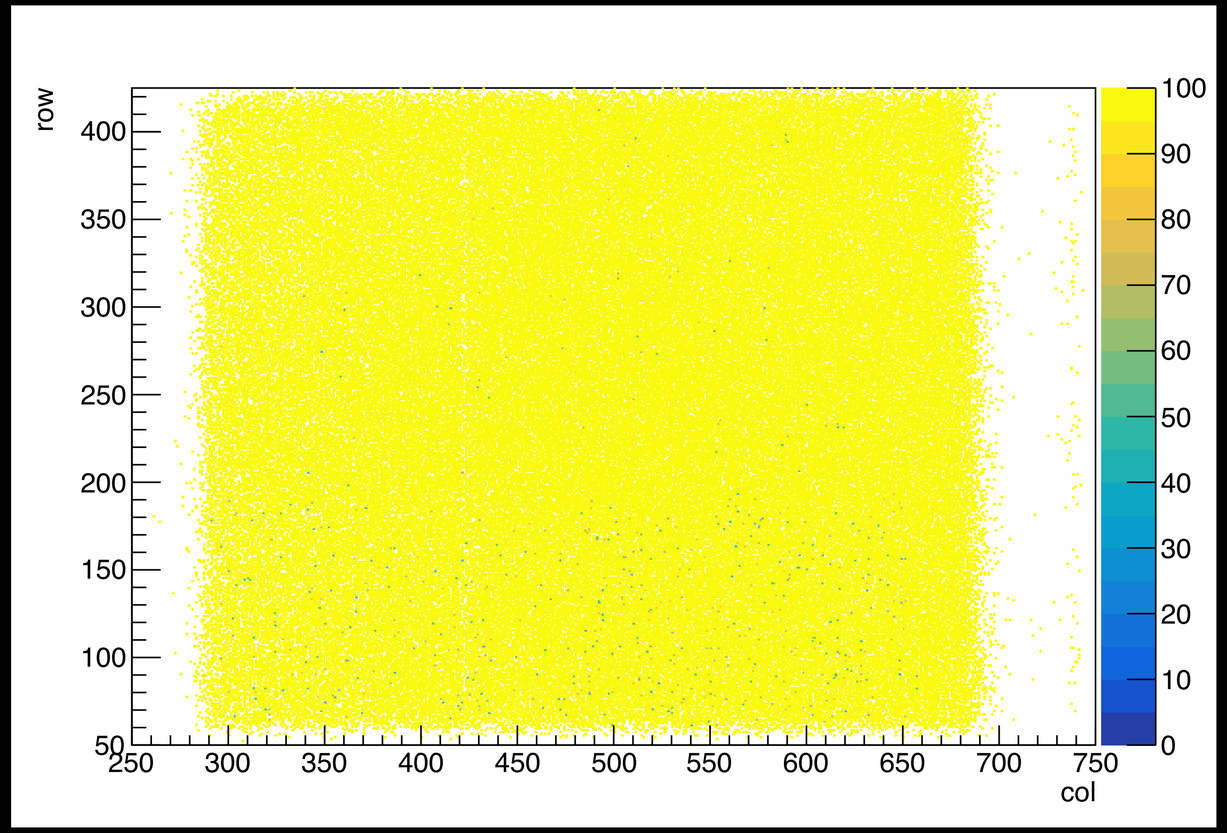




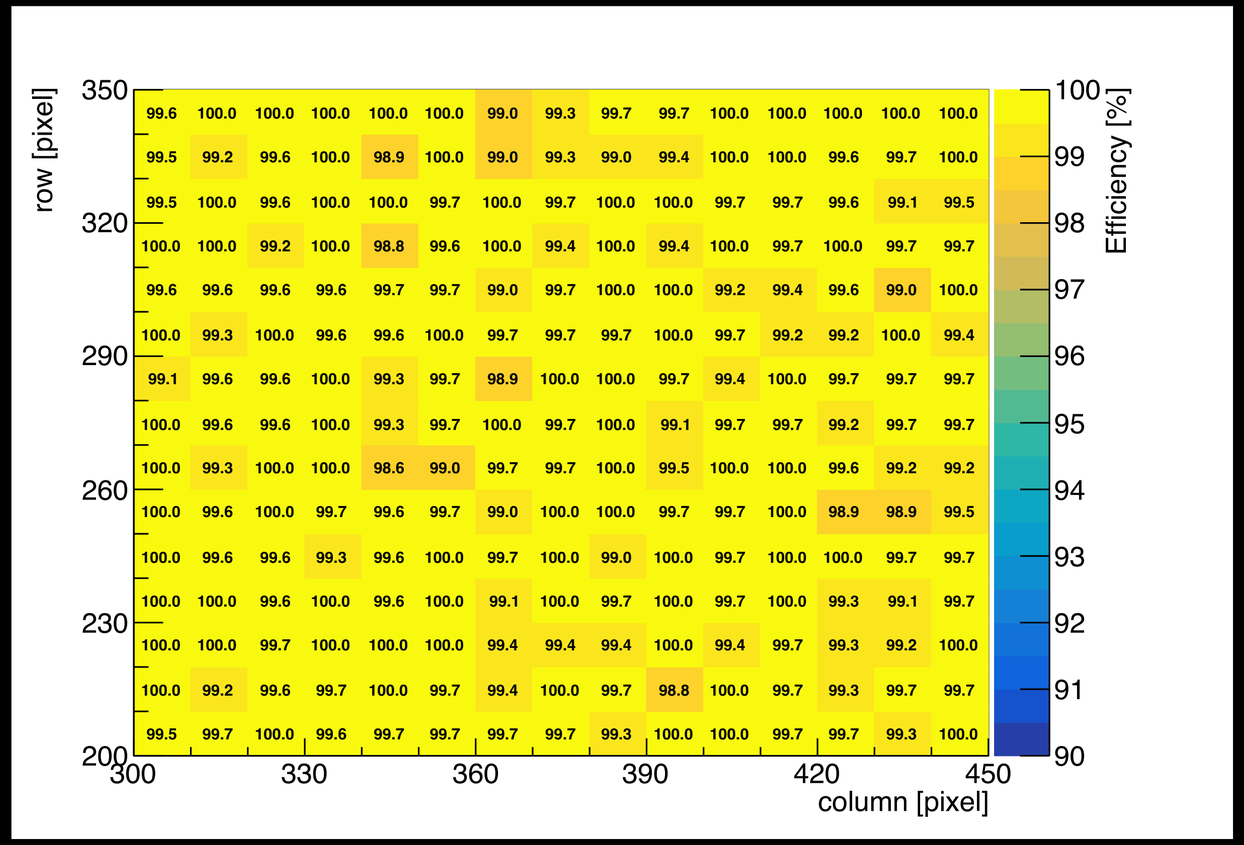
探测效率的均匀性

- 在优化芯片阈值后，探测效率可以达到99.4% efficiency
- 在单个像素内不同位置、与像素阵列内的各像素有很好的效率均匀性

像素阵列中探测效率的均匀性



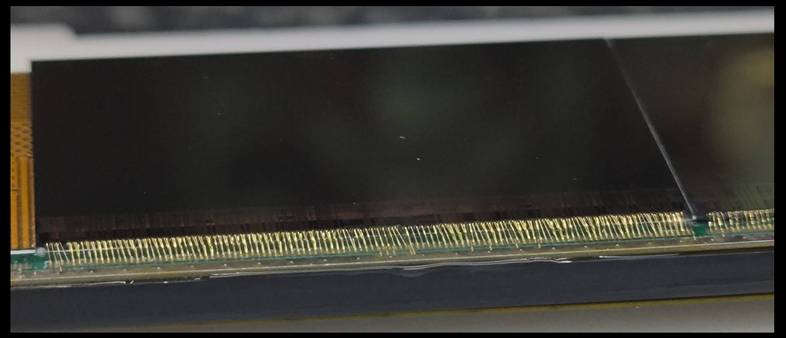
像素阵列中探测效率的均匀性（局部放大）



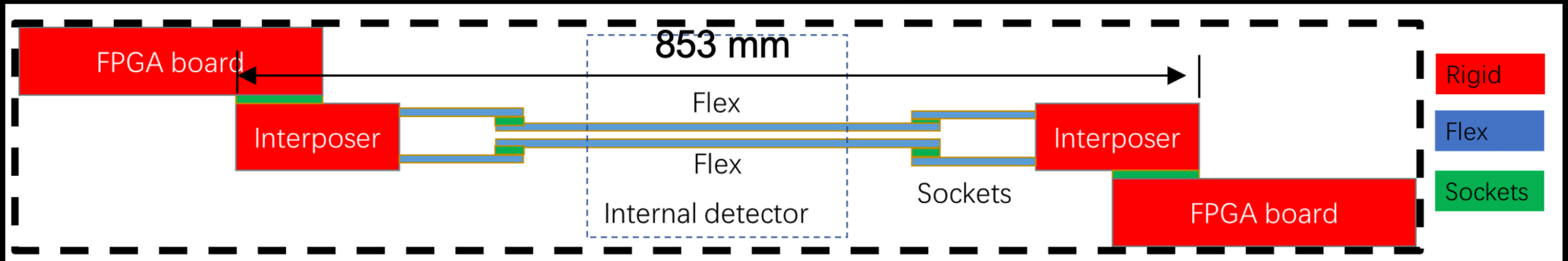
探测器模块的研发

- 探测器模块= 10个太初芯片 + 柔性电路板 + 支撑结构
  - 探测器模块与柔性电路板通过打线连接。
- 挑战
  - 柔性电路板太长，在电源与CEPC需要的高速信号传输方面有挑战
  - 物质量要低，柔性板金属层少，有屏蔽等问题

Taichupix chip wire bonded on FlexPCB

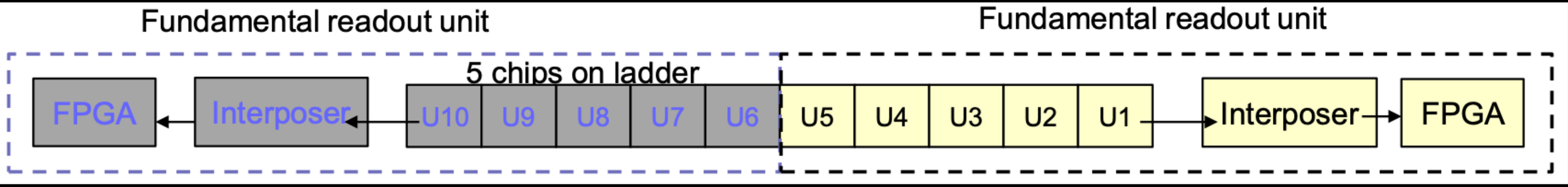


Ladder readout system

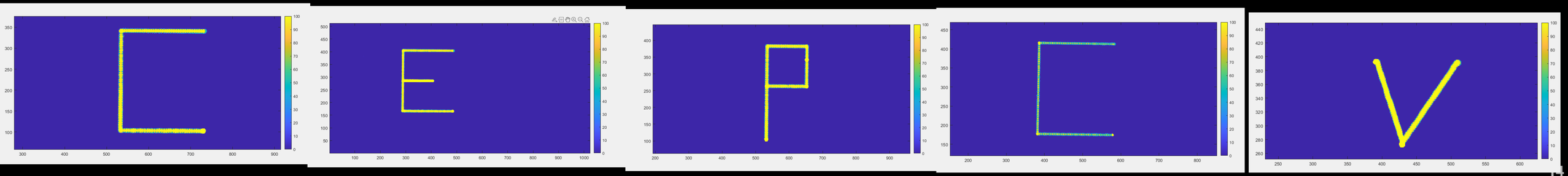


探测器模块的激光测试

- 探测器模块采用双边读出的方式
  - 每一边的FPGA板，读出柔性板上一边5个太初芯片
- 用激光扫描实验进行单个模块的功能性
  - 用激光扫描探测器模块表面，每次移动50 μm
  - →可以清楚看到激光扫描5个芯片，在太初芯片取数中留下“CEPCV”的字样
  - →证明探测器模块中多个太初芯片同时工作



Laser tests on Taichupix chip on full ladder
（”CEPCV” pattern by scanning laser on different chips on ladder ）



双面探测器模块（ladder）的组装

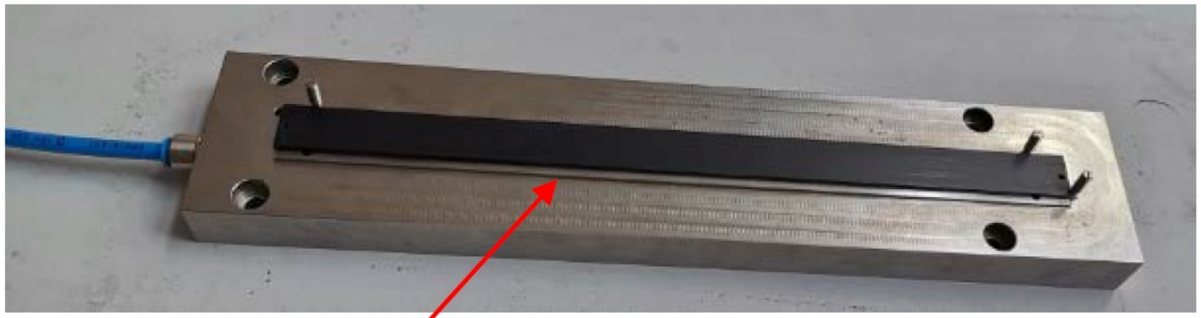
- CEPC顶点探测器模块是双面的
  - 正反两面分别有两个柔性板 + 碳纤维支撑结构
- 挑战：
  - 探测器模块正反两面都有打线
  - 需要专用工装

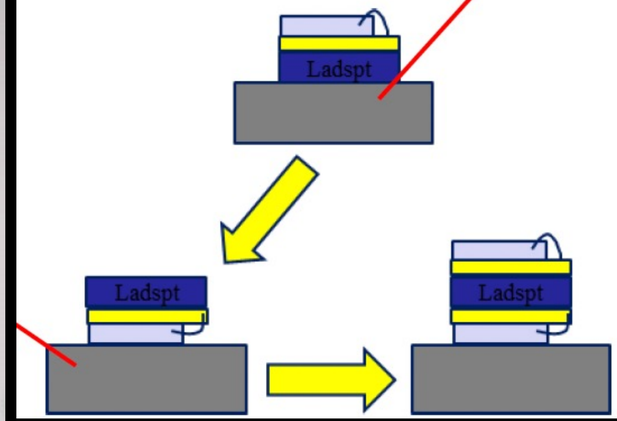
碳纤维支撑结构的设计与研制

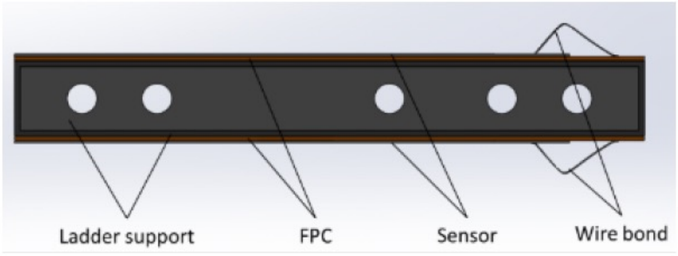
正反两面探测器模块组装工装与流程

Module fixation and protection components

Vacuum plate for flex and CFRP support fixation







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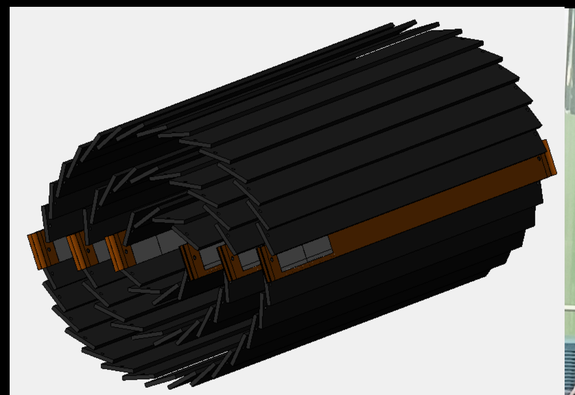
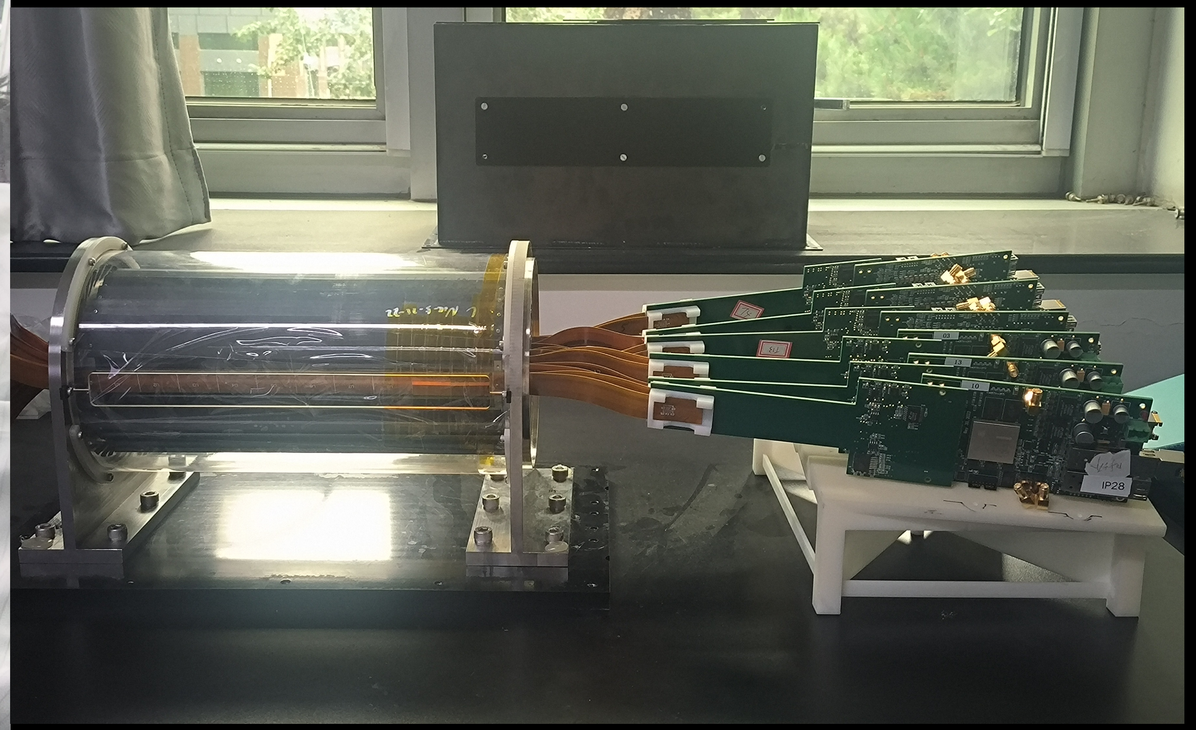
顶点探测器样机的组装

- 筒型的顶点探测器样机组装
  - 6个双面模块，组装到顶点探测器支撑结构上
  - 共有12个柔性电路板，24个太初芯片，同时工作

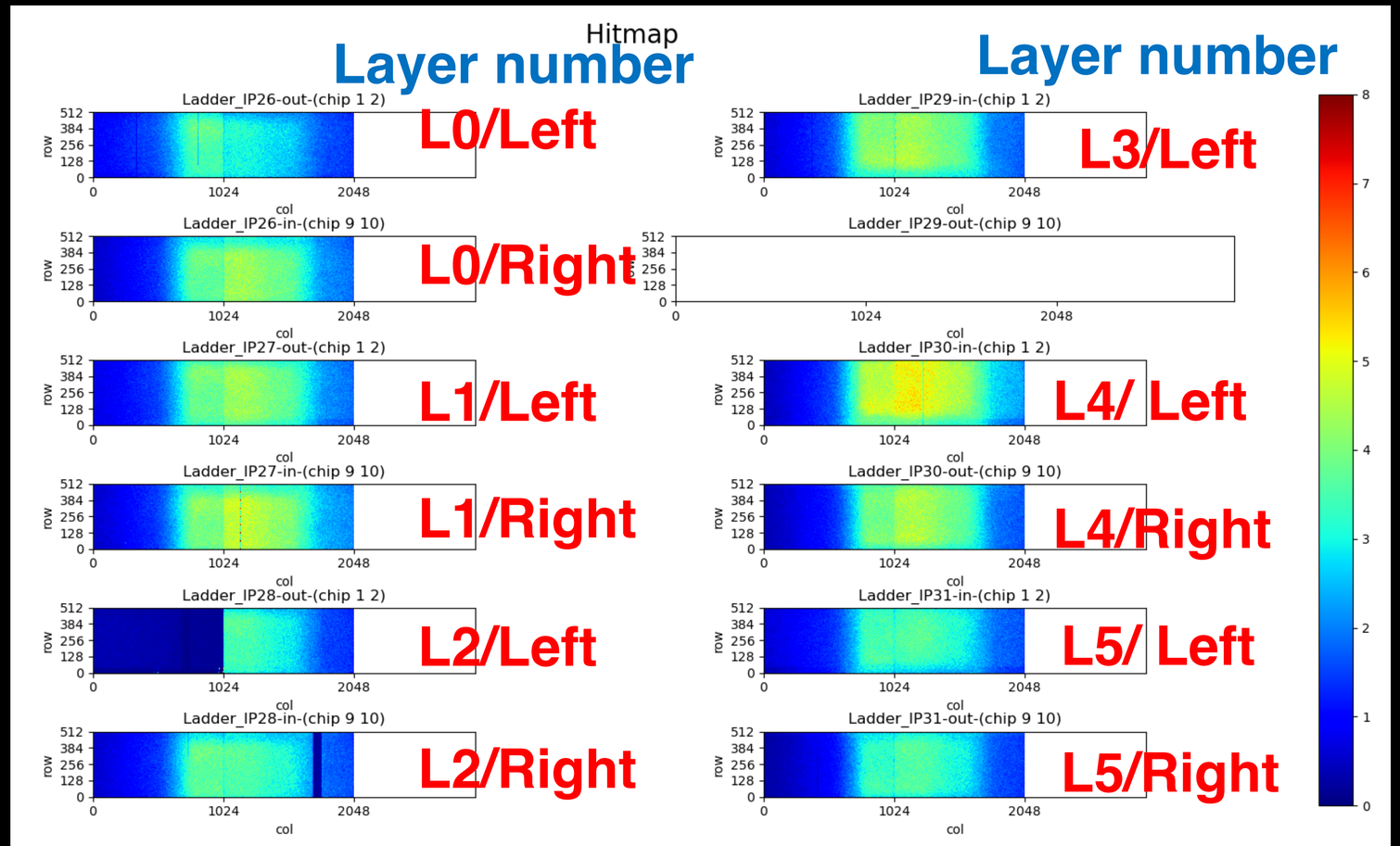




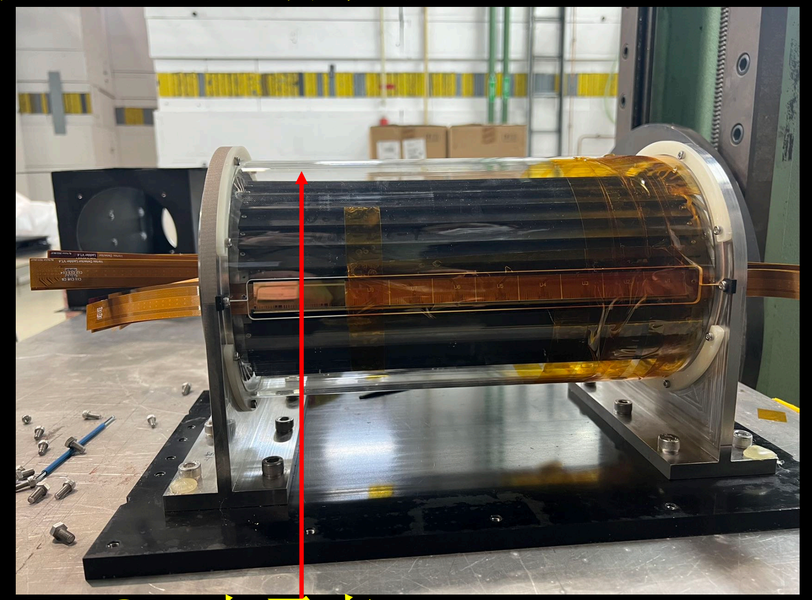
顶点探测器样机的束流测试

- 顶点探测器样机在2023年4月在德国DESY进行束流测试 （5-6GeV电子束）
  - 12个柔性电路板，24个太初芯片，同时工作
  - 电子束斑(~2×2cm)清晰可见
  - 两周取数，记录了10亿条径迹

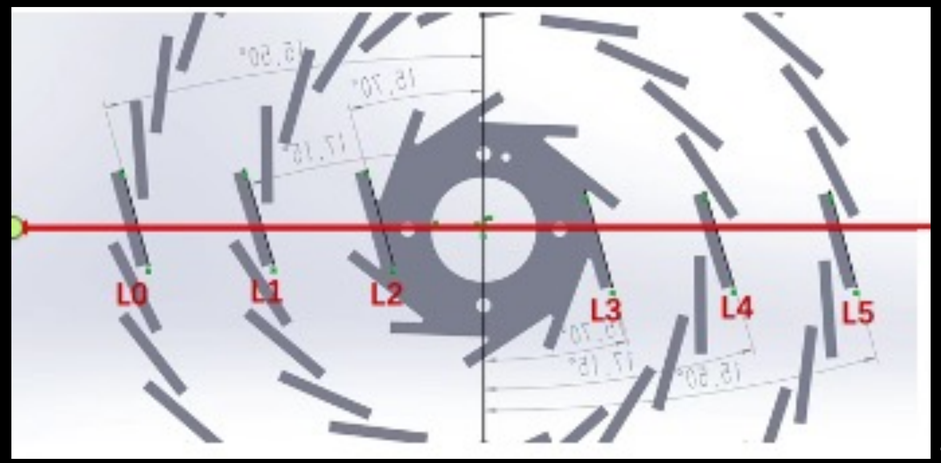
Hit maps of 24个太初芯片在顶点探测器样机上



顶点探测器样机在DESY

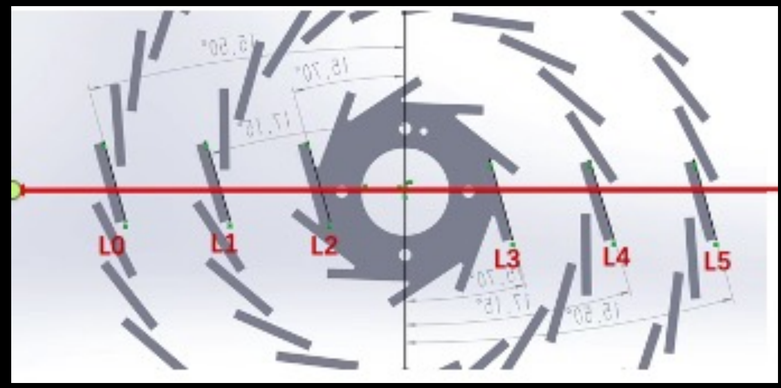


DESY 电子束

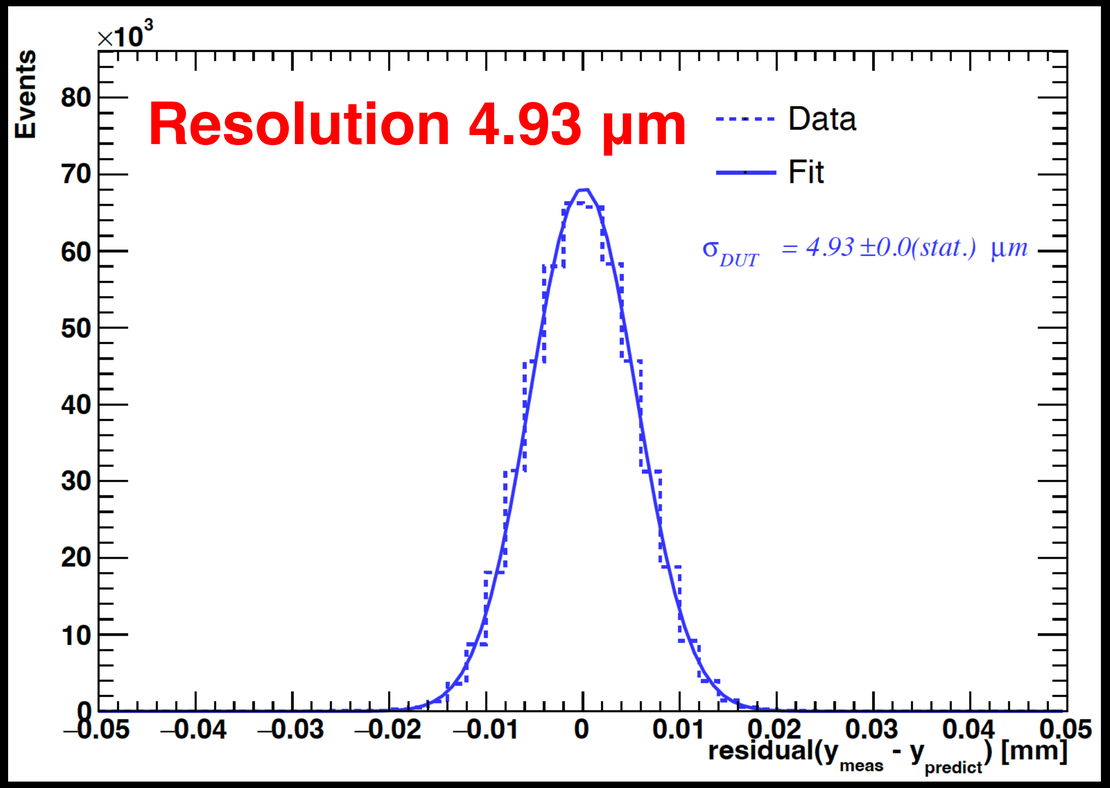


顶点探测器样机的束流测试

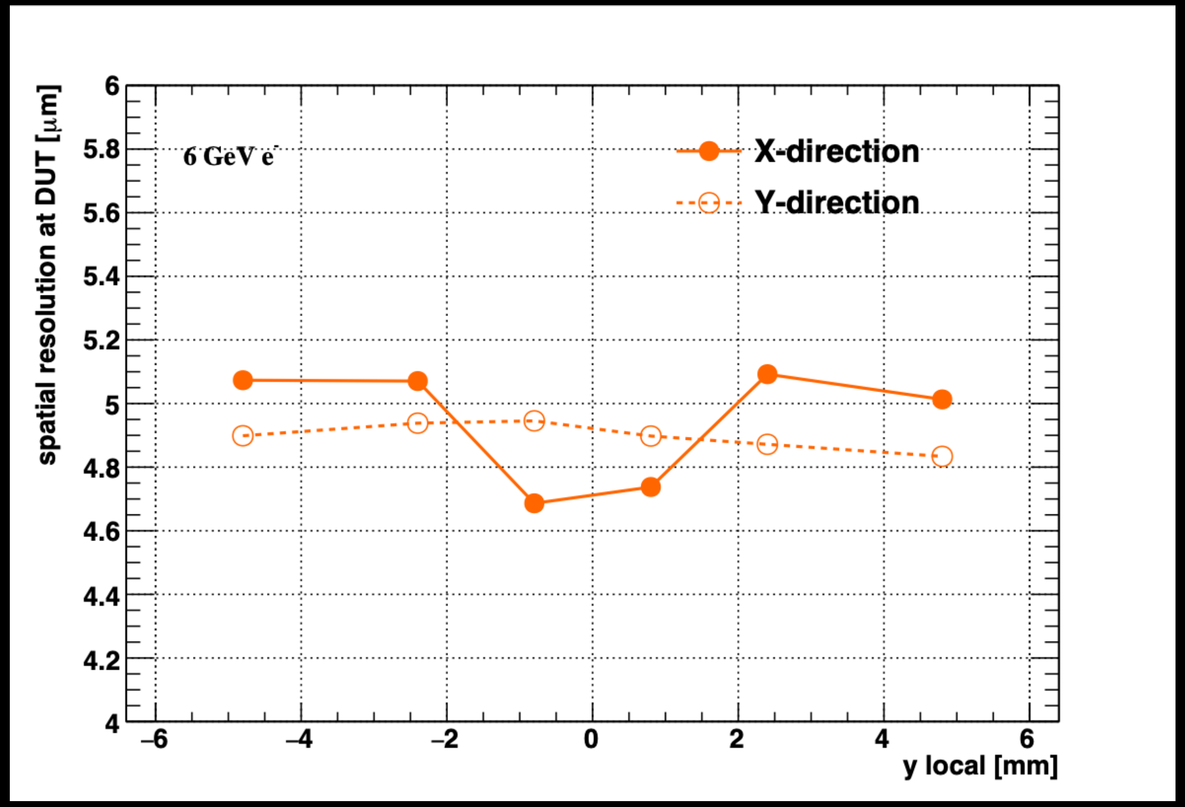
- 在德国DESY束流测试数据分析样机空间分辨率
  - 用其中一个单层太初芯片作为待测芯片（DUT）
  - 顶点探测器样机的其他层作为束流望远镜
  - 空间分辨率 达到 4.9μm (Y 方向）



DUT测量位置与望远镜径迹预测位置的残差



空间分辨率 VS DUT芯片击中位置



总结与展望

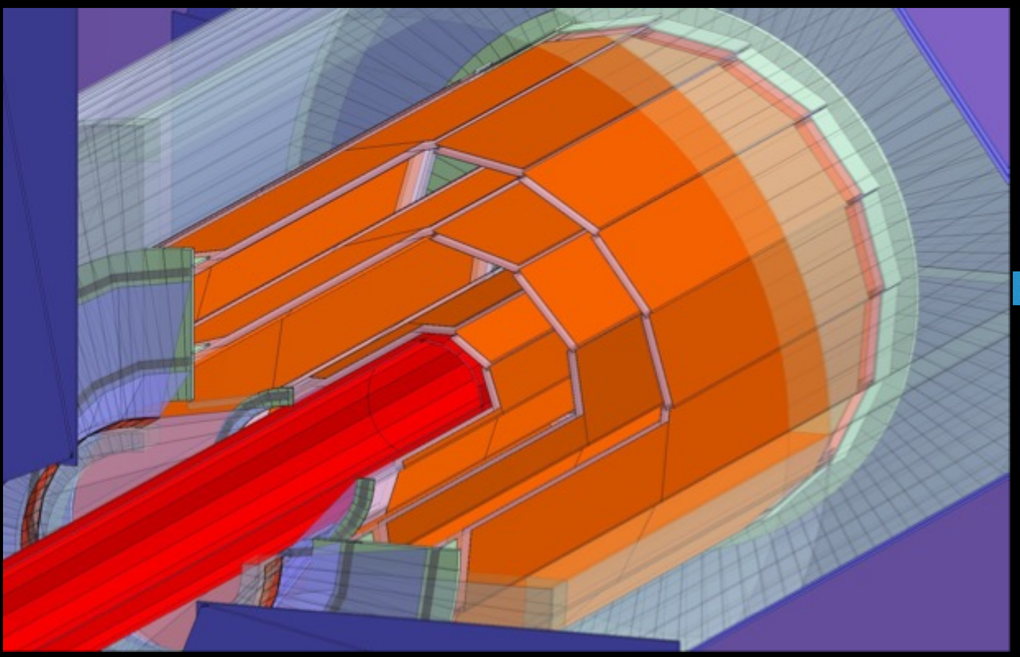
- 面向CEPC顶点探测器需求，开展TaichuPix芯片研发
  - 经过三次流片实现了全功能全尺寸（25.7 mm × 15.9 mm）芯片，CEPC首个全尺寸芯片
  - 采用单片式 CMOS像素探测器技术
  - 像素尺寸 25 μm × 25 μm, 读出时间 50 ns/pixel
- 基于全尺寸太初芯片初步研制了束流望远镜和探测器原型样机
  - 国内首个硅顶点探测器样机
  - 在德国DESY束流实验中，验证了其空间分辨率好于5微米，探测效率达到99.4%

	CEPC物理要求	测试结果	
空间分辨率	3-5 μm	束流望远镜：4.5 μm CEPC顶点探测器样机: 4.9μm	World leading
抗辐照性能 (total ionization dose, TID)	>1 Mrad	>3 Mrad	

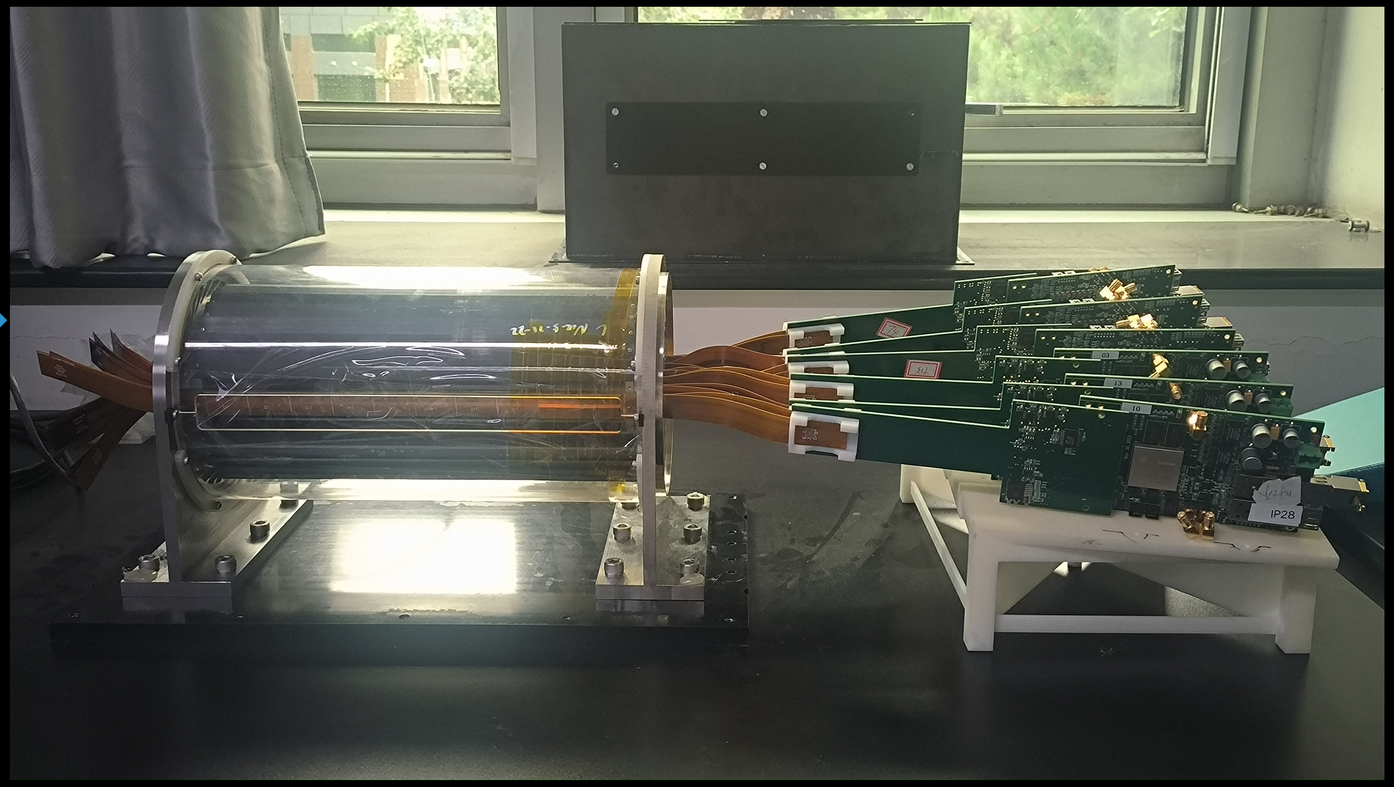
总结与展望（2）

- 从2016年CEPC 概念设计报告中顶点探测器概念
- 到2023年，组装硅顶点探测器样机

2016年CEPC 概念设计报告



CEPC硅顶点探测器样机(2023)

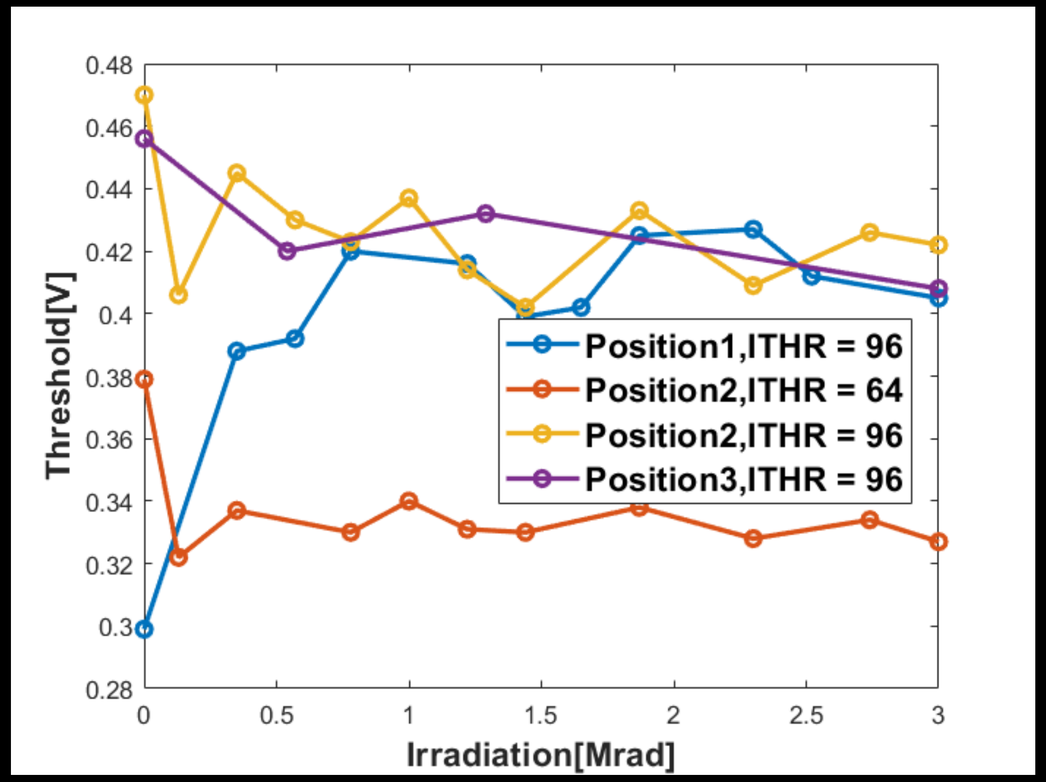


backup

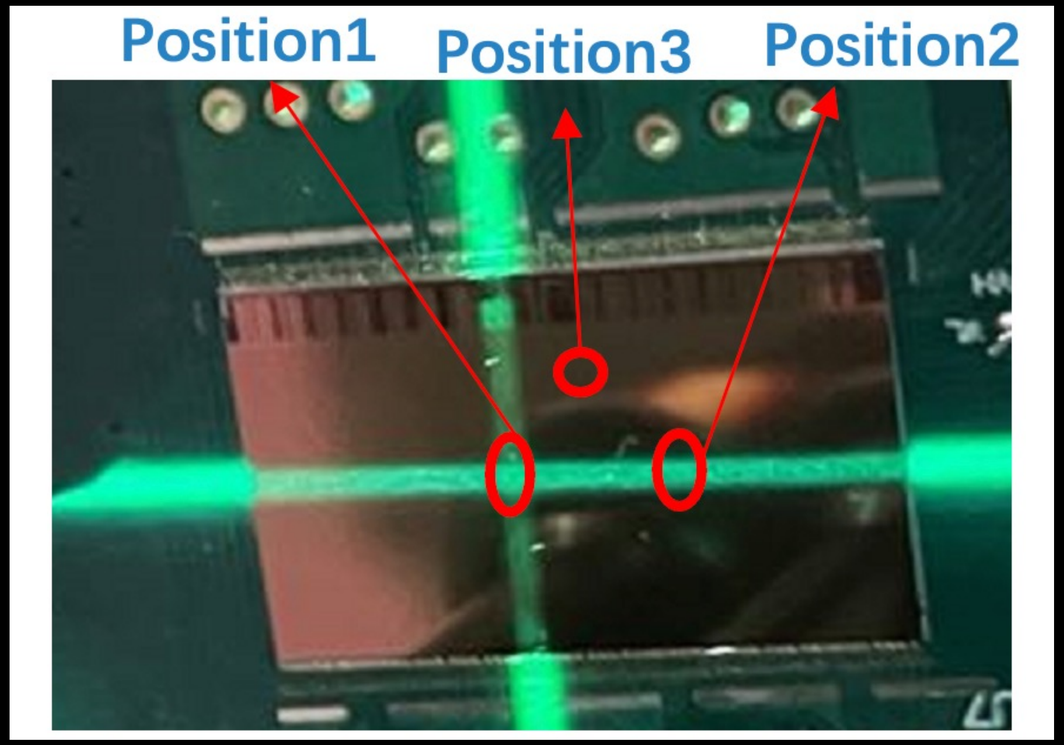
辐照实验

- Taichupix3 芯片在北京同步辐射线站（12keV 同步辐照光）上辐照到3 Mrad
  - 辐照后，芯片性能基本不变，达到项目指标>1 Mrad

Taichupix3芯片的辐照性能
像素的阈值vs. 辐照剂量



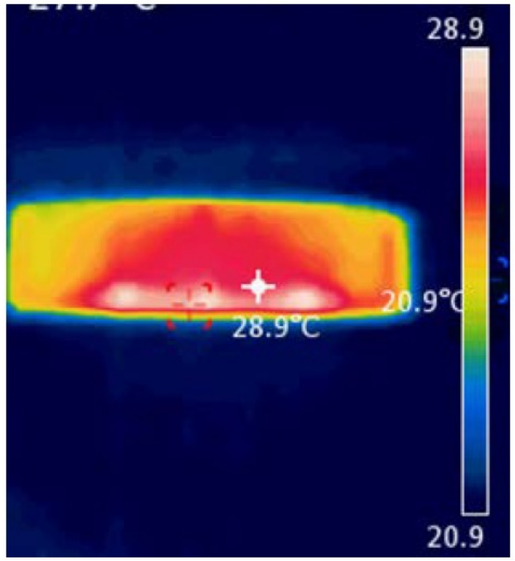
TaichuPix-3 irradiated at Synchrotron radiation beamline (12 keV X-ray)



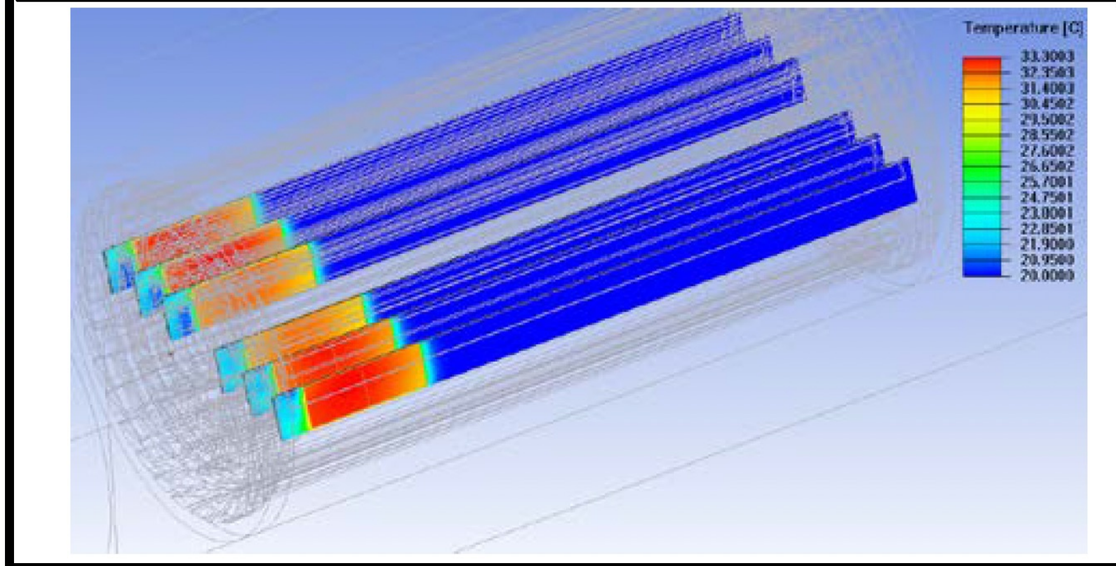
Air Cooling for vertex prototype

- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm2 (17.5 MHz clock in testbeam)
  - Before turning on the fan, chip temperature can go above 41 °C.
  - With air cooling, chip temperature can reduced to 25 °C (in average)
    - In good agreement to our cooling simulation
  - No visible vibration effect observed in position resolution offline analysis when turning on the fan

Chip temperature under cooling during beam test: Max 28.9 ℃



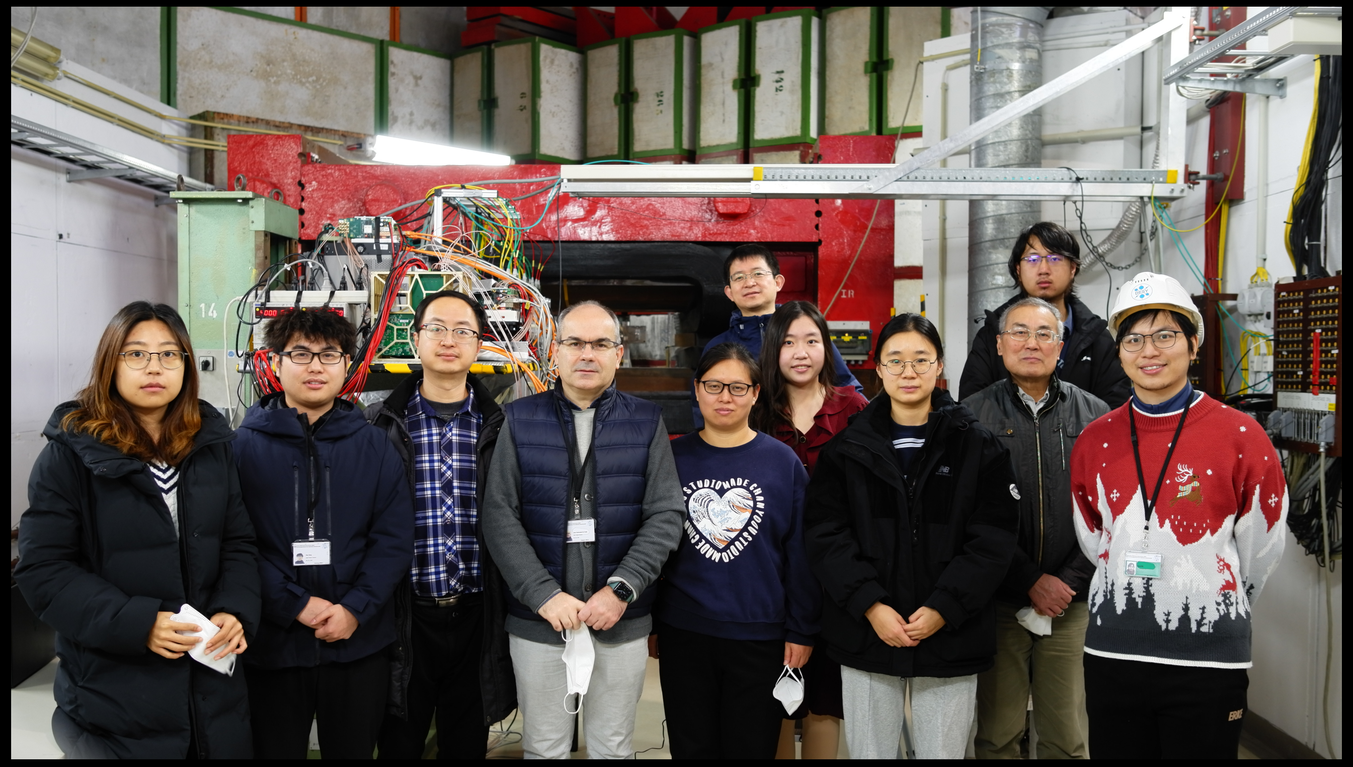
Prototype cooling simulation： Max 33.3 ℃



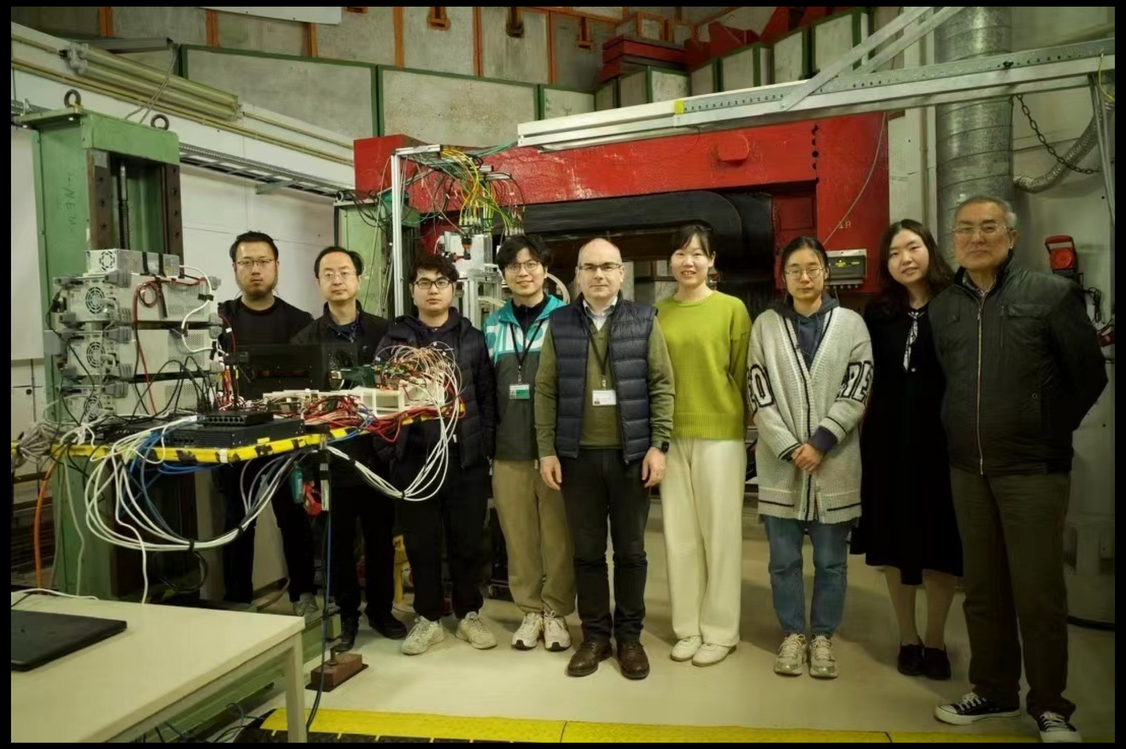
Test beam @ DESY

- 2nd testbeam: April 11-23 2023 DESY test beam in Germany (4-6GeV electron)
  - Vertex detector prototype testbeam
- 1st testbeam: Dec 12-22 2022 DESY test beam in Germany (4-6GeV electron)
  - TaichuPix Beam Telescope testbeam

2022 DESY test beam



2023 DESY test beam



Carbon fiber Support structure of the ladder

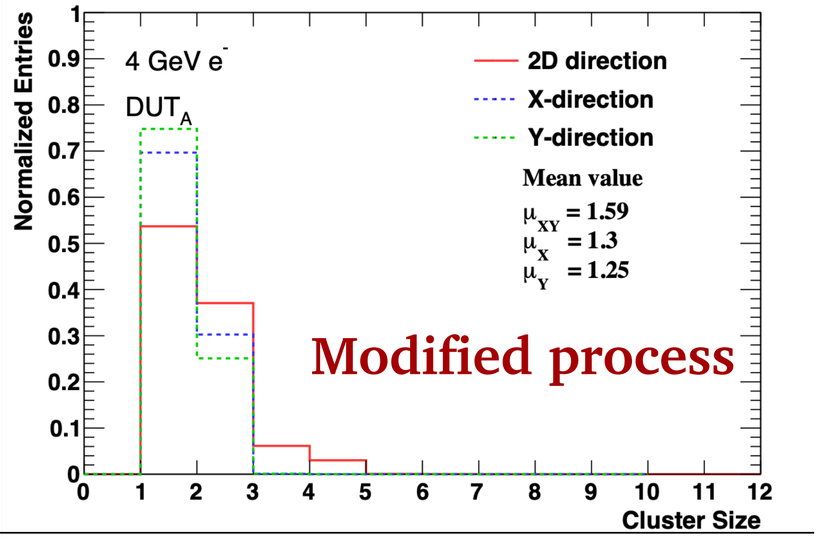
- Fabricated support structure prototype of the ladder (IHEP designed)
  - **4 layer of carbon fiber, 0.12mm thick for the whole support**
    - **Shallow design inside ladder support to reduce material**
  - **2~3 time thinner than conventional carbon fiber in China**

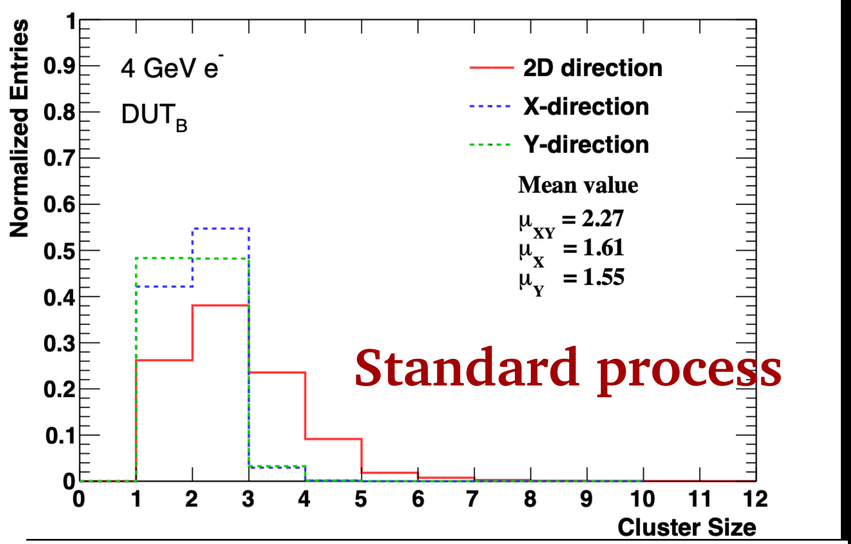
Air cooling for CEPC vertex detector

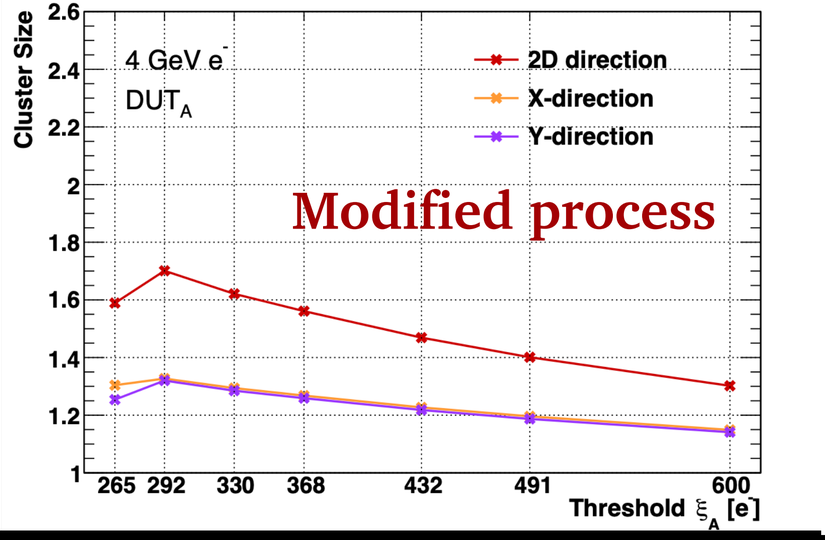
- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix design : $\leq 100\ mW/cm^2$. (trigger mode), $\leq 150\ mW/cm^2$ (triggerless mode),
  - Taichupix measured result: $\sim 60\ mW/cm^2$(triggerless mode, 17.5MHz)
  - CEPC final goal : $\leq 50\ mW/cm^2$
- Cooling simulations of a single complete ladder with detailed FPC were done.
  - Need $2\ m/s$ air flow to cool down the ladder

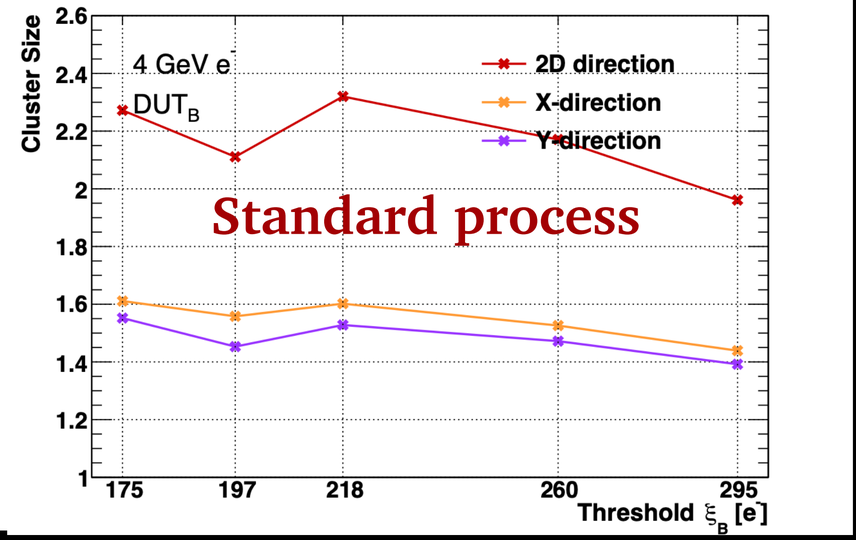
Max temperature of ladder (℃) (air temperature 5 ℃)					
Power Dissipation (mW/cm2) \ Air speed (m/s)	5	4	3	2	1
100	19.6	21.8	25.0	*30.6*	*43.4*
150	26.9	30.1	35	*43.4*	*62.6*

Offline analysis results of first test beam







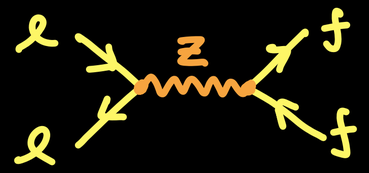


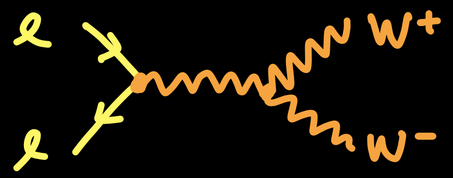
- Less charge sharing effects in modified process with full depletion
- If lowering the threshold, cluster size will be dominated by noise
-

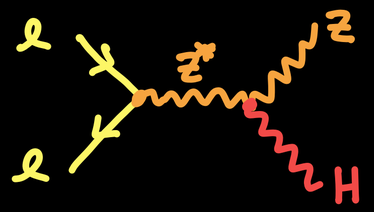
CEPC对撞机的设计指标

CEPC Operation mode		ZH	Z	W^+W^-	ttbar
$\sqrt{s}$ [GeV]		~ 240	~ 91.2	~ 160	~ 360
Run time [years]		7	2	1	-
CDR (30MW)	L / IP [$\times 10^{34}$ $cm^{-2}s^{-1}$]	3	32	10	-
	$\int L\,dt$ [ab^{-1}, 2 IPs]	5.6	16	2.6	-
	Event yields [2 IPs]	1×10^6	7×10^{11}	2×10^7	-
Run time [years]		10	2	1	5
Latest TDR (50MW)	L / IP [$\times 10^{34}$ $cm^{-2}s^{-1}$]	8.3	191.7	26.6	0.8
	$\int L\,dt$ [ab^{-1}, 2 IPs]	20	96	7	1
	Event yields [2 IPs]	4×10^6	4×10^{12}	5×10^7	5×10^5

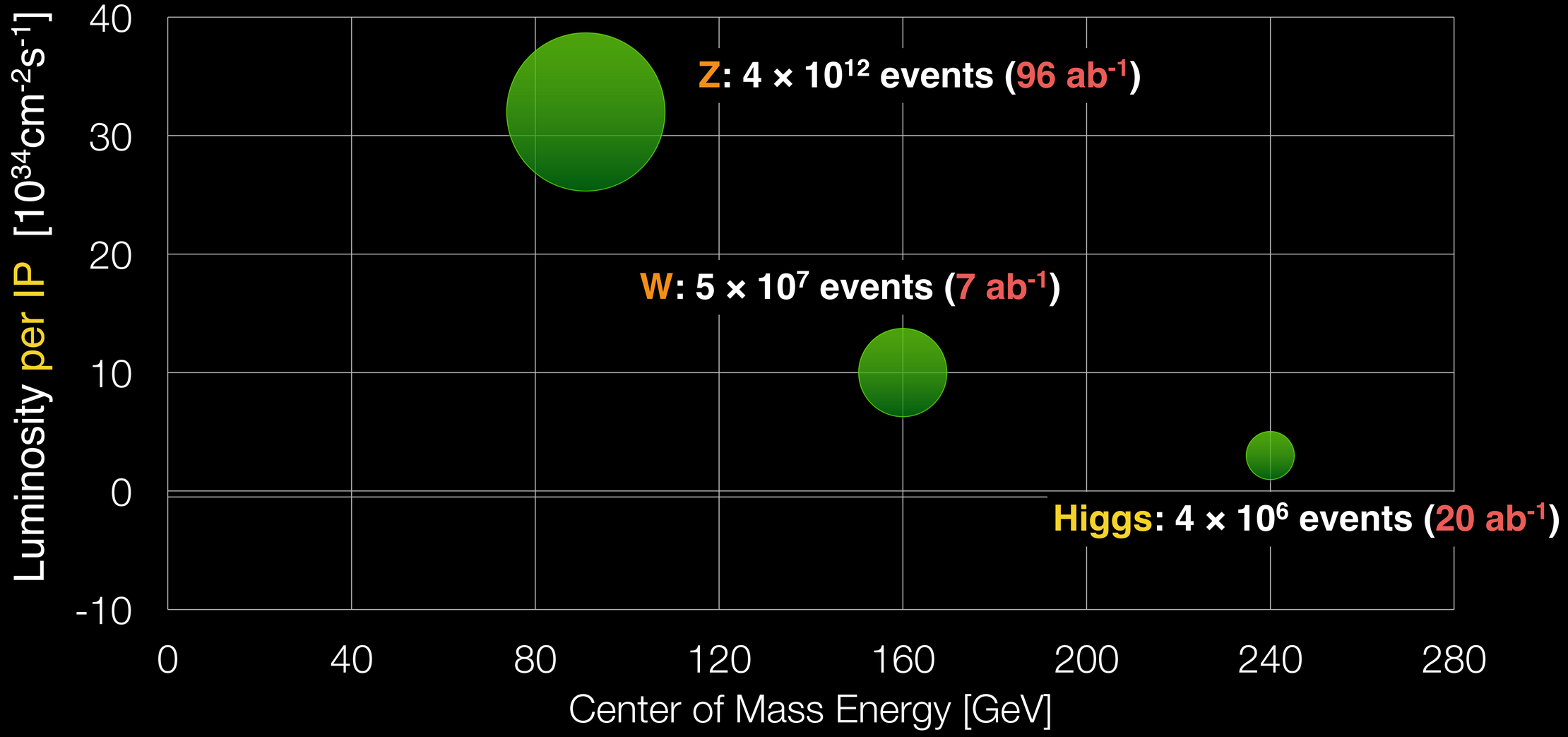
CEPC的物理





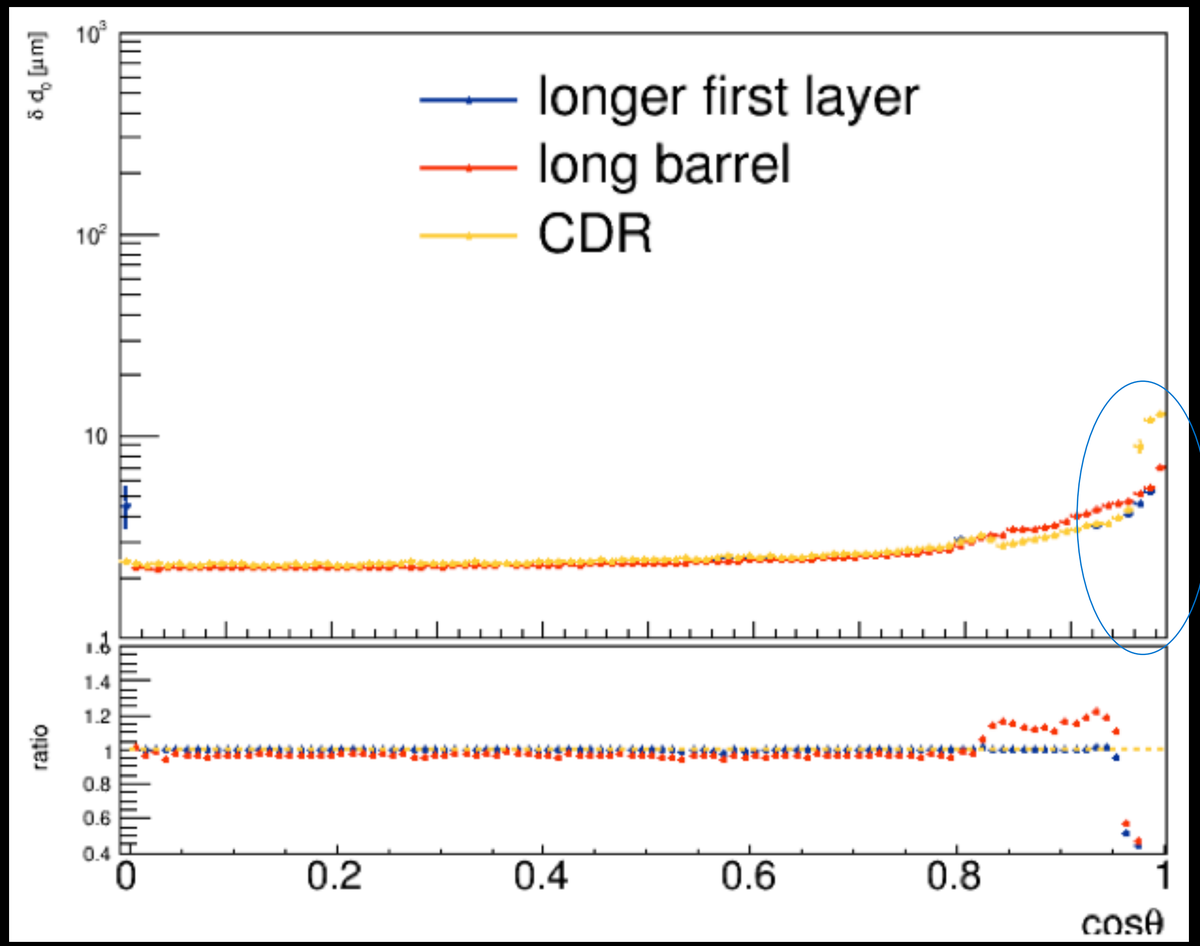


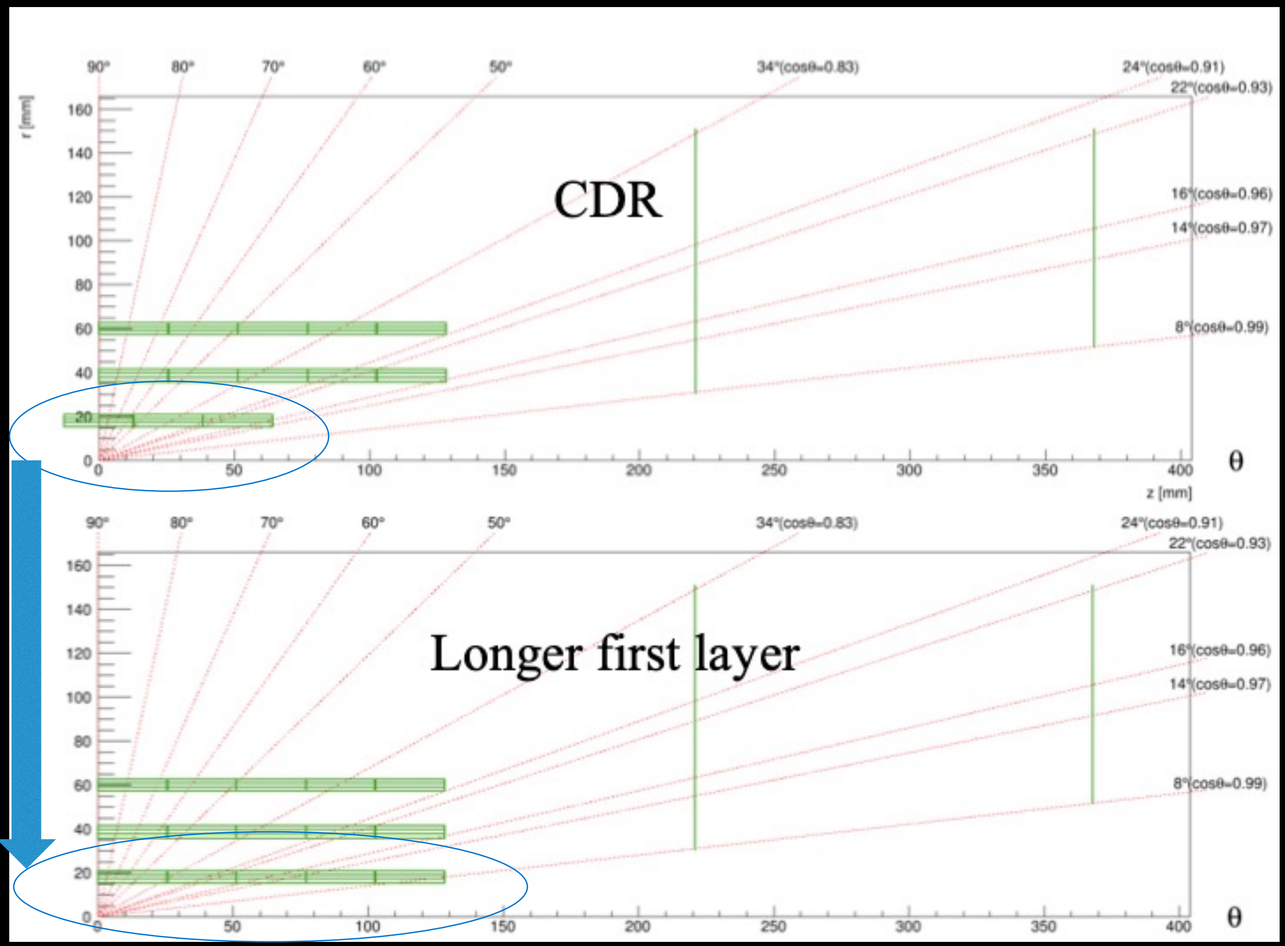
2 IPs



Vertex detector prototype structure optimization

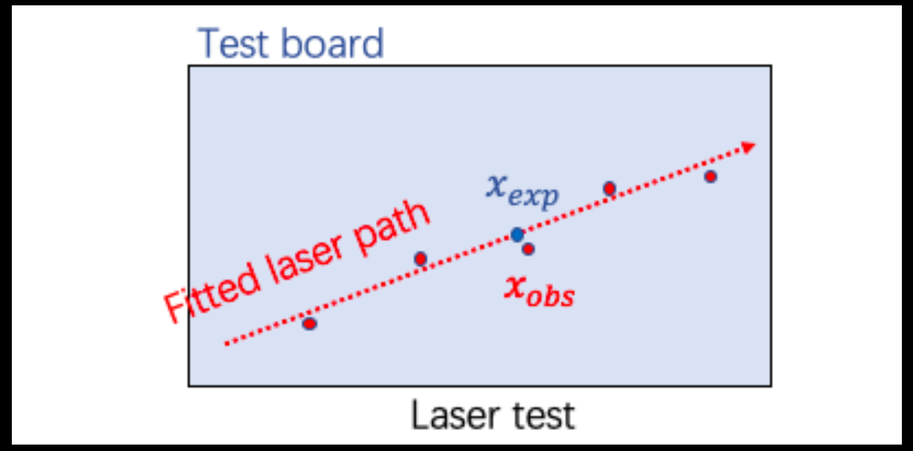
- One example of detector geometry optimization based on simulation :
  - Increase the length of the inner layer of the detector
  - To improve the impact parameter resolution for forward tracks



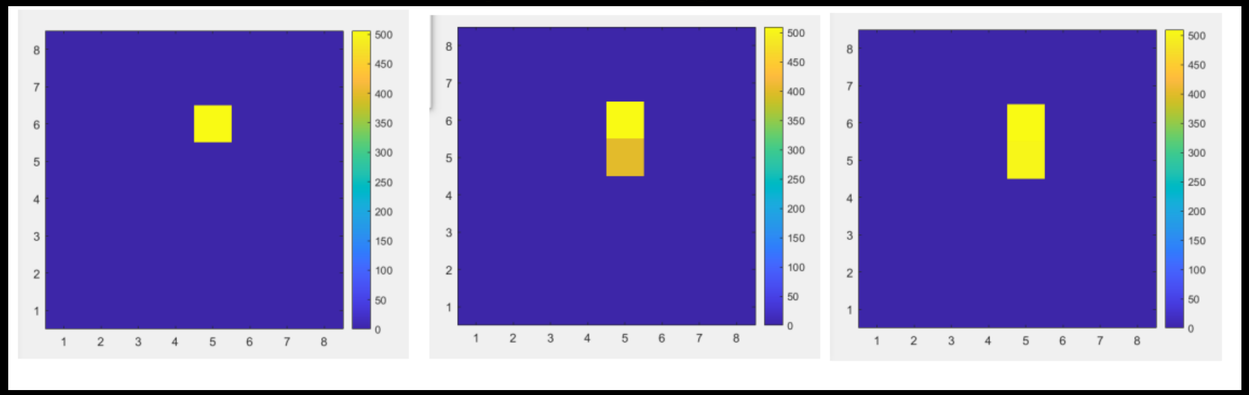


Spatial resolution measured by Laser tests

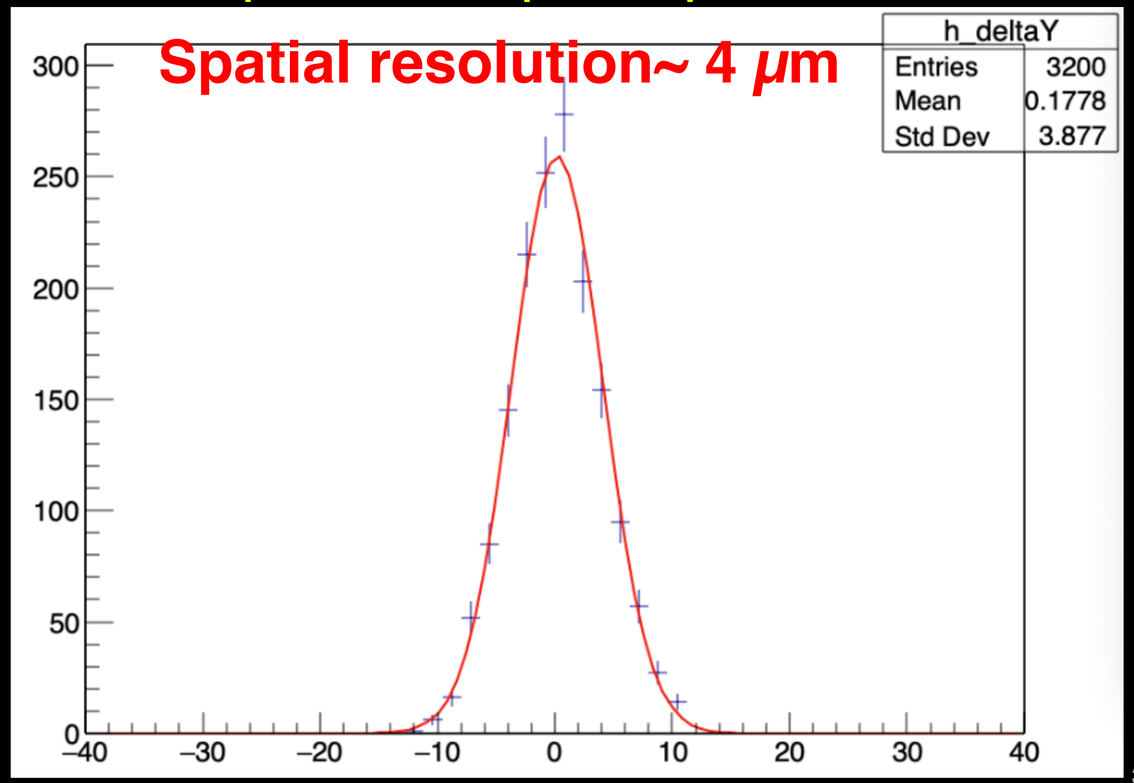
- Spatial resolution of Taichu2 can reach ~4 μm in laser tests
  - Use high precision 2D movable station in laser scan
  - Laser was scanning with a step of 1 μm



Laser beam spot during scan



Residual distribution
(measured position – expected position from station)



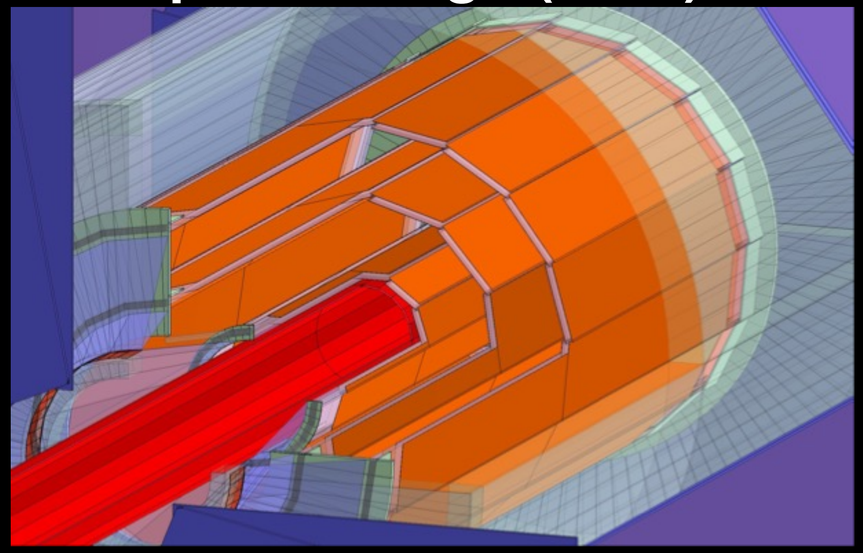
Spatial Resolution in X and Y direction

	Resolution (μm)	Overall error (μm)
X	3.98	±0.23
Y	4.12	±0.25

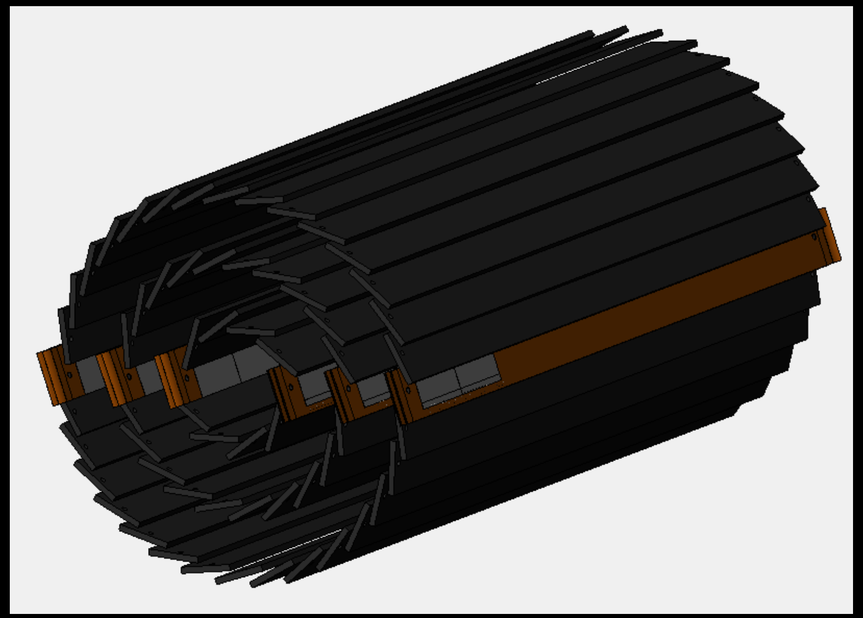
Vertex detector prototype structure optimization

- Based on CEPC vertex detector conceptual design → Three double-layer barrel detector
  - This project plan to prototype the important part of vertex detector (CDR design)
  - The cost for the full vertex detector is high (eg: ~50 M CHF for ATLAS ITk pixel detector)
    - → Plan to build full mechanical part of the detector
    - → install a sector of ladders in prototype , not necessary to build full vertex for R & D
- Optimize the geometry based on real ASIC and electronics dimension
  - Optimize geometry based on its physics performance from simulation
  - Engineering design of prototype structure

CEPC Vertex detector
Conceptual design (2016)

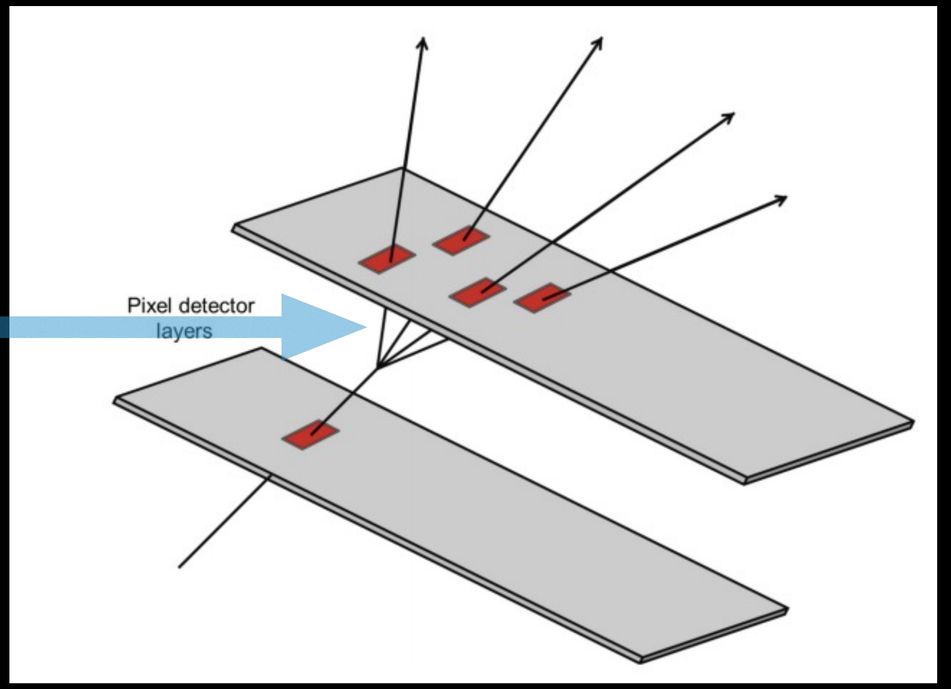


This project
Vertex detector prototype design



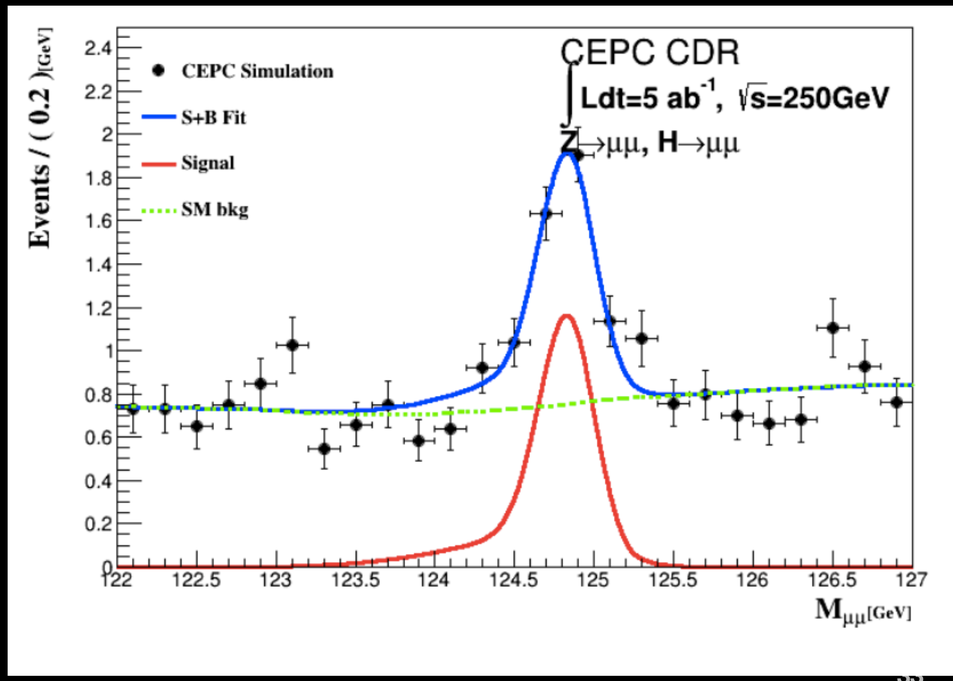
Vertex detector: Physics goal

- Produce a world-class vertex detector prototype
  - 空间分辨率 3~5 μm (pixel detector)
  - 抗辐照性能(>1 MRad)
- Physics motivation
  - Higgs precision measurement
  - H → bb precise vertex reconstruction
  - H → μμ (precise momentum measurement)



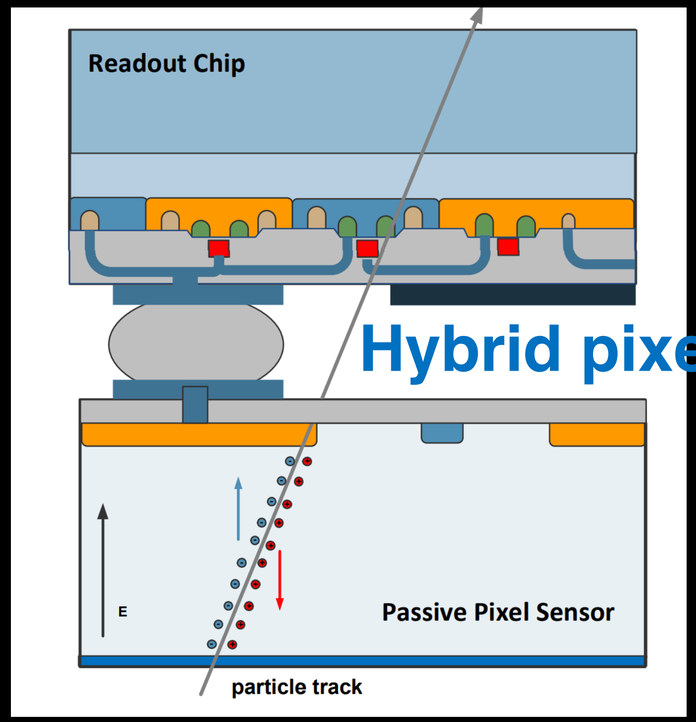
Need tracking detector with high spatial resolution

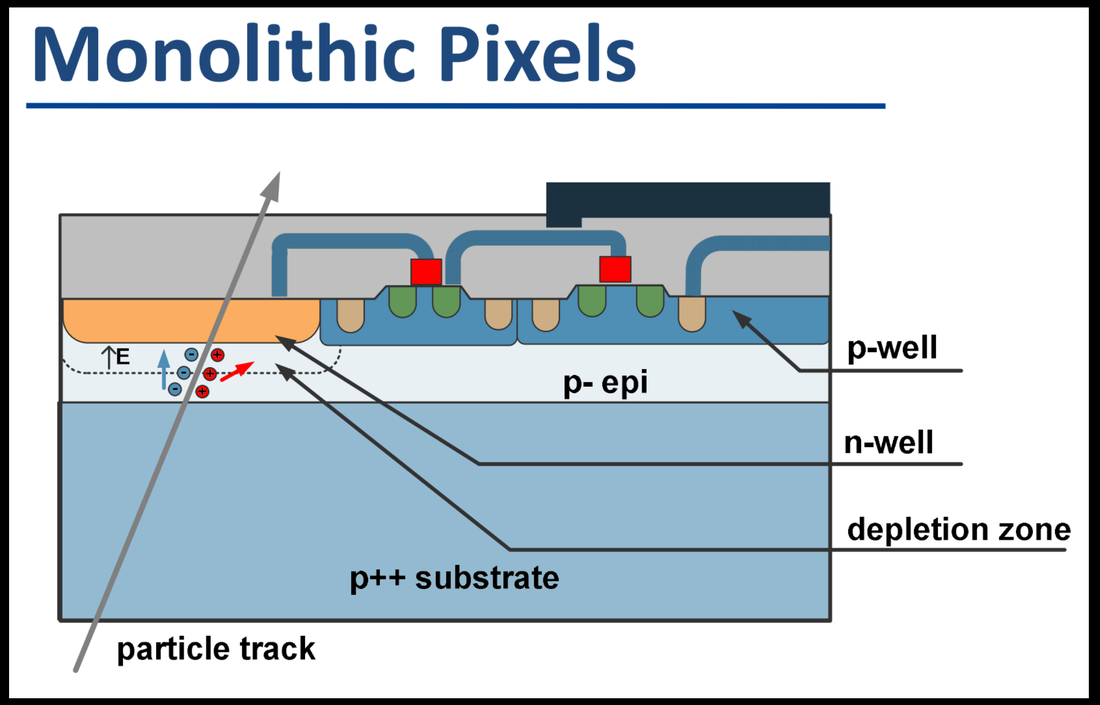
- Main technology
  - Develop the know-how in China to build such detector
  - High spatial resolution technology → pixel detector
  - Radiation resistance technology



CMOS Monolithic pixel sensor

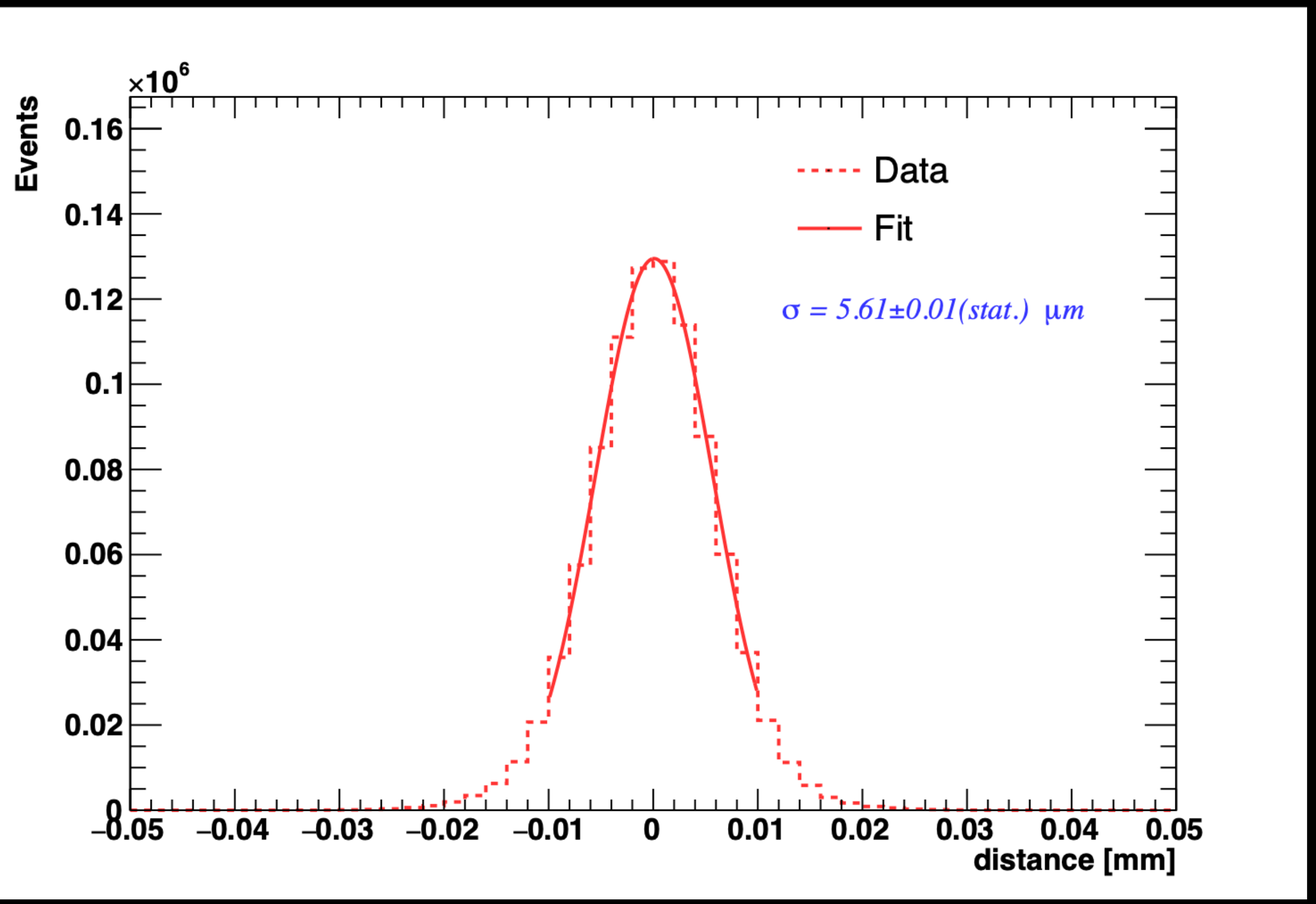
- Conventional Hybrid pixel technology at Large Hadron Collider
  - Need to bump bonding with readout ASIC
  - Typical pixel size >=50μm, much more difficult for bump bonding with smaller pixels
- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - Sensor and ASIC high integrated in one chip, easier for detector assembly
  - Can have compact structure in pixel array design.
    - Pixel size can be reduced to 25um or below → can achieve better spatial resolution

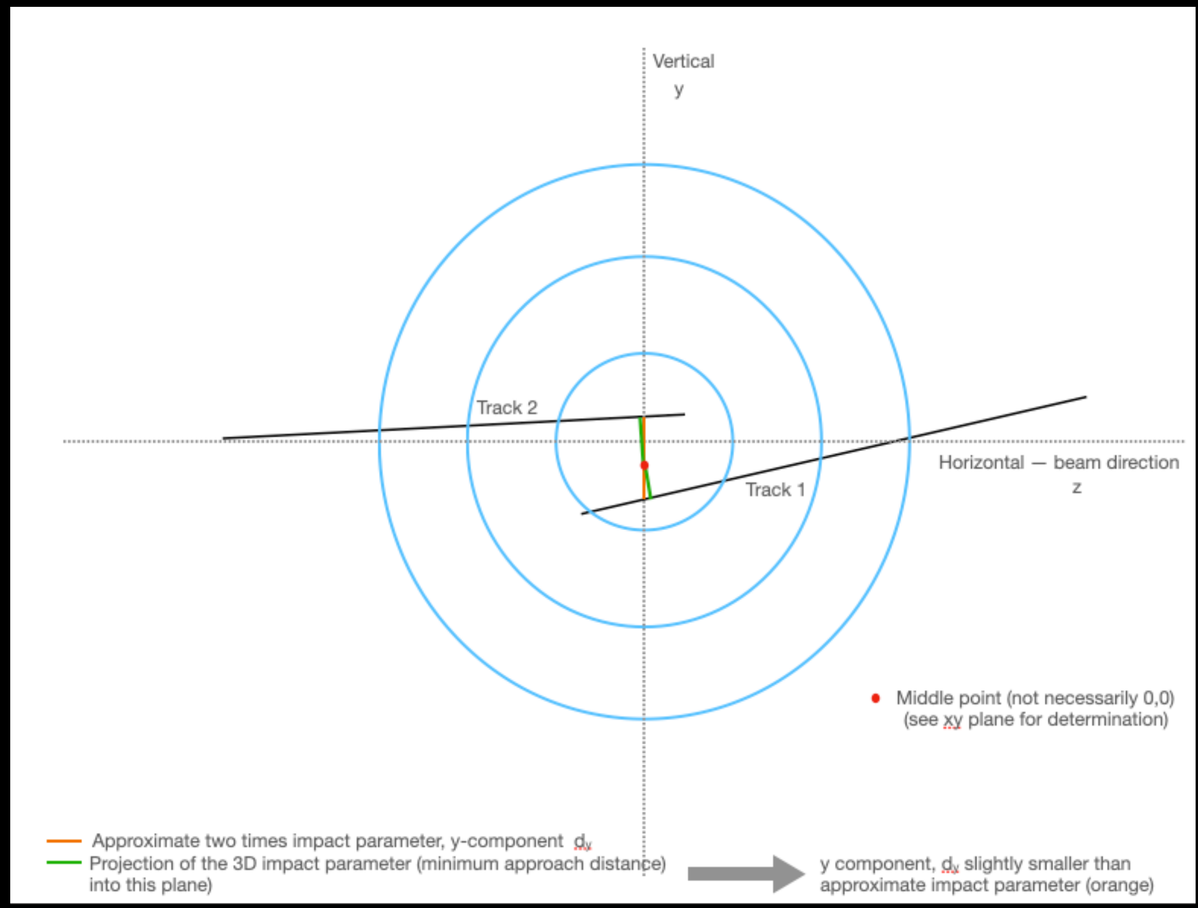




Preliminary result of impact parameter resolution

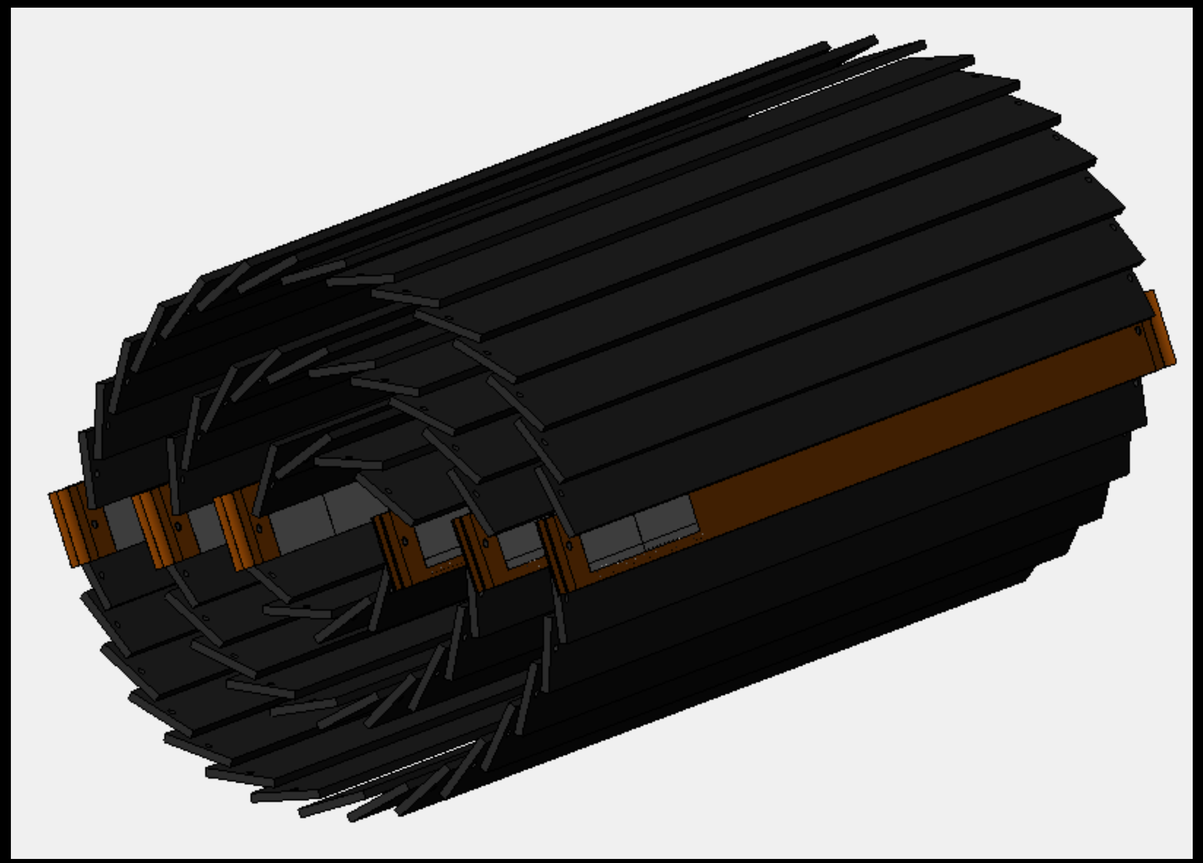
- No real interaction point or real primary vertex (PV) in testbeam setup
  - Define PV as the centre of the point in xy plane extrapolated from the up/downstream
  - Calculate the impact parameter between primary vertex and upstream/downstream tracks





Estimated Material budget for vertex detector prototype

- Estimated material budget 0.026 X0 for three double ladders vertex detector (6 layers)
  - Target for final CEPC vertex detector is 0.009 X0 (0.015% X0 per layer)
  - Copper in flexible PCB are major contributions
  - Plan to replace copper into Aluminum in final CEPC vertex detector
  - Further thinning of silicon wafer (150um → 50um)



Estimated material budget for this prototype