Microelectronics at CERN

2023 international workshop on the CEPC
23–27 October 2023
Nanjing, China
https://indico.ihep.ac.cn/event/19316/

Paulo Moreira

Outline

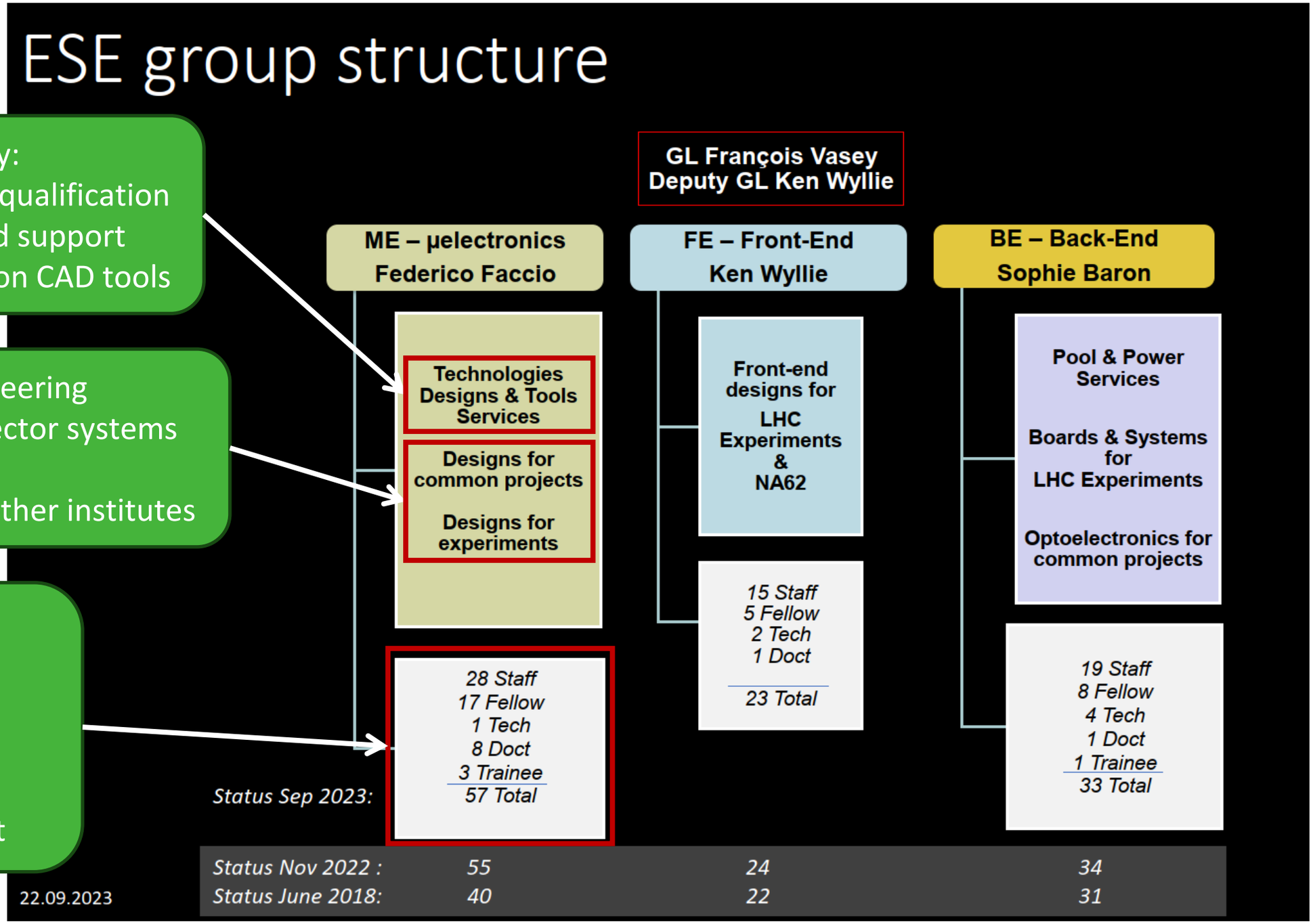
- CERN's Microelectronics section (EP-ESE-ME)
- Why microelectronics at CERN?
  - The two main drivers
- On going ME (and friends) activities
  - Radiation and technologies
  - Foundry Service and ASIC support
  - Power
  - Communications
  - Timing
  - Detector specific ASICs
- Often forgotten factors…
- The CHIPS "initiative"

CERN's Microelectronics (ME) section
In the Electronic Systems for Experiments (ESE) group
In the Experimental Physics (EP) Department

For the HEP community:
- Technology RadTol qualification
- Design kit setup and support
- Training engineers on CAD tools

Microelectronics engineering
- Common to all detector systems
- Detector specific
- Design support to other institutes

57 Members:
- 28 Staff (≈50%)
- 17 Fellows
- 8 PhD Students
- 3 Trainees
- 1 Technical Student



+ Collaborating Institutes

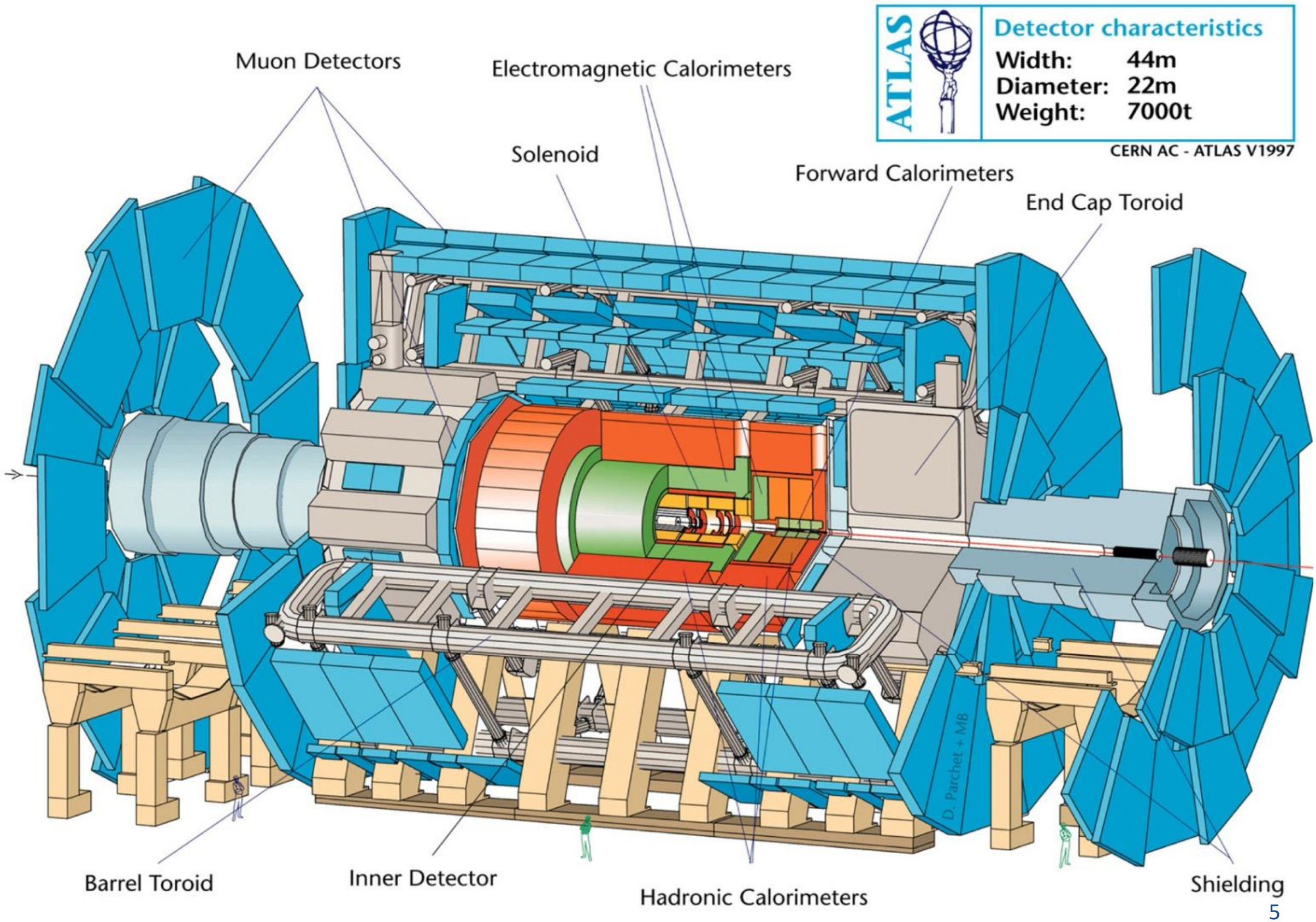
Why Microelectronics in HEP?

Paraphrasing Erik Heijne*

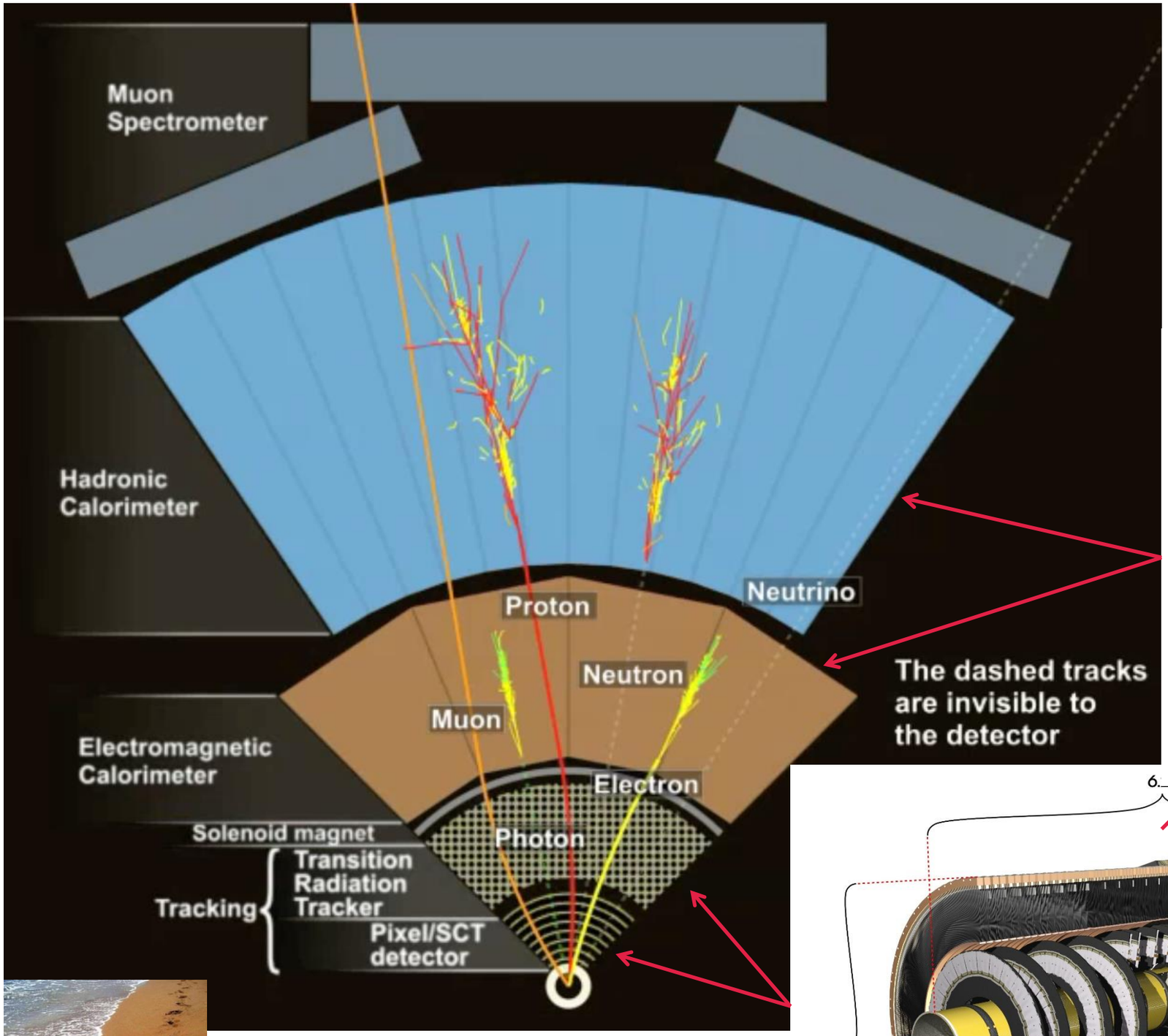
- "Over the last decades the experiments in elementary particle physics ..., have seen profound changes":
- "… **orders of magnitude increases** in physical size, interaction rates, radiation intensity and data volume."
- "…**segmented and pixelated silicon detectors**, …calorimeters and surrounding muon detectors feature a much larger number of sensing elements"
- "…provides **improved precision in particle tracking and momentum measurement**, avoiding a need for even larger overall detector dimensions"
- "**Associated silicon integrated circuits, specifically designed for these applications, improve the speed and reduce the electrical power for signal processing and information extraction**."
- "… detectors can cope with near-GHz interaction rates, more than 1000-fold the rate at the LEP collider ∼1995, and produce distinctive reconstructions of interactions with μm-level precision, even with hundreds of simultaneous particles"
- "All this in the inherently **severe radiation environment** up to tens of Mrad"
- "The unconventional **exploitation of silicon chip technology for radiation sensing and large-scale parallel signal processing has been the most important enabling factor**."

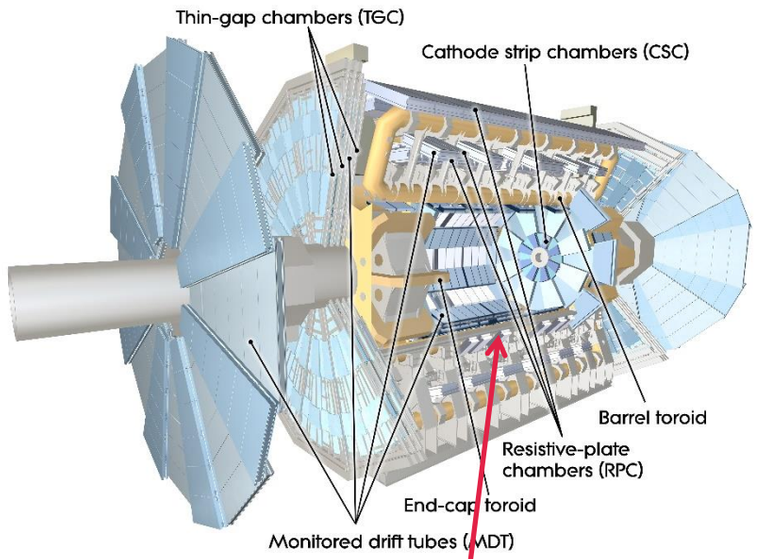
* https://doi.org/10.1016/j.nima.2023.168466

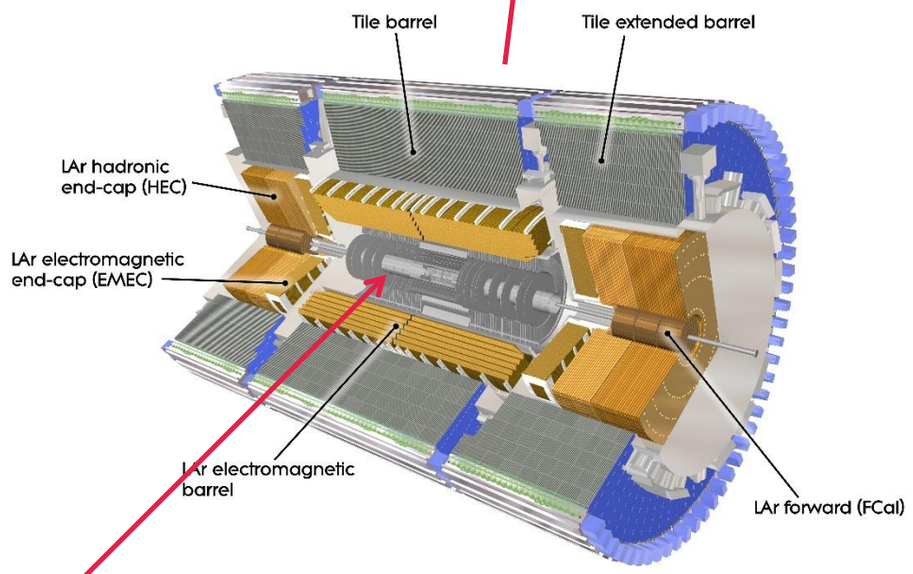
The ATLAS detector

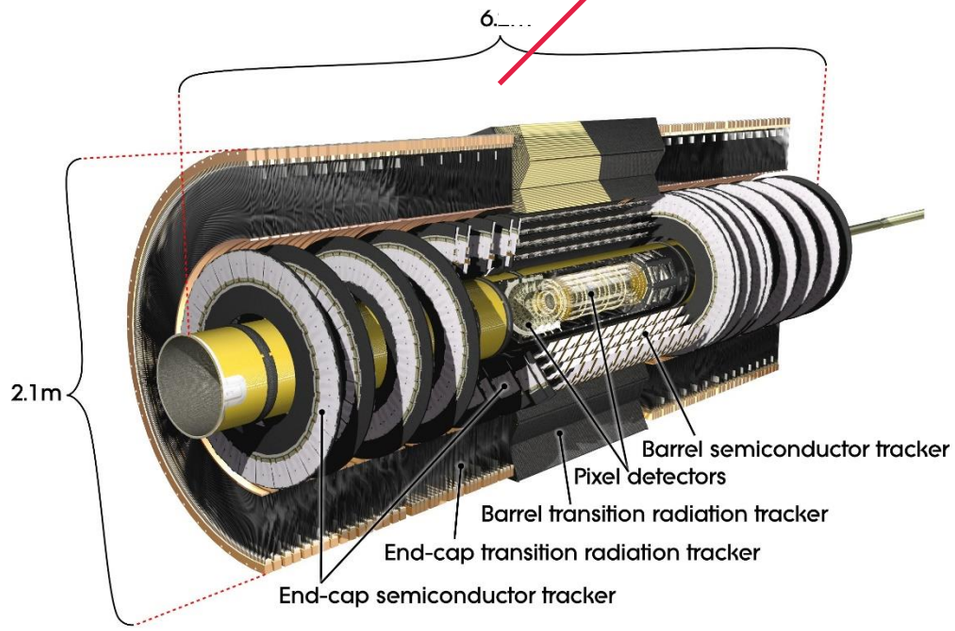


An ATLAS detector segment

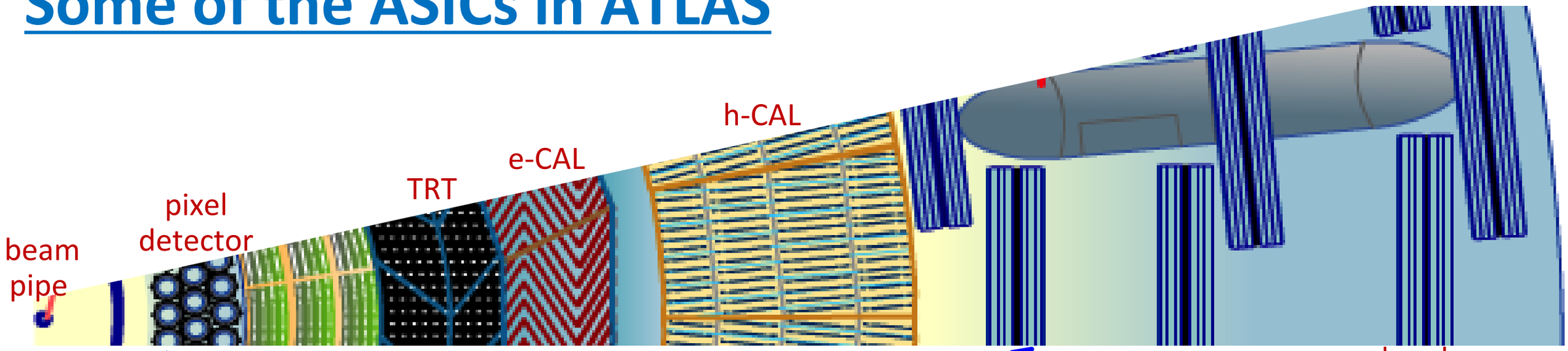








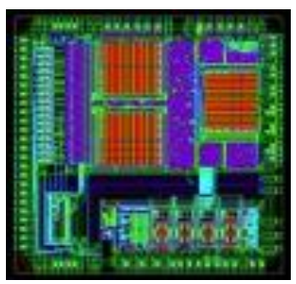
Some of the ASICs in ATLAS



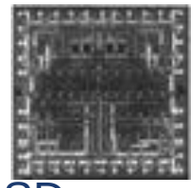
FE-I3 ASIC
- **Pixel detector**
- *250 nm CMOS*
- Rad-tol: 100 Mrad
- 80 M segments
- 28 000 chips
- 1.7 m^2 Si sensor

ABCD ASIC
- **Si-strips detector**
- *800 nm BiCMOS*
- Rad-tol: 10 Mrad
- 6 M segments
- 50 000 chips
- 60 m^2 Si sensor

ASDBLR ASIC
- **TRT detector**
- *800 nm BiCMOS*
- Rad-tol: 10 Mrad
- 38 000 chips



DTMROC ASIC
- **TRT detector**
- 250 nm CMOS
- 19 000 chips



ASD
- **muon detector**
- *500 nm CMOS*
- 148 000 chips

Chips to scale 1 cm

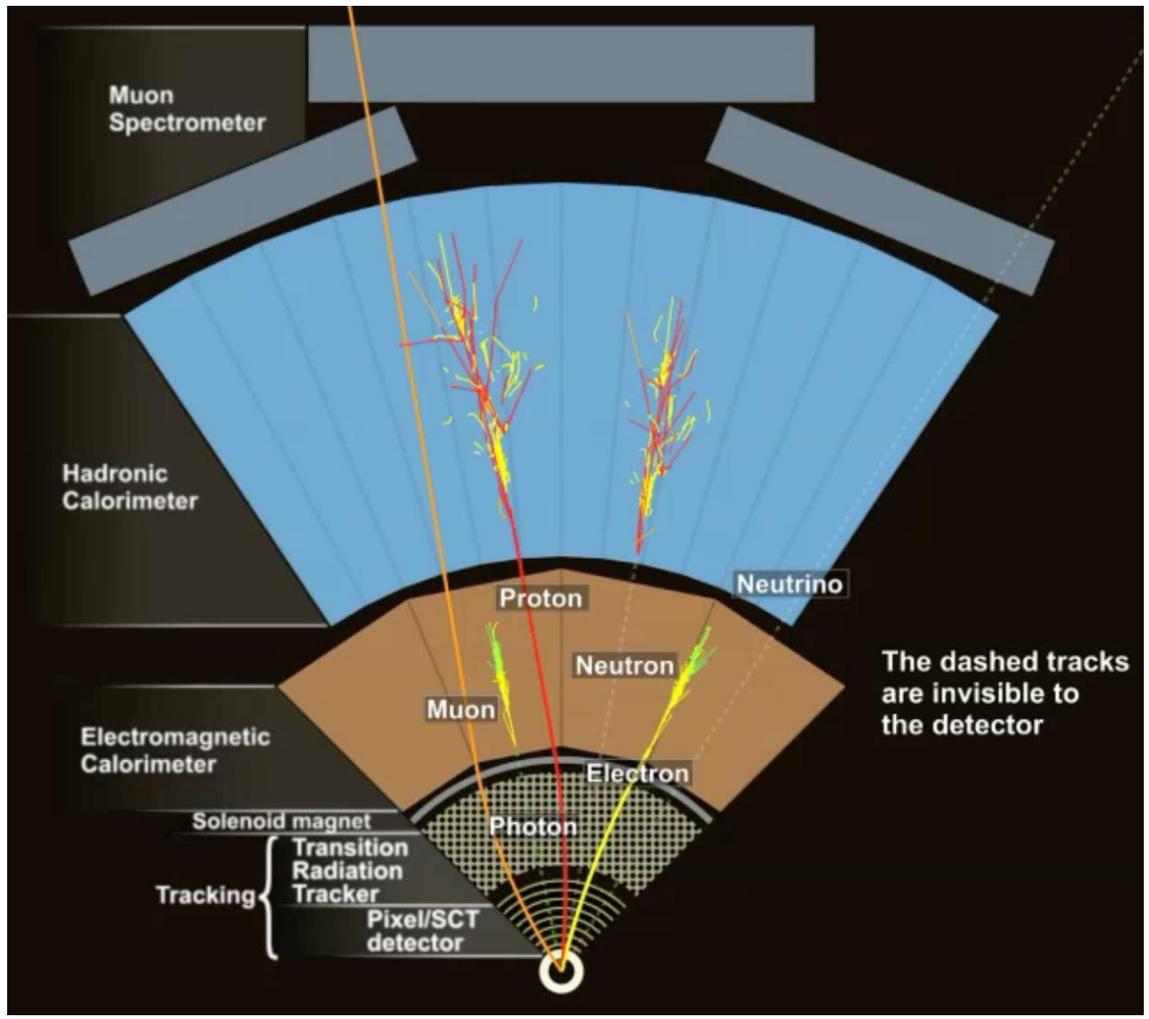
ATLAS:
Sensors: ≈100 M sensors
LHC experiments:
ASICs: >1M ASICs to process signals and control the detector operation

E. Heijne

ATLAS Radiation Environment

Detector zone	Total dose [rad]	Neutron fluence [cm^{-2}]	Charged hadron fluence [cm^{-2}]
Pixel barrel	113×10^6	1.62×10^{15}	2.3×10^{15}
SCT barrel	7.8×10^6	1.6×10^{14}	1.2×10^{14}
ECAL barrel	4.8×10^3	1.8×10^{12}	3.8×10^{11}
HCAL	380	2.7×10^{11}	6.7×10^{10}
Muon detector	23×10^3	6.4×10^{12}	1.3×10^{12}

- High-Luminosity LHC (HL-LHC) upgrade radiation background to increase 10-fold
- ASICs radiation hardness
  - 100 Mrad “typically”
  - 1 Grad for the inner pixel layers (10^{16} n/cm^2 (1 MeV equivalent))

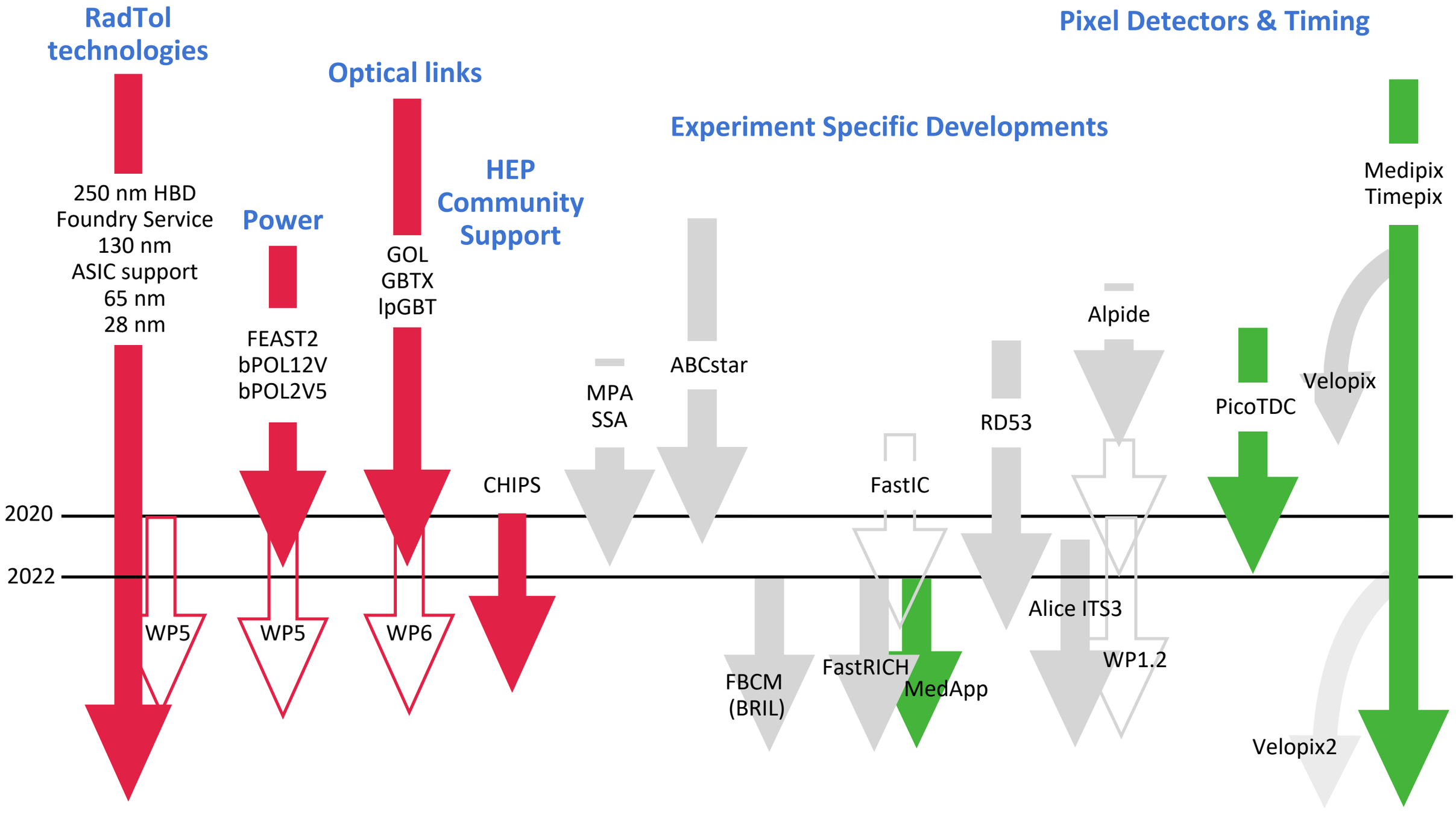


Overview of ME activities

ME = MicroElectronics = ASIC design

Arrow colour code:
- Experiment-specific projects
- Common projects
- Other fields of science

CMOS Technology nodes: …, 130, 65 and 28 nm



This schematic view does not represent all projects in ME

RadTol [CMOS] technologies

Achieving radiation tolerance

Past

- Bespoke technologies
  - e.g. 800 nm BiCMOS (DMILL)

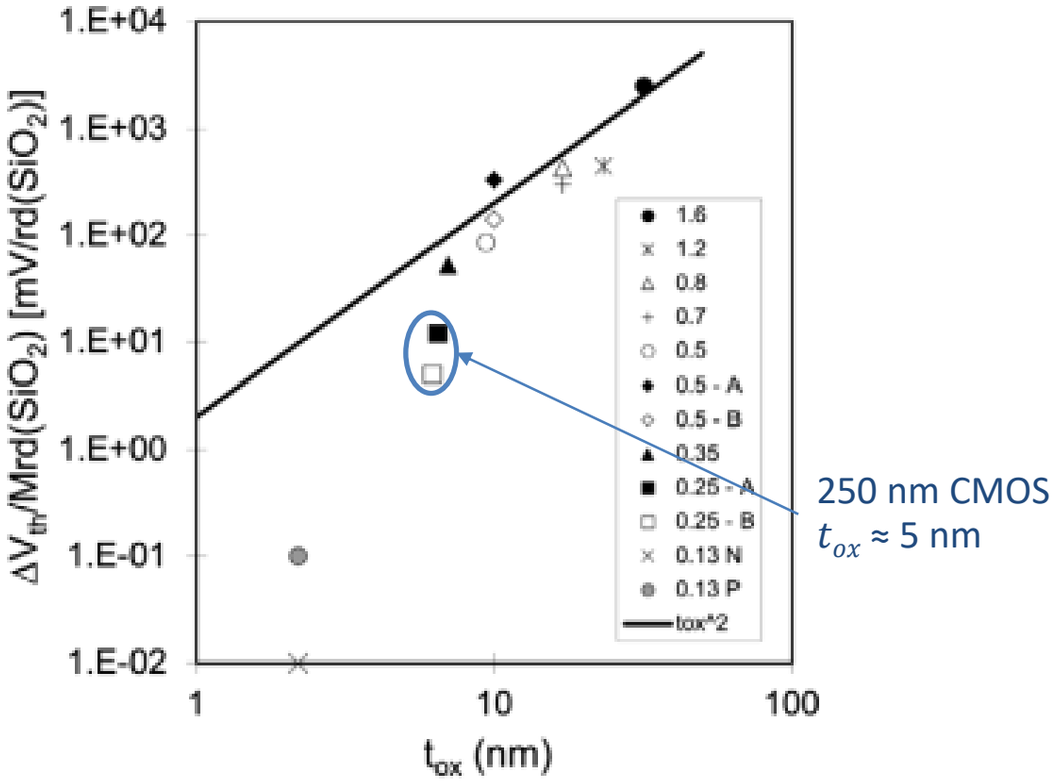
Recent past

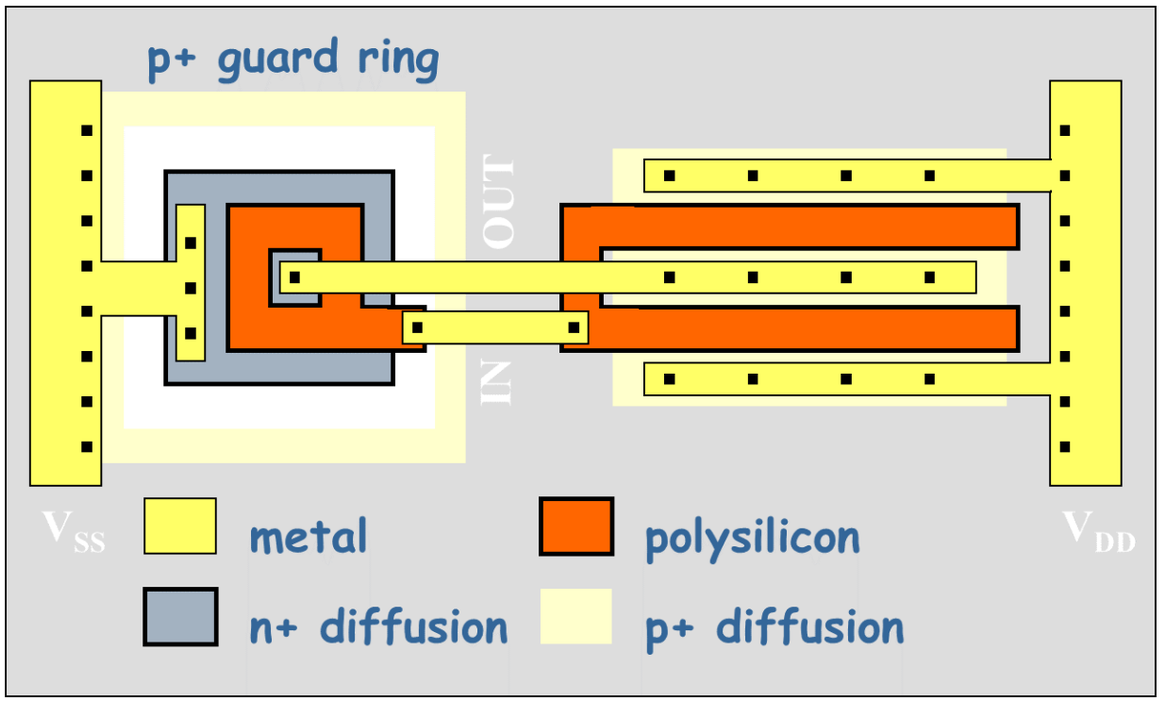
- For t_{ox} > 12 nm
  - Radiation sensitivity decreases with thickness: $\propto t_{ox}^{n}, n \cong 2$
- For t_{ox} < 12 nm
  - Stepper decrease with t_{ox}
  - Enabling the use of commercial CMOS technologies to design RadTol ASICs
  - **If combined with** Radiation Hardness By Design techniques (RHBD)
  - e.g. in 250 nm and 130 nm CMOS

Now and [future?]:

- Modern processes (≤65 nm CMOS) allow to achieve very high radiation tolerance (> 100 Mrad) with minimum precautions:
  - e.g. bigger than minimum transistor sizes and controlled (during operation) annealing condition
- For bulk technologies the trend is promising **but**
  - Each node needs to be carefully characterised
  - Not all fabs, for the same technology, are equally good
  - Must monitor the production to ensure the RadTol quality
- More advanced is not necessarily better
  - e.g. 22nm Fully Depleted Silicon-On-Insulator
- **A constant effort to evaluate and qualify new technologies for radiation hardness is needed**

Threshold voltage shift of transistors in commercially CMOS technologies





RadTol [CMOS] technologies

TID on ring-oscillators

Purple bars: frequency degradation at 1 Grad

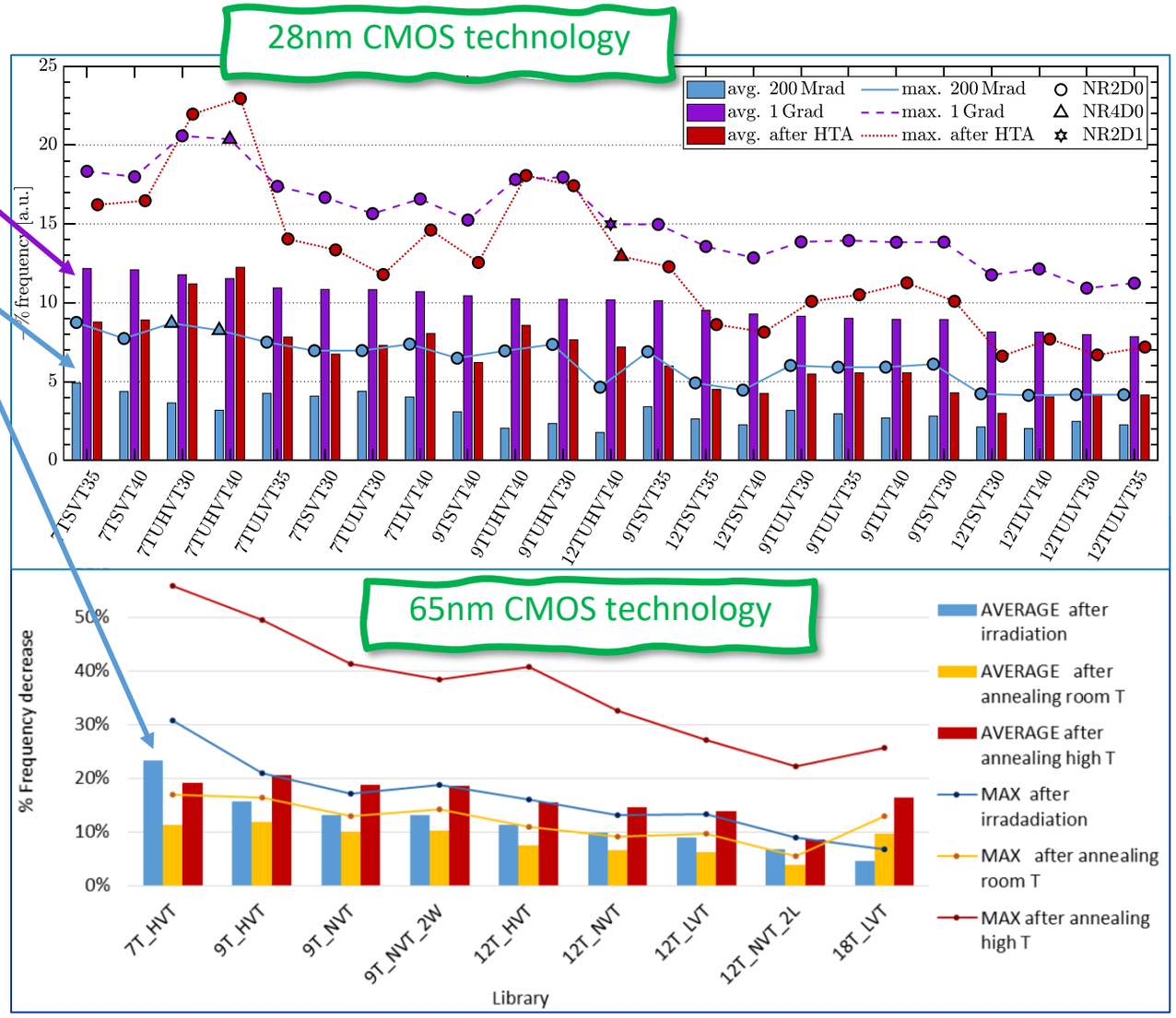
Blue bars: frequency degradation at 200 Mrad

Worst RO @ 200 Mrad in 65nm: ~ -23%
Worst RO @ 200 Mrad in 28nm: ~ -5%
Worst RO @ 1 Grad in 28nm: ~ -13%

+

- Post-irradiation annealing “forbidden” for 65 nm CMOS
- High-temperature annealing reduces radiation effects in 28nm CMOS (red bars)

- No evidence of low dose rate effects, down to 0.1 Mrad/hour, in 28 nm CMOS (Lower DR, still being studied.)



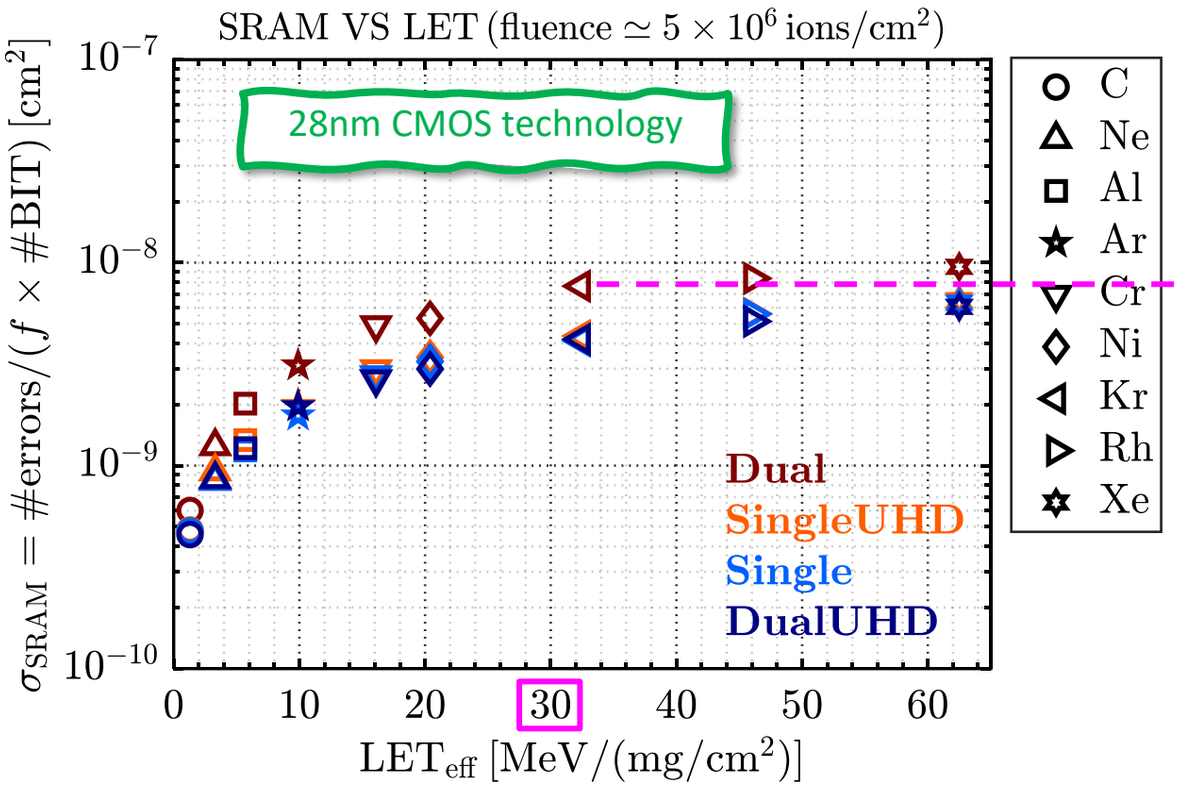
[28nm] Borghello, G., et al. "Total ionizing dose effects on ring-oscillators and SRAMs in a commercial 28 nm CMOS technology." *Journal of Instrumentation* 18.02 (2023): C02003.
[65nm] https://cds.cern.ch/record/2725573/files/DRAD%20report.pdf

Preliminary studies show 16 nm FinFET technologies to have good radiation tolerance. doi: 10.1109/TNS.2021.3076977.

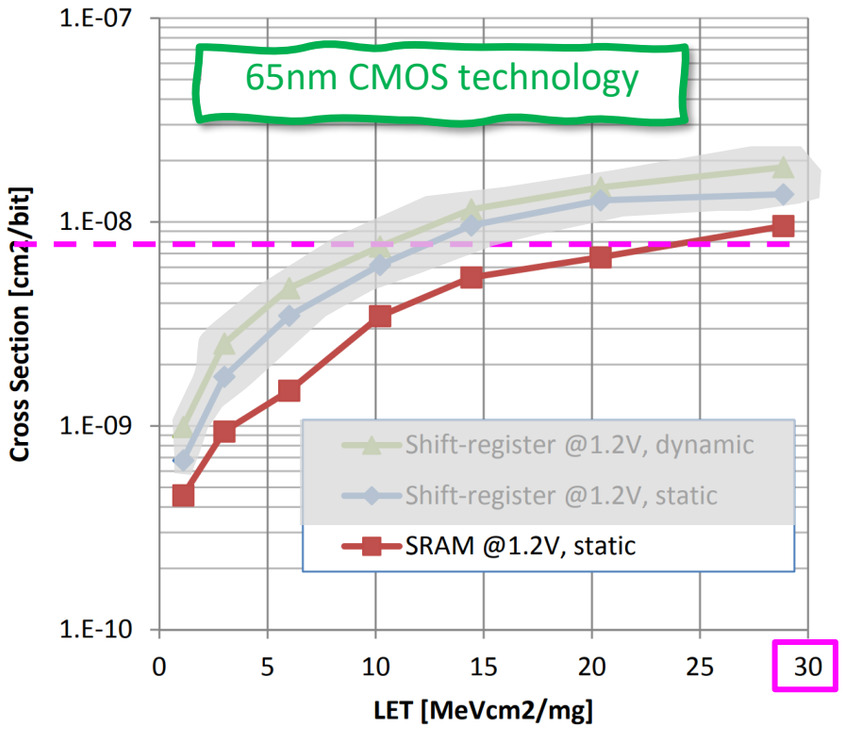
RadTol [CMOS] technologies

SEU on SRAM

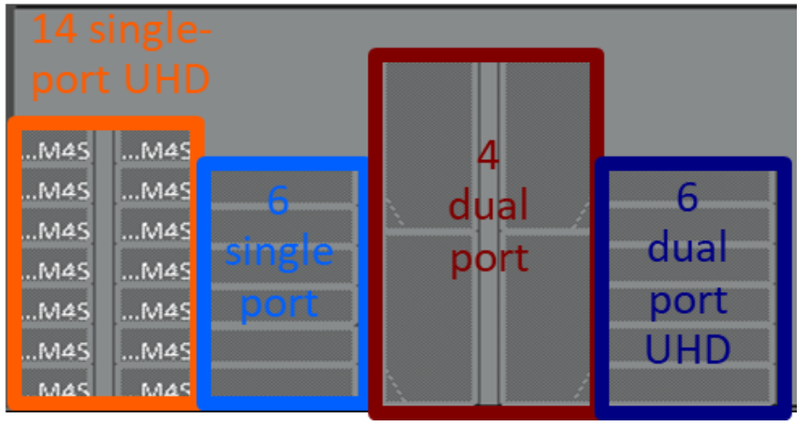
SRAM cross section



G. Borghello, et al., Single Event Effects characterization of a commercial 28 nm CMOS technology, TWEPP 2023



Bonacini, S., et al. "Characterization of a commercial 65 nm CMOS technology for SLHC applications." *Journal of Instrumentation* 7.01 (2012): P01015.

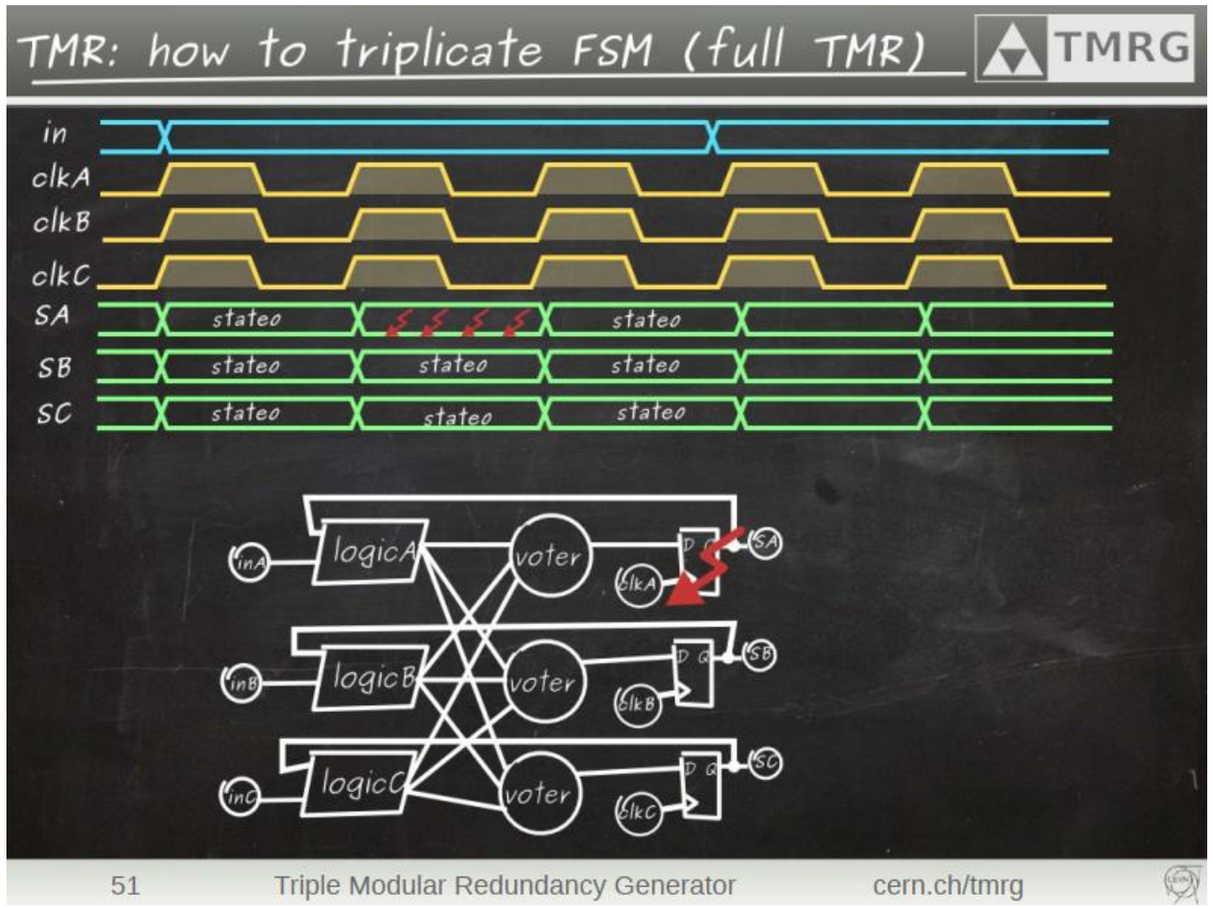


RadTol [CMOS] technologies

Achieving SEU tolerance

- Single Event Effects (SEE) do not improve with Technology Scaling
- These need to be dealt at:
  - Circuit level
  - System level
- The “solution” is not unique:
  - Strategies are abundant
- CERN’s Triple Modular Redundancy Generator (TMRG)
  - Automatizes the triplication of digital circuits
  - Frees the designer from introducing TMR code manually during the design stage
  - Ensures triplication is maintained through the full design process
  - Streamlines the process of introducing SEE in the gate level simulations for final verification

TMRG
Triple Modular Redundancy Generator
https://tmrg.web.cern.ch/tmrg/
https://media.ccc.de/v/36c3-10575-how_to_design_highly_reliable_digital_electro



Foundry Service and ASIC support

CMOS Technology nodes: …, 130, 65 and 28 nm

Foundry Access Services

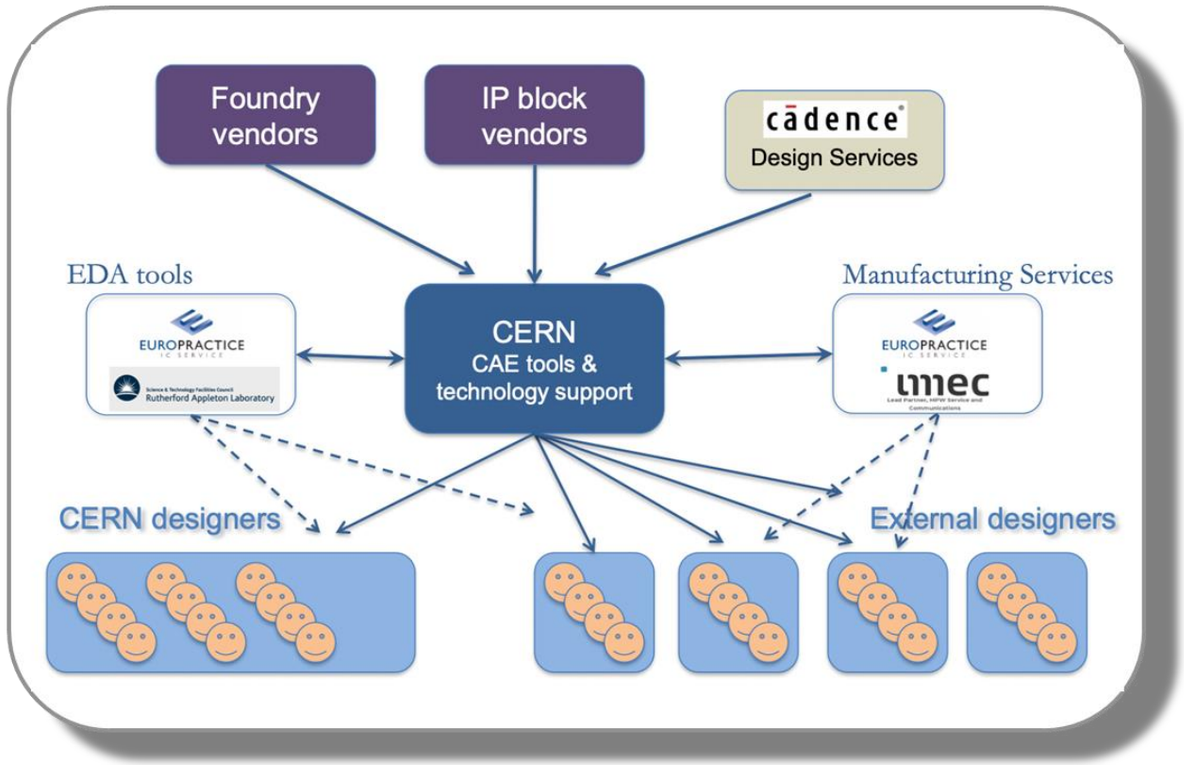
- Establish contracts with silicon vendors
- Establish NDAs for collaborative work
- Organize MPW runs & share costs
  - Coordinate fabrication
  - MPW, Engineering & Production

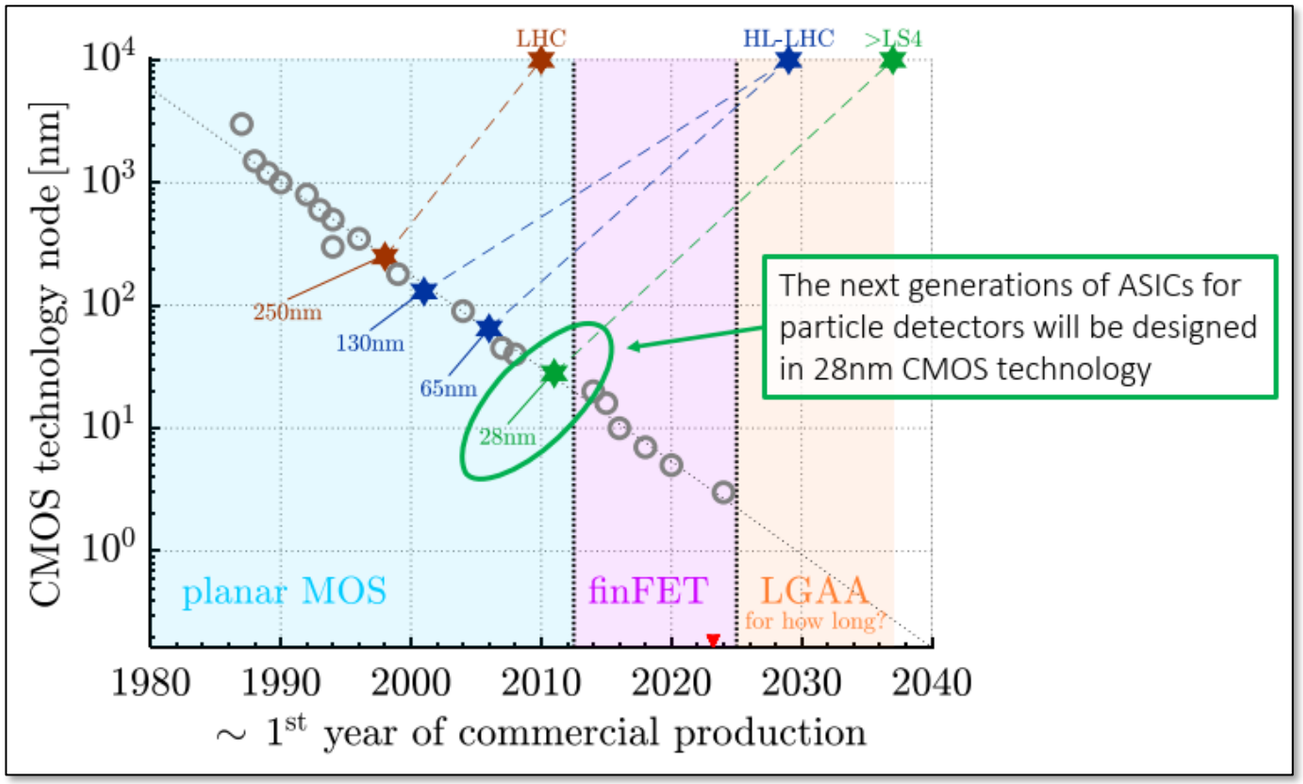
ASICs Support Services

- Develop and distribute the Common Design Platforms for mixed-signal ASICs design
  - Maintain/distribute PDKs
  - Prepare/distribute design flows
  - Maintain/distribute “macro blocks”
  - Support System-on-Chip design
- Provide support to HEP IC designers community
  - Support technology and EDA tool usage requests
  - Promote the collaborative works and knowledge sharing
  - Organize training workshops about design for HEP environment

R&D WP5

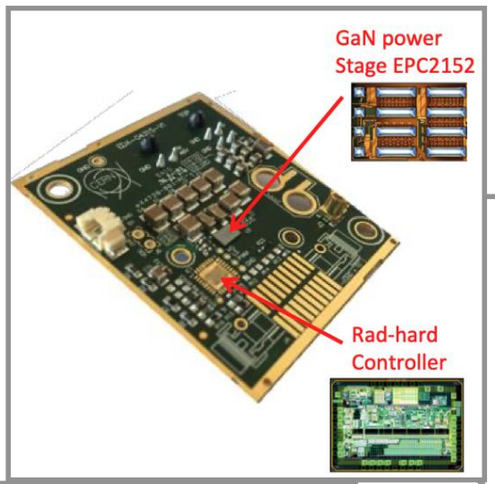
- 28nm RadTol qualification
- Development of macroblocks
- Development towards SoC
- RISC V and programmability

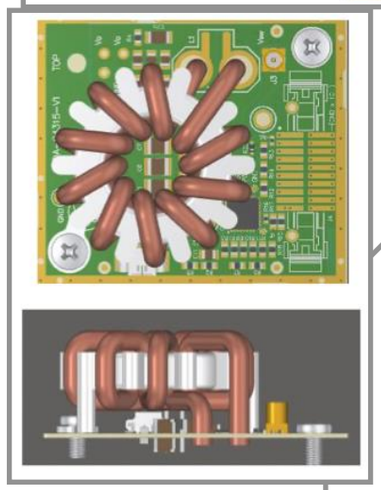


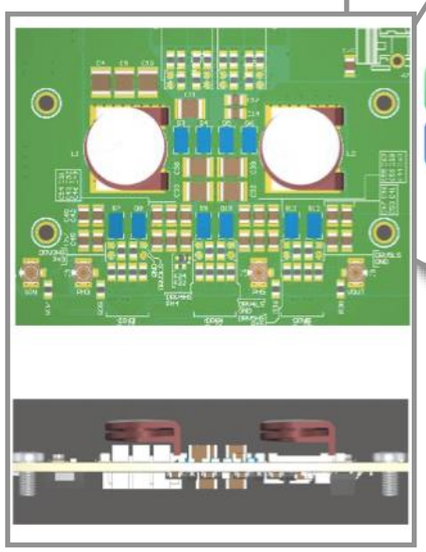


On-detector power supply

Radiation and magnetic-field tolerant family of components







Stage 1: $48V \rightarrow 12V$

bPOL48V
buck converter
(0.35 µm HV-CMOS and GaN)

rPOL48V:
switched-tank converter
(0.35 µm HV-CMOS and GaN)

linPOL48V:
Linear regulator
(0.35 µm HV-CMOS)

Stage 2: $12V \rightarrow 1.8 - 2.5V$

(FEAST2: discontinued)
bPOL12V:
POL buck converter
(0.35 µm HV-CMOS)

linPOL12V:
Linear regulator
(0.35 µm HV-CMOS)

Stage 3a: $2.5V \rightarrow 1.2V$

bPOL2V5:
POL buck converter
(130 nm CMOS)

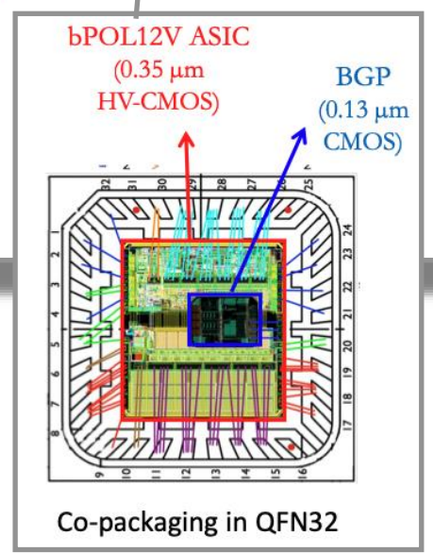
rPOL2V5:
POL resonant switched-capacitor converter
(130 nm CMOS)

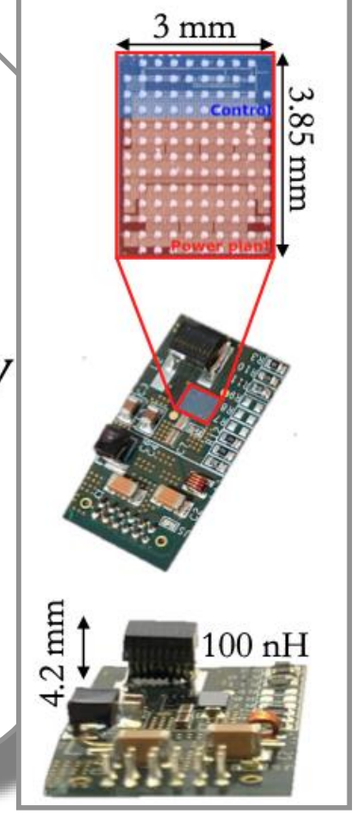
Stage 3b: $1.8V \rightarrow 0.9V$

28nm On-Chip Regulators:
DCDC
LDO

R&D stage

Production grade/in production

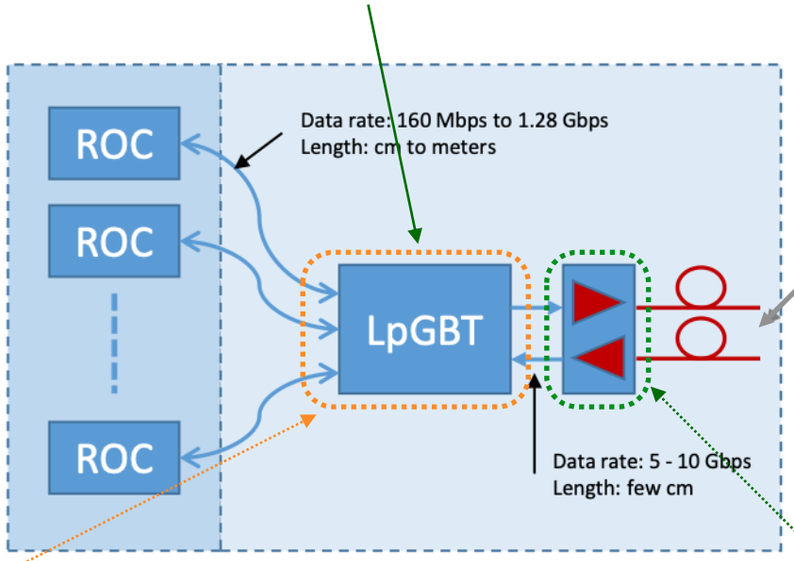




ASICs for optical links

lpGBT chipset

lpGBT ASIC
Communication hub with on-detector electronics



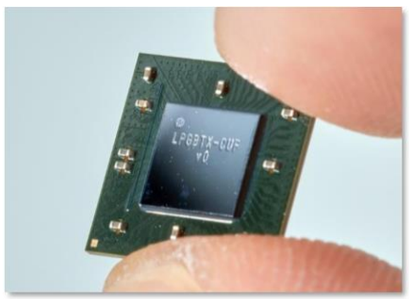
Data + timing communication

&

Control and monitoring Functions

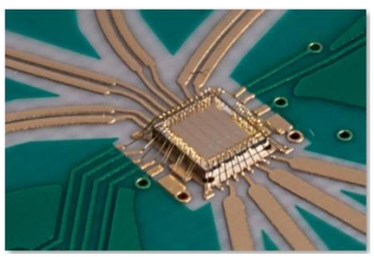
Opto module: **VTRX+** (2 ASICs)
Optical-electrical interface

lpGBT



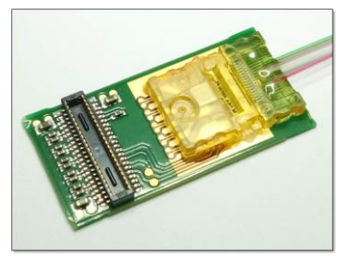
5.12/10.24 Gb/s Transceiver
(65 nm CMOS)

LDQ10



10.24 Gb/s Quad VCSEL driver
(65 nm CMOS)

GBTIA

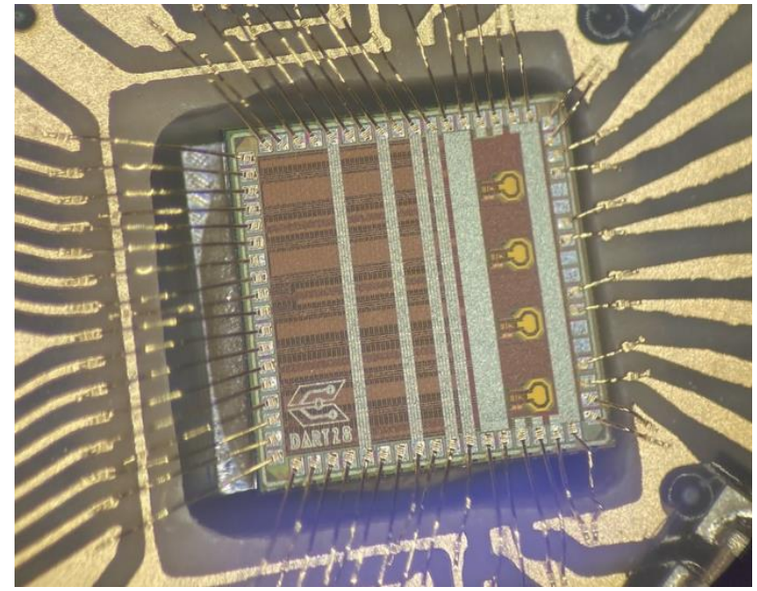


4.8 Gb/s TIA
(130 nm CMOS)

ASICs for optical links

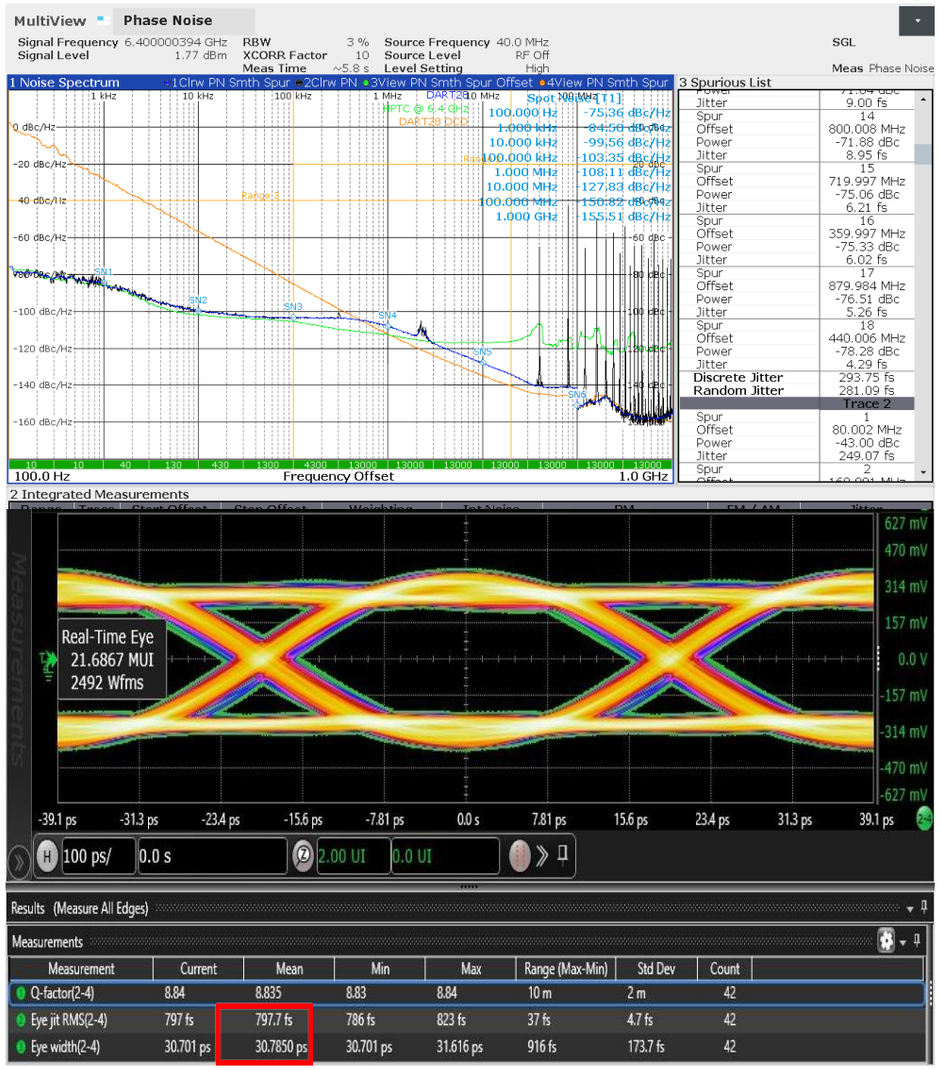
DART28

Demonstrator ASIC for Radiation-Tolerant Transmitter in 28 nm



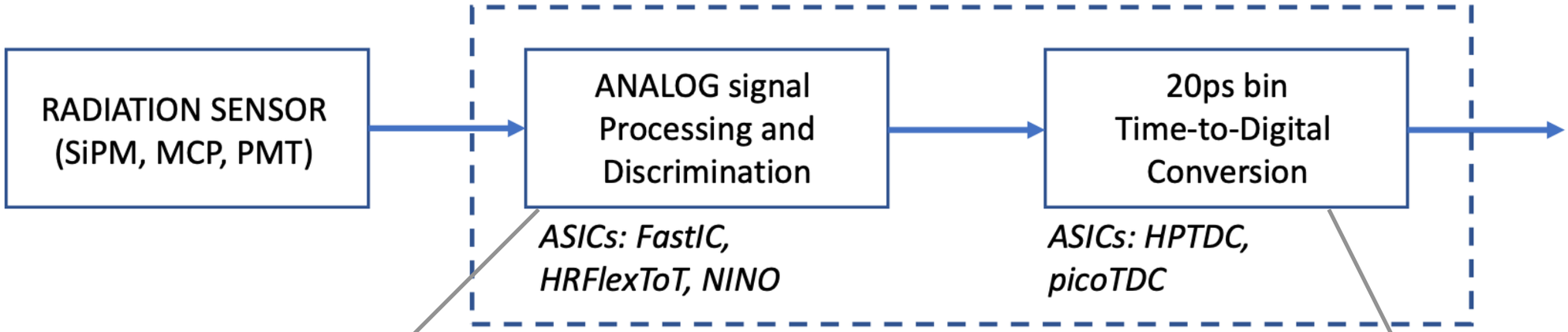
Four-channel serializer

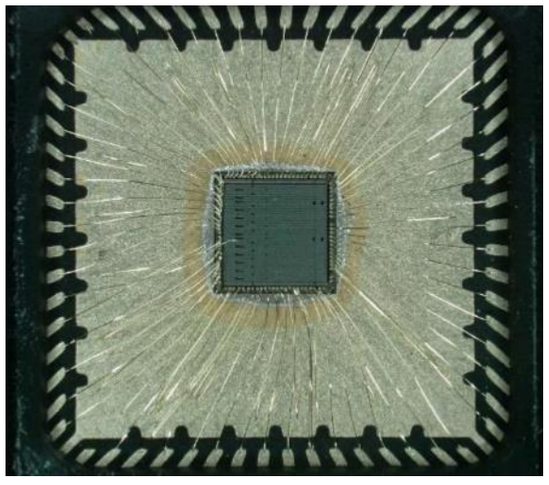
- Each channel:
  - Multiple PRBS generator
  - LC based “ADPLL”
  - Duty-cycle correction circuit
  - 25 Gbps Serializer
  - Multi-mode driver
    - Cable / Ring Modulator
    - Pre-emphasis
    - Edge-pre-emphasis
- Clock jitter
  - RJ < 300 fs rms (FD)
  - RJ: 250 fs rms (TD)
  - DJ: 786 fs pk-pk (TD)
  - TJ: 4.3 ps pk-pk (TD)
- Eye jitter
  - Random < 800 fs
    (when using some “magic”)
- Main challenge:
  - Power delivery to the ASIC
  - Bump bonding under development



ASICs for fast timing detectors

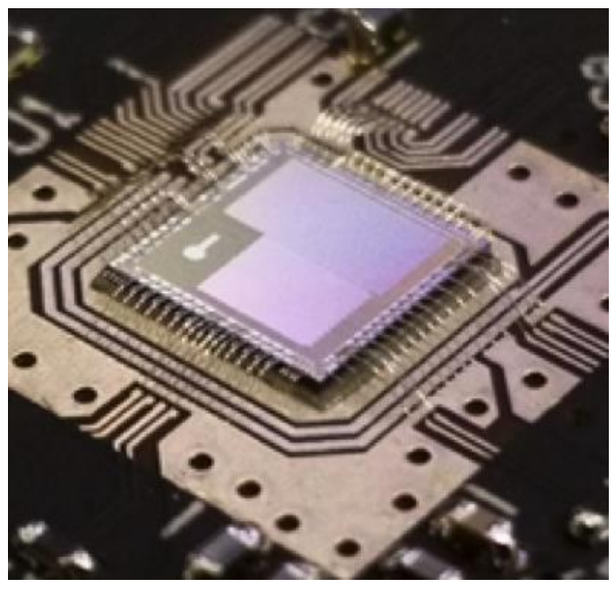
FastIC & PicoTDC





FastIC
First prototype of Analog Signal Processing and Discrimination
Better than **100ps** FWHM demonstrated
(65 nm CMOS)

On-going development:
Full Analog + TDC on-chip
- **FASTRICH** (for LHCb RICH)
- **Medical application**



PicoTDC
64 channel Time to Digital Converter
with **3ps or 12ps** time binning
(65 nm CMOS)

Detector-specific ASICs for HL-LHC:

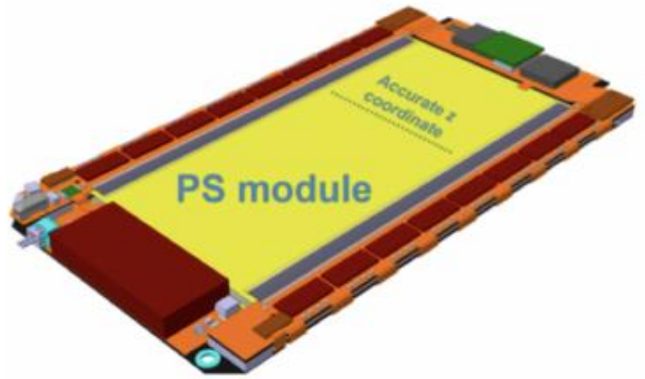
CMS Outer Tracker

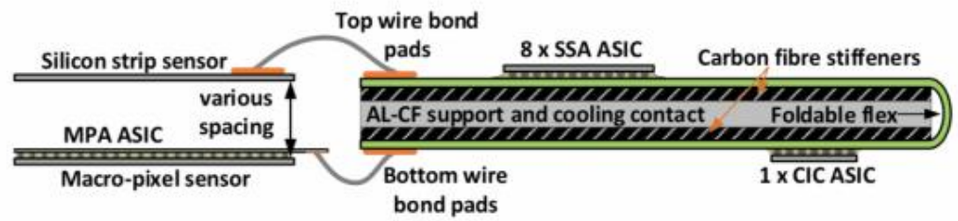
The p_T modules

- Part of the CMS LV1 trigger:
  - Measurement of transverse momentum of tracks
  - Rejection of p_T < threshold

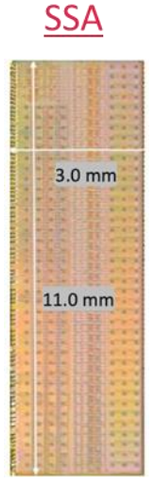
PS module

- Silicon micro-strip sensor
  - 960 strips
  - Cell size of 2.5 cm × 100 µm
  - Readout ASIC: SSA
- Macro-pixel matrix
  - 32 × 960 array
  - pixel size of 1.5 mm × 100 µm
  - Readout ASIC: MPA





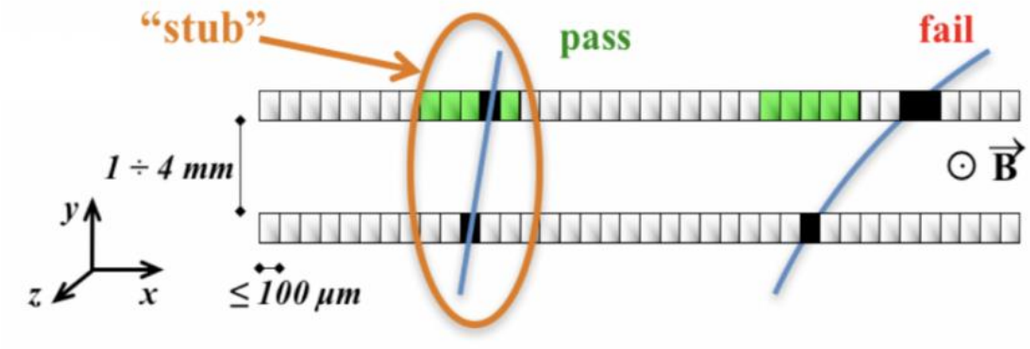
SSA

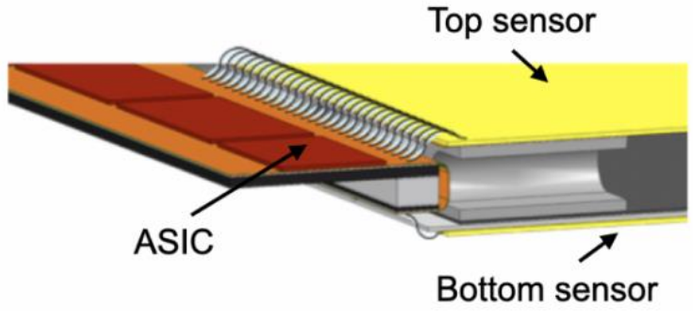


(65 nm CMOS)

MPA

(65 nm CMOS)

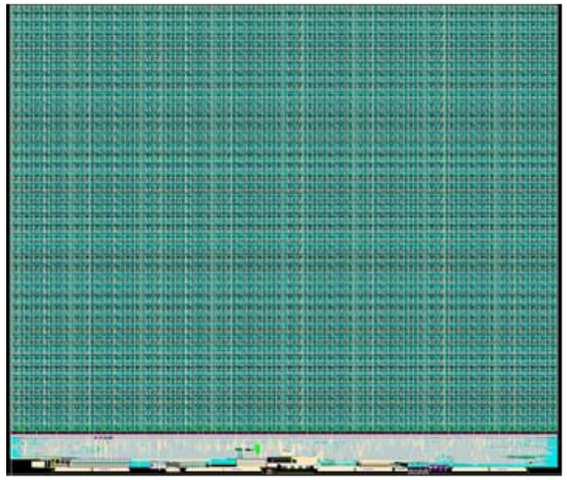




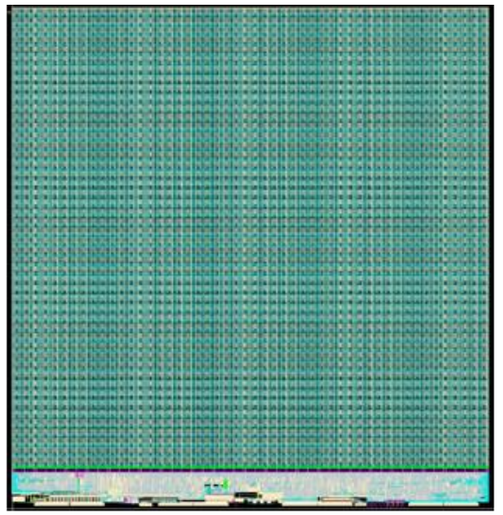
RD53

Pixel detectors for CMS and ATLAS

- ASICs are “instances” of a common design
- Targeting experiment specific requirements:
  - Different sizes
  - Different analogue front-ends:
    - Linear Front-End (CMS)
    - Differential Front-End (ATLAS)
- Links:
  - Command, control and timing: 160 Mb/s
  - Data: 4 x 1.28 Gb/s
- Power:
  - Serial powering
- Collaborative work
  - Since 2013
  - 24 institutes worldwide
  - ATLAS ITkPixV2 currently under test
  - CMS CROCv2 submission end 2023



RD53C-CMS (CROCv2)
Sept. 2023



RD53C-ATLAS (ItkPix2)
March 2023

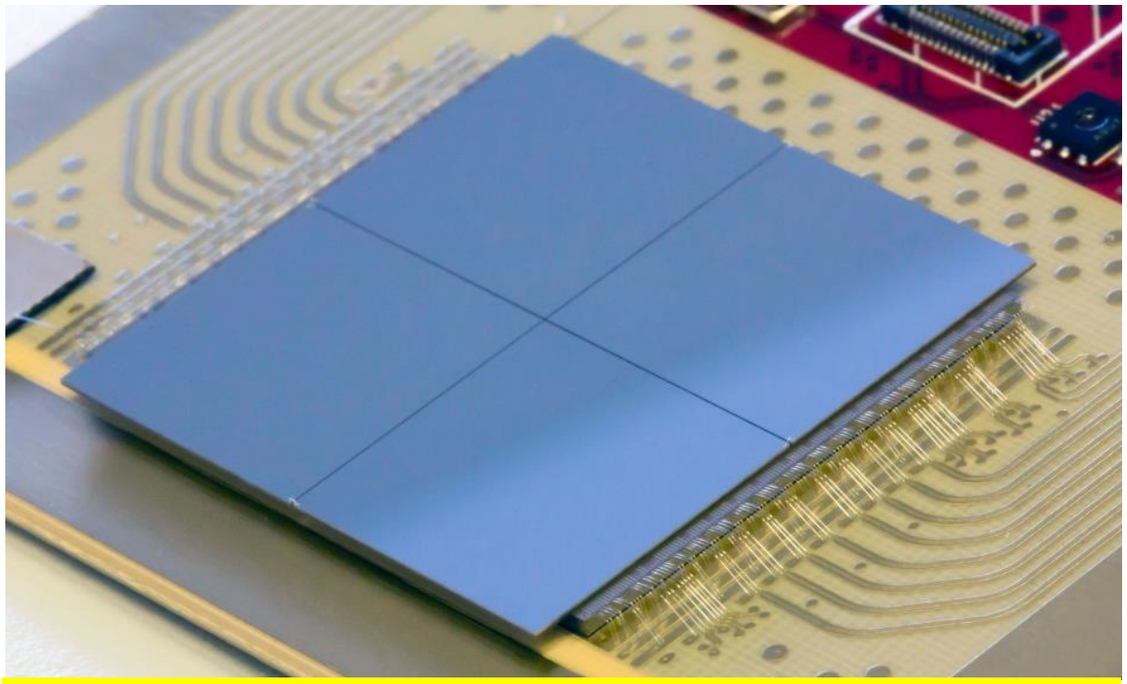
Parameter	Value (CMS/ATLAS)
Technology	65 nm CMOS
Max. hit rate	**3.5 GHz/cm²**
Trigger rate	**750 kHz / 1 MHz**
Trigger latency	**12.5 µs**
Pixel size (chip)	**50 x 50 µm²**
Pixel size (sensor)	50 x 50 µm² or 25 x 100 µm²
Pixel array	432 x 336 pixels / 400 x 384 pixels
Chip dimensions	21.6 x 18.6 mm² / 20 x 21 mm²
Detector capacitance	< 100 fF (200fF for edge pixels)
Detector leakage	< 10 nA (20nA for edge pixels)
Min. threshold	**< 1000 e-**
Radiation tolerance	**1 Grad** over 10 years at -15°C
SEE tolerance	**SEU rate, innermost: ~100Hz/chip**
Power	**< 1W/cm²**, Serial powering
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Temperature range	-40°C ÷ 40°C

Timepix4

Imaging and timing

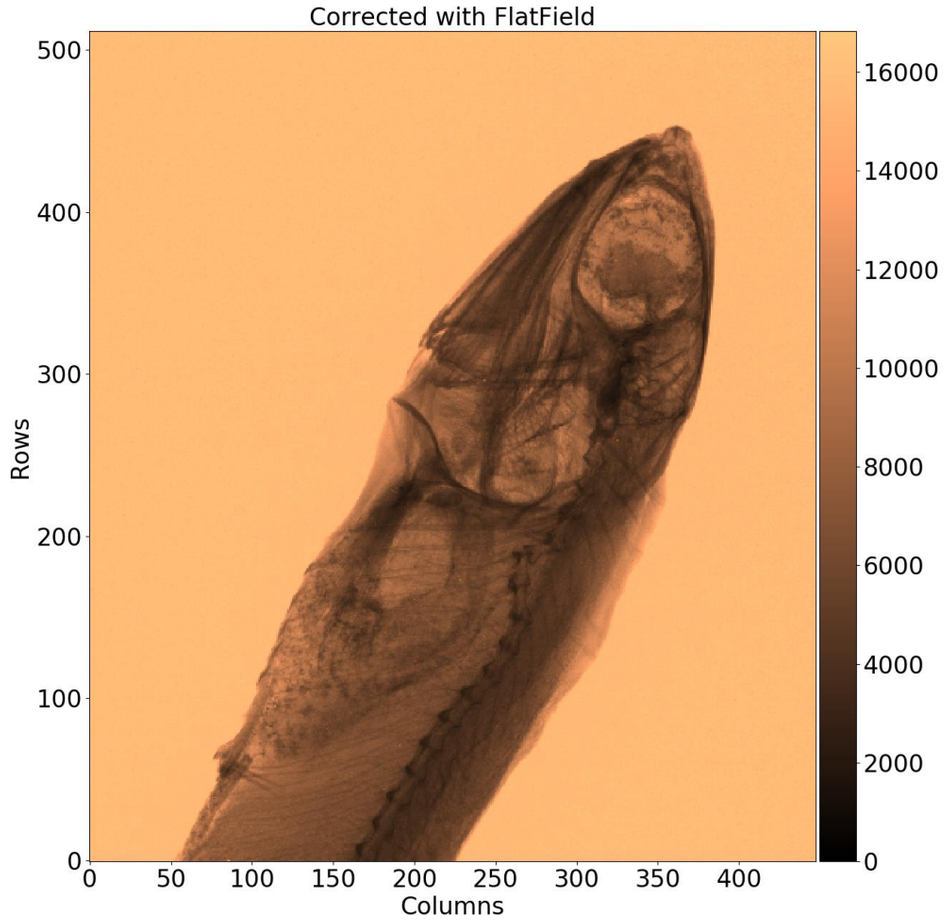
Technology			65nm – 10 metal
Pixel Size			55 x 55 µm
Pixel arrangement			4-side buttable* 512 x 448
Sensitive area			6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA
		Event Packet	64-bit (Addr + TOA + TOT)
		Max rate	**$3.58x10^6$ hits/mm^2/s**
		Max Pix rate	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	CRW: PC (8 or 16-bit)
		Frame	Not-zero-suppressed
		Max count rate	~5 x 10^9 hits/mm^2/s
TOT energy resolution			**< 1Kev**
Time resolution			**195ps bin → ~60ps_{rms}**
Readout bandwidth			16 x @10.24 Gbps
Minimum threshold			<500 e^-

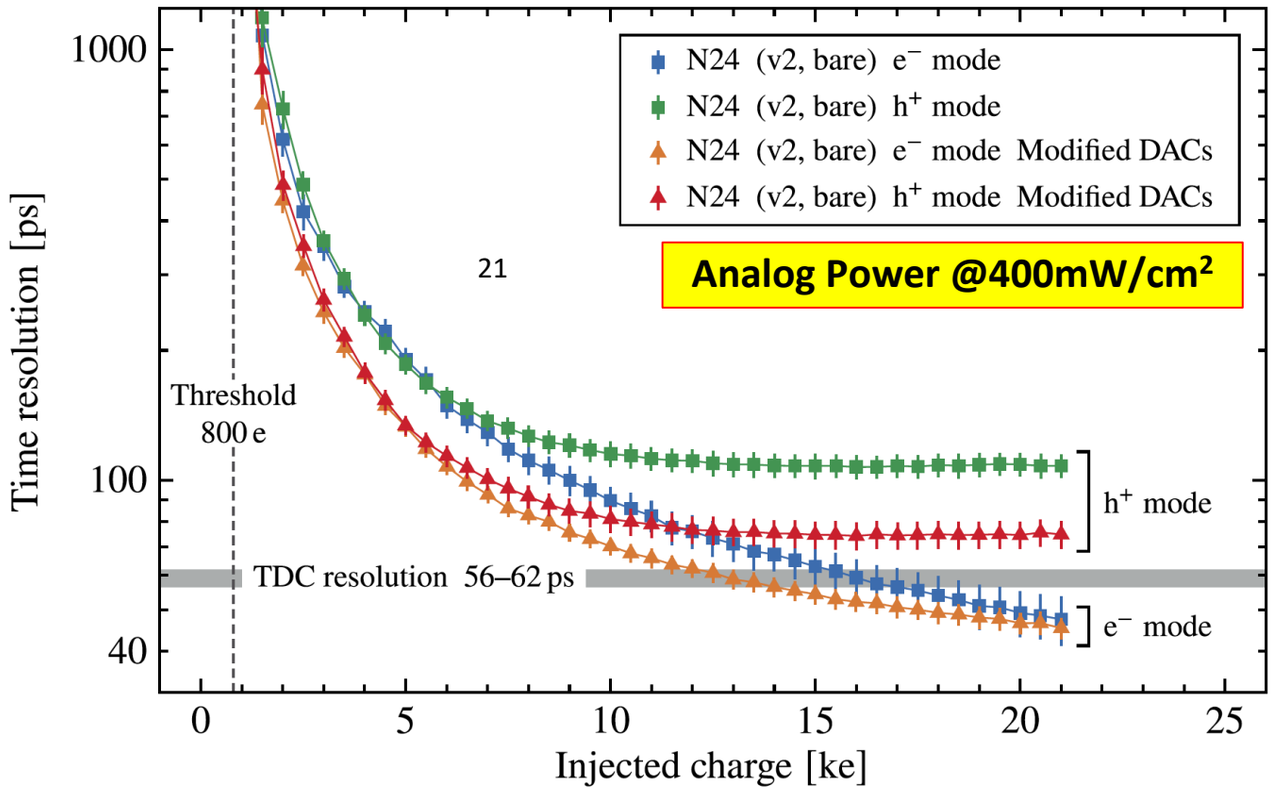
* With TSV technology



Timepix4v0 with 4x300 µm (256x256) edgeless Si sensor (August 2020)

https://indico.cern.ch/event/1121147

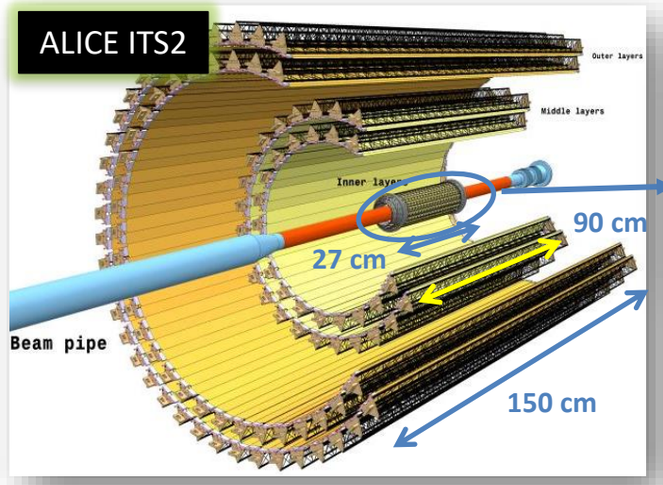




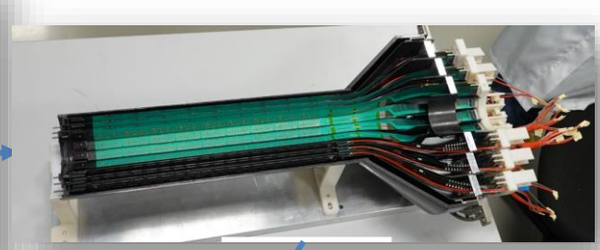
Monolithic pixel detectors

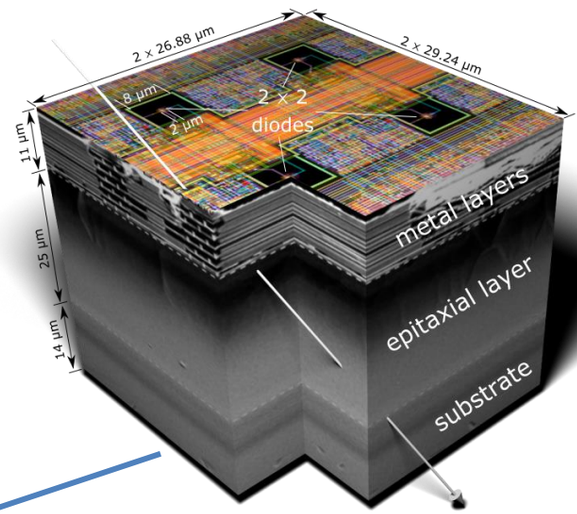
Monolithic Stitched Sensor (MOSS & MOSAIX)

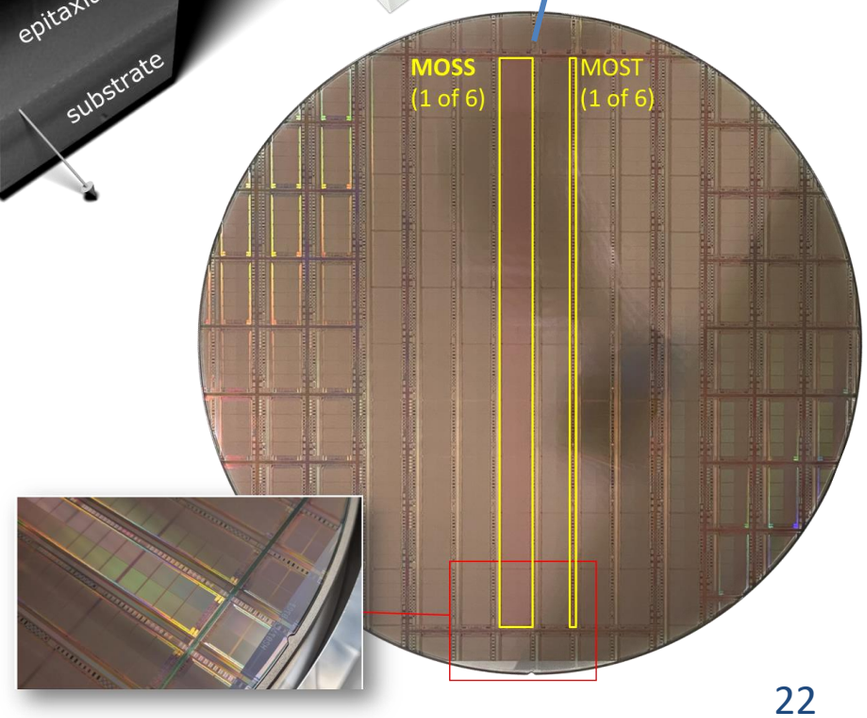
- ALICE Inner Tracking System (*ITS*) replacement
- Layers
  - With dimensions up to 266 mm × 92 mm
  - Made with single die sensors
  - The sensors thinned below 50 µm and bent as true half-cylinders
- Monolithic pixel prototype chip (MOSS)
  - Proof of concept for the ALICE ITS3 upgrade
  - To explore the stitching technique
    - Technique to manufacture modular chips that are much larger than the design reticle
  - Investigate the achievable yield
  - Fabricated in a 65 nm CMOS Imaging Process
  - Measuring 259 mm × 14 mm
    - Wafer scale integration
  - Chips available April 2023
- MOSS Architecture
  - Ten abutted and Repeated Sensor Units (RSU) of 25.5 mm × 14 mm
  - Two small end-cap regions at the two sides of the abutted RSUs
  - Top pixel array: 4 × (256 × 256 pixels) with pitch of 22.5 µm
  - Bottom pixel array: 4 × (320 × 320 pixels) with pitch of 18 µm
  - 6.72 million pixels

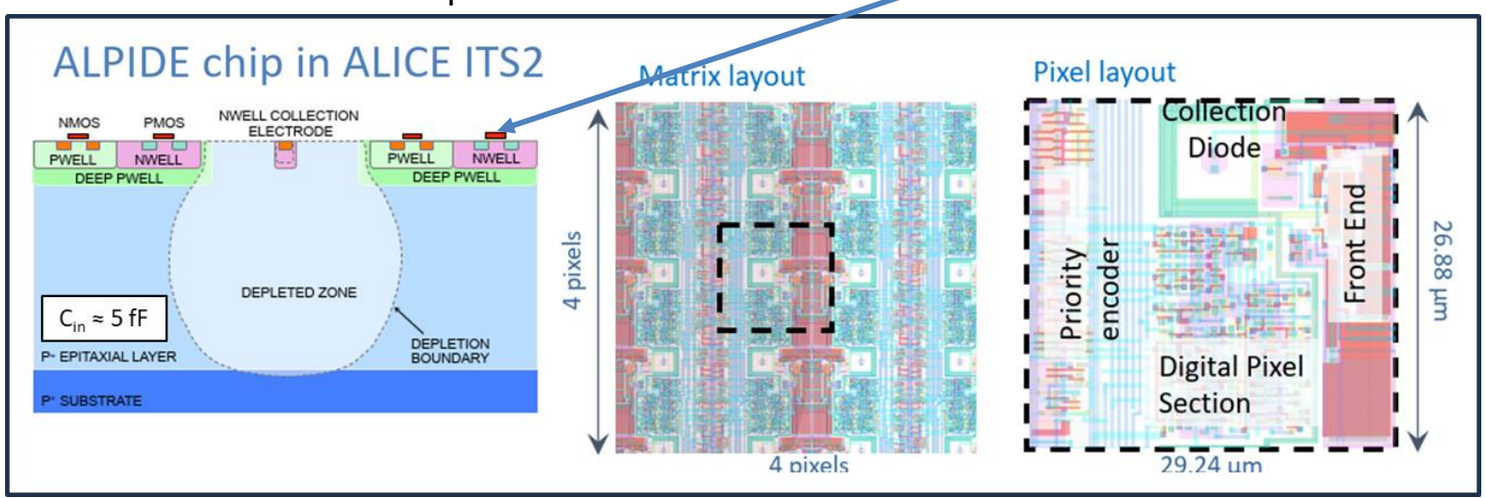


~12.5 Gpixels, 10 m^2 sensitive area
24120 **ALPIDE** Pixel Sensors (CMOS 180 nm)









(65 nm CMOS Imaging Process)

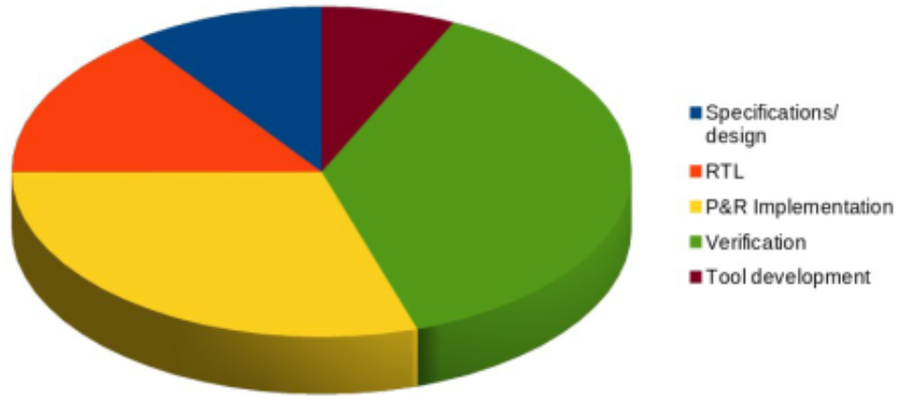
The “hidden faces” of microelectronics

Digital Design

- ASIC designs are becoming evermore complex
  - In industry
  - In HEP
- The CAD tools complexity follows to coupe with
  - Technology complexity (“exploding” number of design rules)
  - Functionality
  - Density
  - Design for reliability
- Teams naturally increase to cope with design complexity
- Engineers specialize to deal with:
  - Complexity (divide and conquer)
  - Efficient used of CAD tools
- Verification becomes a must
  - Indispensable for “first time right” ASICs
  - e.g. Four of the last hirings in ME were verification engineers.

Digital design is not only about RTL

- Best effort estimate of the time spent on various steps of block-level and top-level digital design processes (lpGBTv0 and lpGBTv1)
  - Error bars on this plot should be at least 10%



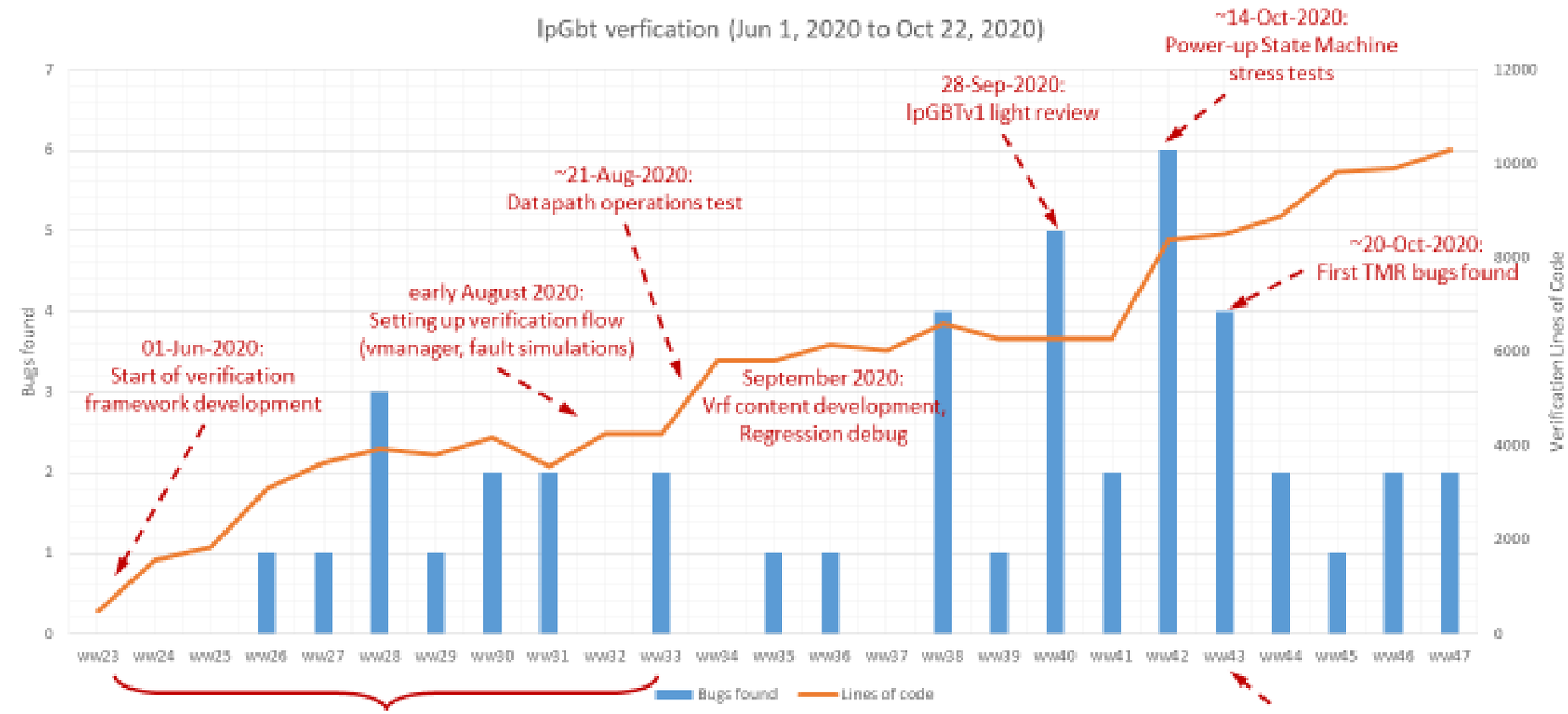
RTL coding is only a small fraction of the total time

Lessons Learned https://lpgbt.web.cern.ch/lpgbt/ 27

The “hidden faces” of microelectronics

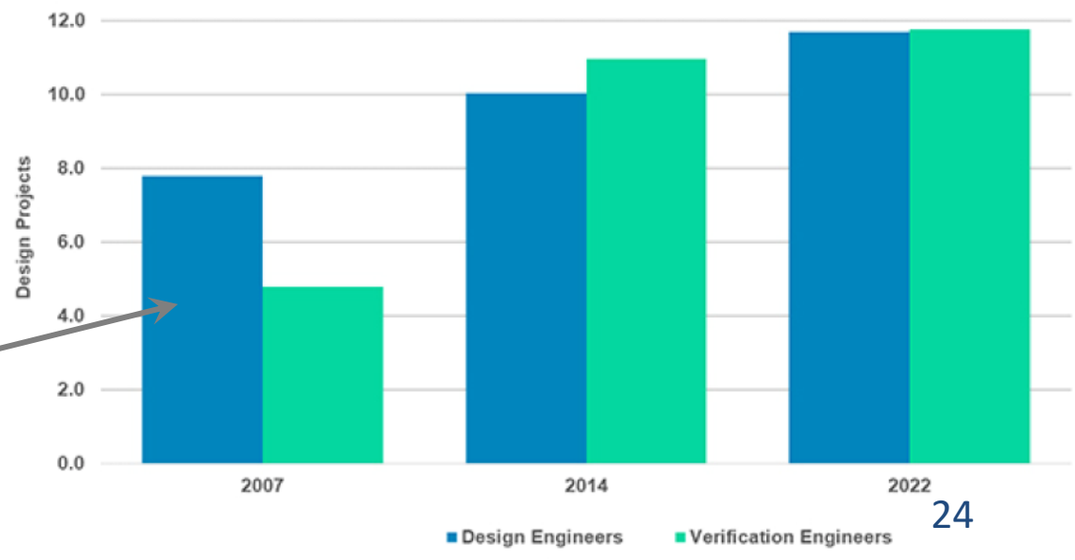
Verification

Verification statistics



“Design engineers spend a significant amount of their time in verification too. …spend on average 51% of their time involved in design activities and **49% of their time in verification**.”

From: White Paper – 2022 Wilson Research Group IC/ASIC functional verification trends



CHIPS

Community Support

ASIC support service for HEP

- Started in January 2020
- To address delays in ASIC developments
  - That could seriously impact the HL-LHC physics programs
- Delays attributed to:
  - Increased complexity of ASICs and CAD tools

IC design Platform & Services

- ASIC design support
  - By EP-ESE-ME experienced designers to HEP community
- Subcontract specialised ASIC design tasks
- Train HEP ASIC designers in medium to long term

Common type of Support

1. Functional verification
2. Digital design (RTL) + PNR
3. SEE robust designs (TMR)
4. Transition to digital-on-top (DoT) designs
5. Analog design support

Since January 2020

- ASICs for 6 detector systems
  - CMS Outer Tracker
  - CMS pixels
  - ATLAS pixels
  - ATLAS ITK
  - CMS HGCAL
  - ATLAS HGTD