环形正负电子对撞机
Circular Electron Positron Collider

# Development of TaichuPix pixel chips for the first CEPC vertex detector prototype


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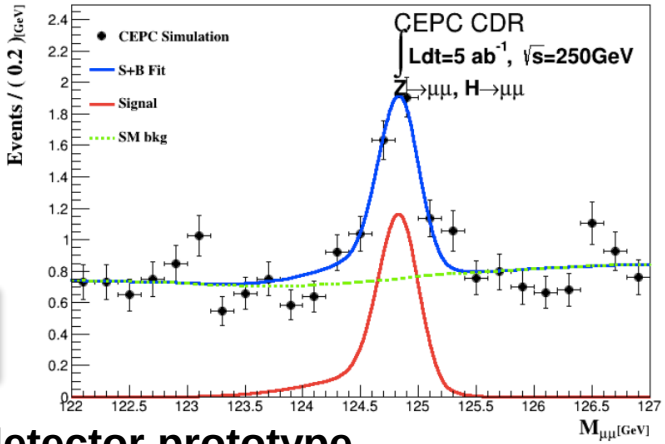
# Vertex detector: Physics goal

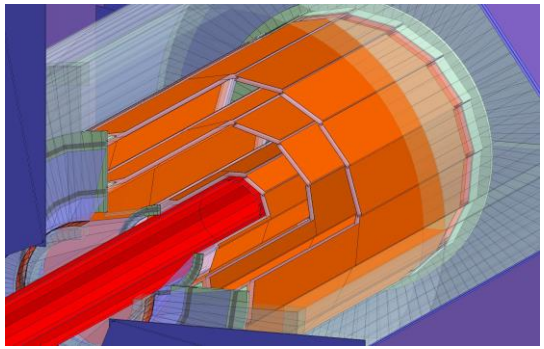
- **Physics motivation**
  - Higgs precision measurement
  - H → bb precise vertex reconstruction
  - H → μμ (precise momentum measurement)

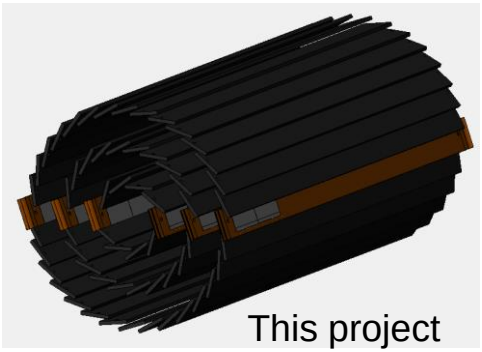



**Need tracking detector with high spatial resolution**

- **Project MOST2 target: produce the first vertex detector prototype**
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (> 1 MRad)

CEPC Vertex detector conceptual design (2016)



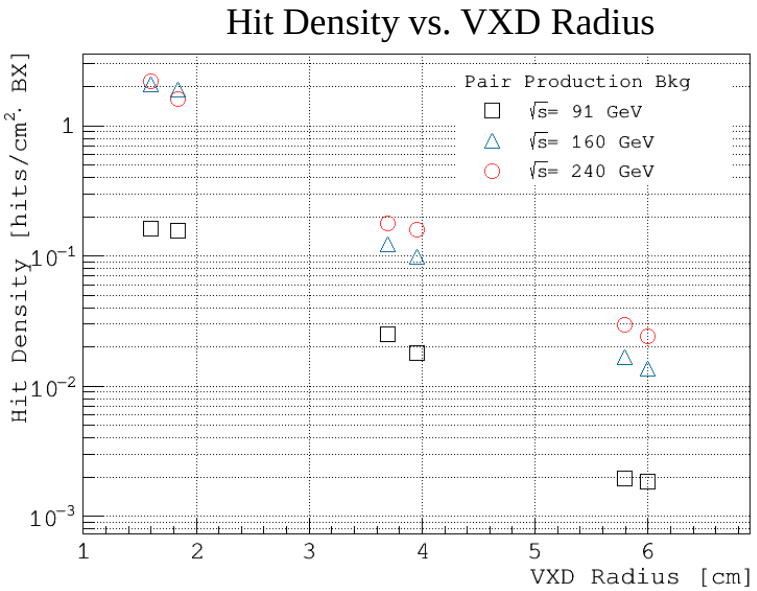


This project
First vertex detector prototype

- **Main technology**
  - High spatial resolution technology → design high granularity pixel chip
  - Radiation resistance technology
  - Detector module prototyping and assembly technology

# Main specifications of the full-scale chip

- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: 25 ns
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm$^2$ for Higgs/W; 0.2 hits/bunch/cm$^2$ for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm

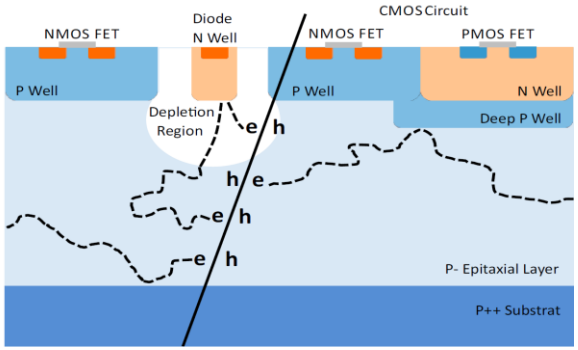



*Ref: CEPC Conceptual Design Report, Volume II*

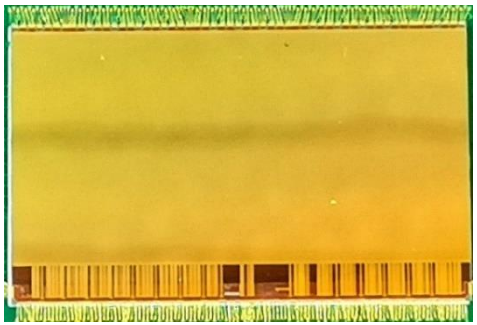
| For Vertex | Specs | For High rate Vertex | Specs. | For Ladder Prototype | Specs. |
|---|---|---|---|---|---|
| Pixel pitch | ≤ 25 μm | Hit rate | 120 MHz/chip | Pixel array | 512 row × 1024 col |
| TID | >1 MRad | Data rate | 3.84 Gbps --triggerless ~110 Mbps --trigger | Power Density | < 200 mW/cm$^2$ (air cooling) |
| | | Dead time | < 500 ns --for 98% efficiency | Chip size | ~1.4 × 2.56 cm$^2$ |

# TaichuPix prototypes overview

- **Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype**
- **Major challenges for design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz ) → for CEPC Z pole
  - Radiation tolerance (per year): 1 MRad TID
- **Completed 3 rounds of sensor prototyping in a 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm )
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023



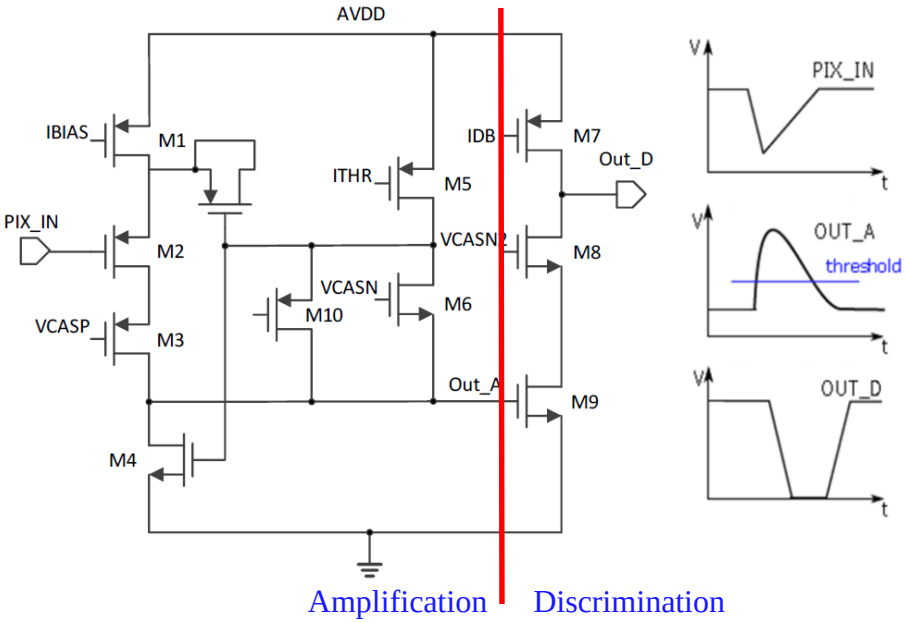

**CMOS monolithic pixel sensor**

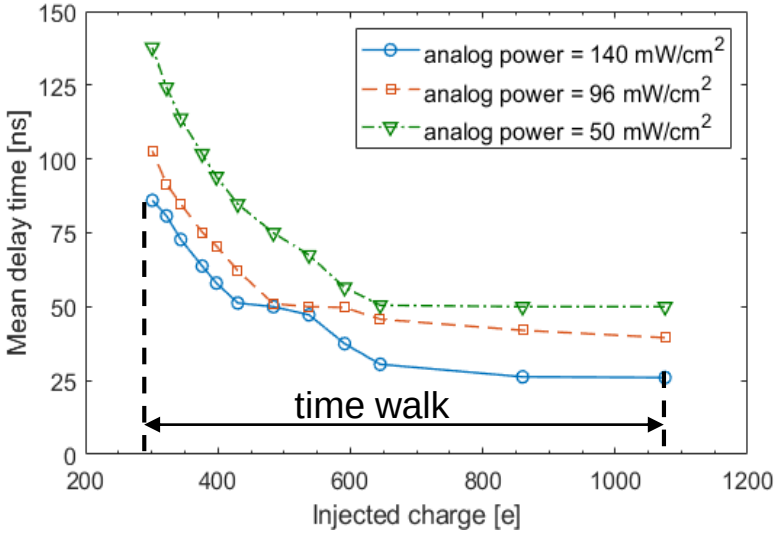


**TaichuPix-3**
(15.9 × 25.7 mm$^2$)

# Pixel architecture – Analog

Ref : D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

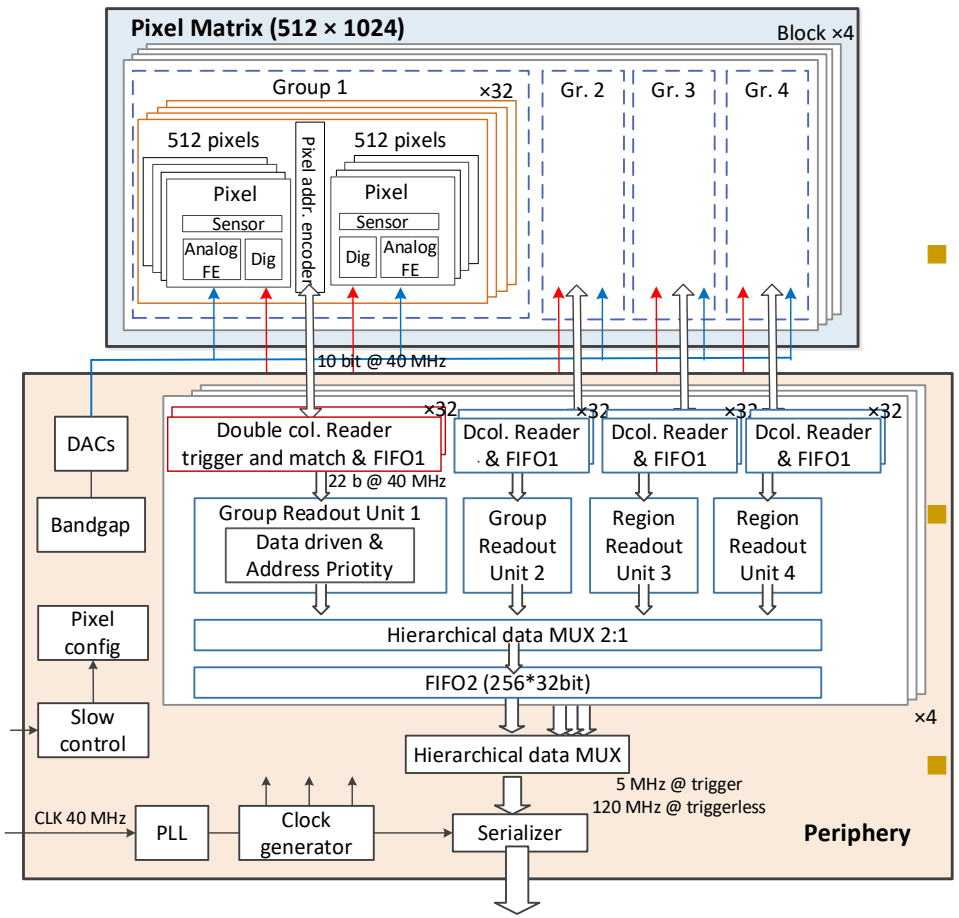



Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp with a step of 25 ns.

- **Digital-in-Pixel scheme: in pixel discrimination & register**
- **Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)**
  - As most of ATLAS-MAPS sensors' scheme
- **Biasing current has to be increased, for a time walk of ~25 ns**
  - for 40 MHz BX @ Z pole
- **Consequence:**
  - Power dissipation increased
  - Fast charge collection needed

# TaichuPix sensor architecture

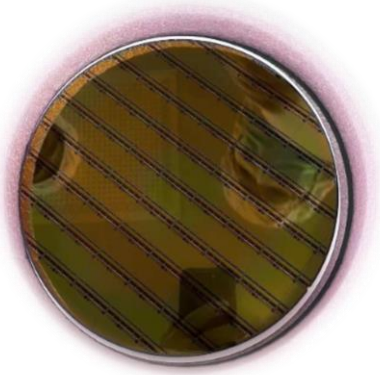



Architecture of the full-scale TaichuPix

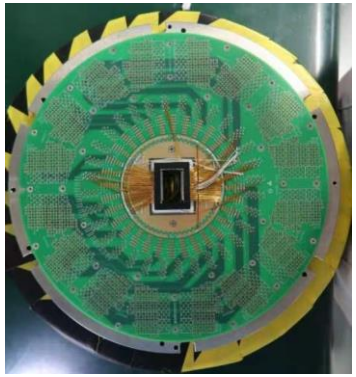
- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

# Full size sensor TaichuPix-3

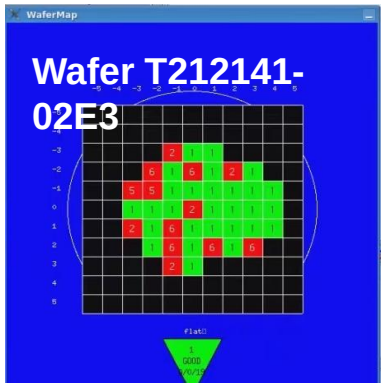
- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafers tested on probe-station** → chip selecting & yield evaluation



8-inch wafer

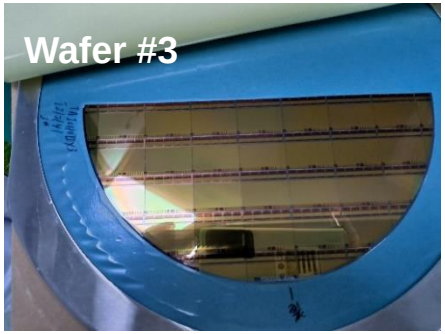


Probe card for wafer test




An example of wafer test result (yield ~67%)

  - **Wafers thinned down to 150 μm and diced**

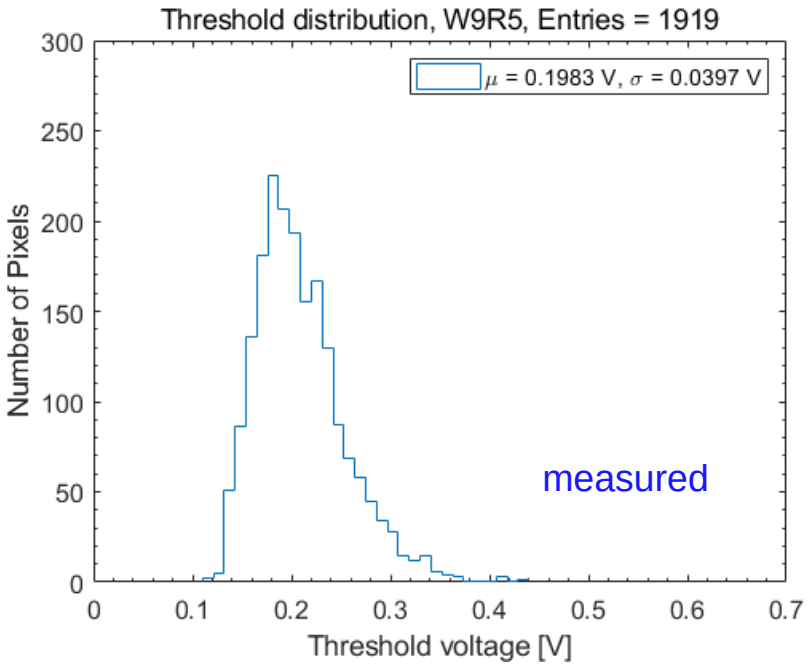


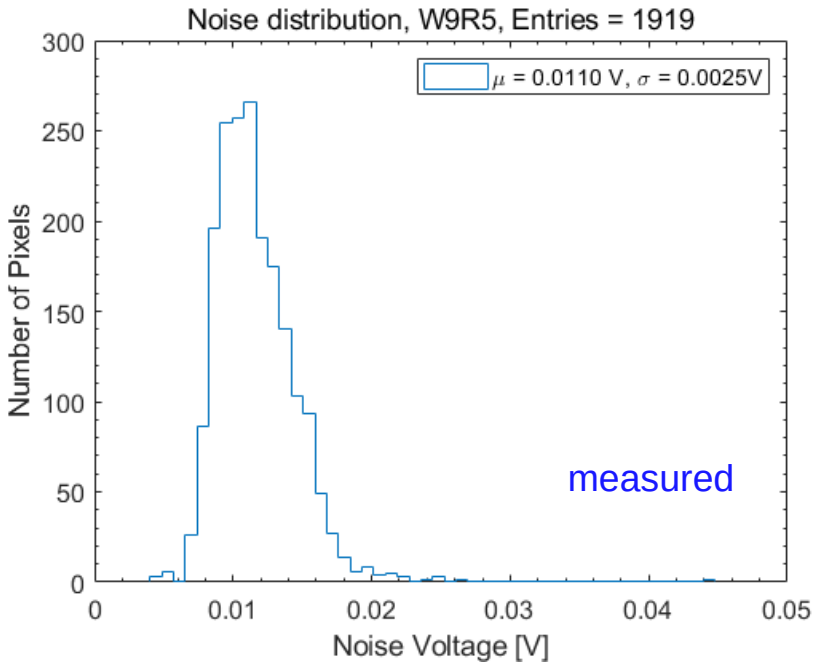

Wafer after thinning and dicing


Thickness after thinning

# Threshold and noise of TaichuPix-3

- **Pixel threshold and noise were measured with selected pixels**
  - S-curve method was used to test and extract the noise and the threshold
  - Average threshold ~215 $e^-$, threshold dispersion ~43 $e^-$, temporal noise ~12 $e^-$ @ nominal bias setting

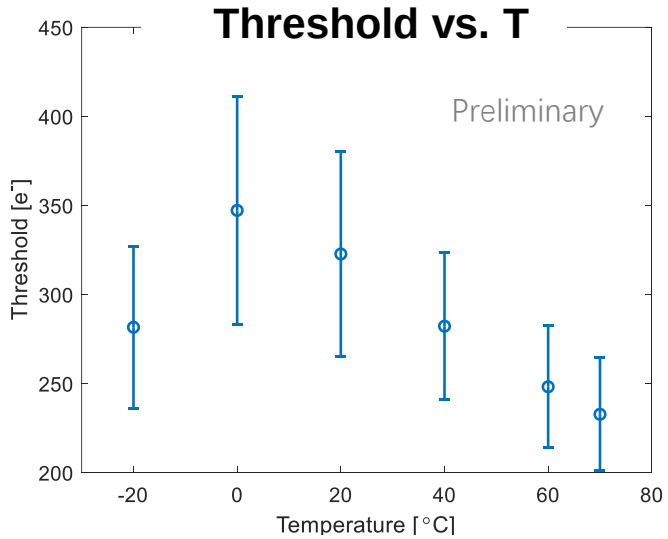


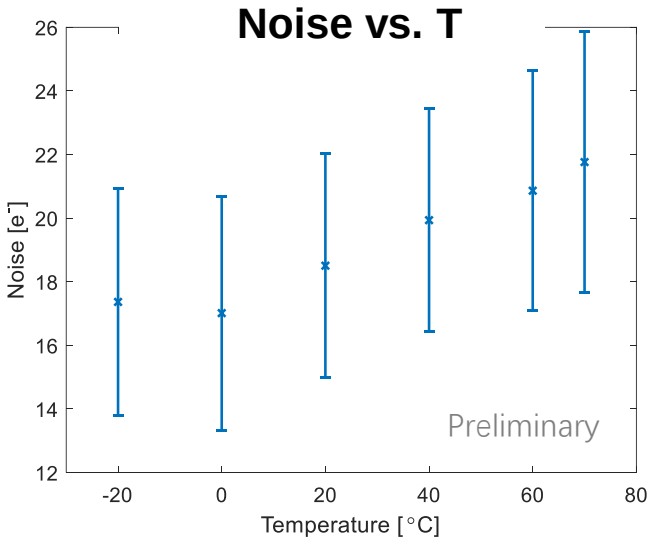



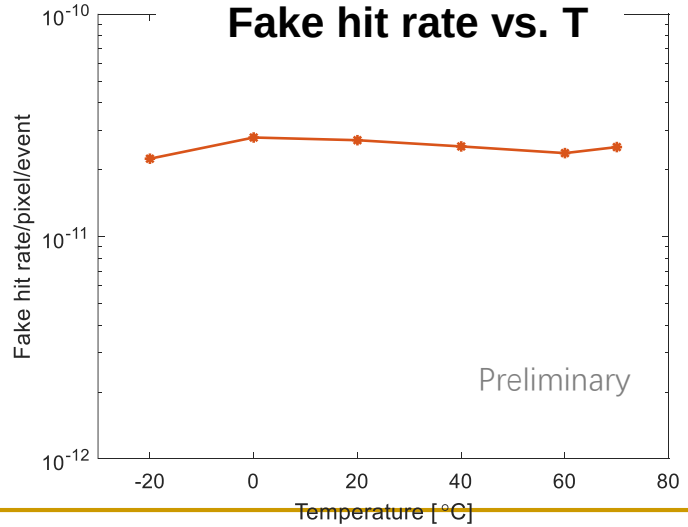

- **Power dissipation of 89 ~ 164 mW/cm$^2$ tested @ 40MHz clk with different biasing condition**

# Performance at different temperatures

- **Test under a consistent configuration @ different T**



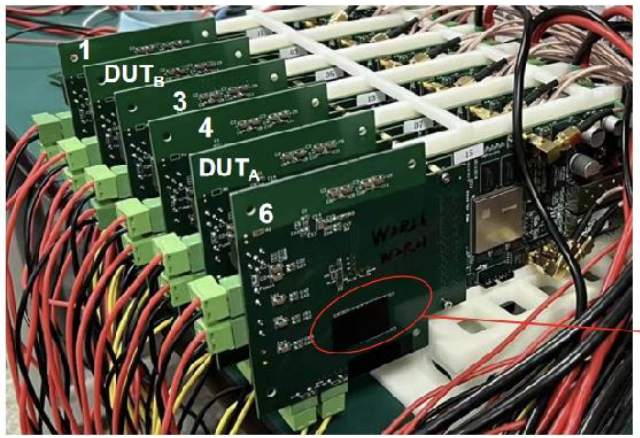



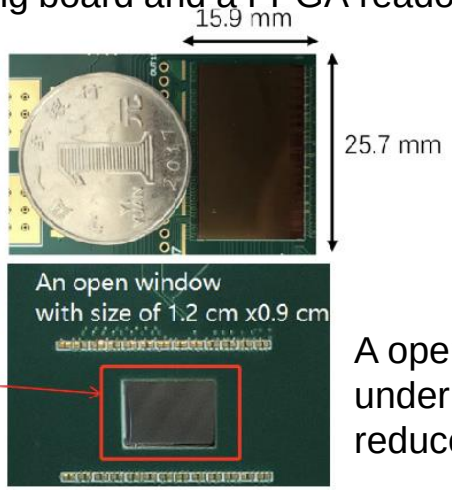




- **TC3 shows a normal functionality @ -20 ~ 70 °C**
- **Main performance (i.e. threshold, noise, fake hit rate) can satisfy the requirements @ -20 ~ 70 °C**
- **Threshold and noise fluctuate with T, probably attribute to the fluctuation of pixel biasing**

# TaichuPix-3 telescope

- **The 6-layer of TaichuPix-3 telescope built**
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board

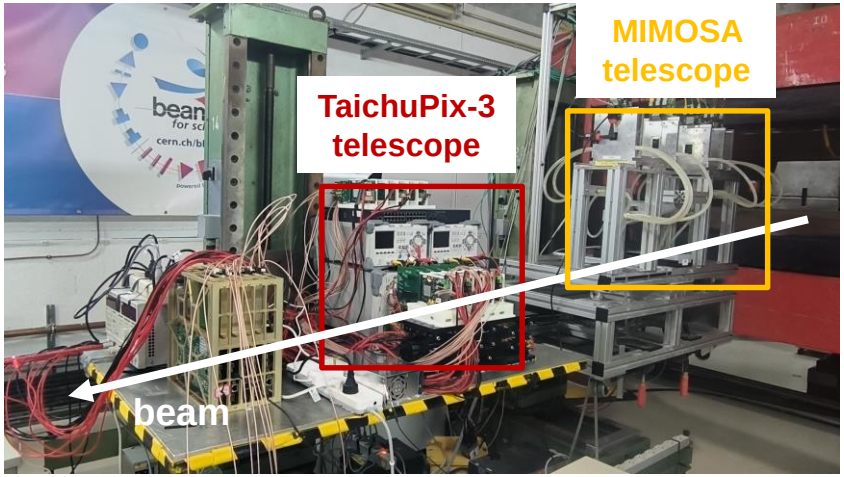



A open window on PCB under TC3 chip to reduce multi-scattering

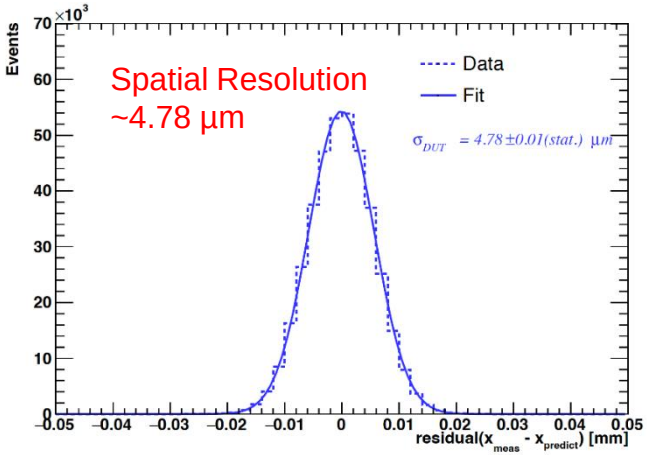
6-layer TaichuPix-3 telescope

- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT (Detector Under Test)

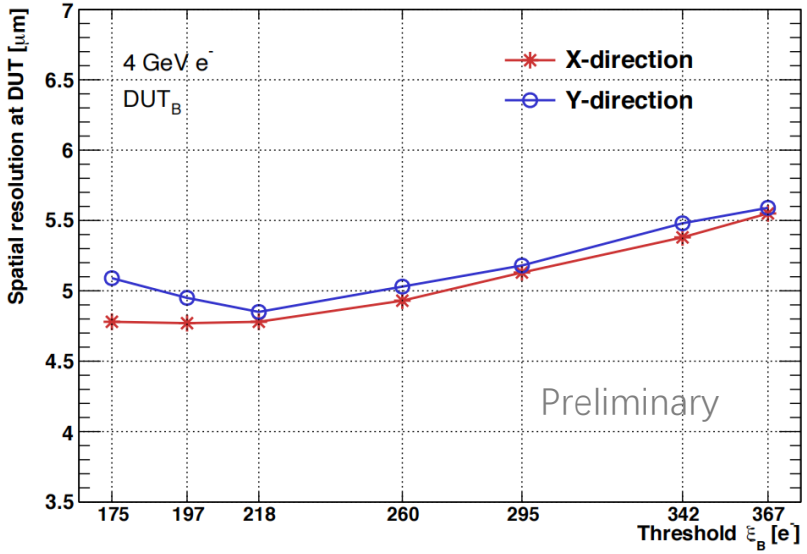


# TaichuPix-3 beam test result

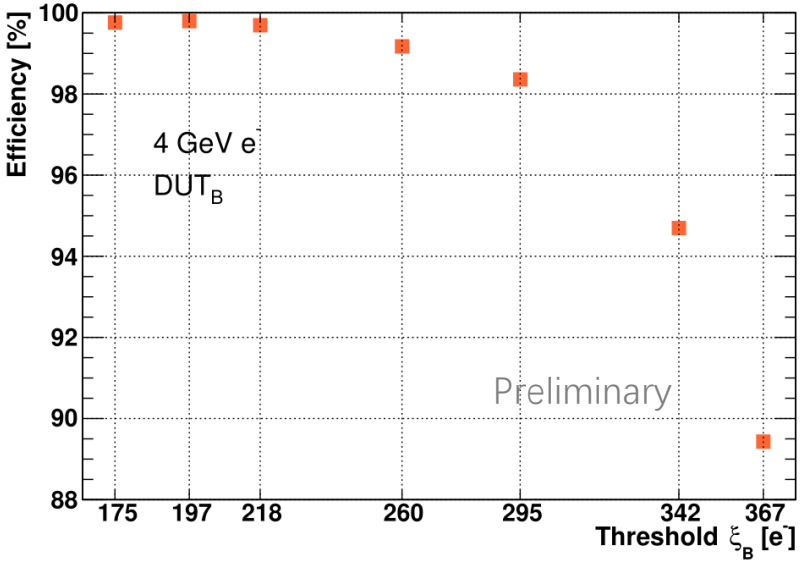
- **Spatial resolution**
  - Gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved, best resolution is 4.78 μm
- **Detector efficiency**
  - Decreases with increasing the threshold, detection efficiency >99.5% at threshold with best resolution




Distribution of residual X



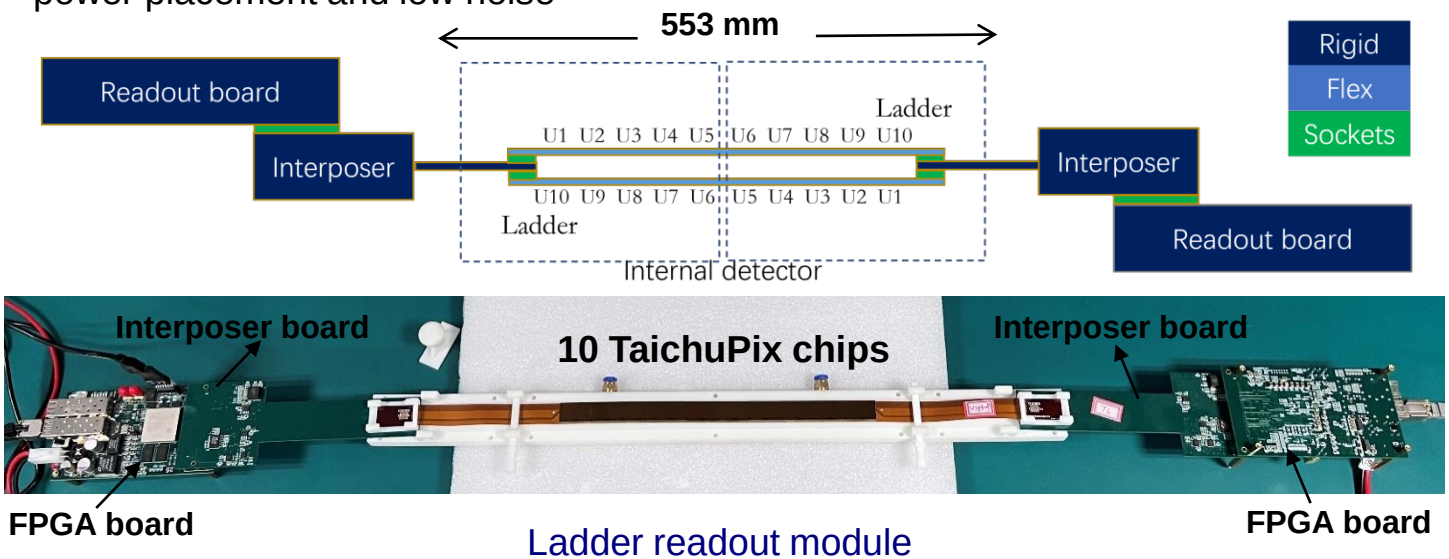

Spatial resolution vs. pixel threshold




Detection efficiency vs. pixel threshold

# Ladder readout design

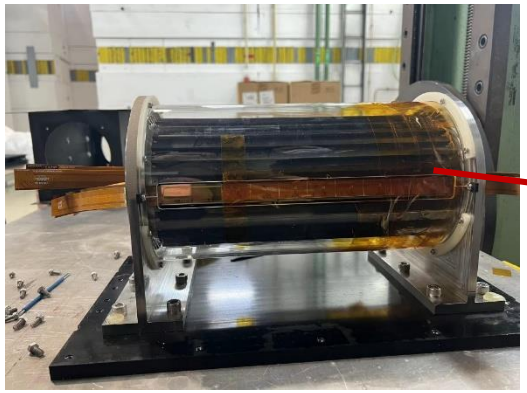
- **Detector module (ladder) = 10 sensors + readout board + support structure + control board**
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Challenges**
  - Long flex cable → hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals
- **Solutions**
  - Read out from both ends, readout system composes of three parts, careful design on power placement and low noise

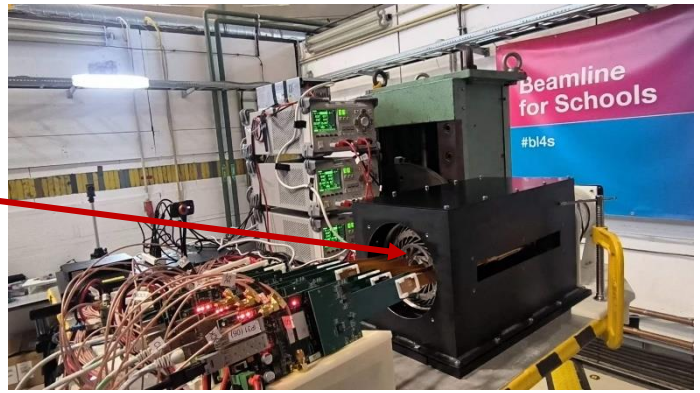


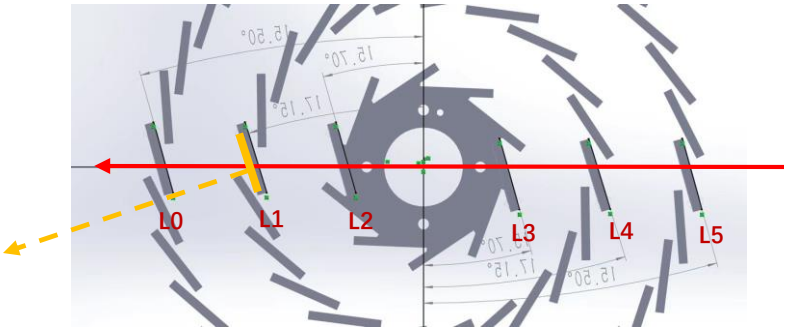

Ladder readout module

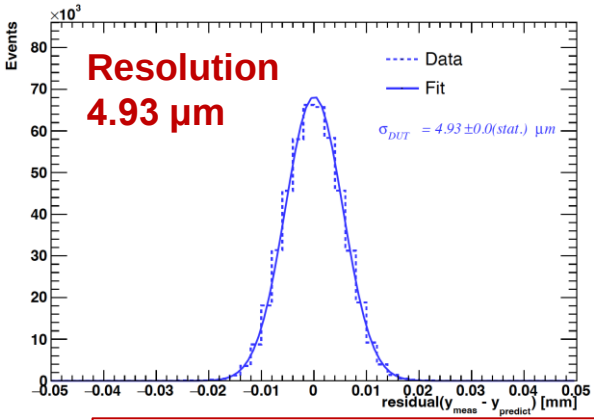
# Detector prototype

- **6 double-sided layers assembled on the detector prototype**
  - 12 flex boards with two TaichuPix-3 chips bonded on each flex
  - Readout boards on one side of the detector






Preliminary offline results indicate a good performance for the vertex detector prototype.

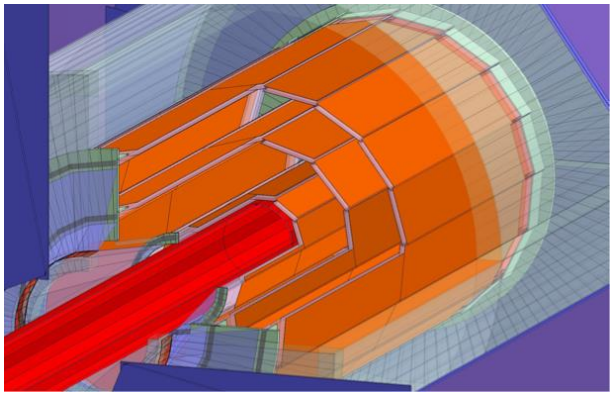
| | L0-L1 | L1-L2 | L2-L3 | L3-L4 | L4-L5 |
|---|---|---|---|---|---|
| L(mm) | 21.2 | 20.6 | 37.46 | 20.6 | 21.2 |

Details find in poster “Offline analysis for the beam test of CEPC vertex detector prototype”

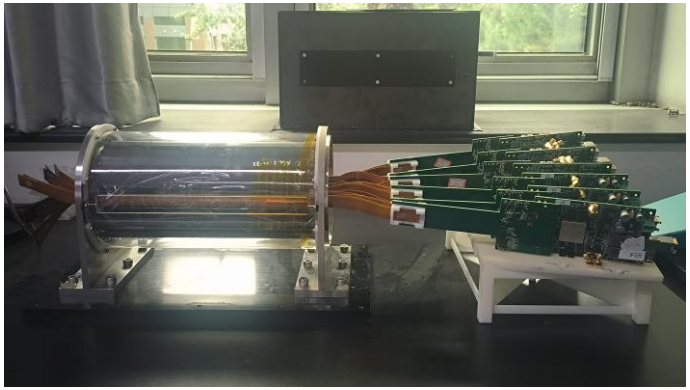
# Summary

- **The full-scale and high granularity pixel prototype, TaichuPix-3, has been designed and tested for CEPC VTX R&D**
  - Spatial resolution of 4.78/4.85 μm measured with 4 GeV electron beam in DESY
  - Total ionization dose (TID) > 3 Mrad

- **Readout electronics for the sensor test and the ladder readout were developed**
  - Performed the sensor characterization in the lab successfully
  - Completed beam tests for the pixel sensor prototype and the vertex detector mechanical prototype



**Concept (2016)**



**1st Vertex detector prototype (2023)**

**Thank you very much for your attention !**