清華大學 Tsinghua University

核电子学实验室 Laboratory of Nuclear Electronics

Development of an energy and timing measurement ASIC for gas and semiconductor detectors

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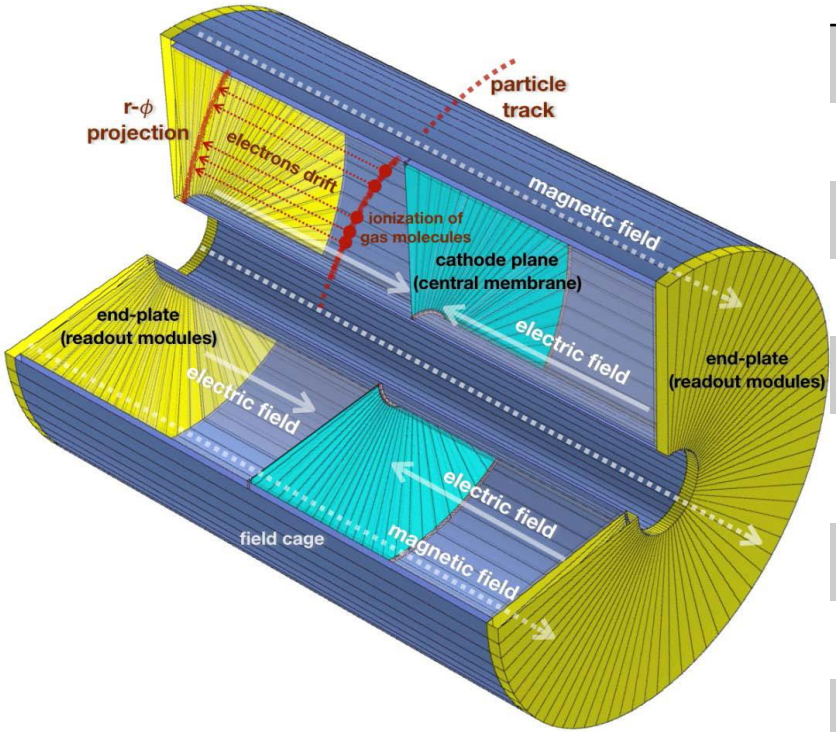
Outlines

- Introduction
- R&D on Macro-pixel TPC readout
- Readout ASIC Test
- Summary

Introduction

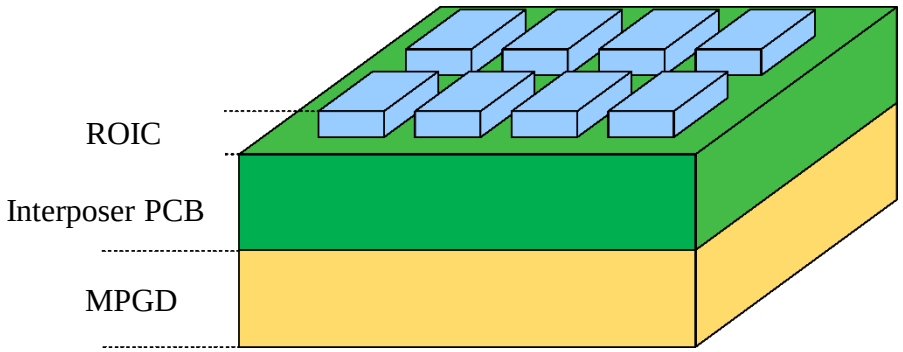


Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm × (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6 mm) are needed, resulting in ~1 million channel of readout electronics
- Need time&energy-resolved, low power readout electronics working at continuous mode

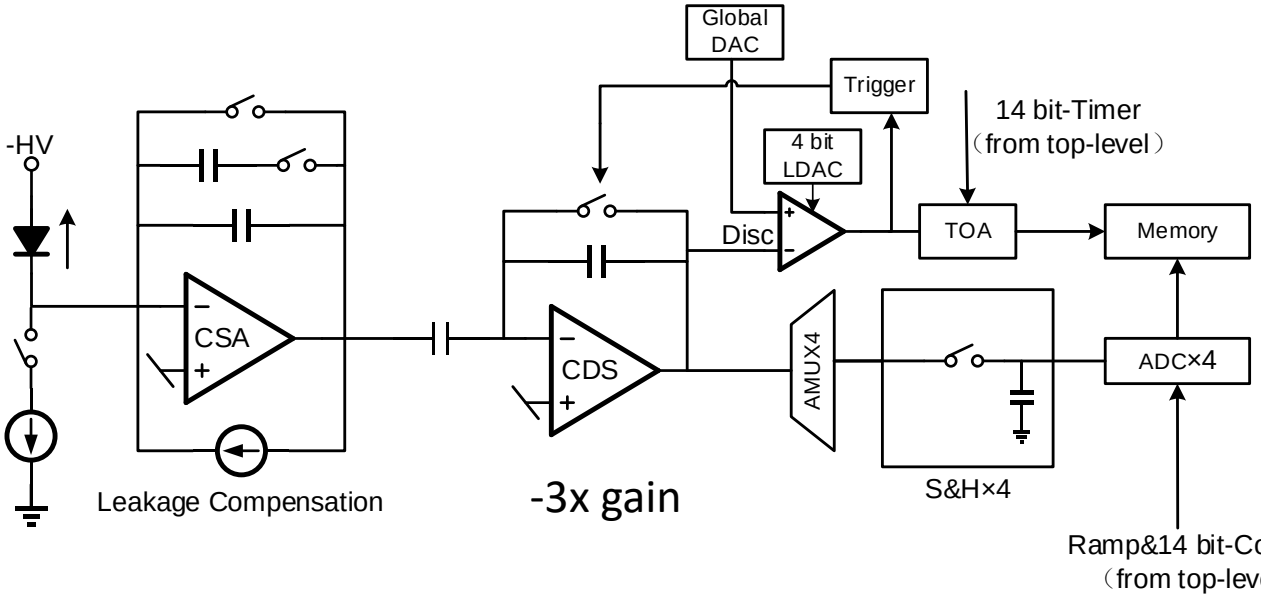
R&D on Macro-Pixel TPC Readout

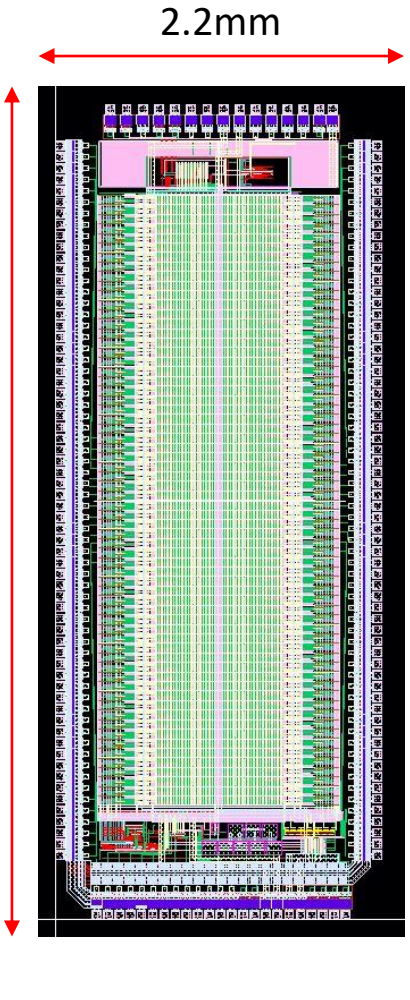
- Large Pixel Readout
  - 1 mm x 6 mm → 0.5 mm pixel
  - Higher precision, higher rate
  - Gas or semiconductor detectors
- Concept Design
  - ROIC +Interposer PCB as RDL
  - High metal coverage, 3~4-side buttable，flexible
  - Low power Timing/ Energy measurement ASIC（TEPIX）
    - ~160 e noise
    - 5 ns drift time resolution
    - ~100 mW/cm^2



Front-end of TEPIX

- Charge Sensitive Preamplifier(CSA) with 2 fixed gains
- CDS amplifier provides additional gain and noise shaping
- 14-bit Wilkinson type ADC each pixel
- Timing discriminator with14-bit TOA (Time of Arrival) information

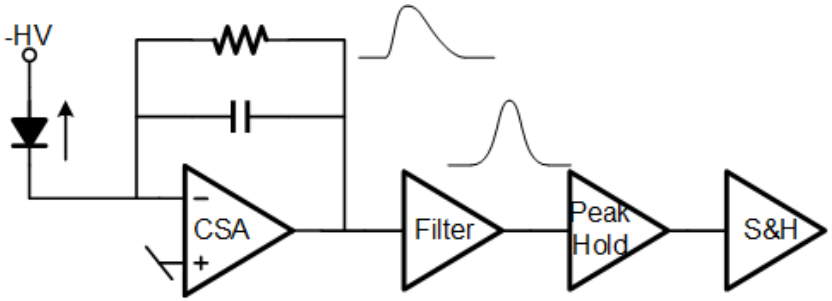




Comparison of Different FE Structures

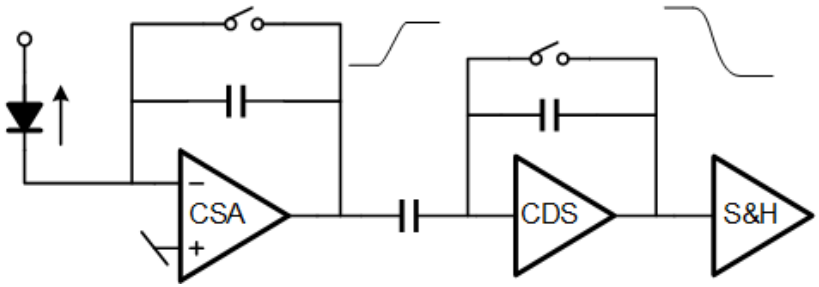
➢ Conventional Structure

- Resistor and capacitor feedback
- Low pass filter to improve SNR
- Trigger-based readout
- Count rate limited by peak time
- High power, high noise(complicated)



➢ Charge Integration Preamplifier

- Pulse reset/feedback
- Correlated double sampling
- Frame-base readout
- Count rate ~ frame rate
- Low power, low noise

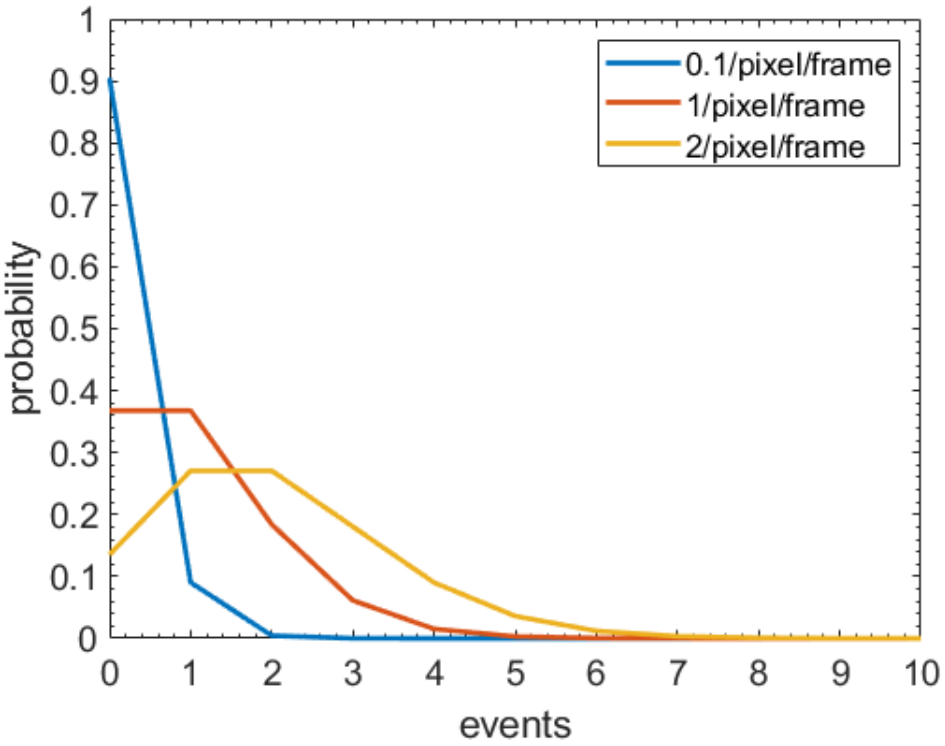


Count Rate

- In-pixel memory to increase detectable count rate for Poisson event

  0.1/pixel/frame: 10% for 1 event， 0.5% for 2 events

  1/pixel/frame: 1.5% for 4 events， 0.3% for 5 events

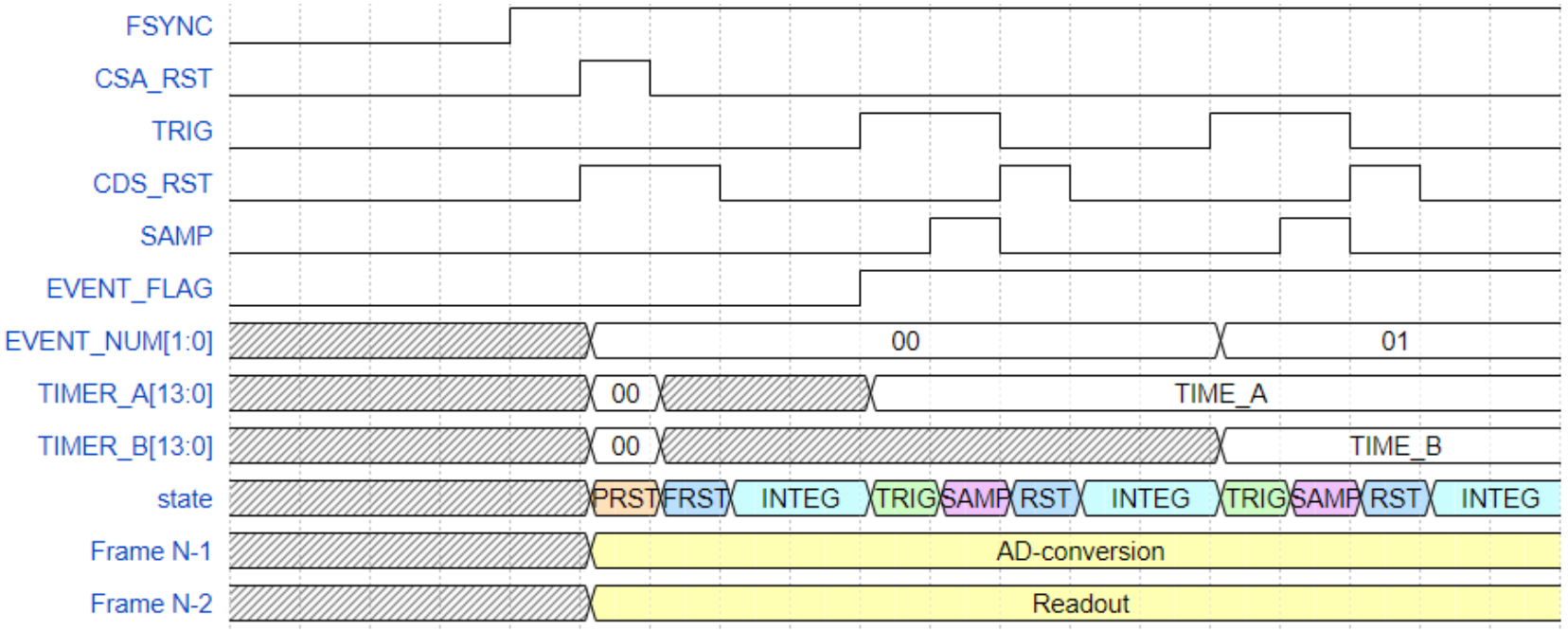


count rate = frame rate *occupancy

Maximum count rate at 10 kfps
Theoretical: 40 kcps/pixel
Recommended： 10 kcps/pixel

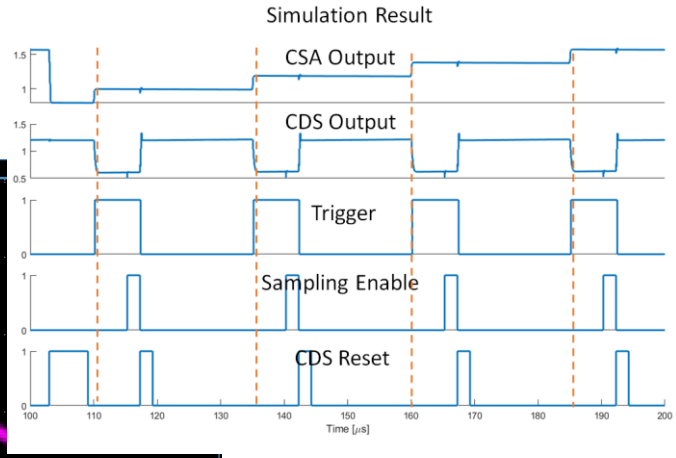
AISC Timing

- Frame-based mode, Token Ring readout
- Near-zero dead time:
  - Dual S/H and register work at ping-pong mode
  - Integration, AD conversion and readout are pipelined



Readout ASIC Test

- v1a(2022.11)：electronic functional verification
- The leakage current of IO is too high

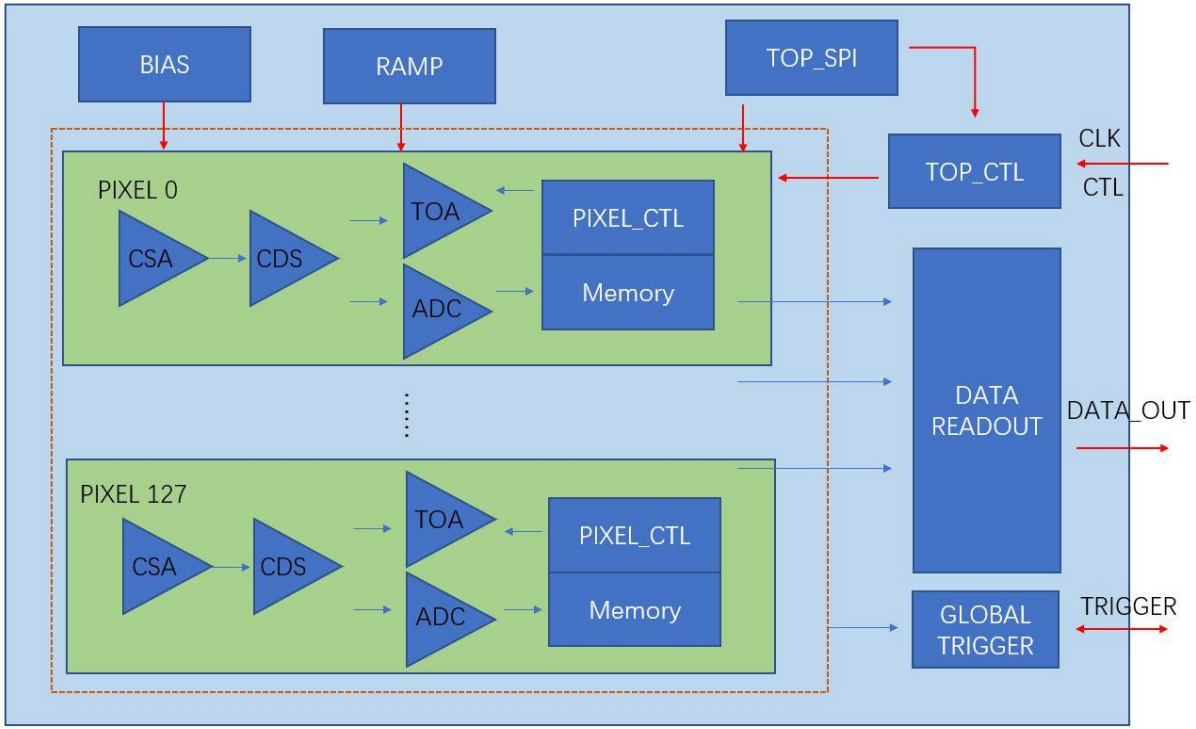


simulation

In-pixel calibration source

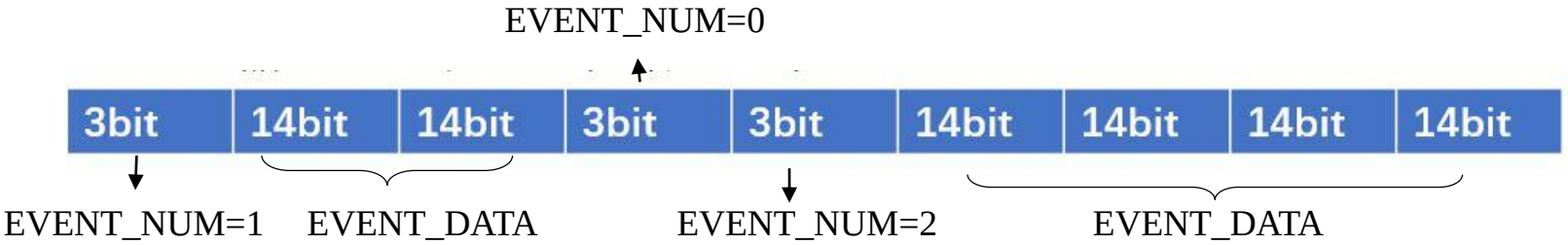
Top-level Design

- On-chip data zero-compression
- Only the fired event can be readout

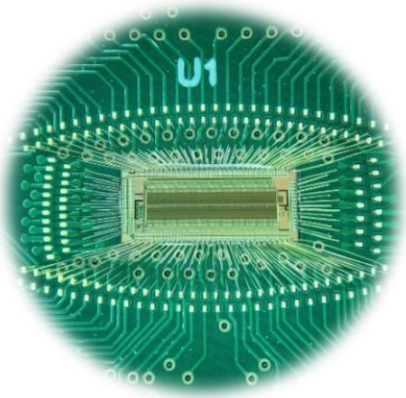


- Trigger Modes

1. Local Self Trigger
2. Global Self Trigger
3. Global External Trigger



Readout ASIC Design



- Specifications

Channel No.	128	Valid Integration Time	≥90% Frame Cycle
Frame Rate	10 kfps	Noise(simulated)	~160 e(ENC@0.5 pF Input)
Gain	40 mV/fC 6 mV/fC	Resolution	Energy:14 bit Time:14 bit(min. 5 ns bin)
Memory Depth	4 events/pixel/frame	Power Consumption	1.36 mW/channel->0.27 mW/channel 531 mW/cm^2->105 mW/cm^2
Input Range	18.75 fC/event(HG) 125 fC/event(LG)	Trigger Mode	1. Local Self Trigger 2. Global Self Trigger 3. Global External Trigger
Count Rate	40 kcps/pixel(Periodic) 10 kcps/pixel(Poisson)	Bandwidth	147 Mbps max.
Leakage Compensation	10 bit@LSB=100 pA		
Discriminator threshold	10 bit GDAC 4 bit LDAC	Technology	180 nm CMOS

v1a: submitted and tested last year

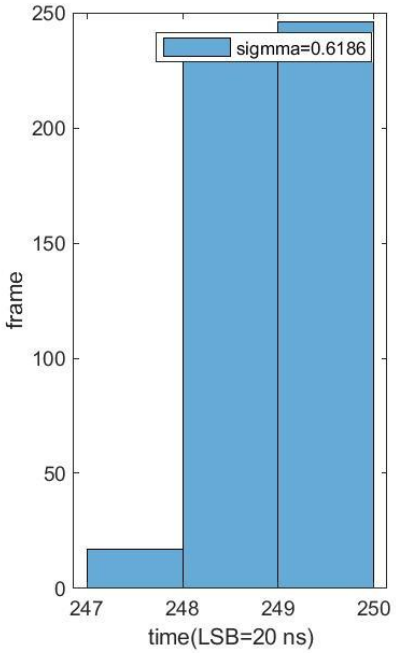
v1b: submitted at Jun. this year and received this month

Readout ASIC Test

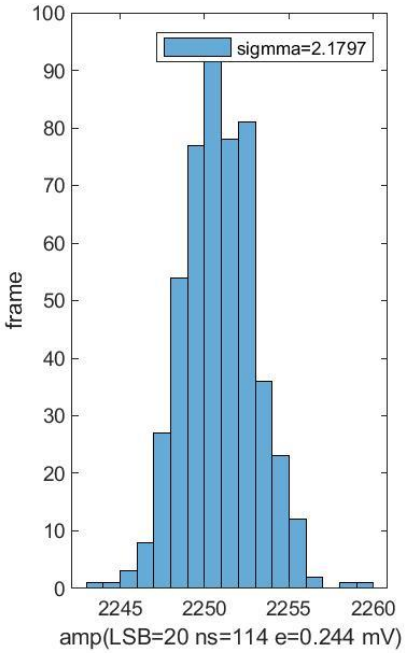
Single channel results

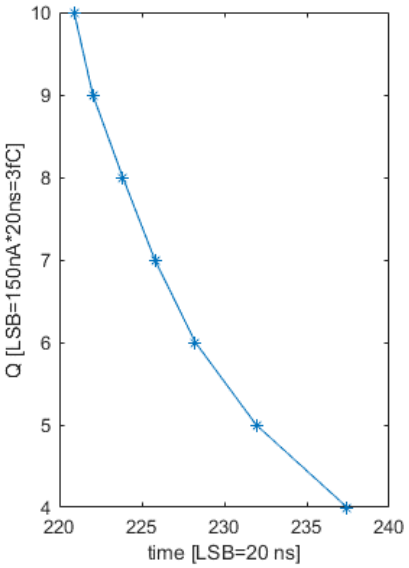
$$C_f V = Q_0 - I_{leak}(TOA + Tdelay + Tsamp - Treset)$$

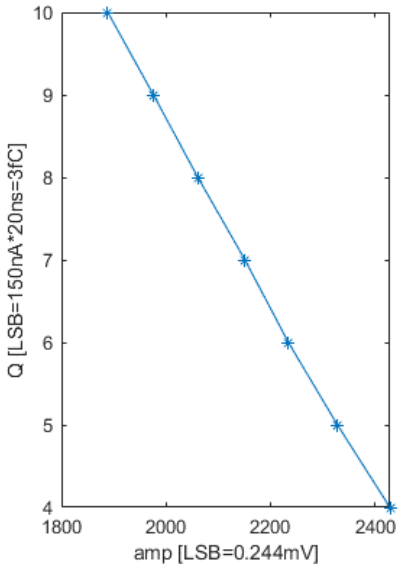
timing rms.~12 ns



ENC~250 e







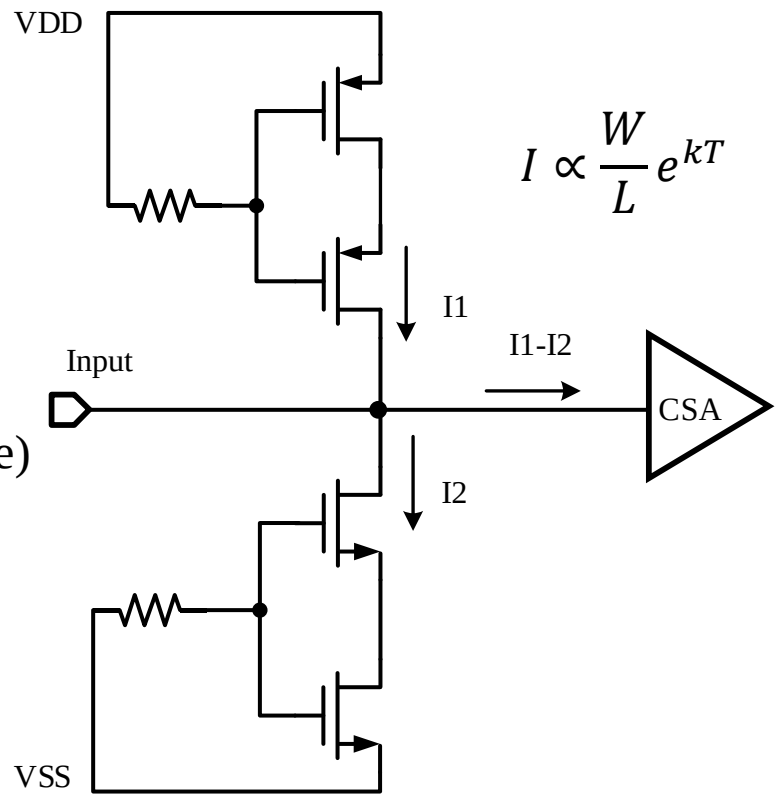
50 MHz timing clock（15 fC input）
high jitter from clock source and quantization error

Due to capacitance errors in the layout, the gain of v1a is only ~1/3 of the design value

$$V(t) = V\left(1 - e^{-\frac{t-t_0}{\tau}}\right) \rightarrow TOA = t_0 + \tau \ln\left(\frac{V}{V - V_{th}}\right)$$

Problems of the First Version v1a

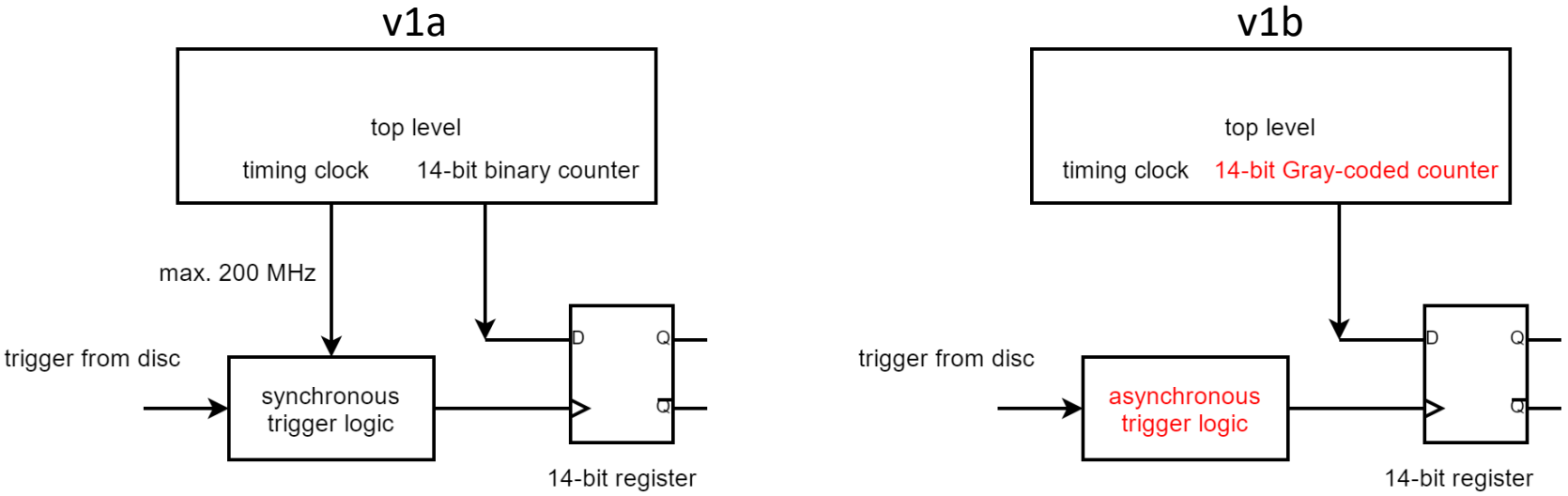
- Leakage current of ESD protection transistors
  - v1a: ~400 pA@ 25 ℃ ambient temperature
  - v1a: ~165 pA@ 25 ℃ junction temperature
  - v1b:~5 pA@ 25 ℃ junction temperature
  - Lower leakage -> lower noise
- Missing capacitance in the pixel layout (LVS rule)
  - CDS gain is only 1/3 of the expected
- Poorly designed clock tree and digital circuit
  - Limited clock frequency and frame rate
  - Very high dynamic power



Power Optimization for the Second Version

- Slower work clock， except for the timing clock
- Synchronous -> asynchronous for timing logic
- Logic reduction and optimization to increase slack

• Dynamic power decreased to ~10%

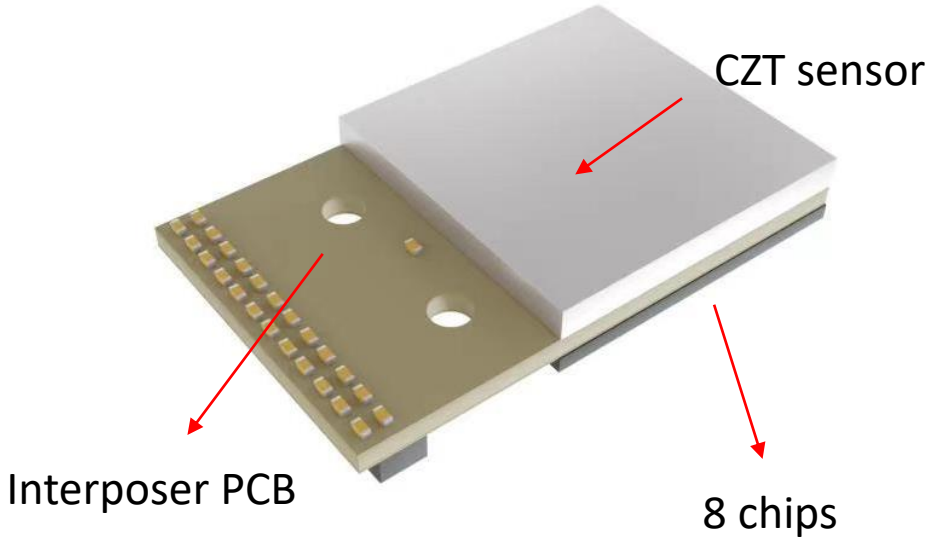


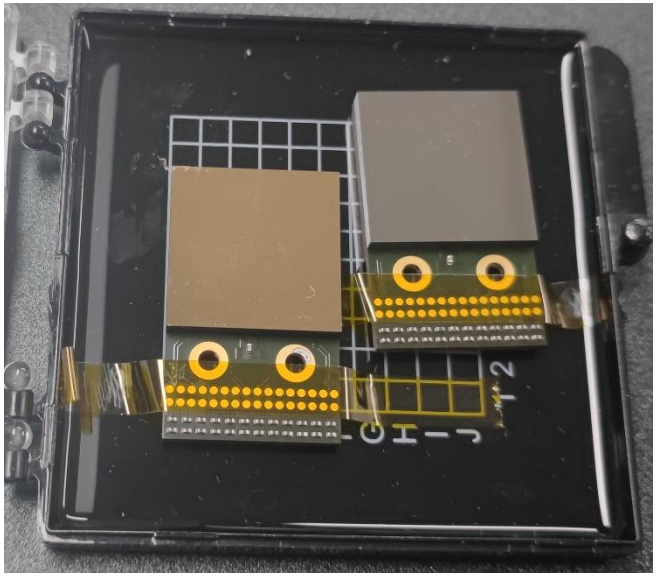
1.36 mW/channel->0.27 mW/channel

531 mW/cm^2->105 mW/cm^2

Readout Module

- PCB interposer as RDL:
  - Pixel size: 0.5 mm x 0.5 mm
  - Pixel array per module: 32 x 32 (1024 channels)
  - Chips per module: 8
  - Example: 3 side buttable CZT detector module





Summary

- R&D on macro-pixel TPC has been started (A new concept and try)
  - The first version ROIC(v1a) was tested last year
  - Primary functions were verified but some problem was still found
  - A new version (v1b) was submitted and received
  - RDL PCB substrate has been designed and module assembly tested
  - ROIC and module test for v1b are on progress

Thank You