ATLAS HIGH GRANULARITY TIMING DETECTOR ON-DETECTOR READOUT SYSTEM

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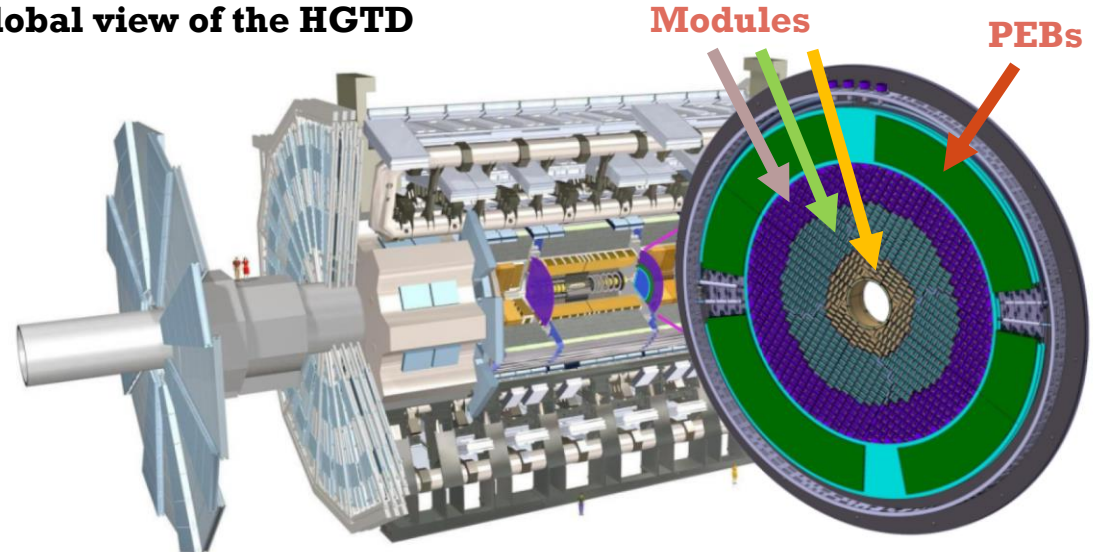
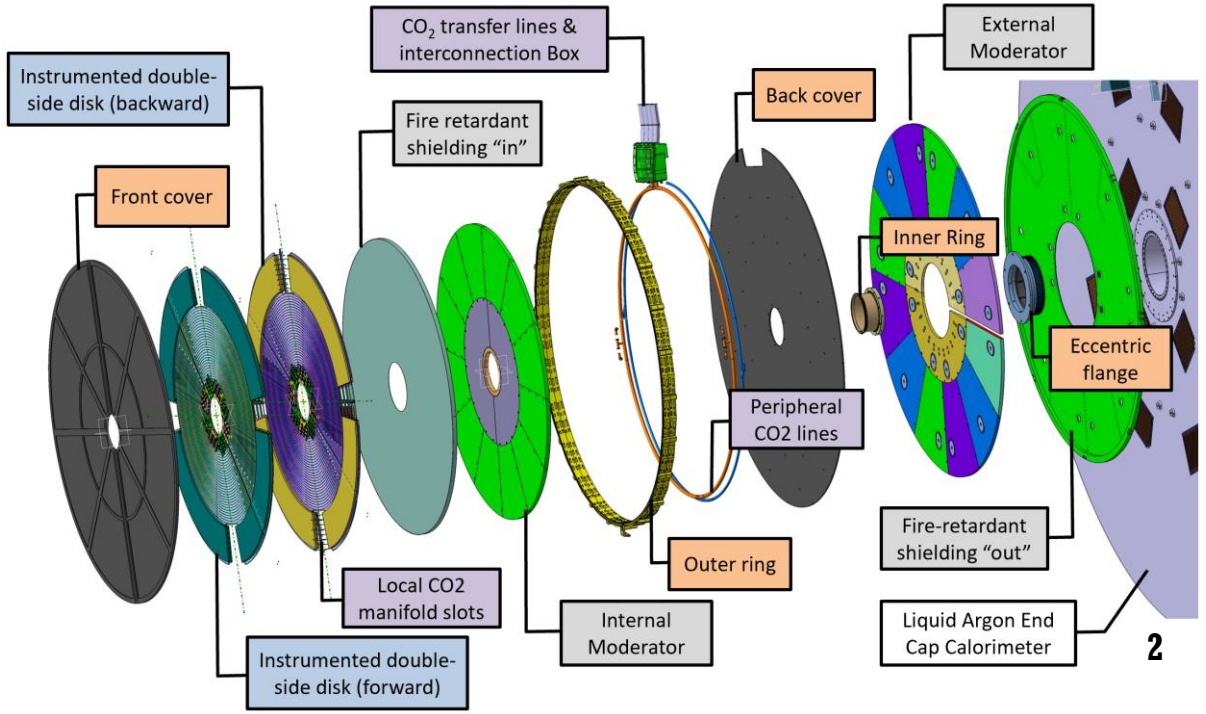
INTRODUCTION

- High Granularity Timing Detector (HGTD)
  - Silicon detector with coarse spatial resolution but precise timing
  - ~3.6 million 1.3×1.3 mm^2 pixels with Low-Gain Avalanche Detector (**LGAD**) technology
  - 6.1 m^2 active area
- Pileup rejection
  - Time resolution at the start (end):
    30 (50) ps per track / 35 (70) ps per hit
- Luminosity measurement
  - Count number of hits at 40 MHz (bunch-by-bunch)
  - Goal for HL-LHC: 1% luminosity uncertainty
- Detector structure
  - Two end-caps
    - $z \approx \pm 3.5$ m from the nominal interaction point
    - $110 < r < 1000$ mm
    - Active detector region: $2.4 < |\eta| < 4.0$
  - Each end-cap
    - Two instrumented disks, rotated by 15°

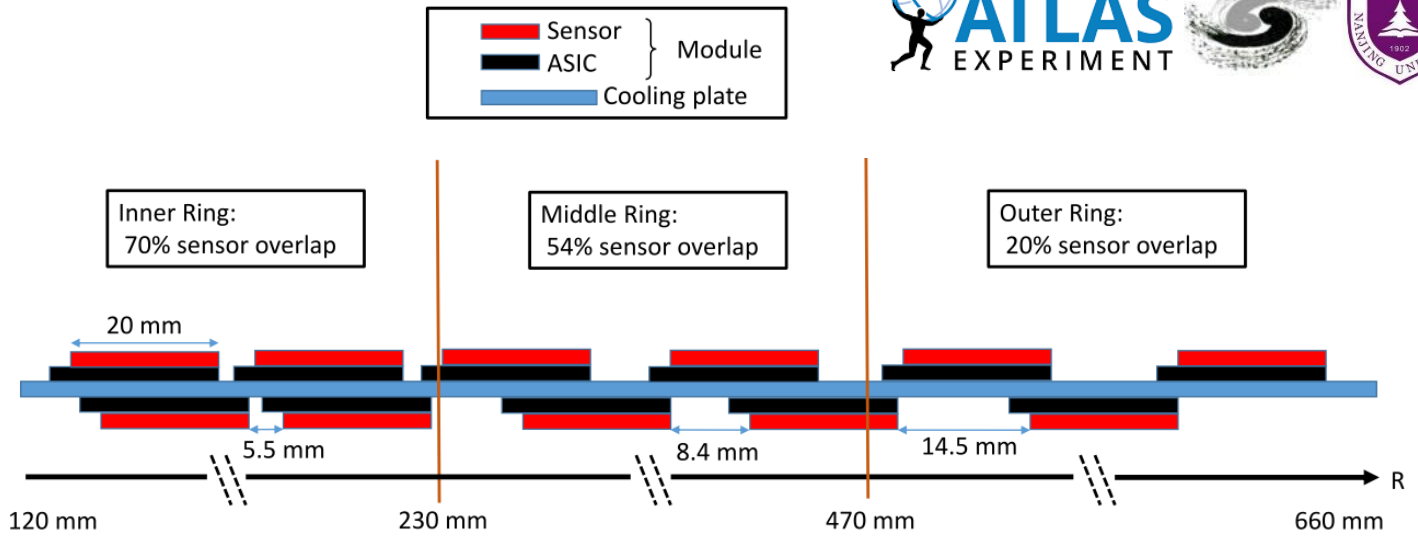
Global view of the HGTD



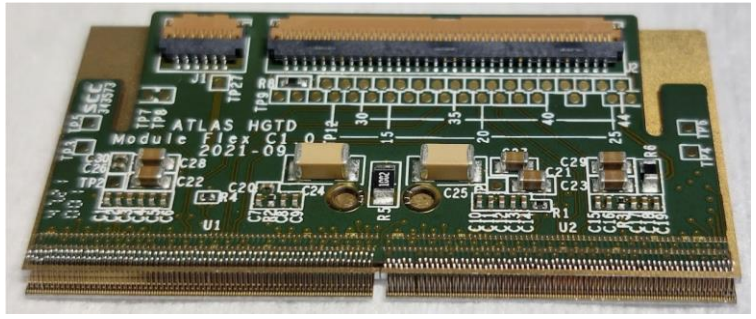


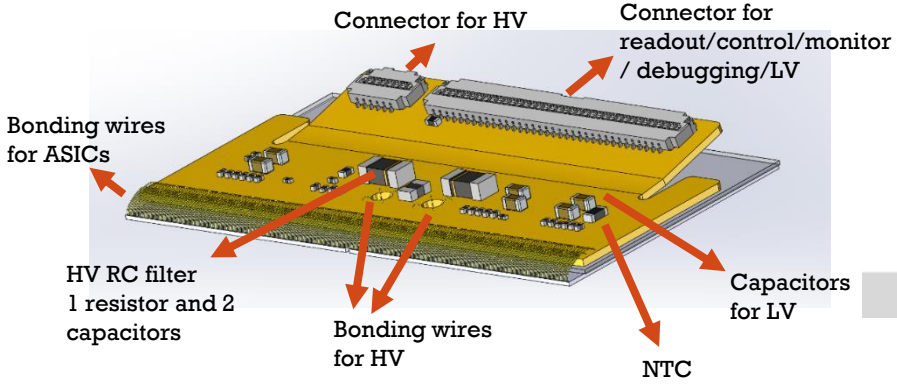
INTRODUCTION

- Each instrumented disk:
  - Double-sided layers mounted on a cooling plate
  - 3 ring layout for front-end modules
- Front-end module
  - Flex PCB
  - Two **LGAD** sensors
  - Two ASICs
    - ATLAS LGAD Timing Integrated Read-Out Chips (ALTIROC)
  - Radiation tolerance for modules
    - Up to 8.3×10^{15} 1MeV neq/cm^2, 7.5 MGy



The schematic drawing shows the overlap between the modules on the front and back of a cooling disk. There is a sensor overlap of 20% for r > 470 mm, 54% for 230 mm < r < 470 mm and 70 % for r < 230 mm.





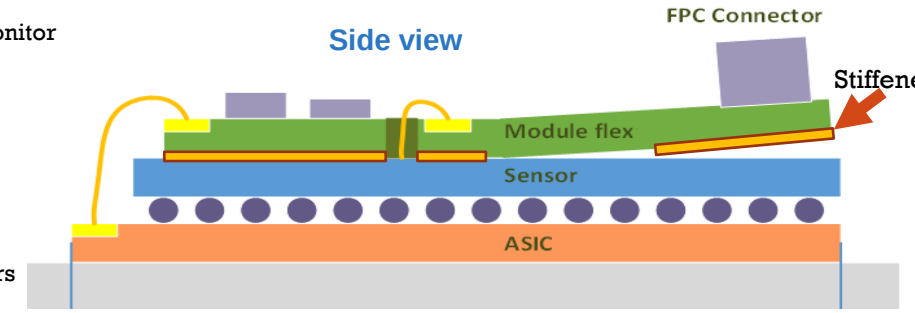
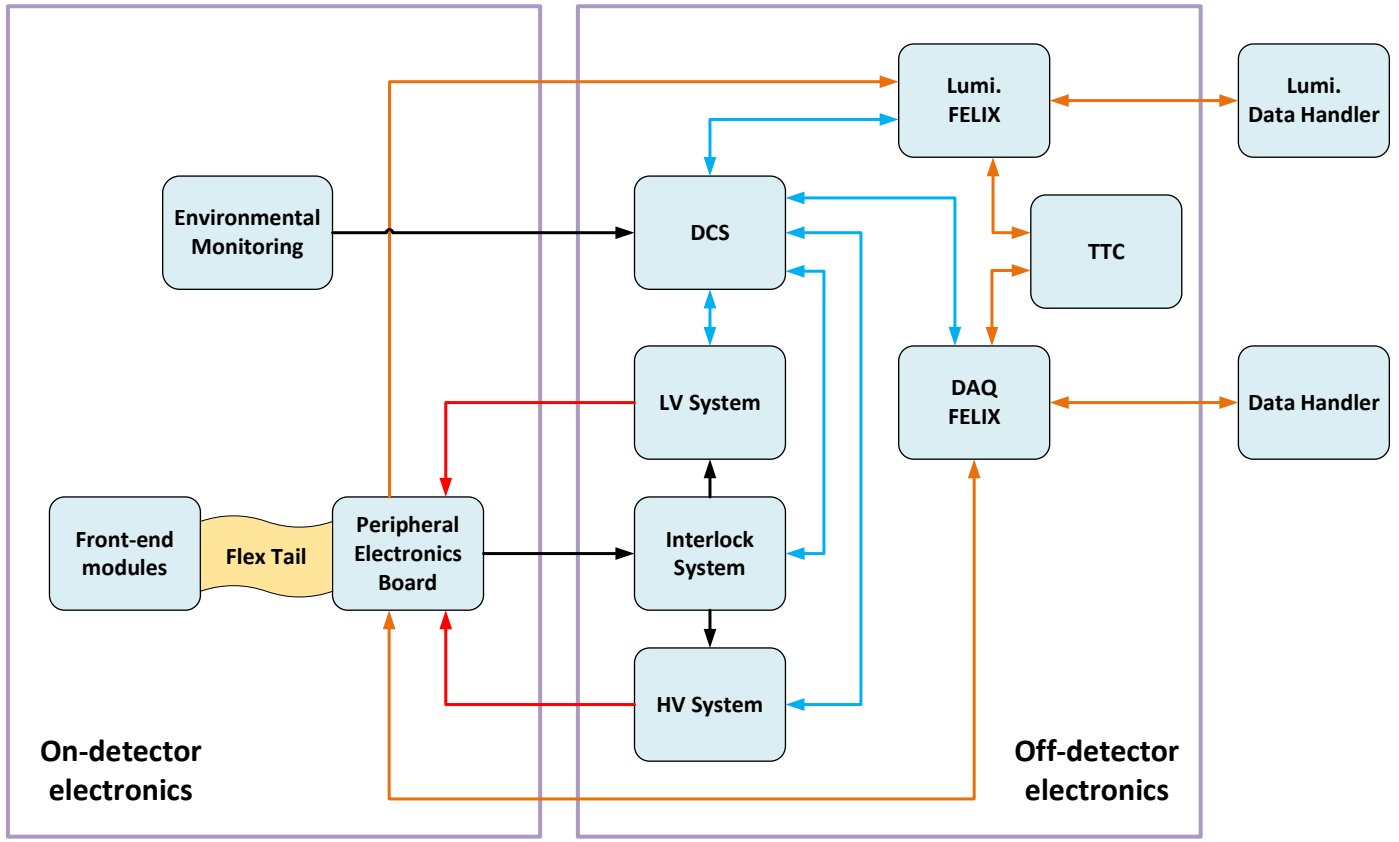


Fig 3. Front-end module

OVERVIEW OF HGTD READOUT ELECTRONICS

- On-detector
  - Front-end modules
  - Flex tail cables
  - Peripheral Electronics Boards (PEB)
- Off-detector
  - Data Acquisition System (DAQ)
  - Luminosity System
  - Timing, Trigger and Control (TTC)
  - Detector Control System (DCS)
  - Low Voltage (LV)/High Voltage (HV) system
  - Interlock system



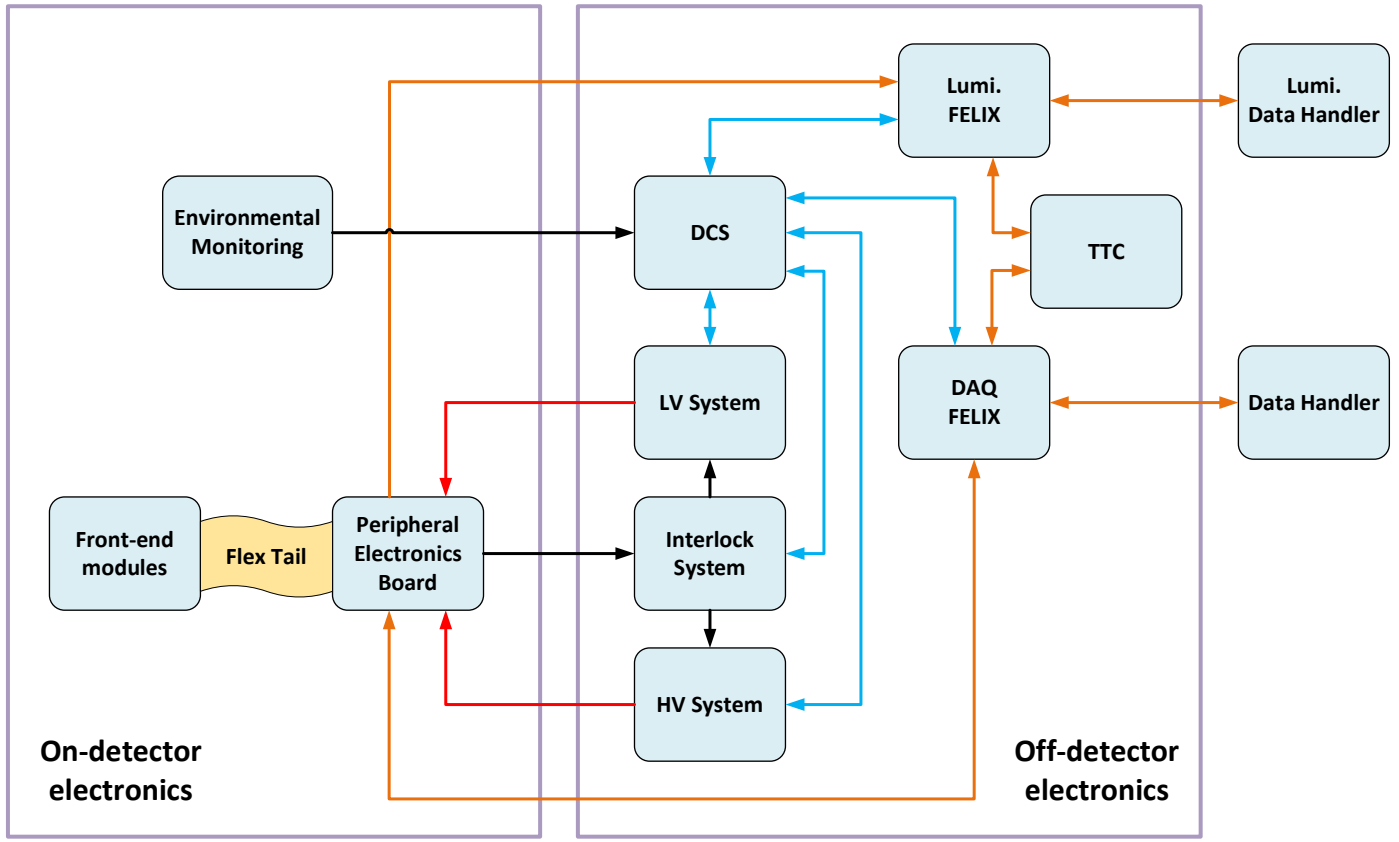
HGTD electronics architecture

Basic functions of PEB

- Control, monitoring & data aggregation and transmission
- Power-supply distribution: LV & HV
- Thermistor connection between the front-end modules and the interlock system

OVERVIEW OF HGTD READOUT ELECTRONICS

- On-detector
  - Front-end Modules
    - Flex PCB: Designed and produced by **IHEP (100%)**
  - Flex tail cables
    - Designed by Mainz
    - Produced by CERN/MAScIR, **Shandong University (33.6% of the cost)**, Mainz, JSI
  - Peripheral Electronics Boards (PEB)
    - Designed by IHEP, NJU (Nanjing University) and Morocco group
    - Produced by **IHEP (50%)** and **NJU (50%)**



HGTD electronics architecture

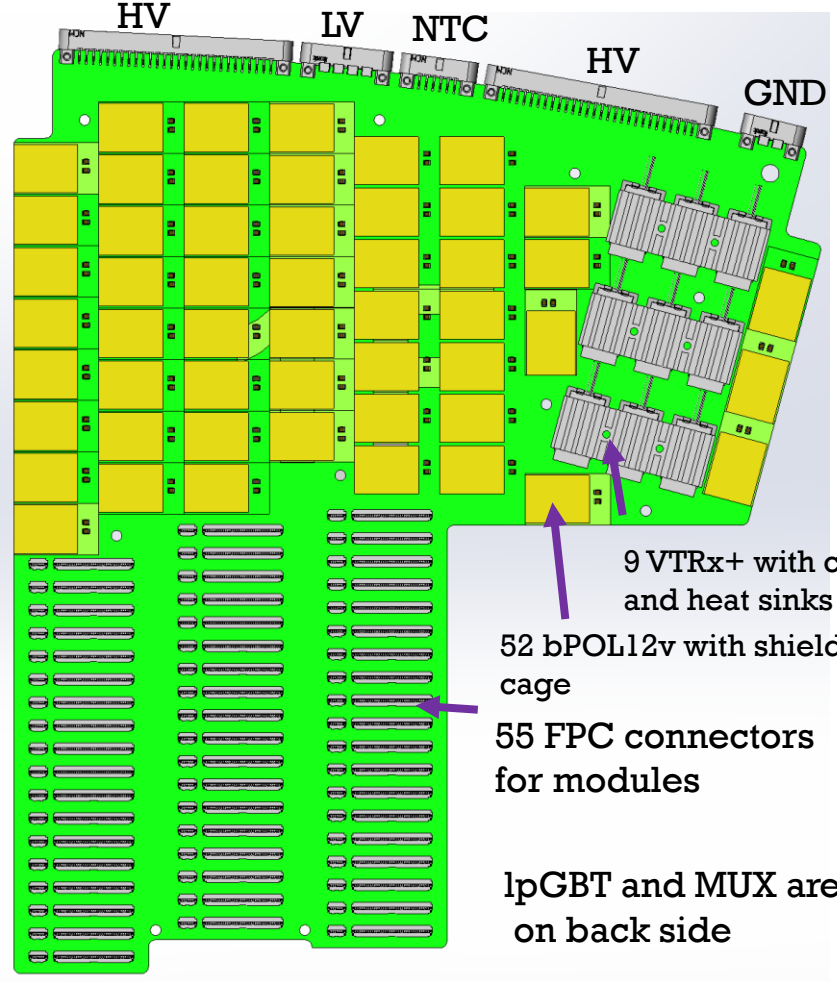
CHALLENGES TO ON-DETECTOR ELECTRONICS

Basic functions of PEB

- Control, monitoring & data aggregation and transmission
  - 8032 front-end modules
    - Clock and fast command distribution
    - Up to 50k analog monitoring
    - TOT/TOA data, up to 10 Tbps to TDAQ, on average, 63 Gbps per PEB
  - LV & HV power-supply distribution
    - Low noise, heat dissipation, system level shielding and grounding considerations
  - Thermistor connection between the front-end modules and the interlock system
    - 896 Negative Temperature Coefficient (NTC) sensors to monitor disk temperature
- Area and height restrictions
  - Limited surface area for connectors, chips and power blocks
  - Height < 10 mm, hard to find low-profile air-core inductors and connectors
- Radiation tolerance for PEB

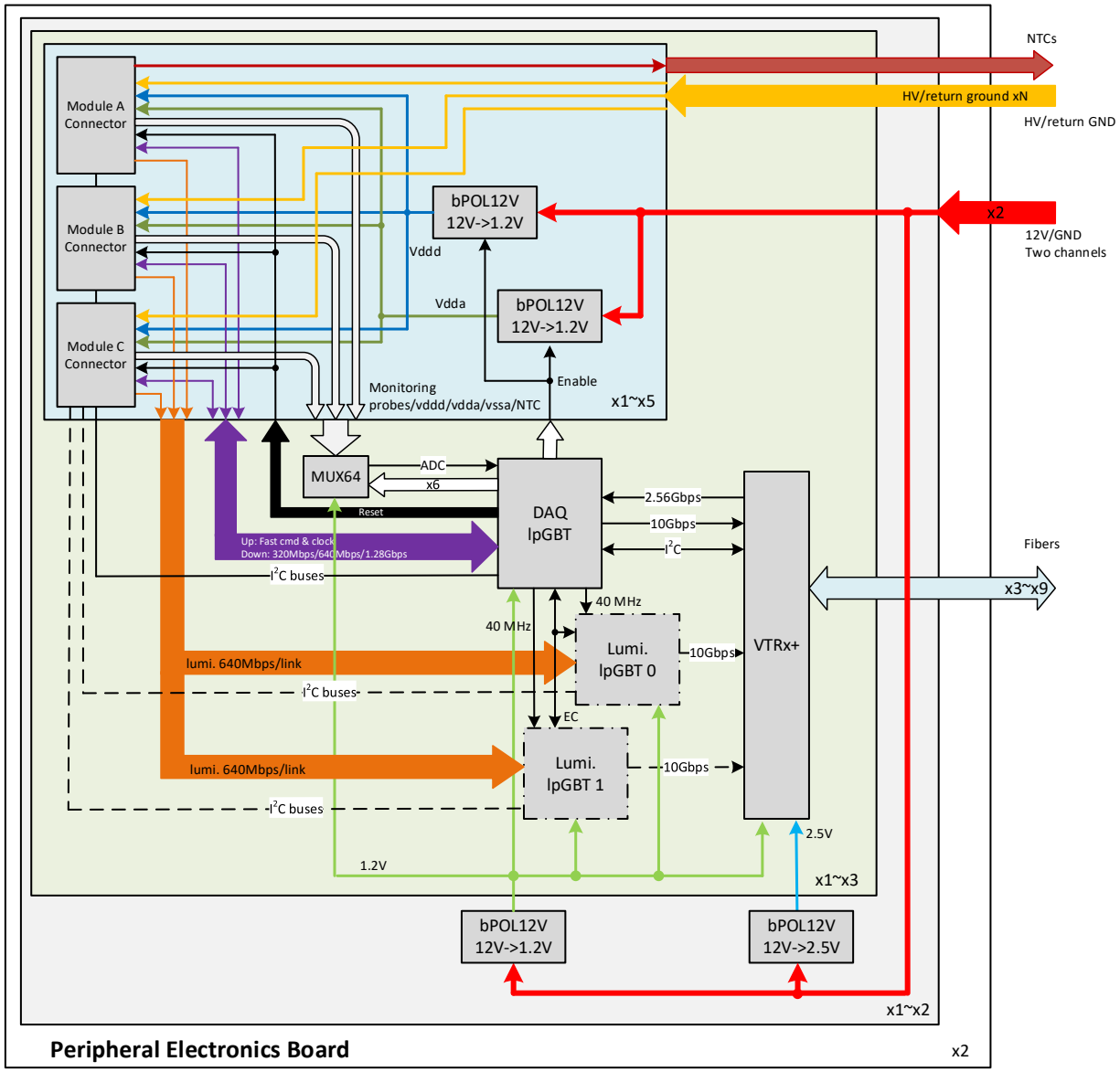
	From simulation	Safety factor	Design requirement
Si 1 MeV neutron equivalent	< 1.4 x 10^{15} neq /cm^2	1.5 x 1.3	2.73 x 10^{15} neq /cm^2
Fluence of hadrons > 20 MeV	< 0.32 x 10^{15} neq /cm^2	1.5 x 1.3 x 2	1.25 x 10^{15} neq /cm^2
TID	< 36 Mrad (0.36 MGy)	1.5	54 Mrad (0.54 MGy)

- Magnetic field
  - Amplitude: 0.382 T ~ 0.433 T
  - Angle 23.1˚ ~ 32.3˚
- Operating Temperature:
  - On disk (with front-end modules and CO2 cooling): -35 ℃ ± 5 ℃
  - Testing/debugging (with cooling): -40 ℃ to 55 ℃



Top view of PEB 1F

CONCEPTUAL DESIGN OF PEB



- Two LV channels
  - Each up to 12A @ 12V
- Up to 3 modules share two bPOL12v
  - One for analog power, the other for digital power
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Control
  - I2C of lpGBT
    - Module and VTRx+ configuration
    - I2C0 of TDAQ lpGBT is connected to the VTRx+ only
  - Output
    - Module reset
    - Module power on/off
    - MUX64 channel selection
- Monitoring
  - ADC of lpGBT
  - Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - On board NTC
  - Input of lpGBT
    - bPOL12v power good signal

bPOL12V:
provide the 1.2V analog and digital voltages for the ALTIROCs

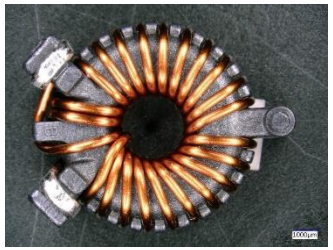
lpGBT:
Bi-directional slow control and monitoring communication between the FELIX and the lpGBT is done via the IC and EC channels.

Each lpGBT has a 8 channel multiplexed ADC.
With ~7 modules/lpGBT, an external 64-to-1 MUX is required: **MUX64**

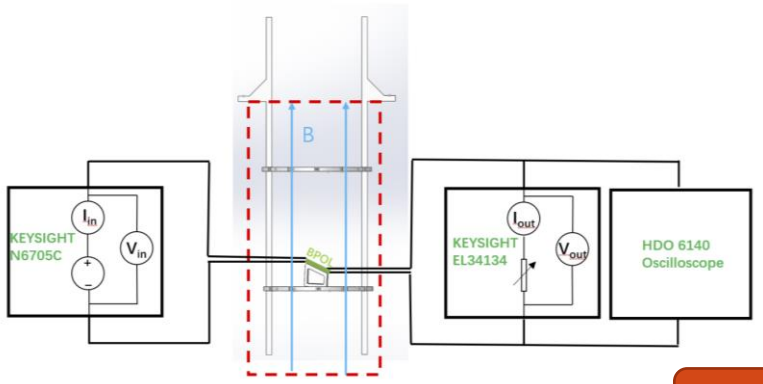
DC/DC CONVERTER

Bpol12V generates analog and digital 1.2 V to the front-end modules

- Height limitation in HGTD
  - < 10 mm (Including PCB and shielding case)
  - Selection for air-core inductor
    - Custom solenoid coil



- Tested in low temperature (-35 ℃), OK
- Tested in magnetic field, up to 4 T, OK

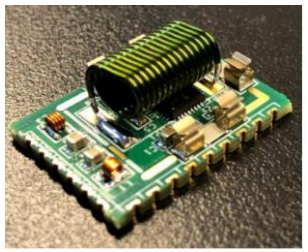


BPOL12V test system in magnetic field

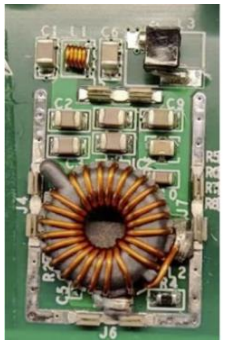
Aachen module

CERN module (FEASTMP)

ITK EoS

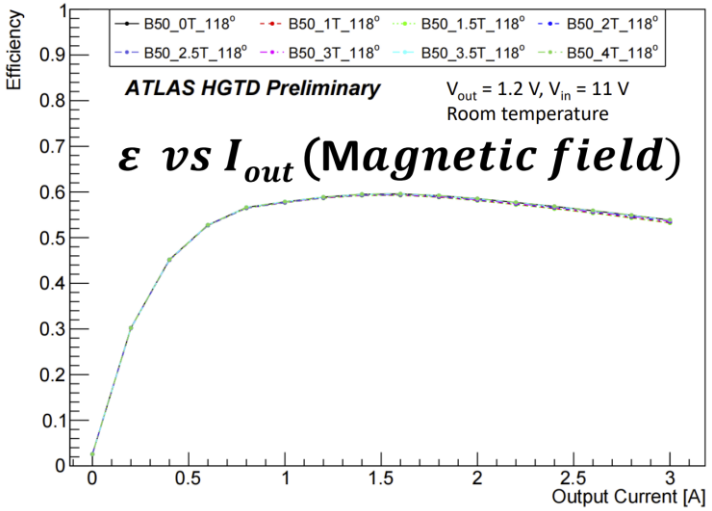


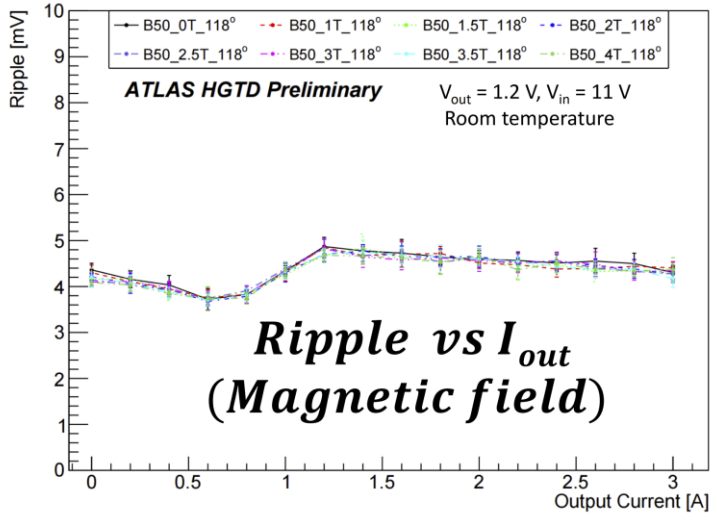
Commercial inductor



HGTD

Inductor candidates

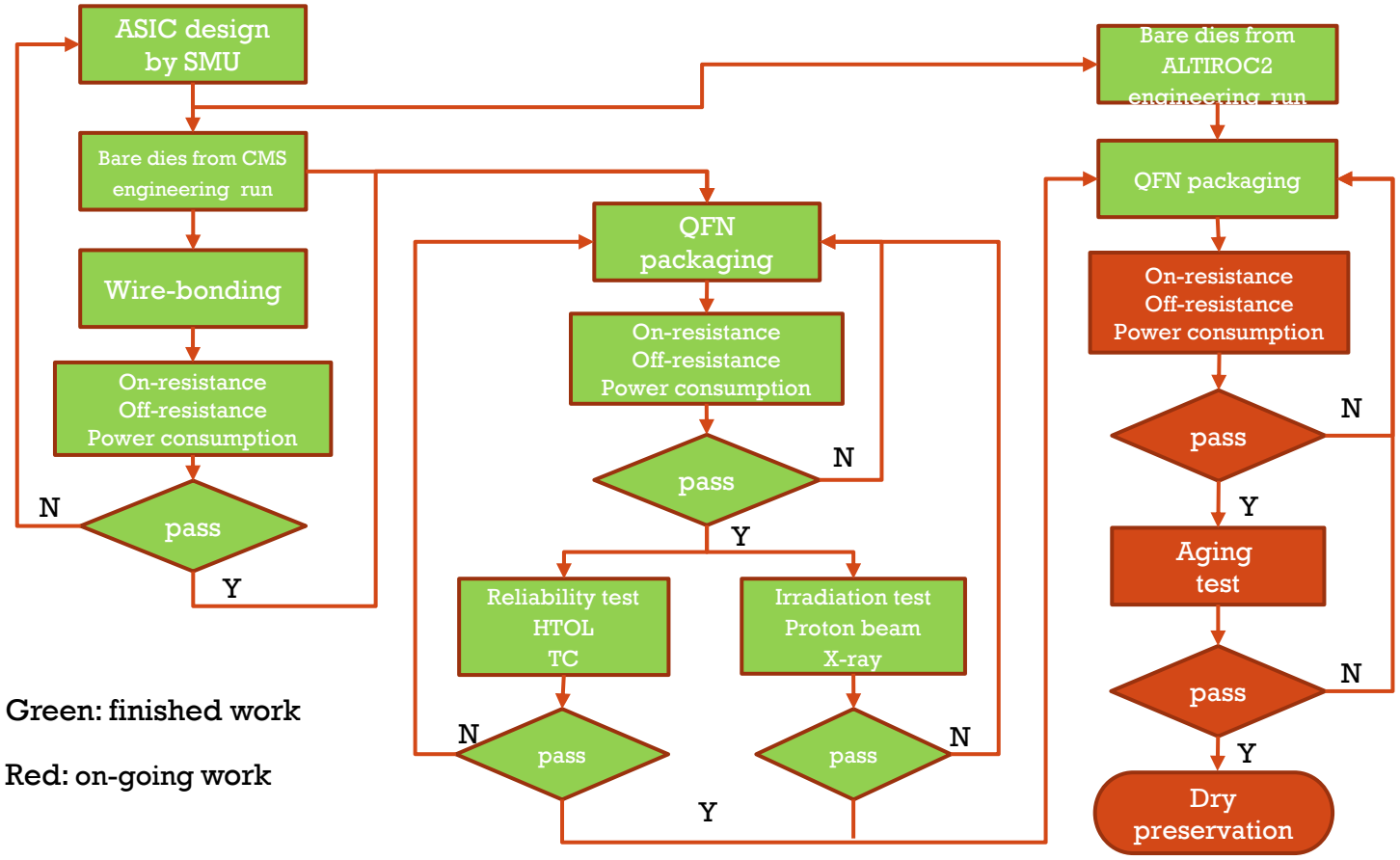




Efficiency and ripple with respect to *Iout* in magnetic field

Thanks to IHEP Accelerator Division for the superconducting magnet

MUX64 PRODUCTION



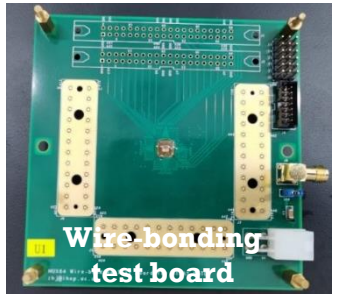
- Green: finished work
- Red: on-going work

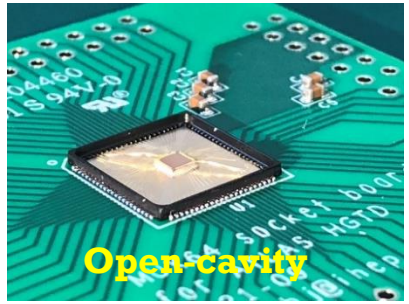
- Reliability test
  - High Temperature Operating Life (HTOL)
    - 32 samples, 85 ˚C, 16days, All pass HTOL
  - Temperature Cycle (TC)
    - 48 samples
    - -40 ˚C to 85 ˚C
    - 4 batches launched, more than 100 cycles per batch, pass TC
- Irradiation test
  - Proton beam
    - Beam energy: 80 MeV.
    - Spot size: 20 x 20 mm^2
    - Measured injection rate: 1.89 × 10^9 pps/cm^2
    - 2 samples, irradiation time: 9.4 days, all pass test
  - X-ray
    - Instrument model: MultiRad160
    - TID dose rate: up to 5 Gray/s
    - 5 samples, pass TID test

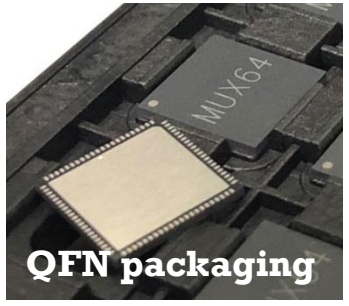
Thanks to CSNS Associated Proton Experimental Platform (APEP) for beam

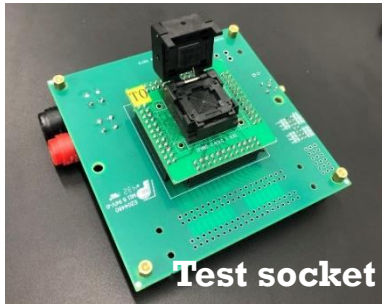
	Requirement	Tested
Si 1MeV n_{eq} fluence	2.5 x 10^{15} n_{eq}/cm^2	3.21 × 10^{15} n_{eq}/cm^2
TID	0.54 M Gy	0.75 M Gy

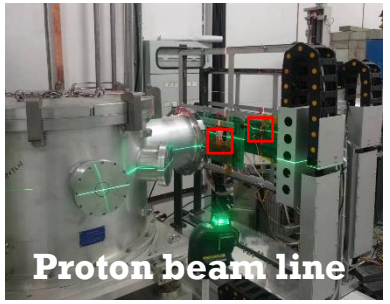
- About 2000 pcs under production



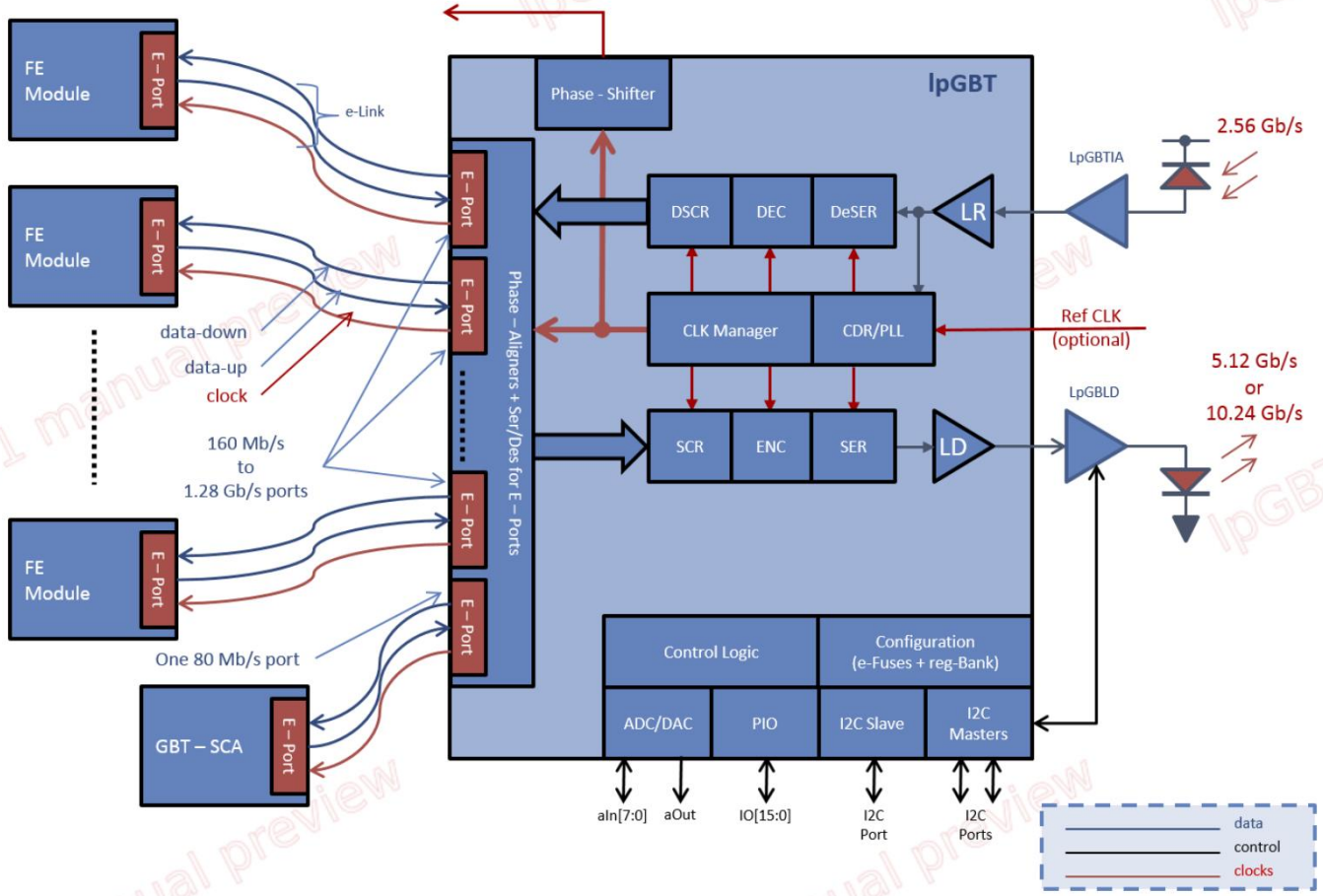








LPGBT FEATURE



lpGBT architecture

- TDAQ interface
  - PEB uses 10.24 Gbps with FEC5
- Front-end interface
  - Up to 28 eclks
  - Up to 28 elinks for data-up

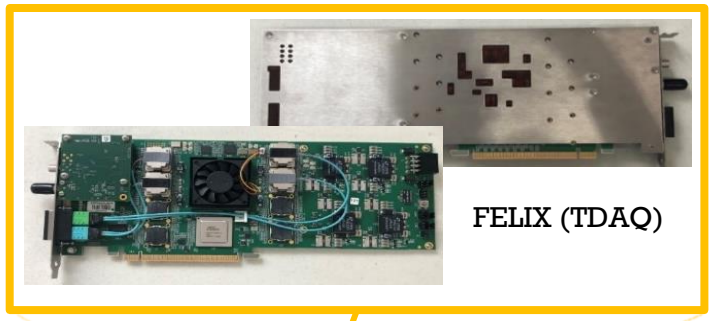
Data-up	320Mbps	640Mbps	1.28Gbps
EDINy0	√	√	√
EDINy1	√	×	×
EDINy2	√	√	×
EDINy3	√	×	×

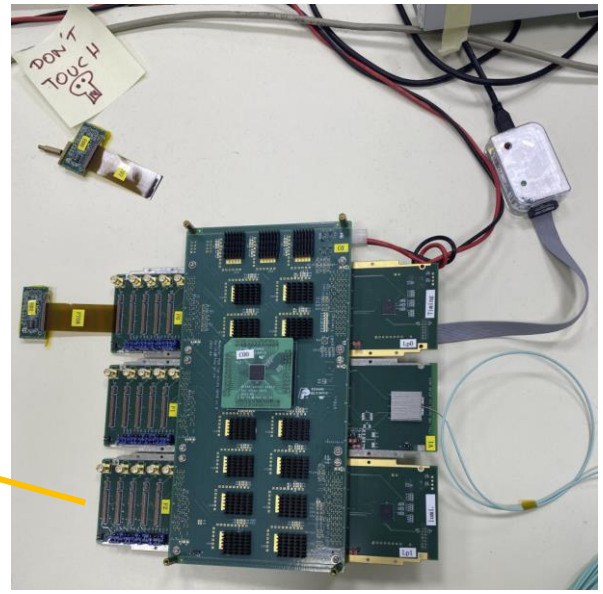
Note: y=0,…,6

  - Up to 16 elinks for data-down
    - 4 groups
      - 4 channels in the one group have the same data (“mirror” function) at 320 Mbps
  - Up to 3 I2C buses
  - Up to 16 GPIOs

DEMONSTRATION SYSTEM

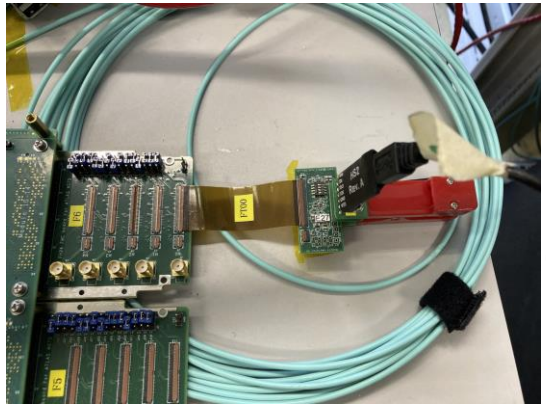
- Complete the prototype demonstration system
- The full chain readout from the front-end modules to back-end TDAQ system
- Delivered to CERN, Nikhef and KTH



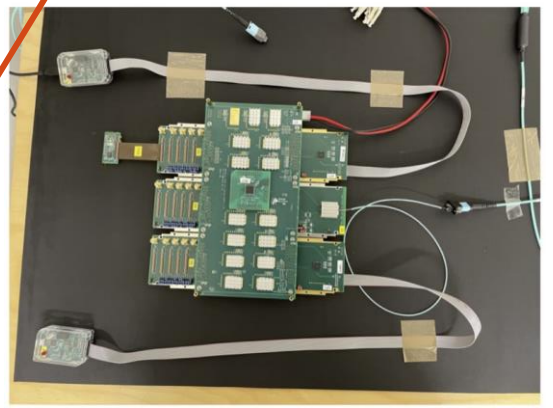


@CERN

FELIX Server



@ Nikhef



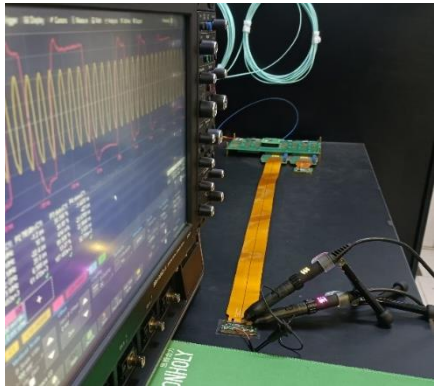
@KTH

COMMUNICATION TEST

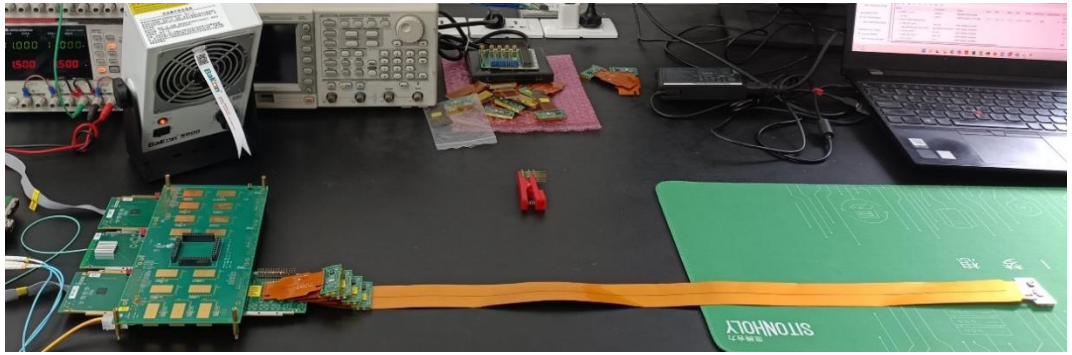
- Elink Skew and Jitter
  - 40 MHz for ALTIROC2, 320 MHz for ALTIROC3
  - Jitter < 9 ps

FELIX and modular PEB	Jitter (ps)			Duty			Skew between clk and fast-cmd (ns)		
ECLK	40MHz	320MHz	640MHz	40MHz	320MHz	640MHz	40MHz	320MHz	640MHz
Test points on PEB (without flex tail)	5.256	6.473	6.291	50.20%	50.95%	51.32%	1.353	1.446	0.020
Test points on bare module flex with 70 cm flex tail (without ALTIROC)	7.314	7.586	7.254	50.19%	50.90%	51.28%	1.498	1.489	0.099
Test points on digital module with 70 cm flex tail (with ALTIROC)	8.052	7.863	7.747	50.19%	50.88%	50.87%	1.550	1.548	0.119

- Elink Bit Error Rate Test (BERT)
  - Down link @ 320 Mbps, BERT < 10^{-12}
  - Up link @ 1.28 Gbps, BERT < 5 x 10^{-13}



Elink skew and jitter tests



Elink BER test with long flex tail and module

- Optical link
  - Pre-emphasis parameters in lpGBT and VTRX+

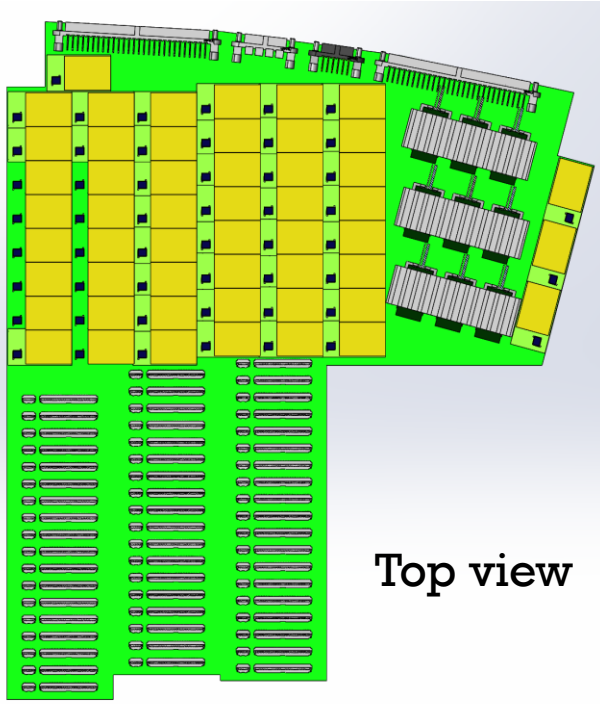
VTRX+		lpGBT	
Parameters	**Range**	**Parameters**	**Range**
Bias Current	0~127	LDModulationCurrent	0~127
Modulation enable	0,1	LDEmphasisEnable	0,1
Modulation Current	0~127	LDEmphasisAmp	0~127
Pre-emphasis amplitude	0~7	LDEmphasisShort	0,1
Rising edge pre-emphasis enable	0,1		
Falling edge pre-emphasis enable	0,1		

  - Developed automatic scripts to get the best config

Optical Eye Diagram tests @ 10.24 Gbps

PEB 1F DESIGN

Peripheral board	Modules	lpGBT	bPOL12v	MUX	VTRx+
1F	55	9+3	52	9	9



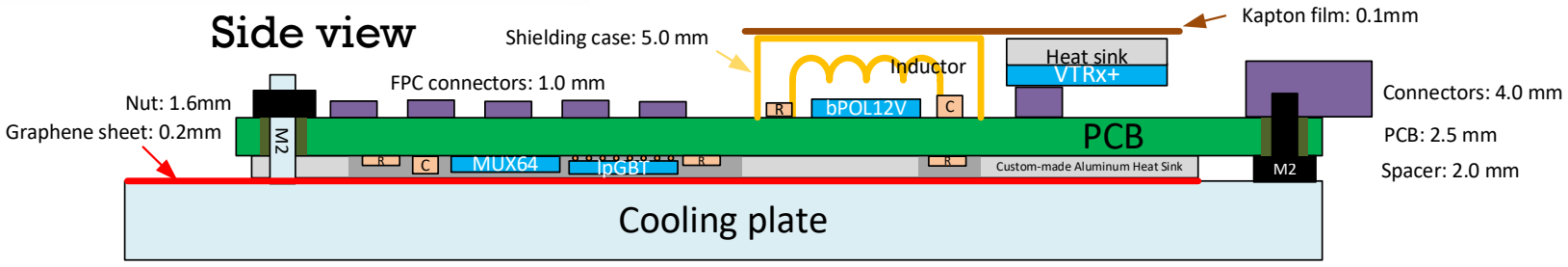
Top view

Key dimensions

- Total thickness: 2.5 mm
- 55 FPC connectors
  - Center to center distance: **6.5 mm**
- 52 bPOL12v power blocks
  - Size: **24 mm x 14.5 mm**
  - Height above PCB: 5 mm
  - Height under PCB: 2 mm

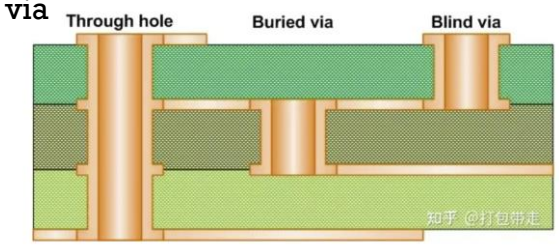
PEB 1F prototype is under production

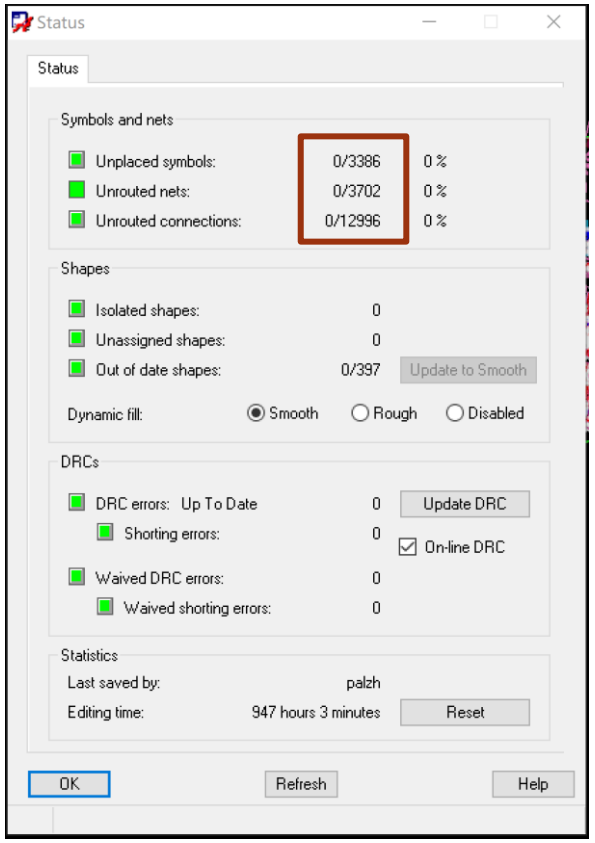
Side view



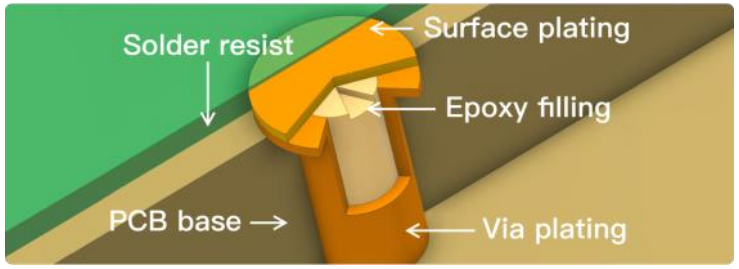
Complex PCB

- High speed, low loss multi-layer material
  - Impedance control
- Halogen free
  - EM-890 or IT-170/988 or R-5375(E)
- Symbols and nets
  - 3140 components, 10953 connections
- 22 layers PCB for PEB 1F, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power
- HDI (High Density Interconnector)
  - Micro via





- VIPPO / POFV: Via-in-Pad Plated Over PCB

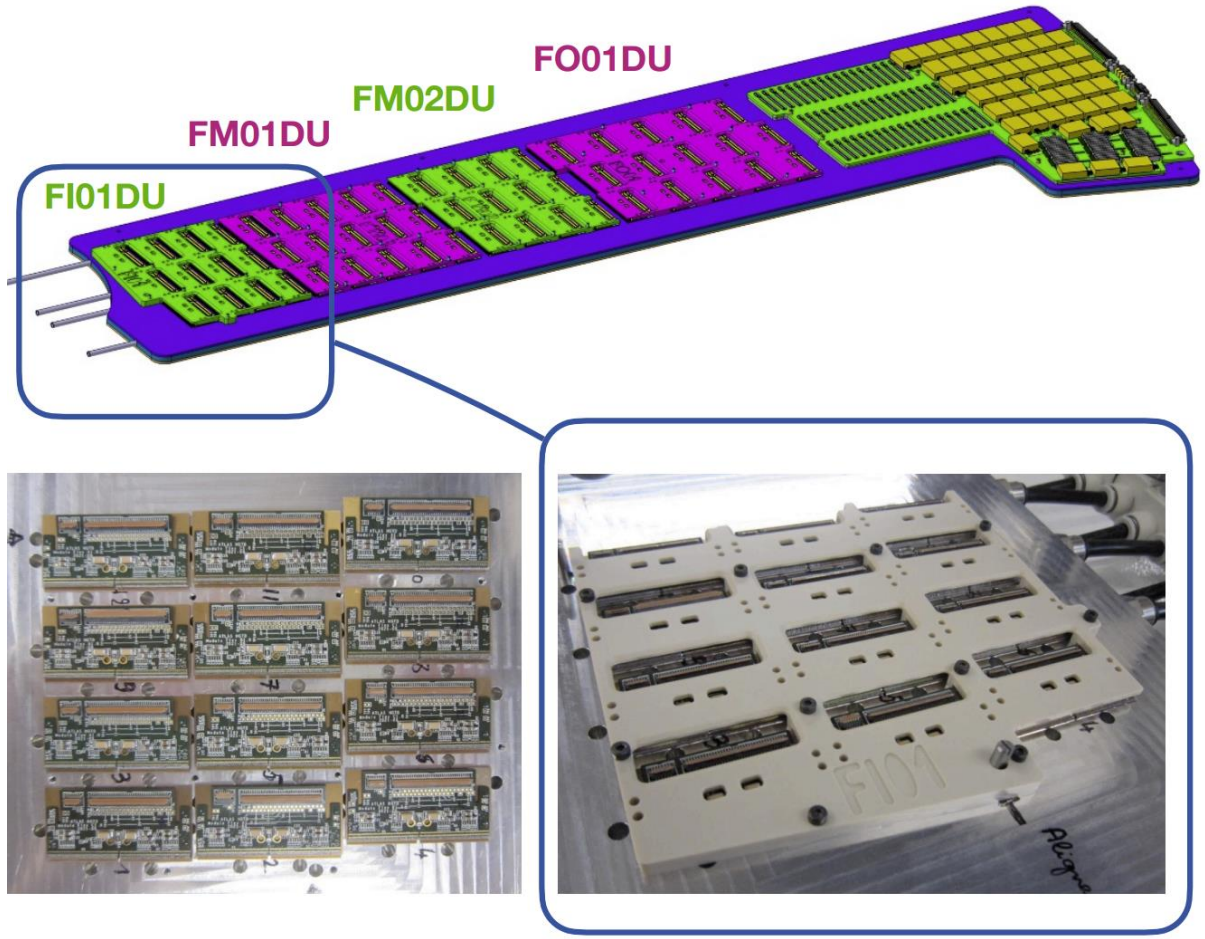


CONCLUSION AND OUTLOOK

- PEB 1F prototype under production
- HGTD on-detector electronics moving towards the FDR phase

- Focus on the full demonstrator
  - Electronics : 54 modules mounted on 4 support units + flex tails + PEB 1F + LV + HV
  - Cooling plate prototype
  - Detector assembly
  - TDAQ + Lumi. DAQ + DCS

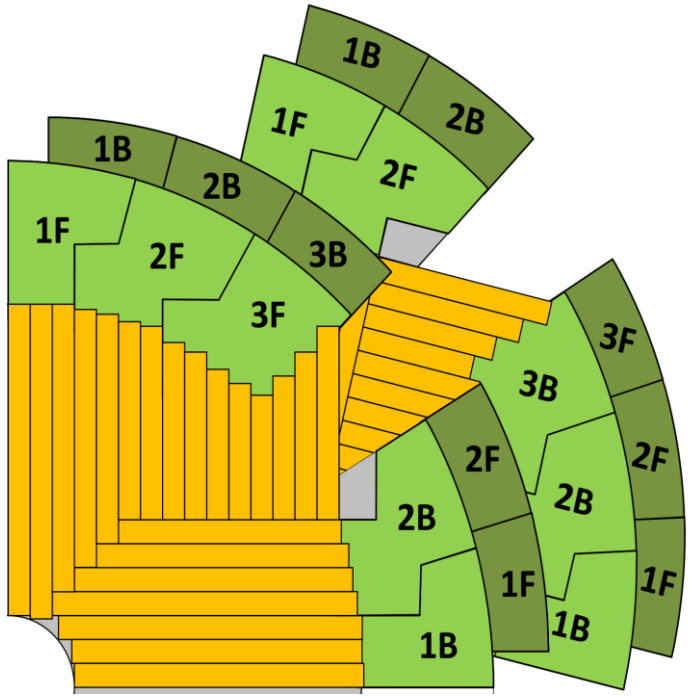
Many challenges ahead, but remarkable technical progress achieved



FI01DU loaded at LPNHE Paris and send to CERN

THANKS TO YOUR ATTENTION

PERIPHERAL ELECTRONICS BOARDS (PEB)



One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- Six types of PEB to be designed (front and back side)
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules
- The front-end modules are connected via flex tails, arranged in rows, to the PEB @ 660 < r < 920 mm

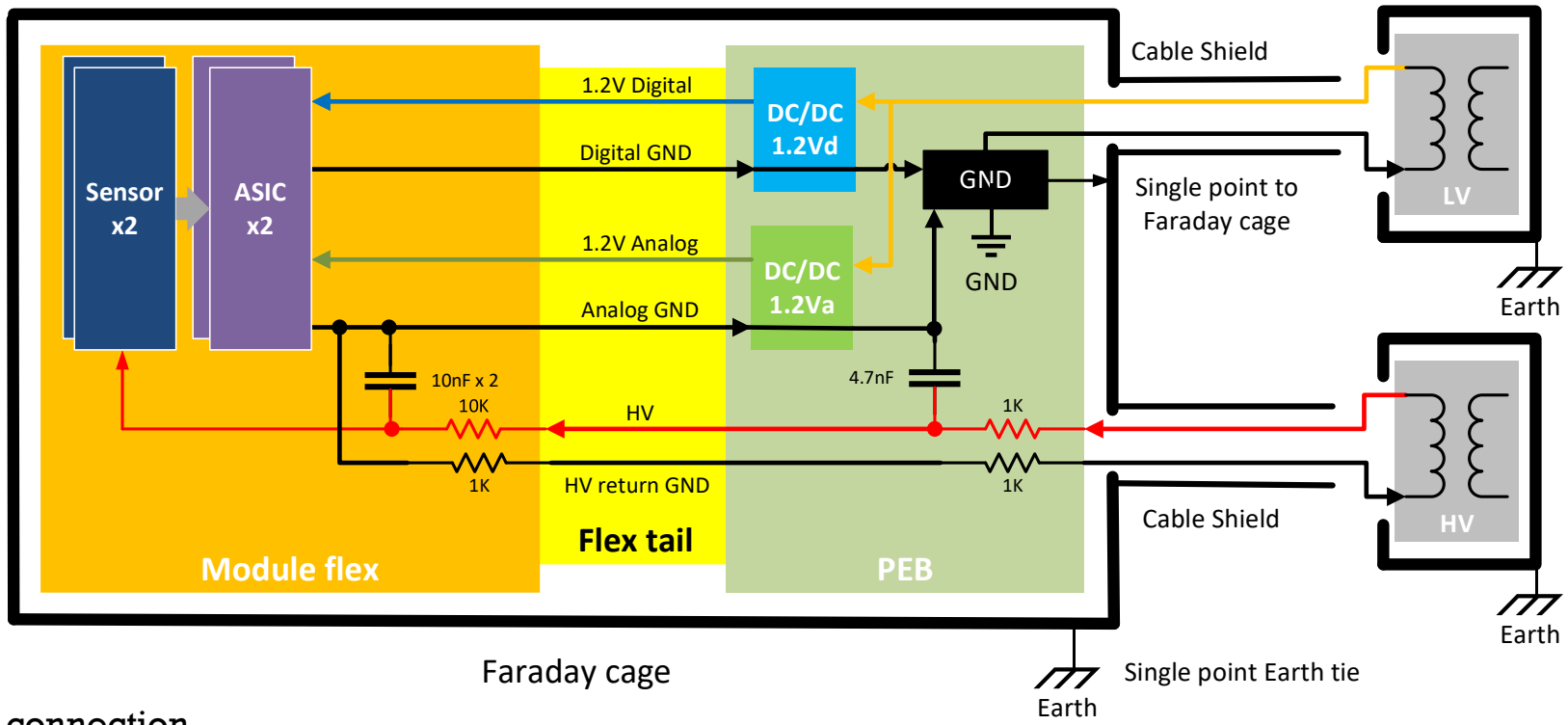
PEB	Front side	Back side
1F	54 modules	55 modules
2F	52 modules	56 modules
3F	39 modules	-
3B	-	39 modules
2B	52 modules	48 modules
1B	54 modules	53 modules

Number of modules attached to the different PEBs at the front and back sides

- 80 boards per HGTD vessel, thus 160 boards in total.

PEB	1F	2F	3F	3B	2B	1B
Total Qty.	32	32	16	16	32	32

GROUNDING & SHIELDING



- Single point connection
  - The hermetic vessel acts as the Faraday cage, which is referenced to the experiment ground by a single dedicated copper braid per end cap.
- Each PEB will have be referenced to the Faraday cage by one single low ohmic strap to the conductive layer of the outer ring.
  - The modules and the PEB shall have thermal conductive connection to the cooling plate but be electrically isolated from the cooling plate.
- The stage2 LV supplies are referenced to ground by their return lines being connected to the ground planes of the PEB which they supply.
- The HV at each module is then referenced to ground through the analog ground plane at the module end.

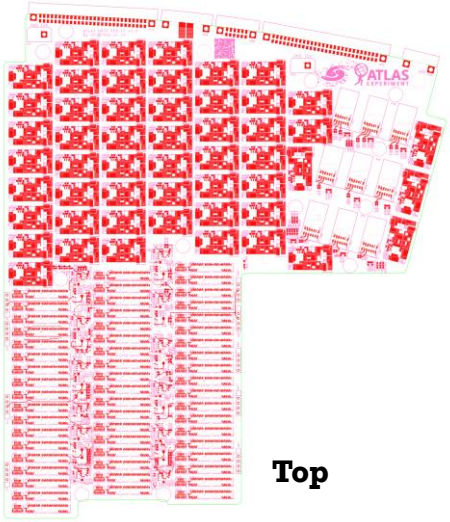
LPGBT ELINK ASSIGNMENT IN HGTD

Model ID	lpGBT Elinks	Mix230	Mix150	Mix310	Mix046(with lumi)	Mix00D(with 2 lumi)
M0	ECLK0, EDIN00, EDIN10, EDOUT00	1280, P0, I2C1	1280, P0, I2C1	1280, P0, I2C1	640, P0, I2C1	320, P0, I2C1
M1	ECLK1, EDIN01, EDIN11, EDOUT01	-	-	-	-	320, P0, I2C1, L640
M2	ECLK2, EDIN02, EDIN12, EDOUT02	-	-	-	640, P0, I2C1	320, P1, I2C2, L640
M3	ECLK3, EDIN03, EDIN13, EDOUT03	-	-	-	-	320, P1, I2C2, L640
M4	ECLK4, EDIN20, EDIN30, EDOUT10	1280, P0, I2C1	640, P0, I2C1	1280, P0, I2C1	640, P1, I2C2	320, P2, L_I2C0, L640
M5	ECLK5, EDIN21, EDIN31, EDOUT11	-	-	-	-	320, P2, L_I2C0, L640
M6	ECLK6, EDIN22, EDIN32, EDOUT12	-	640, P0, I2C1	-	640, P1, I2C2, L640	320, P2, L_I2C0, L640
M7	ECLK7, EDIN23, EDIN33, EDOUT13	-	-	-	-	320, P3, L_I2C1, L640
M8	ECLK8, EDIN40, EDIN50, EDOUT20	640, P1, I2C2	640, P1, I2C2	1280, P0, I2C1	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M9	ECLK9, EDIN41, EDIN51, EDOUT21	-	-	-	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M10	ECLK10, EDIN42, EDIN52, EDOUT22	640, P1, I2C2	640, P1, I2C2	-	320, P2, L_I2C1, L640	320, P4, L_I2C2, L640
M11	ECLK11, EDIN43, EDIN53, EDOUT23	-	-	-	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M12	ECLK12, EDIN60, EDIN62, EDOUT30	640, P1, I2C2	640, P1, I2C2	640, P1, I2C2	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M13	ECLK13, EDIN61, EDIN63, EDOUT31	-	-	-	320, P3 L_I2C2, L640	-

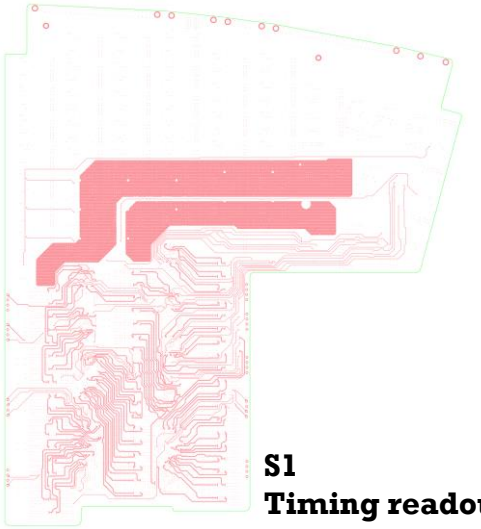
Basic patterns used in PEB, Mix XYZ

- X: number of module run 1.28 Gbps,
- Y: number of module run 640 Mbps,
- Z: number of module run 320 Mbps

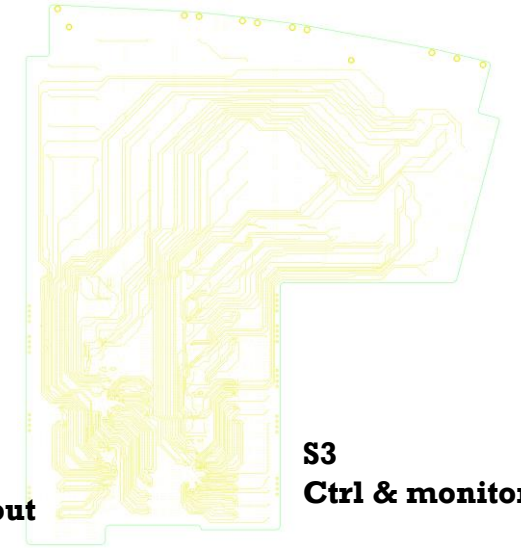
PEB 1F ROUTING



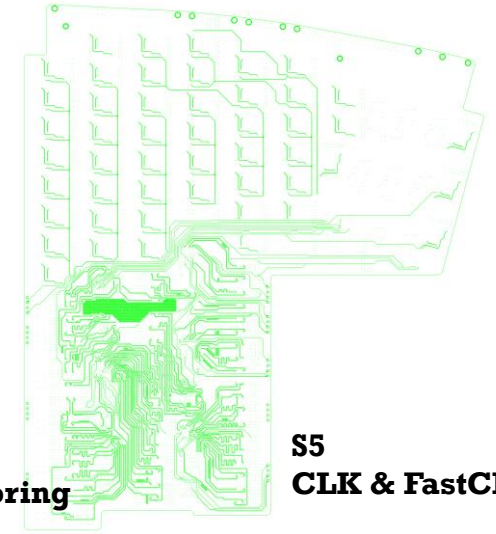
Top



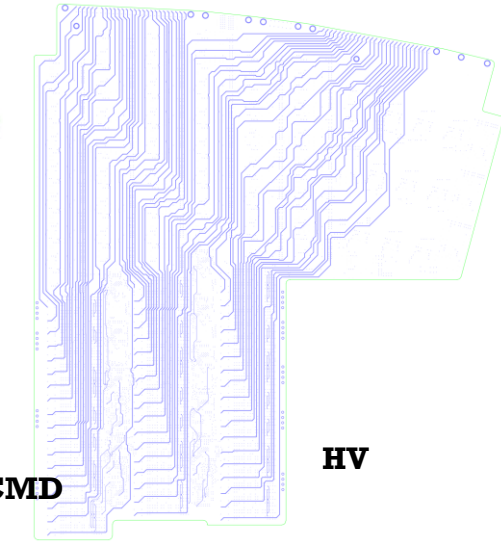
S1
Timing readout



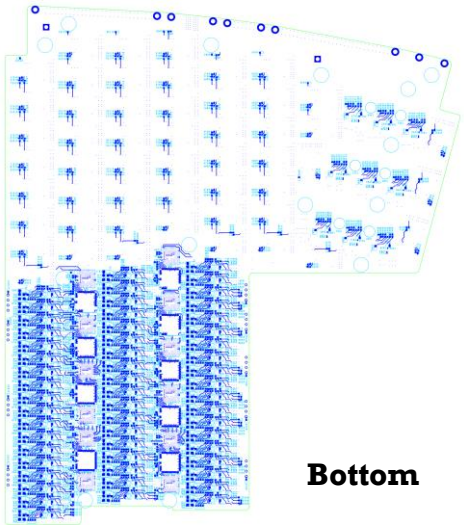
S3
Ctrl & monitoring



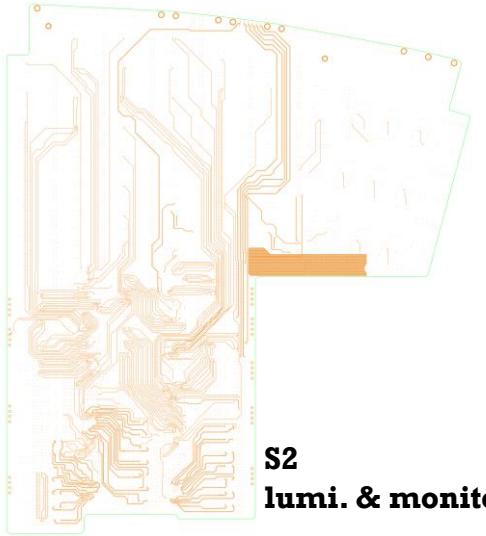
S5
CLK & FastCMD



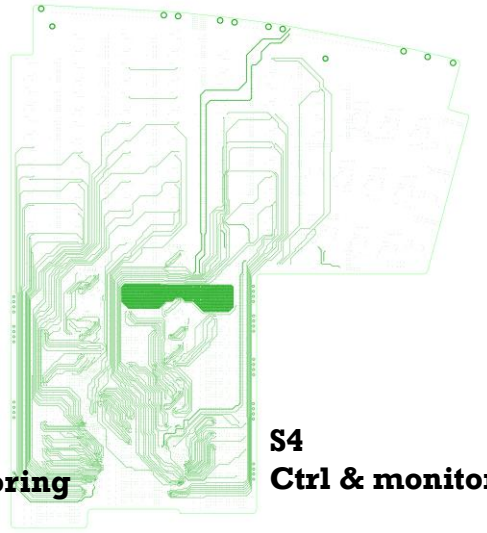
HV



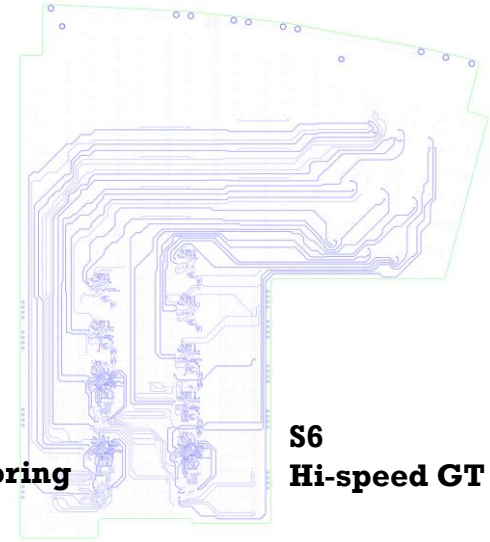
Bottom



S2
lumi. & monitoring



S4
Ctrl & monitoring

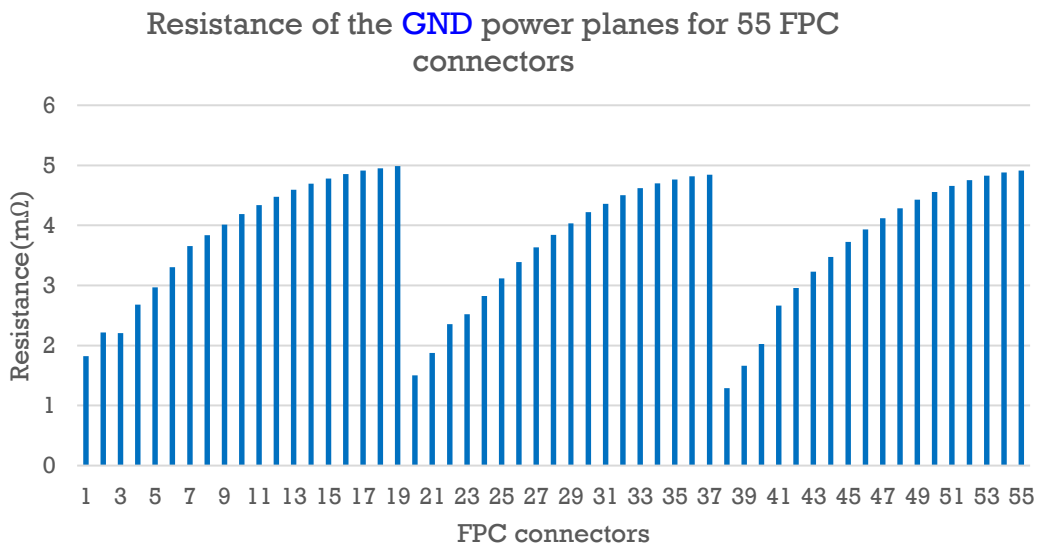


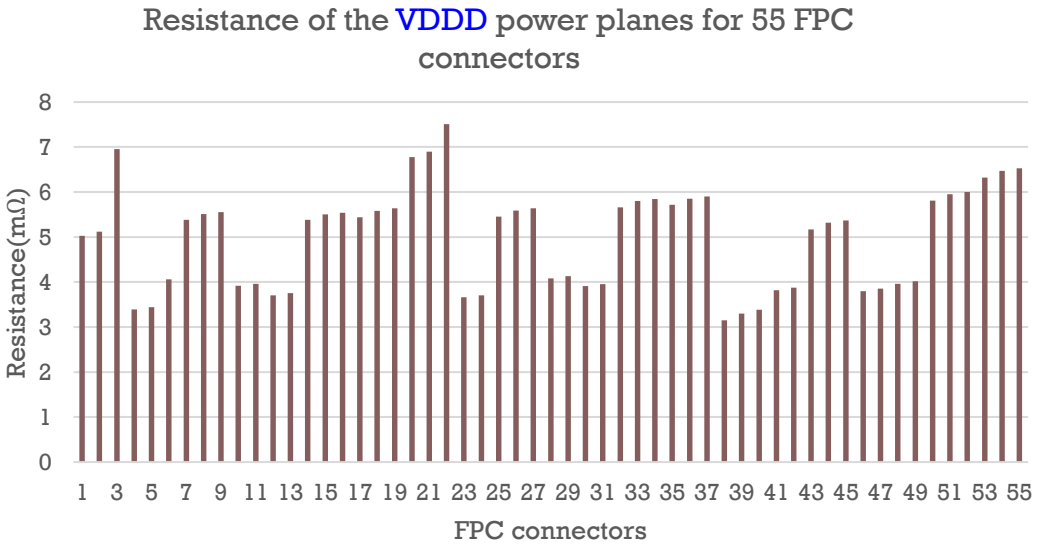
S6
Hi-speed GT

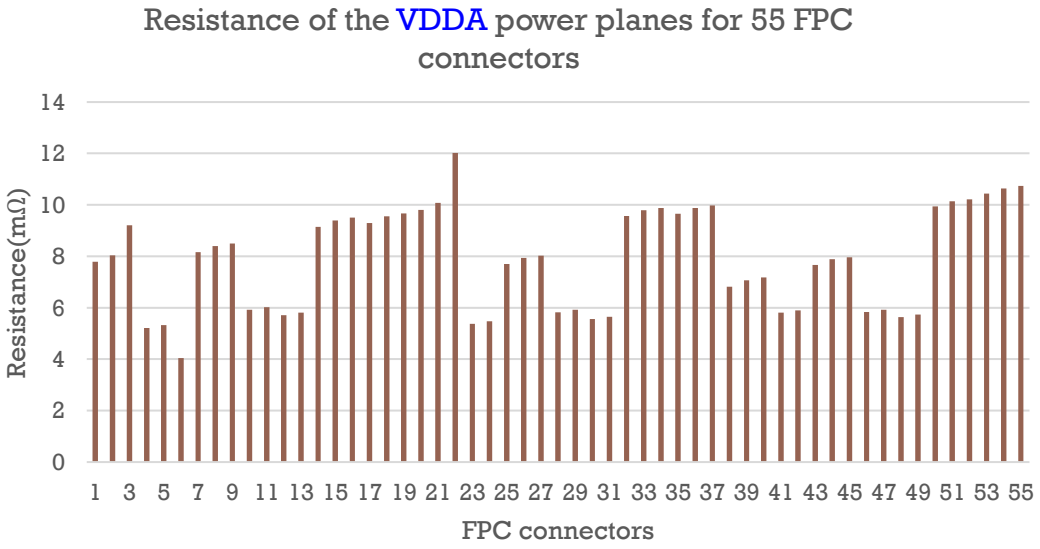
HV return ground

VOLTAGE DROP SIMULATION FOR PEB PLANES

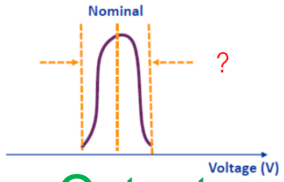
- Simulation result
  - Less than 12 mΩ



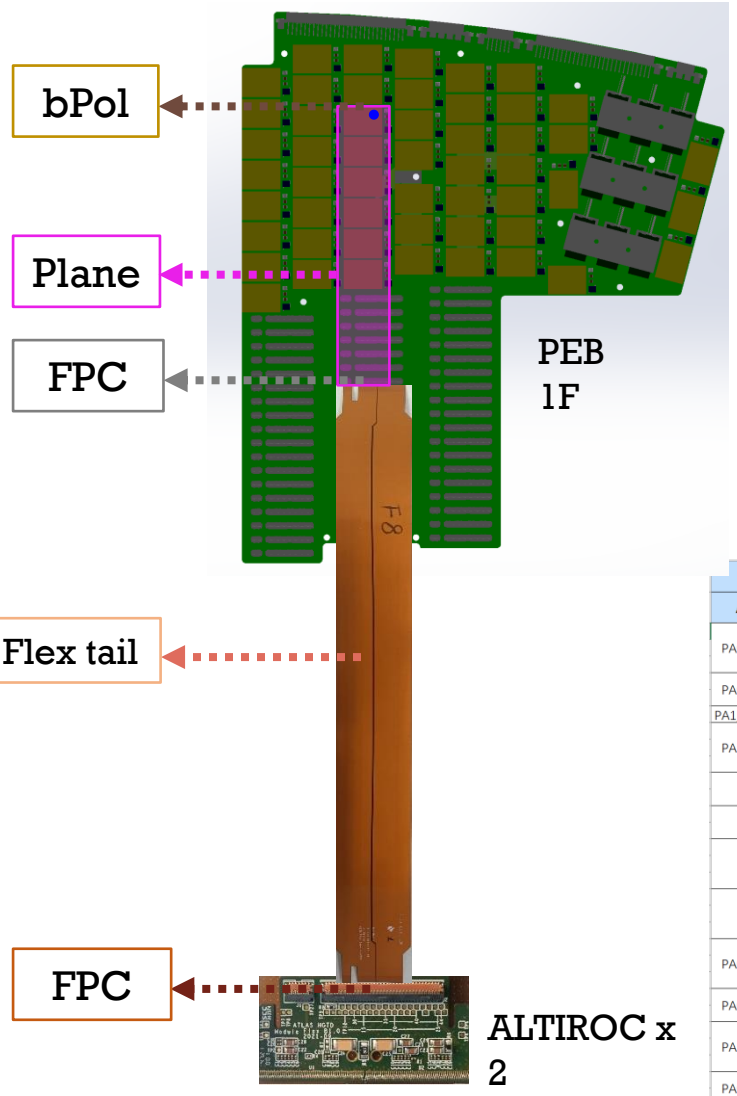




PEB POWER SETTINGS



Output Distribution



Output voltage selection

The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout and gnd (Figure 1). In doing so, it is important to know as precisely as possible the value of the reference voltage (Vref) to the Error Amplifier. The production lot has been tested and the average value of the Vref is 630mV with st dev of 7mV (calculated over 3175 samples in January 2022)
The formula to calculate the proper R selectable for a wanted Vout Vout and given the Vref as above is:
Rsel=500KOhm*Vref/(Vout-Vref)

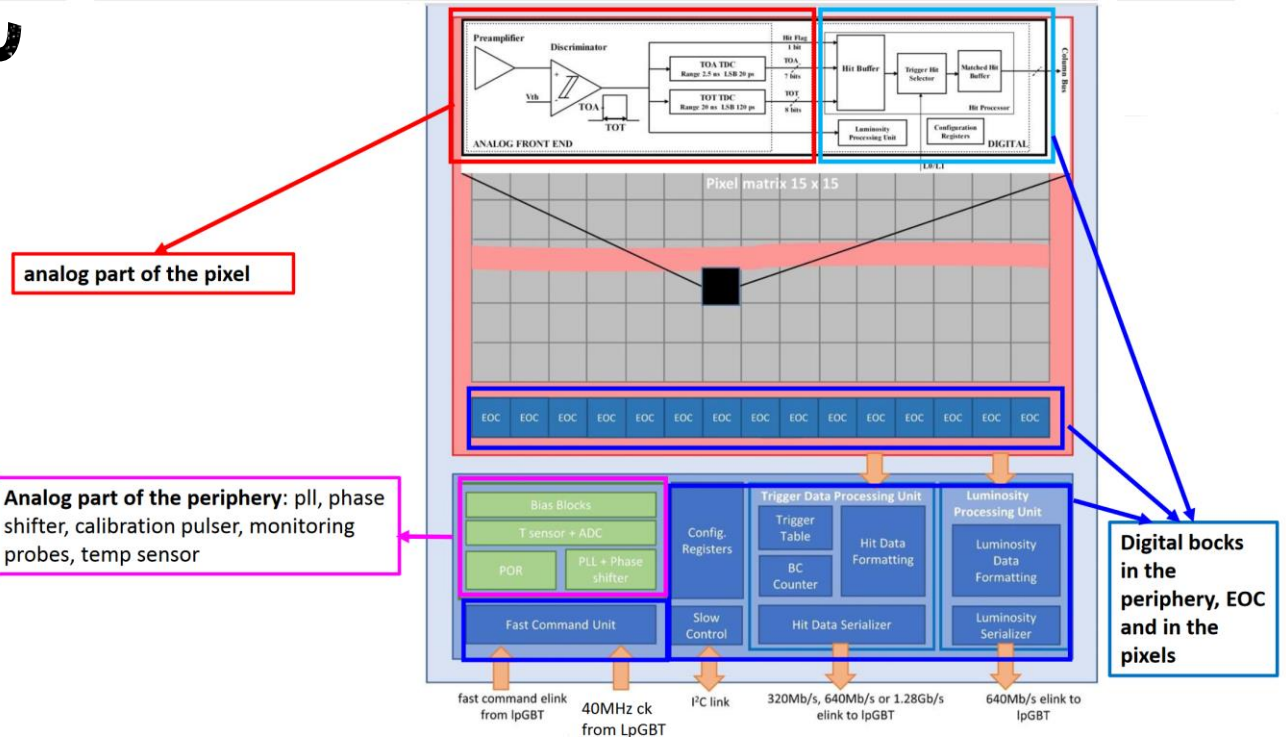
Required output of bPol12V and R_sel determination

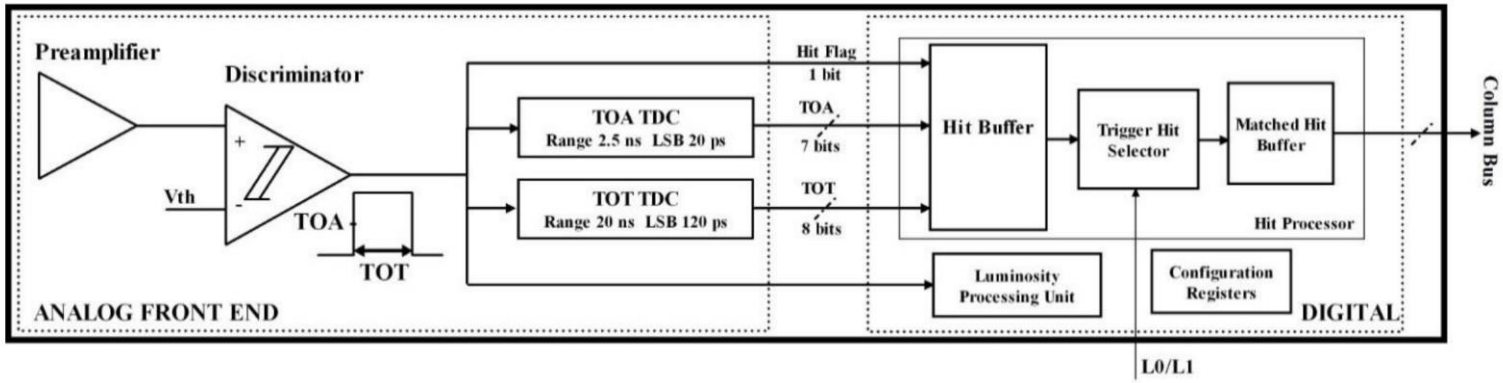
Power Plane_PEB		Row	Module	Flex Distance	R_PEBpath(mΩ)			R_flexTailPath(mΩ)			R_FPC(mΩ)			working currennt(A)		Total IR drop(mV)		Variation_bPol_output		bPol_output(V)		R1_bPol 12V(kΩ)	R_sel_bPol12V(kΩ)	
Analog	Digital				Analog	Digital	GND	Analog	Digital	GND	Analog	Digital	GND	Analog_Max	Digital_Max	Analog	Digital	Analog	Digital	Analog	Digital		Analog	Digital
PA0_344503	PD0_344507	1	18	637.6	7.8	5.0	1.8	116.7	117.5	32.3	12.7	12.1	5.8	0.833	1.167	162.9	224.6	1.7%	1.8%	1.589	1.654	499	328	307
		1	17	605.5	8.0	5.1	2.2	110.8	111.6	30.6	12.7	12.1	5.8	0.833	1.167	157.2	216.4	1.7%	1.8%	1.584	1.645	499	330	310
		2	16	582.2	9.2	7.0	2.2	106.5	107.3	29.5	12.7	12.1	5.8	0.833	1.167	153.7	212.1	1.7%	1.8%	1.580	1.641	499	331	311
PA0_294580	PD0_344507	1	16	573.2	5.2	3.4	2.7	104.9	105.6	29.0	12.7	12.1	5.8	0.833	1.167	149.0	206.1	1.6%	1.7%	1.575	1.633	499	333	313
		1	15	541.1	5.3	3.4	3.0	99.0	99.7	27.4	12.7	12.1	5.8	0.833	1.167	143.1	197.7	1.6%	1.7%	1.569	1.625	499	335	316
PA1_17040112	PD1_17040121	1	14	509	4.0	4.1	3.3	93.1	93.8	25.8	12.7	12.1	5.8	0.833	1.167	136.0	190.0	1.6%	1.6%	1.561	1.616	499	338	319
		1	13	476.9	8.2	5.4	3.7	87.3	87.9	24.1	12.7	12.1	5.8	0.833	1.167	133.5	183.1	1.7%	1.8%	1.559	1.612	499	338	320
PA1_294756	PD1_294764	1	12	441.9	8.4	5.5	3.8	80.9	81.4	22.4	12.7	12.1	5.8	0.833	1.167	127.0	173.9	1.7%	1.8%	1.553	1.602	499	341	323
		1	11	406.9	8.5	5.5	4.0	74.5	75.0	20.6	12.7	12.1	5.8	0.833	1.167	120.4	164.6	1.7%	1.8%	1.546	1.593	499	343	327
PA0	PD0	1	10	371.8	5.9	3.9	4.2	68.0	68.5	18.8	12.7	12.1	5.8	0.833	1.167	111.6	153.3	1.6%	1.7%	1.537	1.579	499	347	331
		1	9	336.8	6.0	4.0	4.3	61.6	62.1	17.0	12.7	12.1	5.8	0.833	1.167	105.0	143.9	1.6%	1.7%	1.530	1.570	499	349	334
PA1	PD1	1	8	301.8	5.7	3.7	4.5	55.2	55.6	15.3	12.7	12.1	5.8	0.833	1.167	98.1	134.2	1.6%	1.7%	1.523	1.560	499	352	338
		1	7	266.8	5.8	3.8	4.6	48.8	49.2	13.5	12.7	12.1	5.8	0.833	1.167	91.4	124.8	1.6%	1.7%	1.516	1.551	499	355	342
PA2	PD2	1	6	231.8	9.1	5.4	4.7	42.4	42.7	11.7	12.7	12.1	5.8	0.833	1.167	87.5	117.2	1.7%	1.8%	1.513	1.544	499	356	344
		1	5	196.8	9.4	5.5	4.8	36.0	36.3	10.0	12.7	12.1	5.8	0.833	1.167	80.9	107.8	1.7%	1.8%	1.506	1.535	499	359	347
		1	4	155.6	9.5	5.5	4.9	28.5	28.7	7.9	12.7	12.1	5.8	0.833	1.167	73.1	96.7	1.7%	1.8%	1.498	1.524	499	362	352
PA3	PD3	1	3	114.5	9.3	5.4	4.9	21.0	21.1	5.8	12.7	12.1	5.8	0.833	1.167	64.9	85.4	1.7%	1.8%	1.490	1.512	499	366	356
		1	2	73.4	9.6	5.6	5.0	13.4	13.5	3.7	12.7	12.1	5.8	0.833	1.167	57.2	74.3	1.7%	1.8%	1.482	1.501	499	369	361
		1	1	32.4	9.7	5.6	5.0	5.9	6.0	1.6	12.7	12.1	5.8	0.833	1.167	49.3	63.2	1.7%	1.8%	1.474	1.489	499	373	366
PA0_329829	PD0_329833	2	18	646.6	9.8	6.8	1.5	118.3	119.2	32.7	12.7	12.1	5.8	0.833	1.167	166.1	228.8	1.7%	1.8%	1.593	1.658	499	327	306
		2	17	614.5	10.1	6.9	1.9	112.5	113.3	31.1	12.7	12.1	5.8	0.833	1.167	160.4	220.5	1.7%	1.8%	1.587	1.650	499	329	308
		3	15	544	12.0	7.5	2.4	99.6	100.3	27.5	12.7	12.1	5.8	0.833	1.167	148.7	202.5	1.7%	1.8%	1.575	1.631	499	333	314
PA0_314860	PD0_314864	2	15	550.1	5.4	3.7	2.5	100.7	101.4	27.8	12.7	12.1	5.8	0.833	1.167	144.5	199.9	1.6%	1.7%	1.570	1.627	499	334	315
		2	14	518	5.5	3.7	2.8	94.8	95.5	26.2	12.7	12.1	5.8	0.833	1.167	138.6	191.5	1.6%	1.7%	1.564	1.618	499	337	318
PA1_315036	PD1_315044	2	13	483	7.7	5.5	3.1	88.4	89.0	24.4	12.7	12.1	5.8	0.833	1.167	133.9	184.3	1.7%	1.8%	1.560	1.613	499	338	320
		2	12	448	7.9	5.6	3.4	82.0	82.6	22.7	12.7	12.1	5.8	0.833	1.167	127.5	175.2	1.7%	1.8%	1.553	1.603	499	340	323
		2	11	413	8.0	5.6	3.6	75.6	76.1	20.9	12.7	12.1	5.8	0.833	1.167	120.9	165.9	1.7%	1.8%	1.547	1.594	499	343	326
PA0_266430	PD0_266434	2	10	377.9	5.8	4.1	3.8	69.2	69.6	19.1	12.7	12.1	5.8	0.833	1.167	112.4	154.7	1.6%	1.7%	1.537	1.581	499	346	331
		2	9	342.8	5.9	4.1	4.0	62.7	63.2	17.3	12.7	12.1	5.8	0.833	1.167	105.8	145.4	1.6%	1.7%	1.531	1.571	499	349	334
PA1_266514	PD1_266516	2	8	307.9	5.6	3.9	4.2	56.3	56.7	15.6	12.7	12.1	5.8	0.833	1.167	98.9	135.8	1.6%	1.7%	1.524	1.562	499	352	337
		2	7	272.9	5.7	4.0	4.4	49.9	50.3	13.8	12.7	12.1	5.8	0.833	1.167	92.3	126.4	1.6%	1.7%	1.517	1.552	499	354	341
PA2_266612	PD2_266614	2	6	237.9	9.6	5.7	4.5	43.5	43.8	12.0	12.7	12.1	5.8	0.833	1.167	88.8	119.0	1.7%	1.8%	1.514	1.546	499	356	343
		2	5	196.8	9.8	5.8	4.6	36.0	36.3	10.0	12.7	12.1	5.8	0.833	1.167	81.1	108.0	1.7%	1.8%	1.506	1.535	499	359	347

ELECTRONICS - ALTIROC

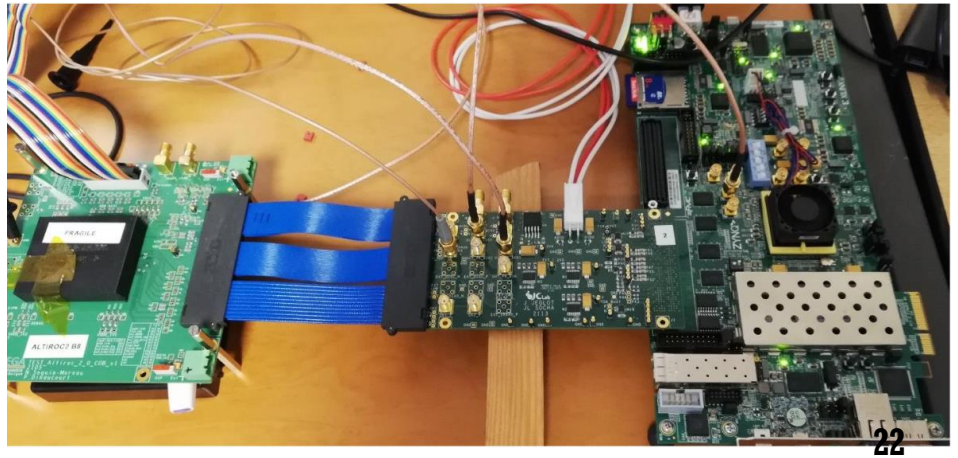
ASIC designed in 130 nm CMOS from TSMC

- Requirements to match the performance of LGADs:
  - Small jitter: 25 ps at 10 fC (< 70 ps at 4 fC)
  - Radiation hard (2.5×10^{15} neq/cm^2, 2.0 MGy)
  - 2 fC minimum discriminator threshold
- Prototype status:
  - ALTIROC 0 and ALTIROC 1: Small prototype for analog FE tests (2020 JINST 15 P07007, 2023 JINST 18 P08019)
  - ALTIROC 2: First full size prototype (15 ×15 pixels, 2 ×2 cm 2) with full electronic chain (VPA and TZ amplifier types)
  - ALTIROC 3: Prototype up to specs presently under test (only TZ amplifiers implemented)



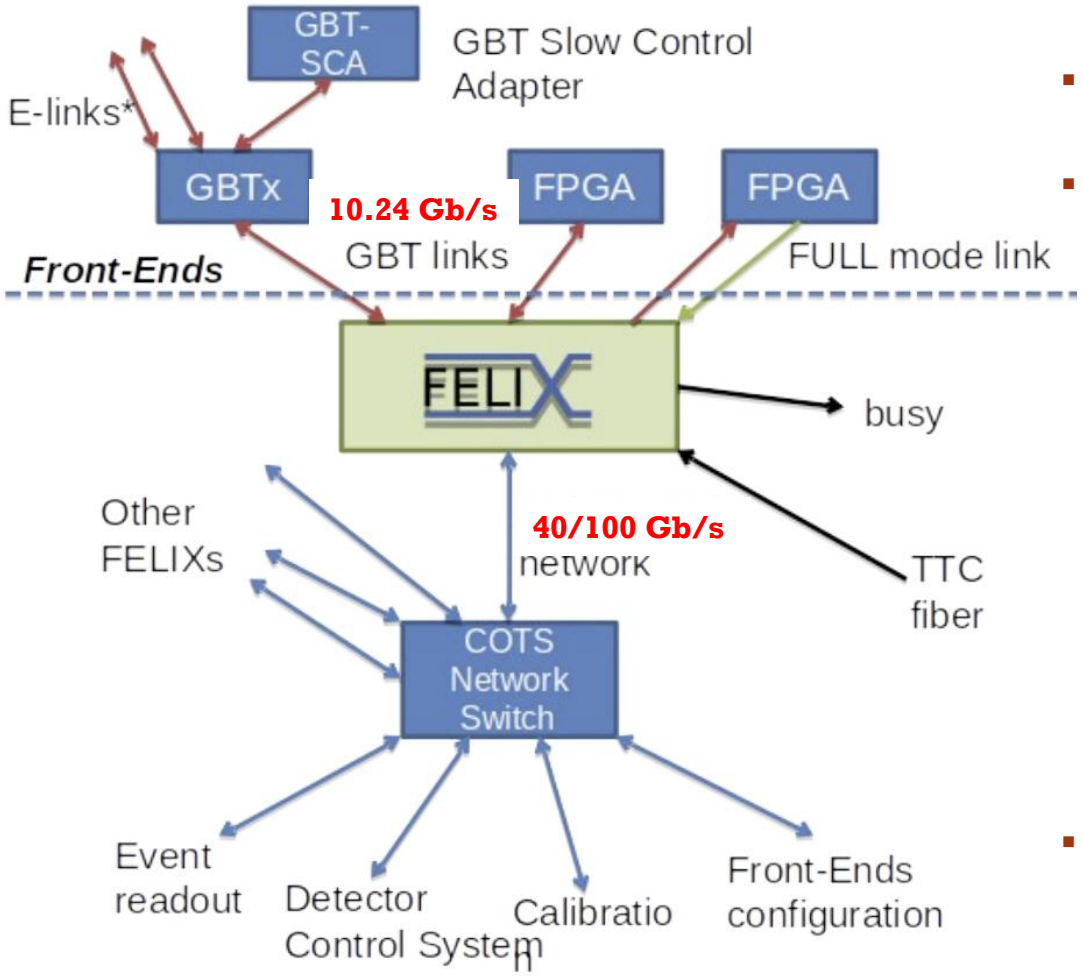


Block diagram of the on-pixel electronics



ALTIROC test system with FPGA

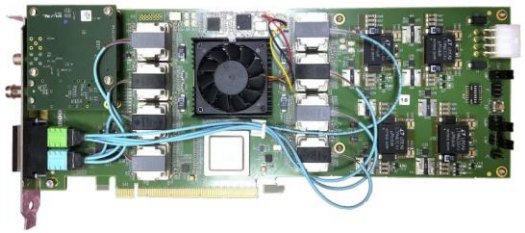
ATLAS TDAQ



- FELIX (Front-End Link eXchange)
  - A system provides radiation-tolerant bidirectional communication for the front-end electronics and data acquisition (DAQ) of the ATLAS detector.
  - It offers clock synchronization, control, configuration, calibration, and monitoring capabilities for the front-end chips.
  - Additionally, FELIX collects and aggregates data from the front-end chips.
- Hardware design of FELIX developed by BNL (Brookhaven National Laboratory), while the FPGA firmware designed by Nikhef
- This system supports user development of custom functionalities.

- FELIX Phase 1 / Run 3 hardware:
  - The FLX-712 card:
    - FPGA: Xilinx Kintex UltraScale KU115
    - 16-lane PCIe Gen3 for a bandwidth of up to 128 Gb/s
    - 4 or 8 MiniPODs to support 24 or 48 bidirectional optical links

- FELIX Phase 2 / Run 4 hardware:
  - The FLX-181/182 card:
    - FPGA: Xilinx Versal Prime VP1802
    - 16-lane PCIe Gen4 for a bandwidth of up to 256 Gb/s
    - 24 Firefly optical links with up to 25 Gb/s
    - 4 FireFly optical links which can be used for a 100GbE port



- HGTD
  - 1728 lpGBTs to transmit hit time data from 8032 front-end modules to 48 FELIX systems.
  - Additionally, luminosity data will be transmitted to 32 FELIX systems.
  - The total data throughput from the front-end to FELIX reaches a remarkable 10 Tbps, with an average of approximately 62.72 Gbps per front-end circuit board.