Development of high-speed serializer circuits for fast readout of pixel detectors

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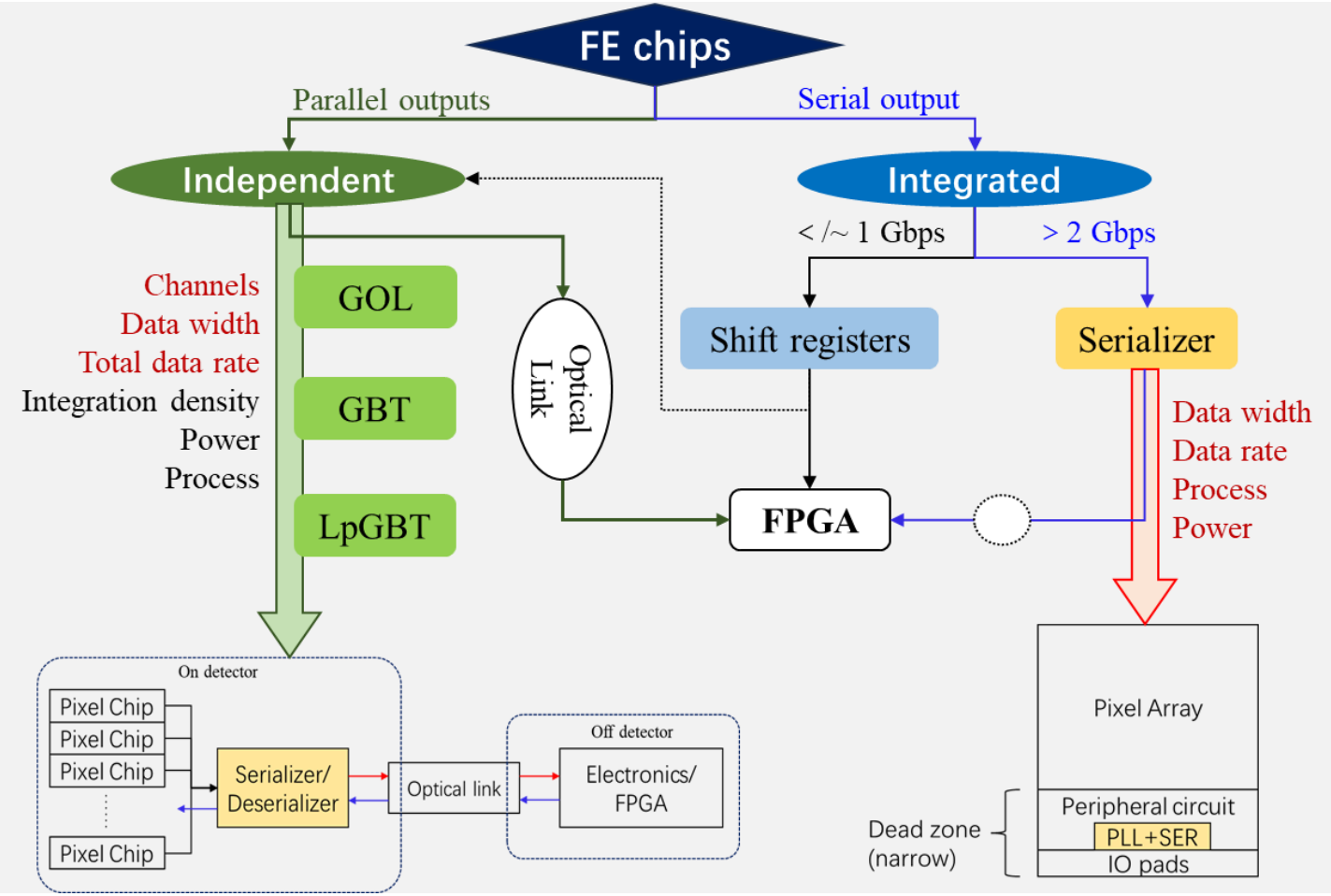
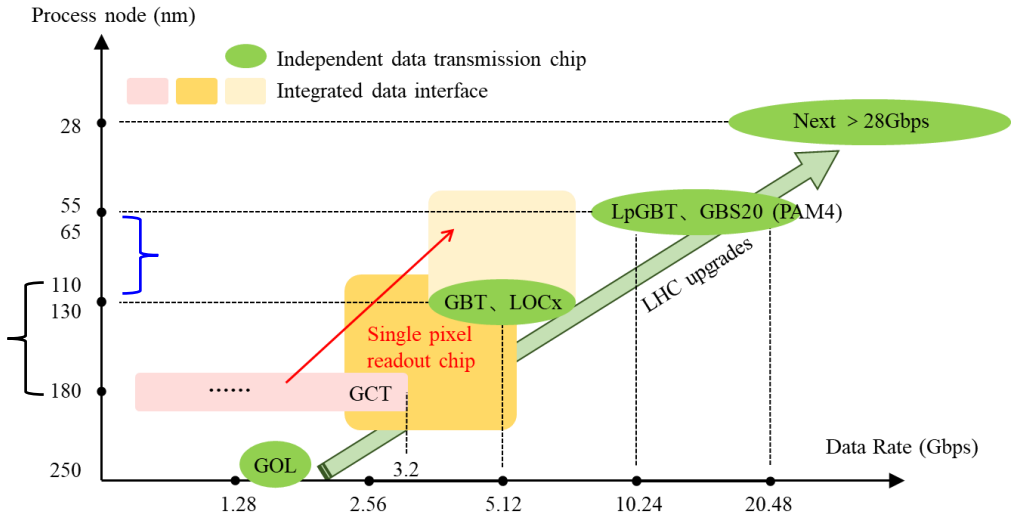
Outline

- Data transmission in HEP experiments
- Serializer for the CEPC vertex detector
- Other research
- Summary

Data transmission in HEP experiments

Application requirements



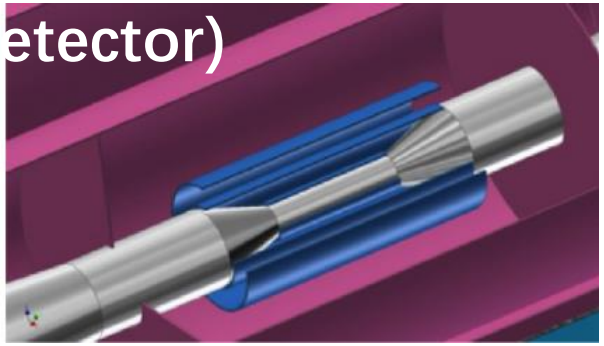


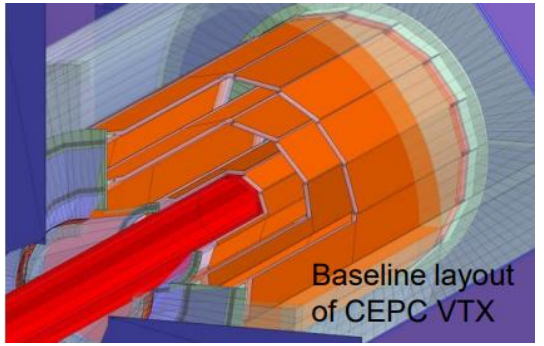
◆ Integrated data interface

Kbps → Mbps → 1 Gbps → 3~4 Gbps

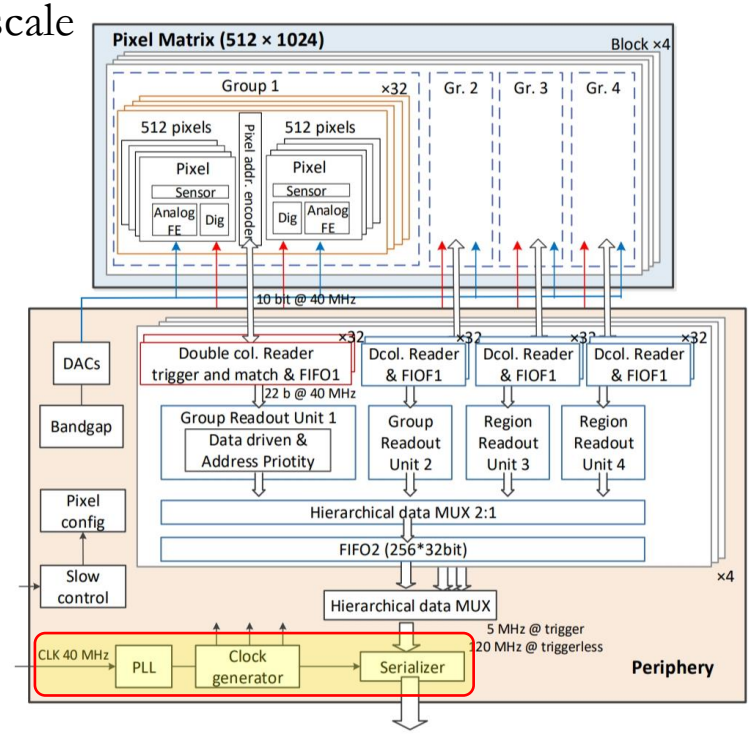
CEPC vertex detector requirements

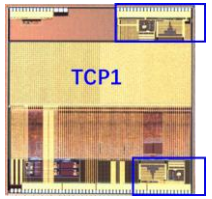
- **Main specifications (Monolithic pixel detector)**
  - Full-scale full-functionality pixel sensor readout chip
  - σ~5 μm： pixel size 25×25 μm², 512×1024
  - Particles： Higgs、W、Z
- **Data rate**
  - Bunch spacing, Hit density, Cluster size, Pixel size and scale
  - Average hit rate ~ 120 MHz/chip @W
  - 32 bits/hit → raw data rate ~3.84 Gbps
  - Trigger mode ~110 Mbps

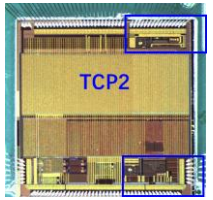




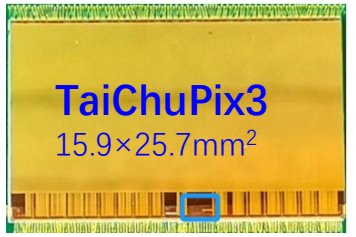
For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Data rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm² (air cooling)
		Dead time	< 500 ns --for 98% efficiency	Chip size	~1.4 × 2.56 cm²







Array:
64×192
5×5 mm²



Serializer for the CEPC vertex detector

Architecture

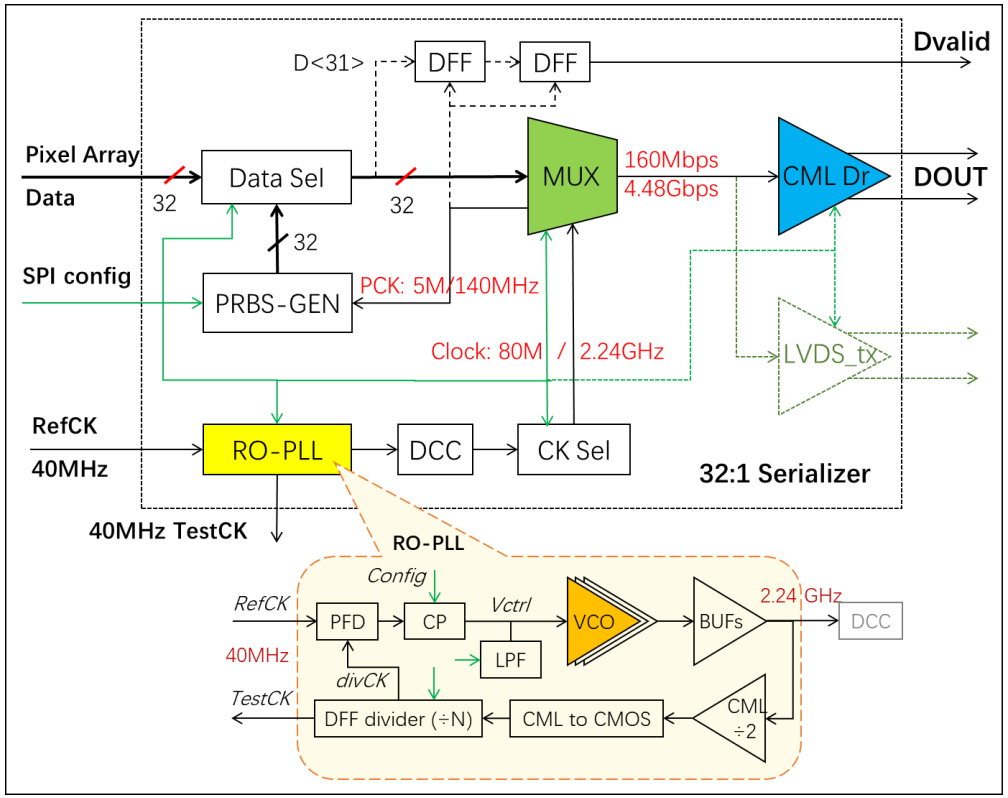
- 32:1 binary-tree structure (MUX)
- Ring-Oscillated Phase-Locked Loop (RO-PLL)
- CML driver & LVDS TX (selectable)
- Data valid signal output

Major challenges

- Speed and power consumption (180 nm)

Simulated performance

- MUX: 8mA @320Mbps, 44.2 mA @4.48Gbps
- RO-VCO： 3.6~26.3 mA
  - 0.34~3.42 GHz @TT27
  - -101 dBc/Hz@1MHz offset
- CML driver: 36.5 mA, LVDS_tx： 4.8 mA @250Mbps
- ＜85 mA @Trigger mode, ＜ 130 mA @Triggerless Mode
- Large-size transistors, large power consumption



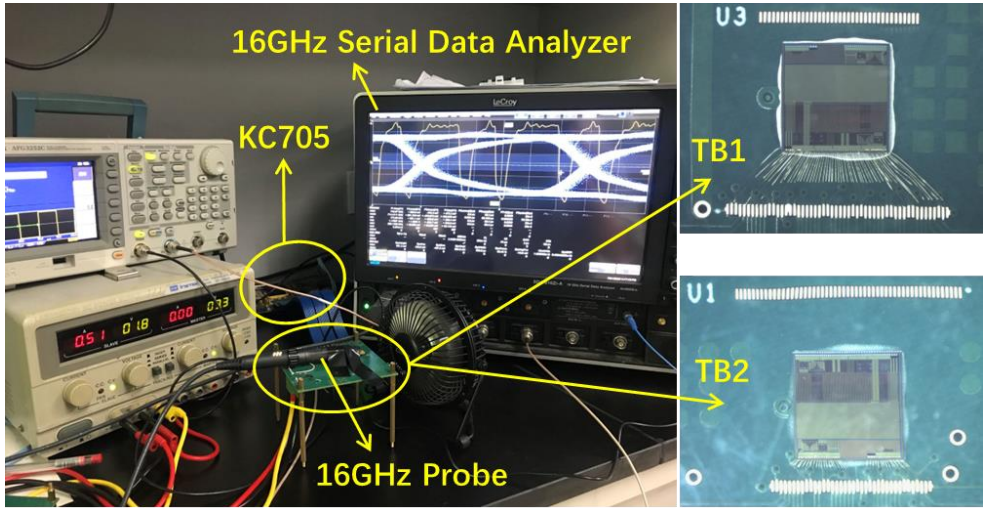
Serializer for the CEPC vertex detector

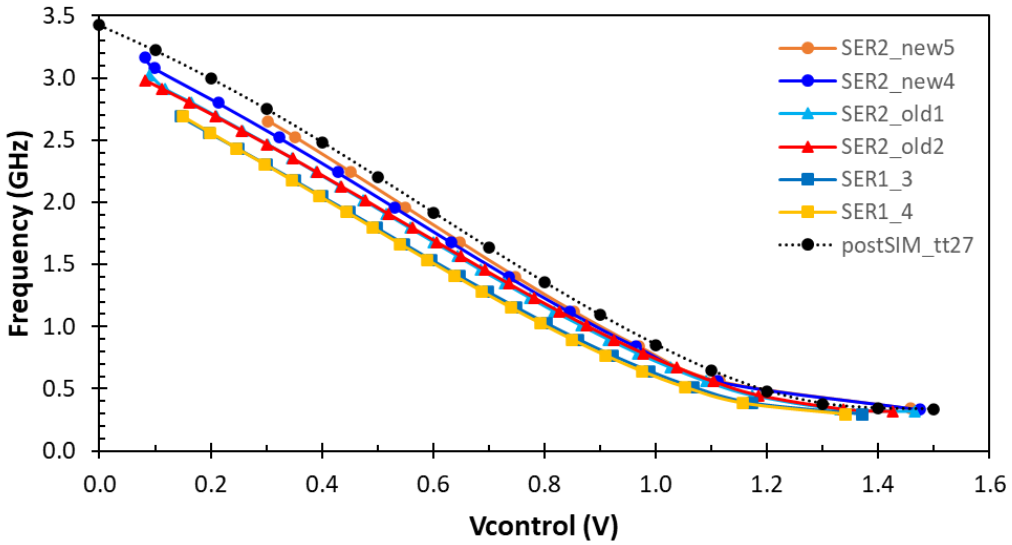
Tests

- CMOS reference clock input (40MHz)
- CMOS test clock (40MHz)
  - Tuning range
    - 0.30~2.68GHz、0.32~2.91GHz、0.34~3.16GHz、0.33~2.65GHz
  - Rj ≈ 9~12 ps
- CML serial data output
  - The output serial sequence is correct up to 4.48 Gbps
  - Large jitter
    - Rj: 5.3 ps ~ 7.3 ps
    - Tj: 147 ps ~ 180 ps

Analysis

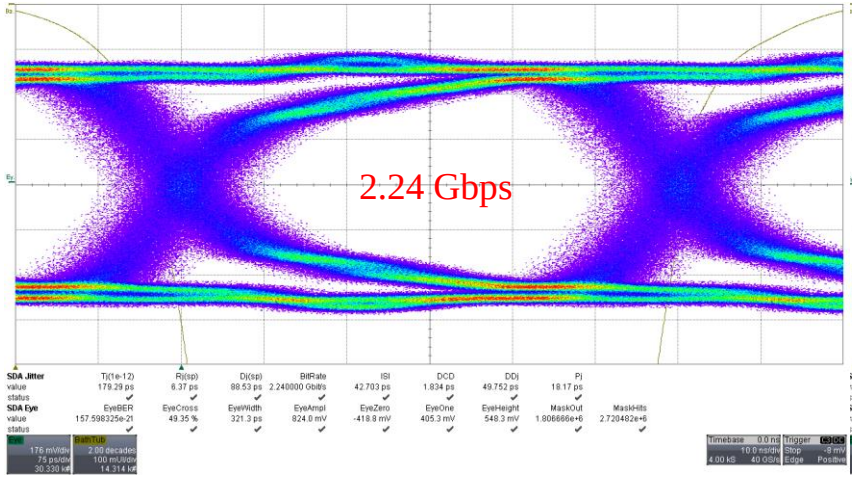
- CMOS reference clock → large jitter
- Insufficient driving capability (& high load)
- Long bonding wire → over 2.5 mm

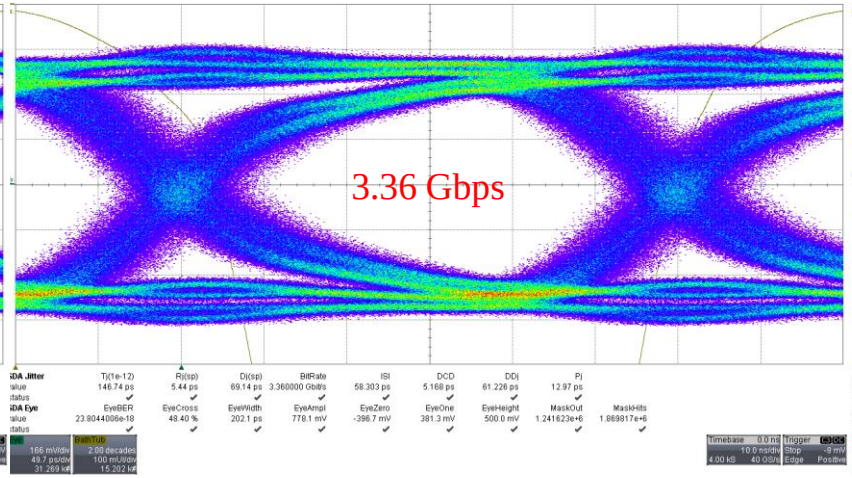


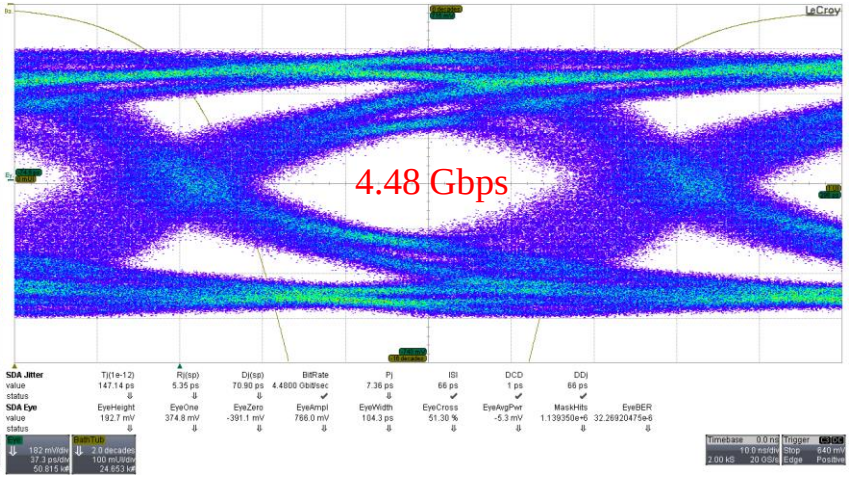


Serializer for the CEPC vertex detector

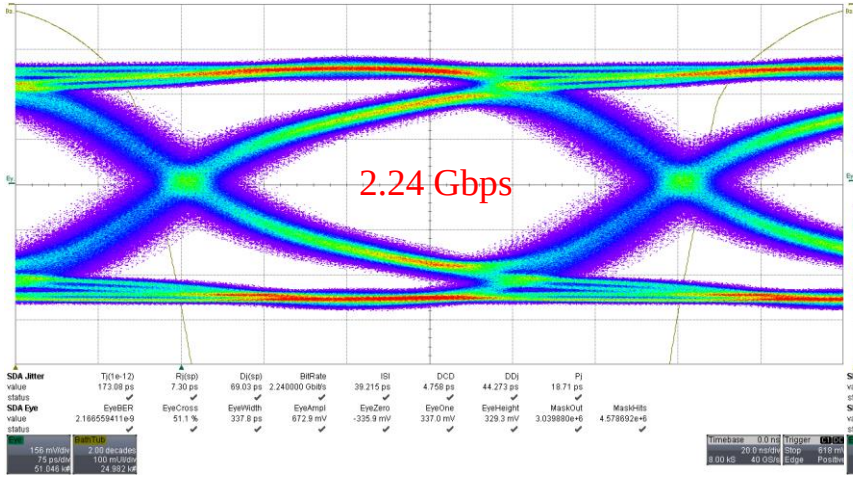
Eye-diagram tests

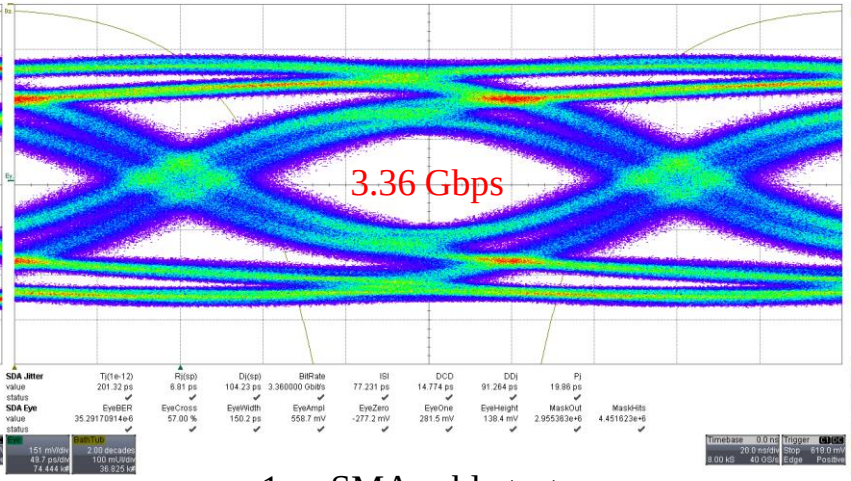


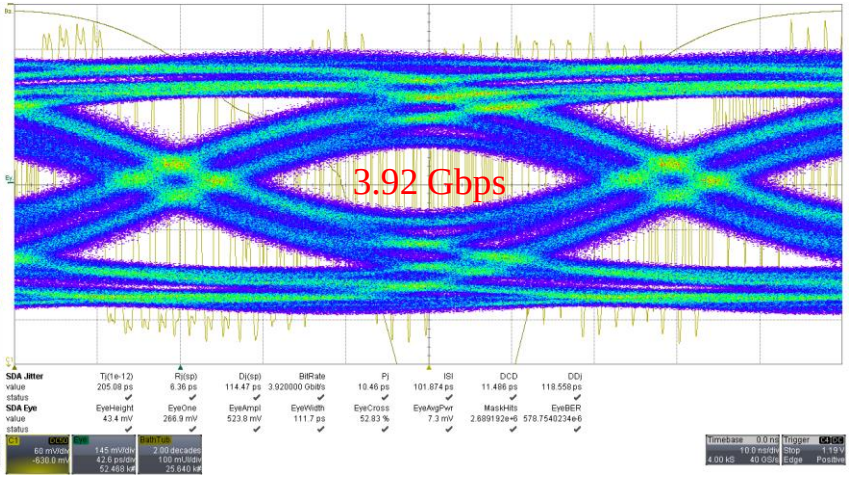




6-GHz differential probe tests







1-m SMA cable tests

Pre-designs for the CEPC vertex detector

Considerations

- Data width requirement & Pre-validation
  - 8B10B encoder
- Another 180 nm process
  - Time, cost and convenience
  - Easy to transplant

Architecture

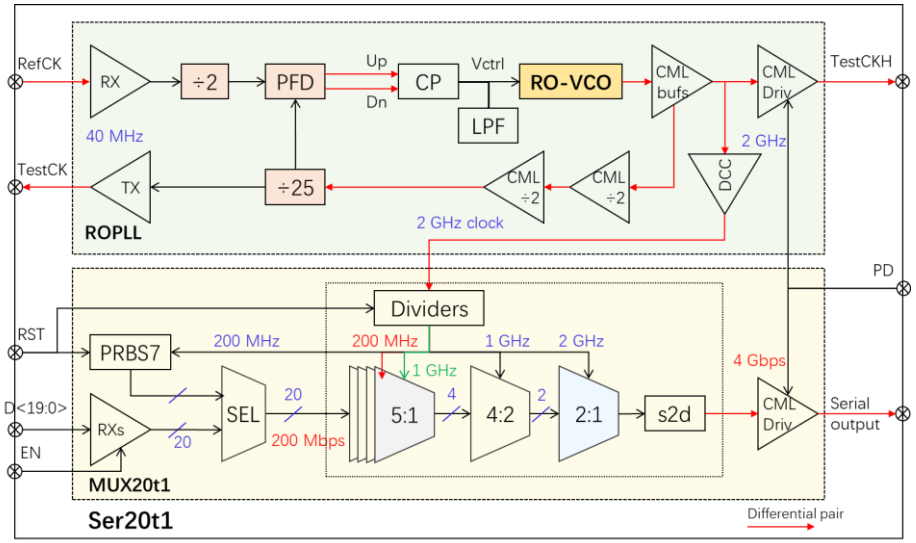
- Differential inputs and outputs
- Including a 20:1 and a 40:1 serializer
- First stage: 4/8×Shift-register chain (5:1)
- Other stages: binary tree (2:1)
- RO-PLL & LC-PLL

Simulations

- 20:1 Ser Core: 75 mA
- 40:1 Ser Core: 84 mA

Revision

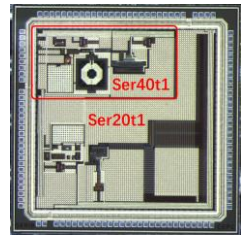
- 40:1 Ser Core: 78 mA
- Corrected the possible errors
- Will tapeout this moon



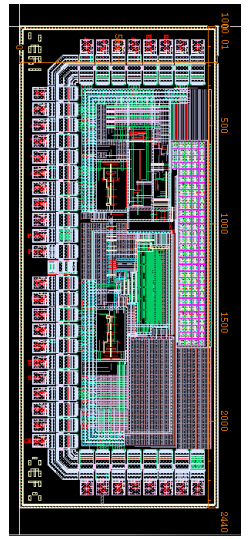
Clock perfomance		Sim-results	Test-results
RO-PLL	Tuning Range	0.34~3.12 GHz	0.32~2.95 GHz
	PN-1M@2GHz	-103 dBc/Hz	
	Random Jitter	~1.4ps (VCO)	#1.1 ps
	Current@2GHz	~27.63 mA	
LC-PLL	Tuning Range	1.8~2.3 GHz	*1.81~2.45 GHz
	PN-1M@2GHz	-118 dBc/Hz	
	Random Jitter	~ (VCO)	#*0.7 ps
	Current@2GHz	~34 mA	

Measured through TestCK (LVDS_TX, larger Rj than CML driver)
* Power=2.6V

- 40:1 Serializer
  - LC-PLL
  - 8× 5:1 units
  - 8:4 unit



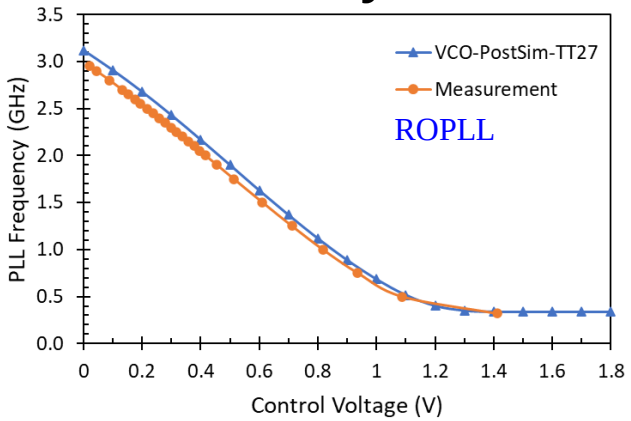
Prototype chip 3×3 mm^2

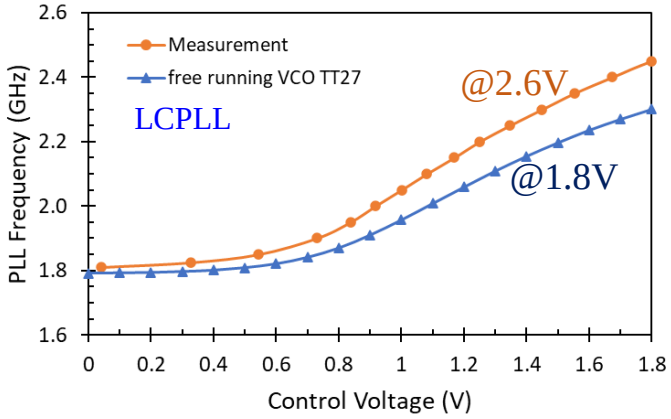


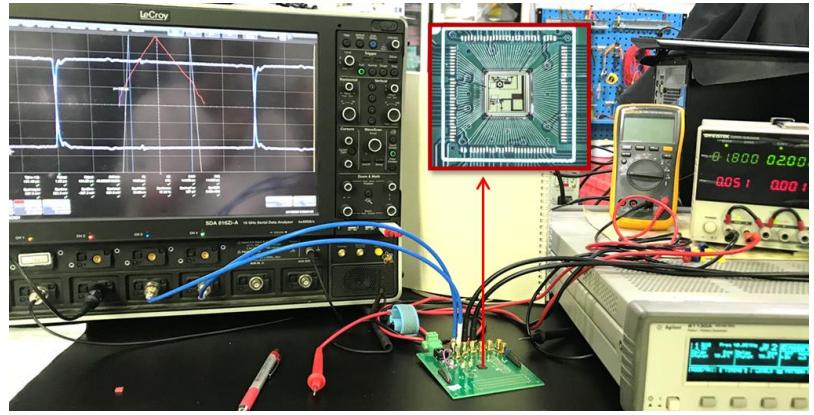
Revision layout 1×2.44 mm^2

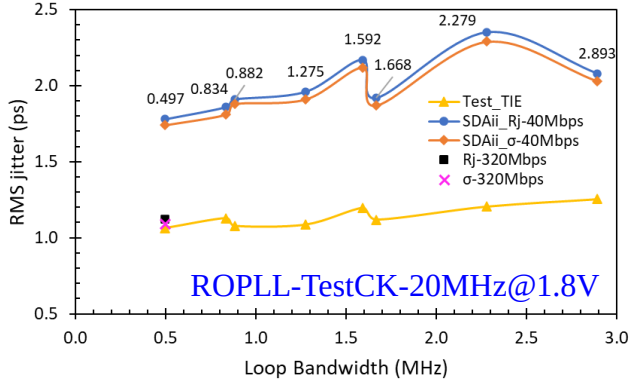
Pre-designs for the CEPC vertex detector

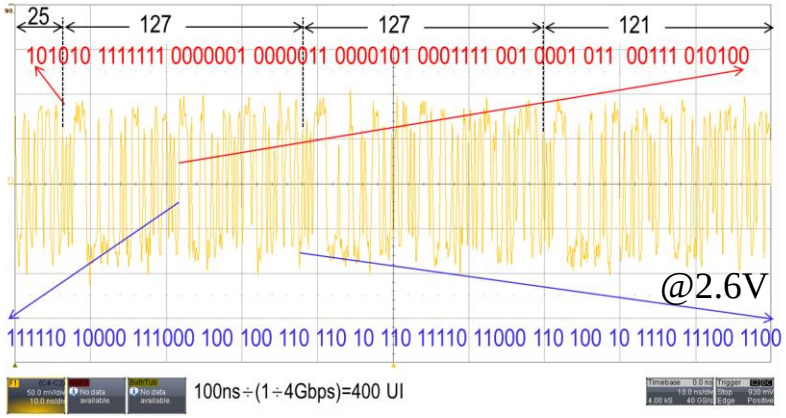
Preliminary Tests

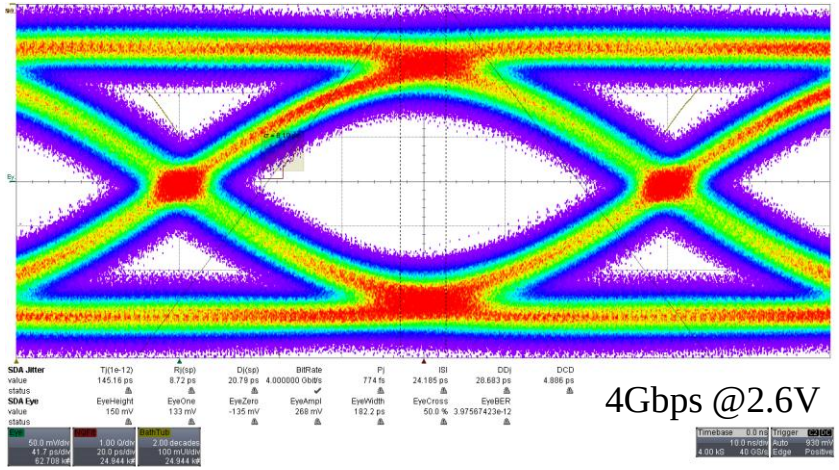










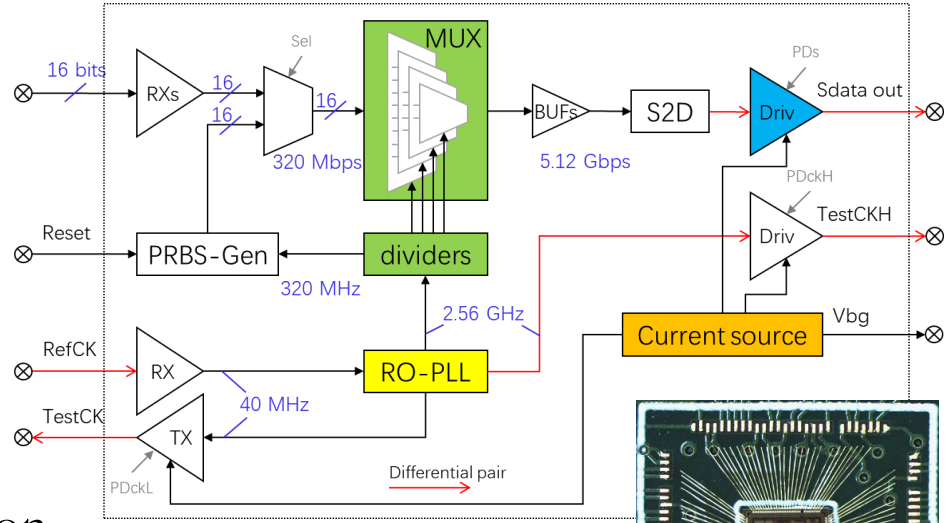


- The RO-PLL worked normally. The LC-PLL worked at a power supply higher than 2 V.
- The output serial sequence was correct up to 4 Gbps.
- The problem might be in the bias circuits which were also used in the CML driver, resulting abnormally small driving current, and leading to no efficient signal output at 1.8-V power supply.
- Debugging and performance evaluation still needs more tests.

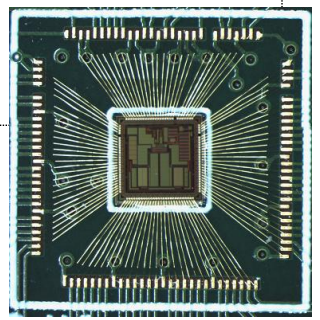
Other research Ser5G: design

- 5.12 Gbps serializer in 130 nm process
- Current application (Hybrid detector)
  - Synchrotron radiation sources:
    - HEPS (High Energy Photon Source)
    - SHINE (Shanghai high repetition rate X-ray Free Electron Laser and extreme light facility) : HYLITE chip

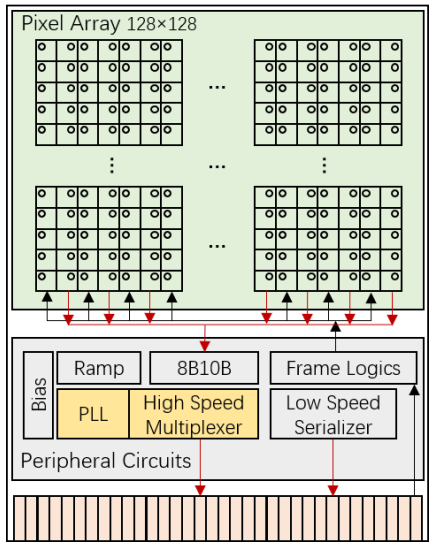
- Architecture
  - Binary-tree structure (32:1/16:1 MUX)
  - RO-PLL
  - CML outputs
  - Common current bias
- Next
  - LC-PLL to improve jitter performance
  - Stronger driving capability & equalization technique
  - CDR circuit for the de-serializer



Architecture



Ser5G prototype chip 2.4×2.4 mm^2

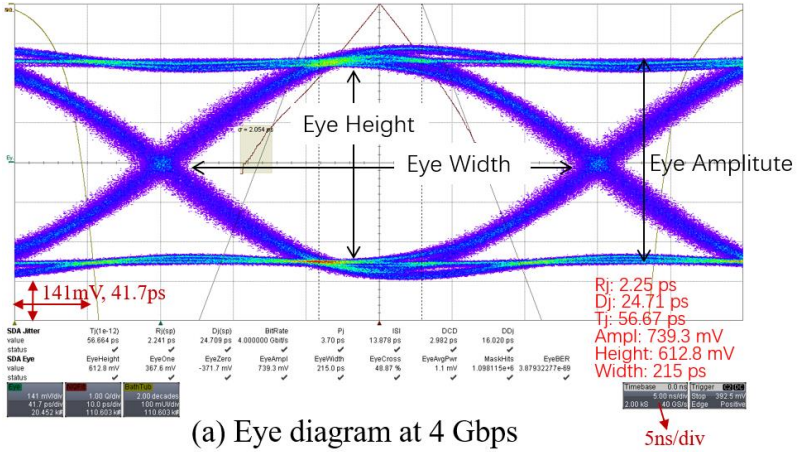


Full-scale HYLITE architecture

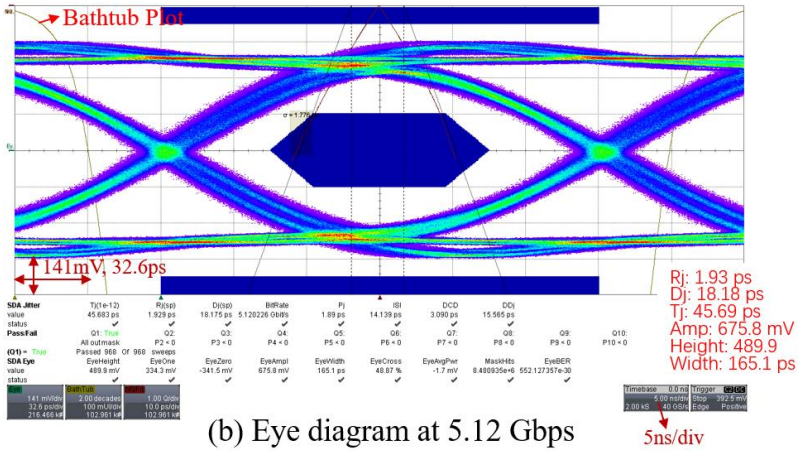
Other research Ser5G: eye and jitter tests

Measured performance

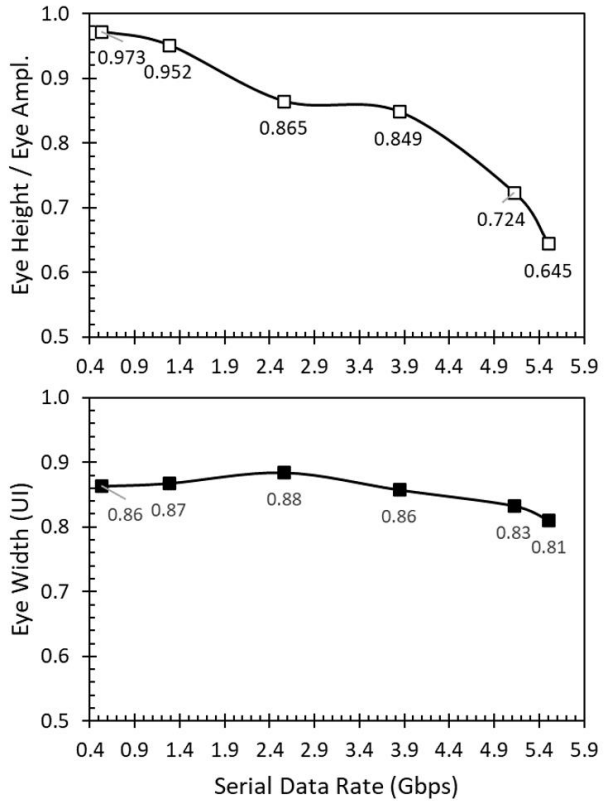
- Data rate: 0.52 Gbps to 5.5 Gbps
- Jitter @5.12 Gbps: Rj≈2 ps, Dj≈20 ps, Tj≈47 ps (10^{-12} BER)



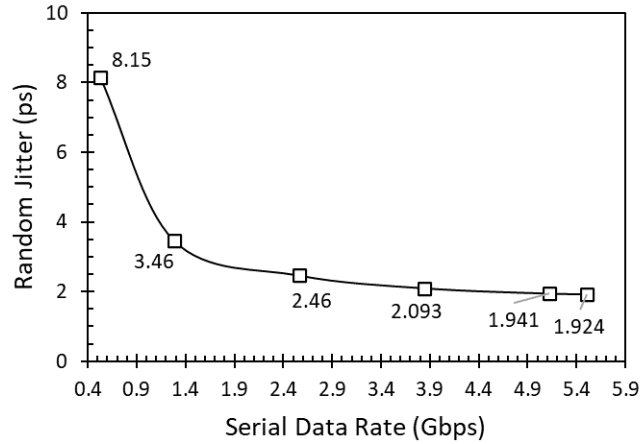
(a) Eye diagram at 4 Gbps

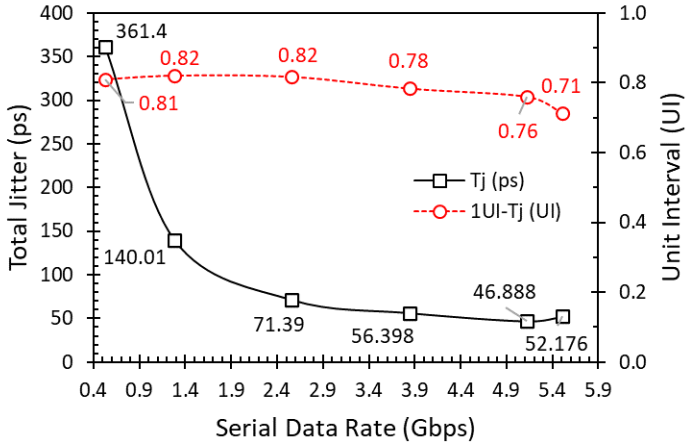


(b) Eye diagram at 5.12 Gbps



(c) Eye opening versus data rate

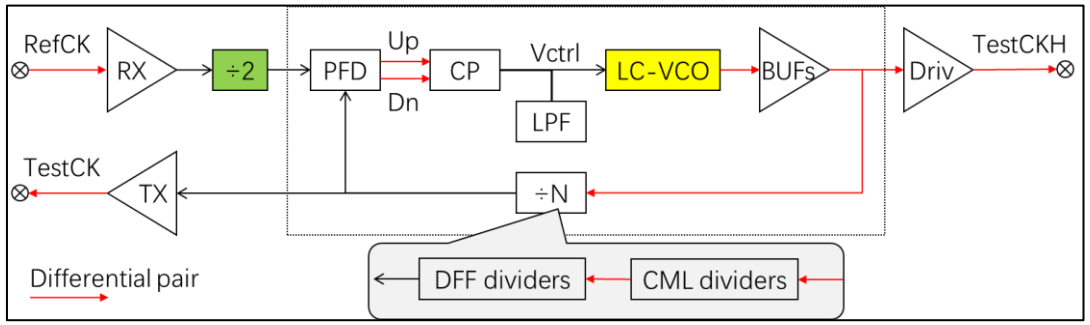


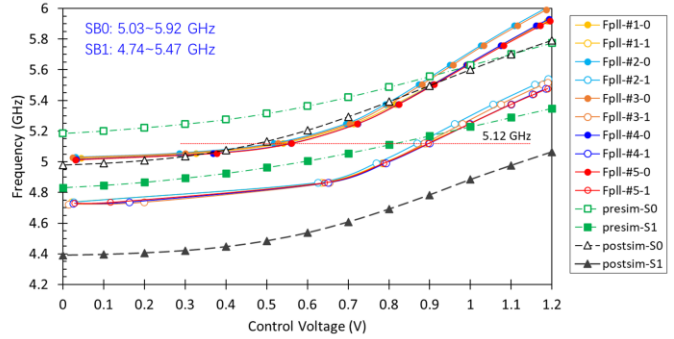


(d) Jitter measurements

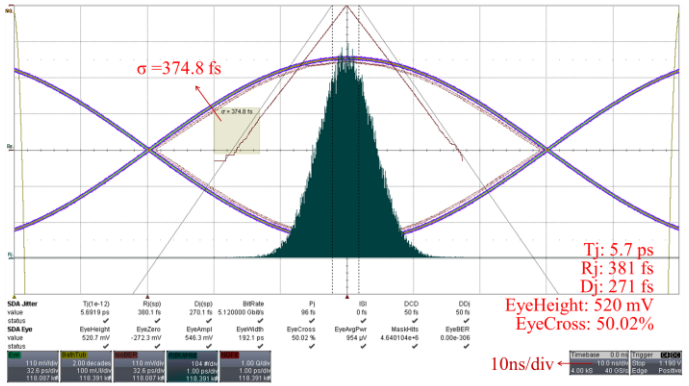
Other research PLL5G: design & tests

- **5.12 GHz PLL in a 55 nm process**
- **Applications**
  - 10 Gbps serializer/SerDes
  - High precision Time-to-Digital Converter
- **Architecture**
  - LC-tank VCO
  - Differential charge pump
  - A divide-by-2 prescaler
  - An 8-division CML divider chain & a 32-division DFF divider chain
- **Measured performance**
  - 4.74~5.92 GHz
  - Pre-sim: -113 dBc/Hz @1MHz offset
  - Best: Rj≈381 fs, Tj≈5.7 ps (0.5 m cable)
  - 5 boards: Rj<460 fs, Tj<7.5 ps (1 m)
  - Core ~ 27 mW, Total ~ 73.8 mW

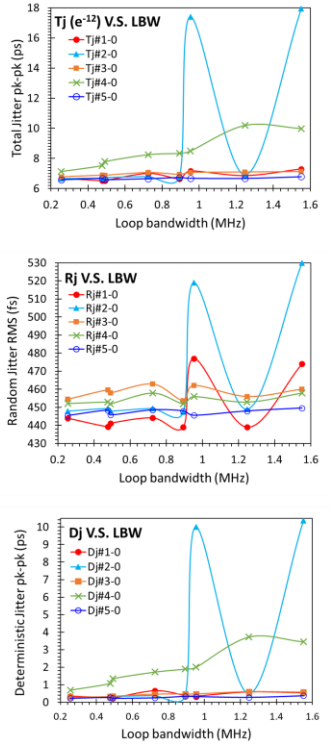




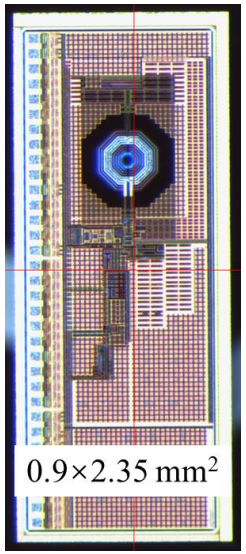
(a) Frequency locking range



(b) Eye and noise histogram of the divide-by-2 output (#1 board)



(c) Jitter performance of the divide-by-2 output (sub-band 0)



PLL5G prototype chip

Xiaoting Li et al.
https://doi.org/10.1007/s41365-022-01074-2

Summary

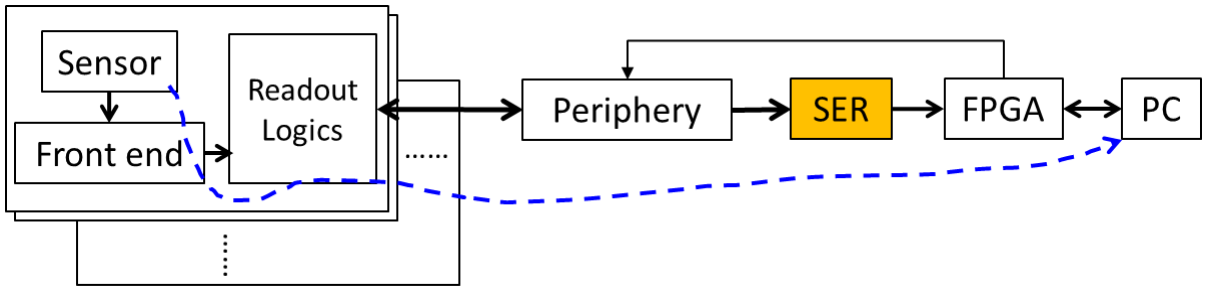
- In 180 nm process, several serializer prototypes have been tried to achieve the 4 Gbps date rate requirement of the pixel sensor detector. The major functionality has been verified. But there're still some bugs need to be revised, and performance evaluation also needs more tests.
- In 130 nm process, a 5 Gbps serializer has been verified. Some improvements are moving on.
- In 55 nm process, we have verified a 5 GHz PLL design, and next a 10 Gbps serializer is pushing.
- These pre-researches and designs may provide some reference value to the on-chip data readout of possible CEPC applications.

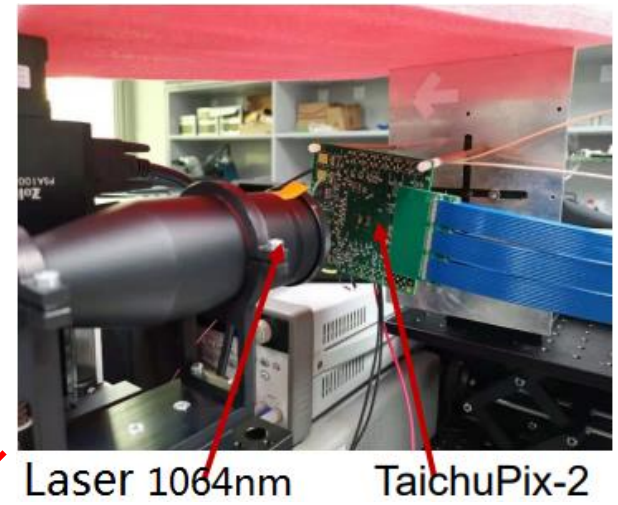
Thanks very much for your attention!

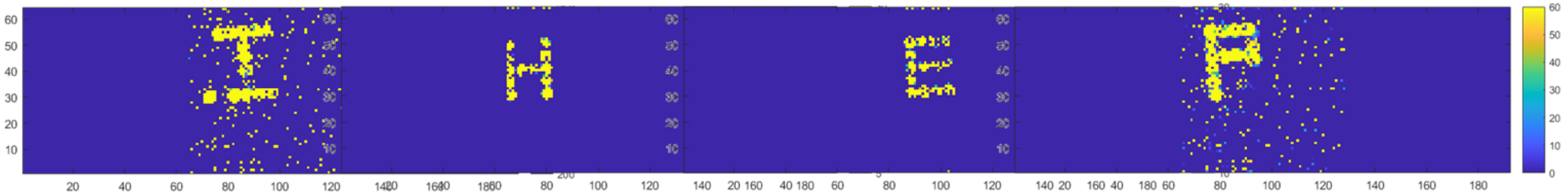
Backup

Laser tests of the TaiChuPix-2 chip

- Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was proved.



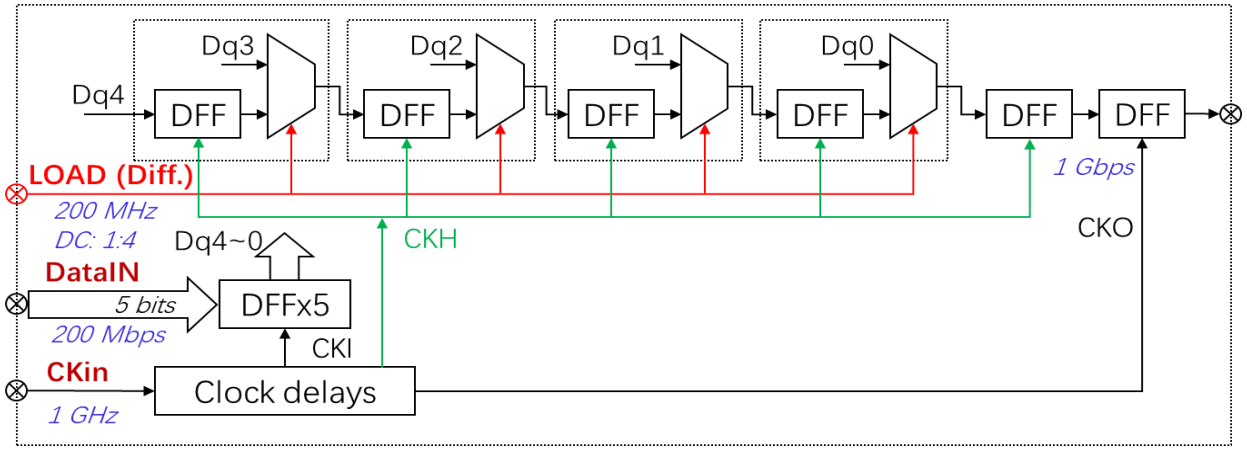




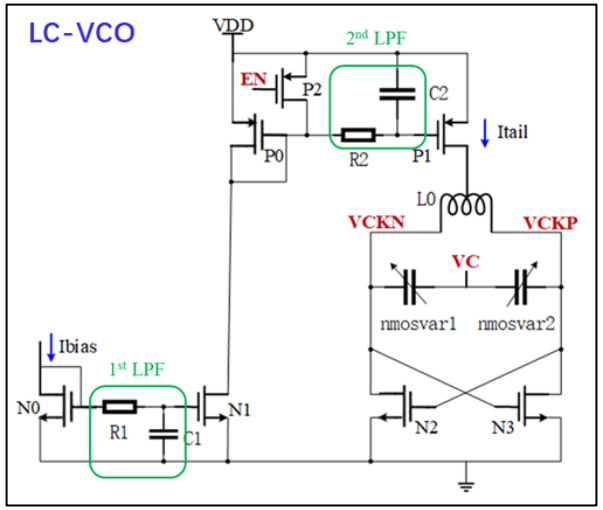
Backup

Ser20t1/40t1 designs

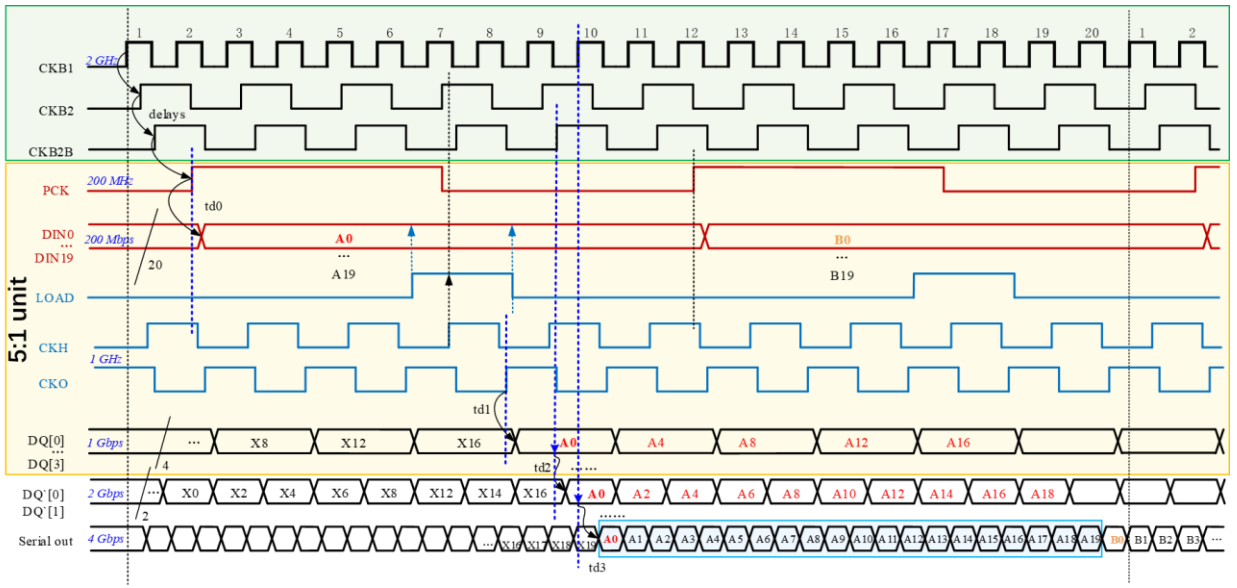
- The 5:1 SFR unit for the Ser20t1/Ser40t1
  - Four/eight duplicates share common clocks (Ckin & Load) generated in the divider
  - When the Load is high, new data is loaded in.
  - Data is shifted to the output at every rising edge of the CKH (1 GHz / 500 MHz)
- The LC-tank VCO uses two RC filters to suppress the bias noise.



5:1 unit scheme for the Ser20t1



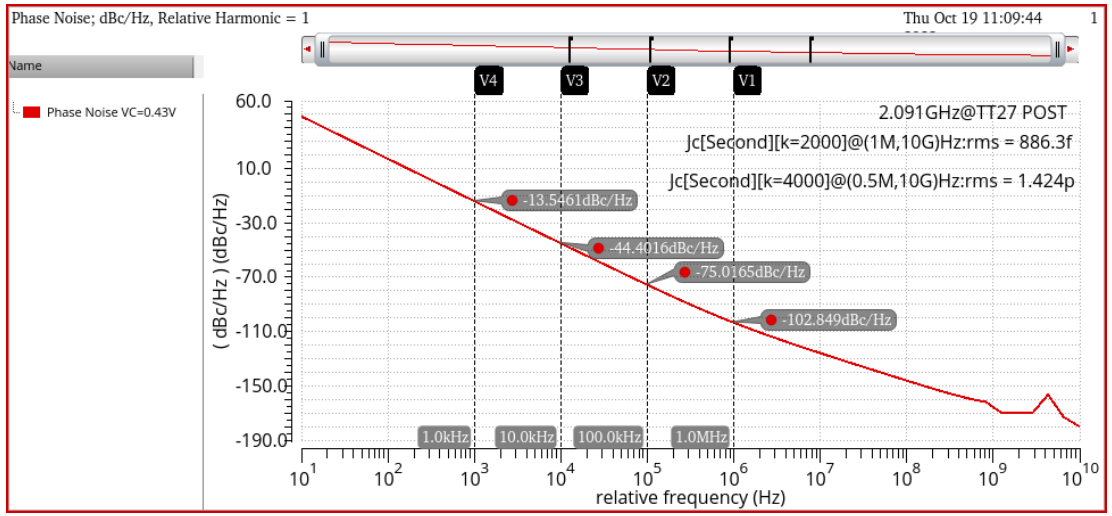
LC-VCO scheme

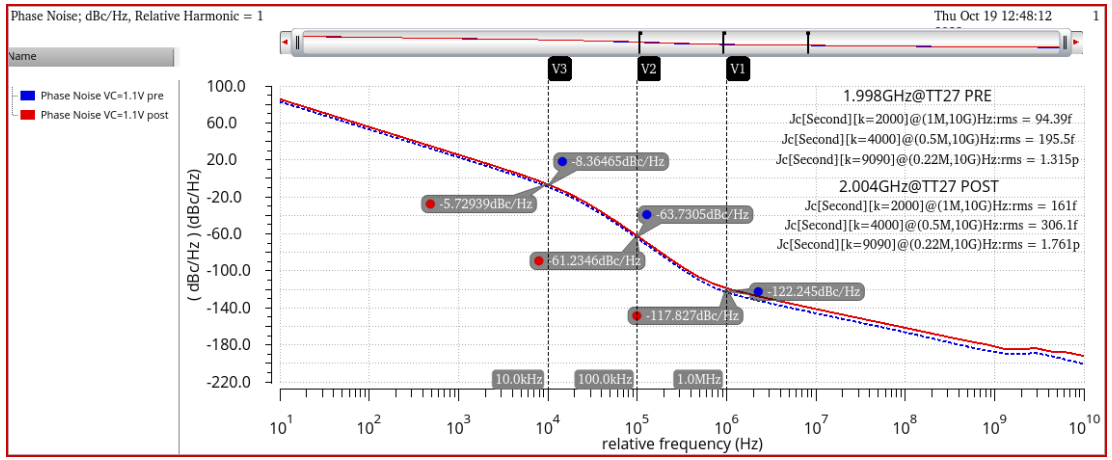


Timing of the 20:1 serializer

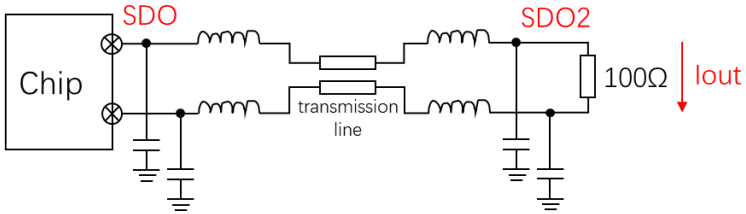
Backup

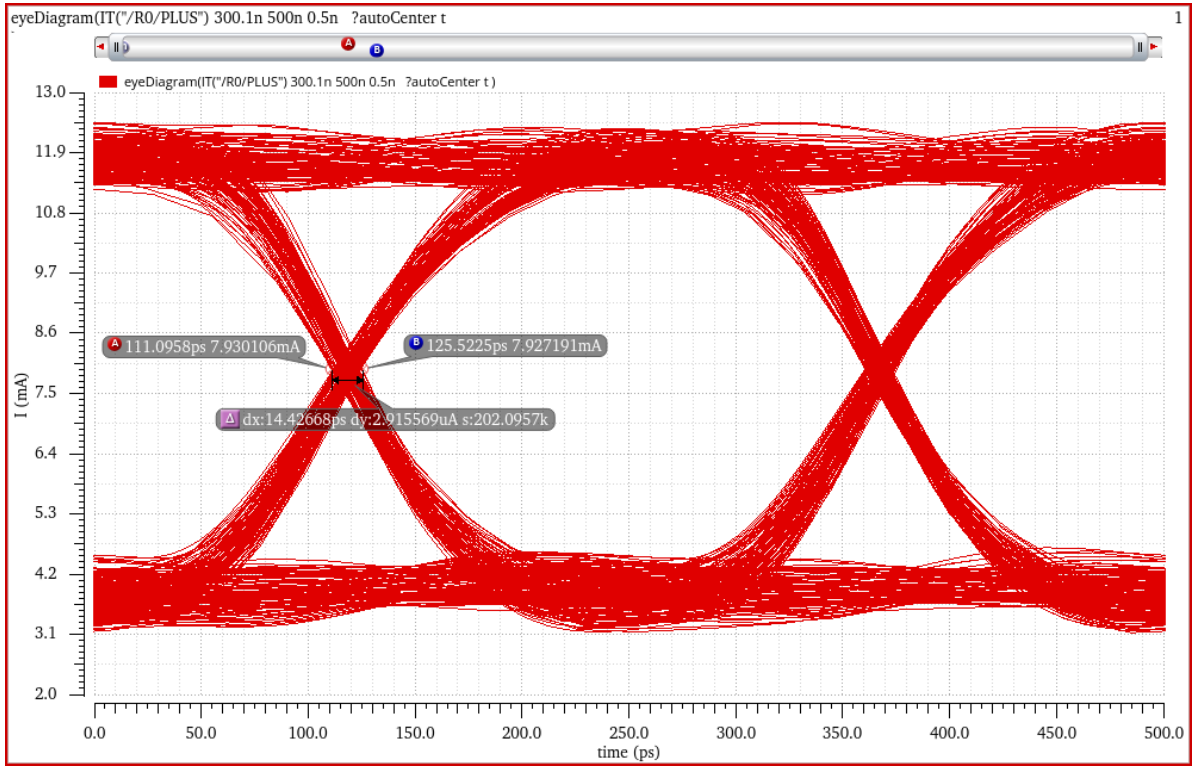
Ser20t1/40t1 simulations





← Phase noise post-layout simulation of the RO-VCO



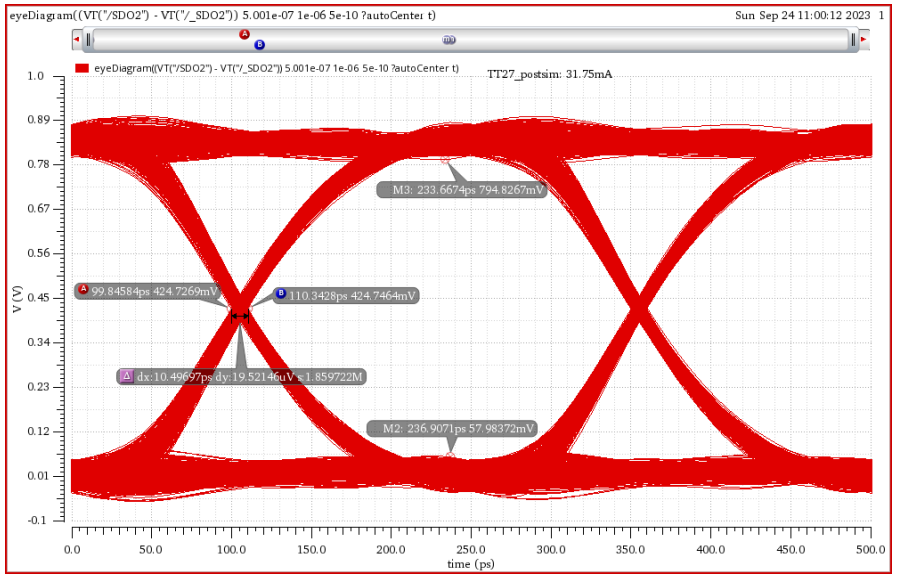


↑ 4 Gbps eye diagram, loads: 1.5pF+1.5nH+1M+1.5nH+1.5pF

← Phase noise pre-/ post-layout simulations of the LC-VCO

Backup

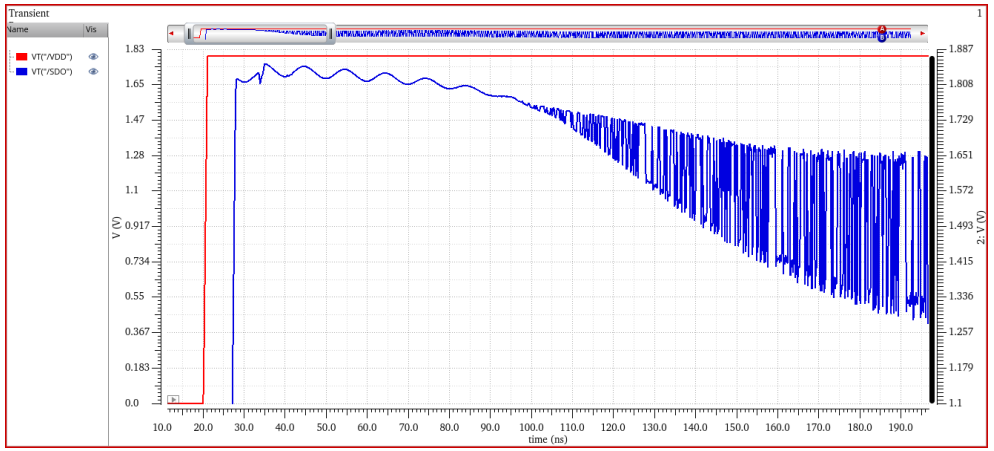
Simulations of the revision chip



(Driver)
4 Gbps eye diagram

← loads: 1pF+1nH+1M+1nH+1pF

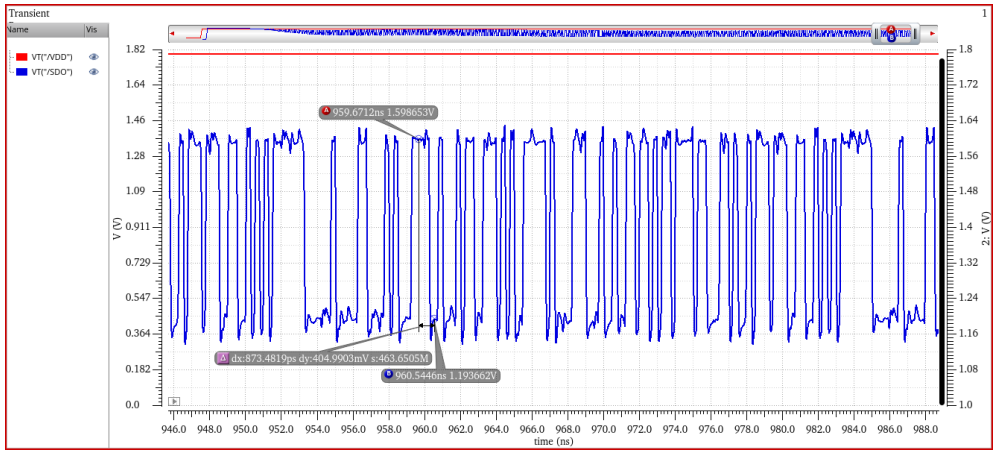
2pF+2nH+1nF+1M+2nH+2pF→



(MUX + driver)
Transient signals
with power up

← Start

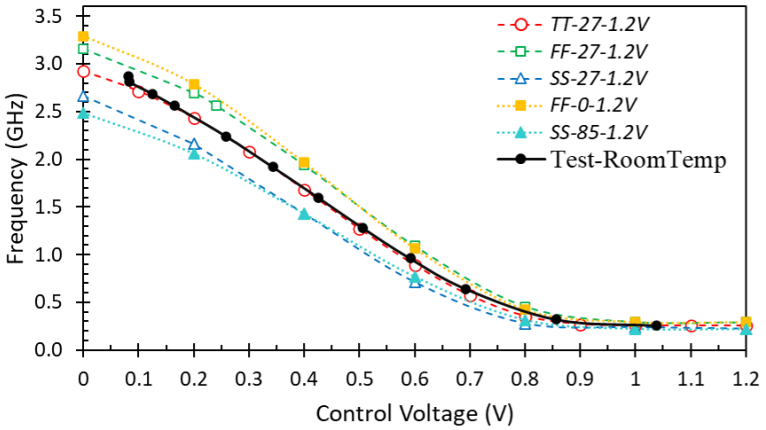
Stop →



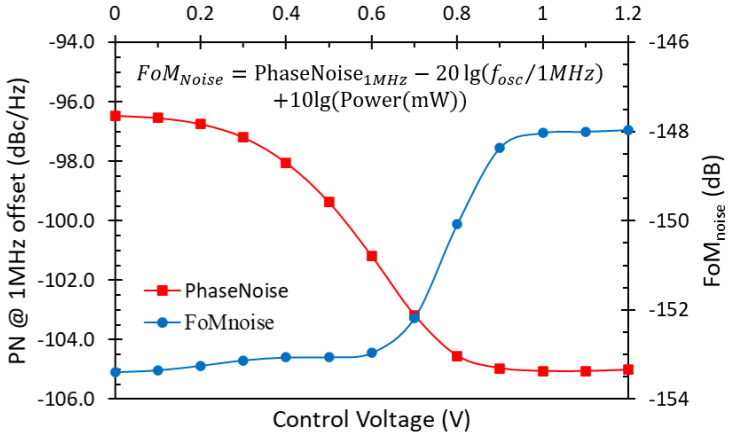
Backup SER5G

RO-PLL performance

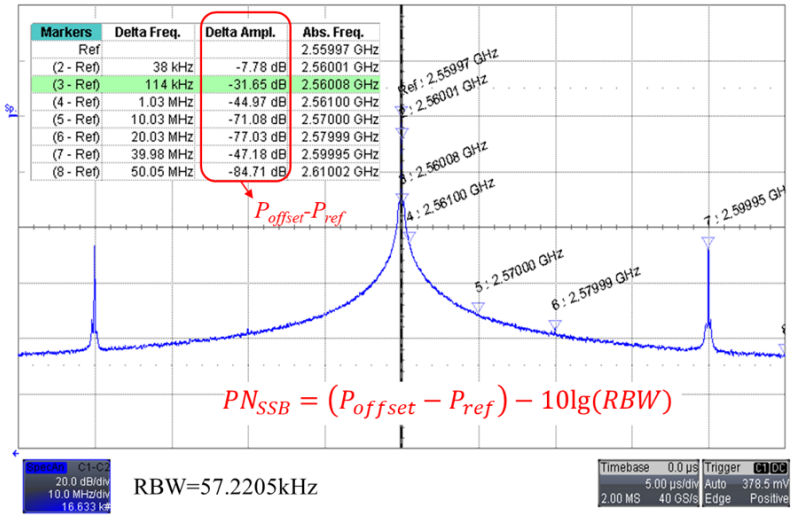
- Simulations
  - 0.26~2.92 GHz
  - -96.6 dBc/Hz @1MHz offset
- Tests
  - 0.26~2.86 GHz
  - -92.5 dBc/Hz @1MHz offset (Oscilloscope)
  - -94.9 dBc/Hz (N9320B)
  - Rj≈1 ps



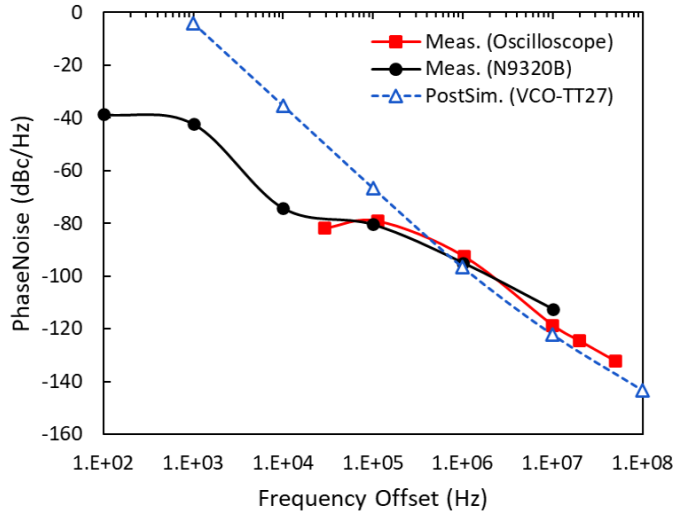
(a) Frequency locking range



(b) Simulated PN-1M and FoM values of the VCO



(c) Clock spectrum at 2.56 GHz

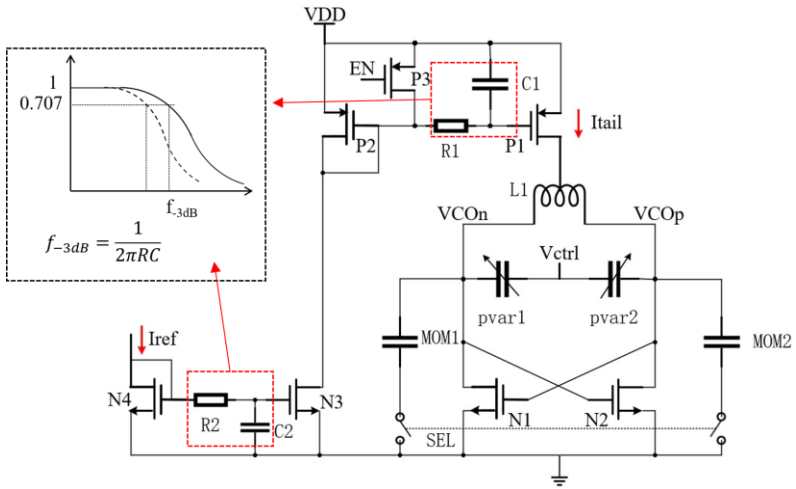


(d) Measured and simulated PN curves at 2.56 GHz

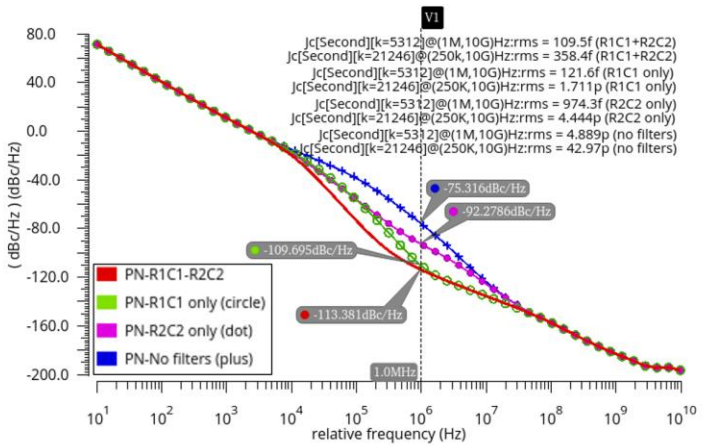
Backup PLL5G

Simulated performance

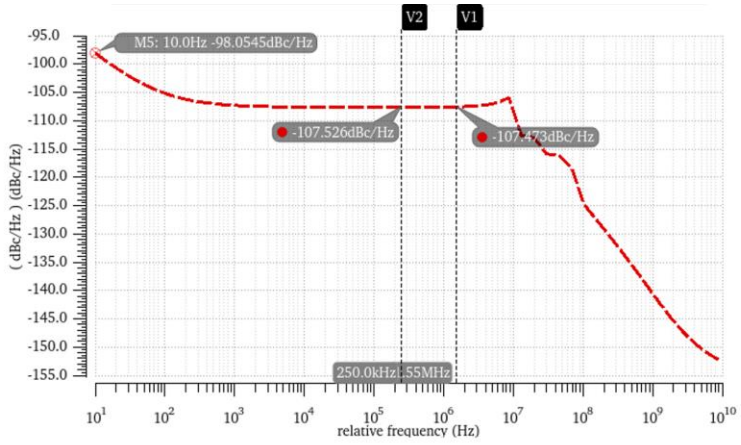
- -113 dBc/Hz @1MHz offset



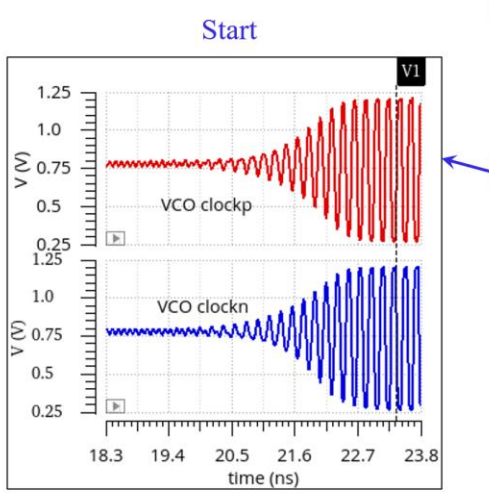
LC-VCO Scheme



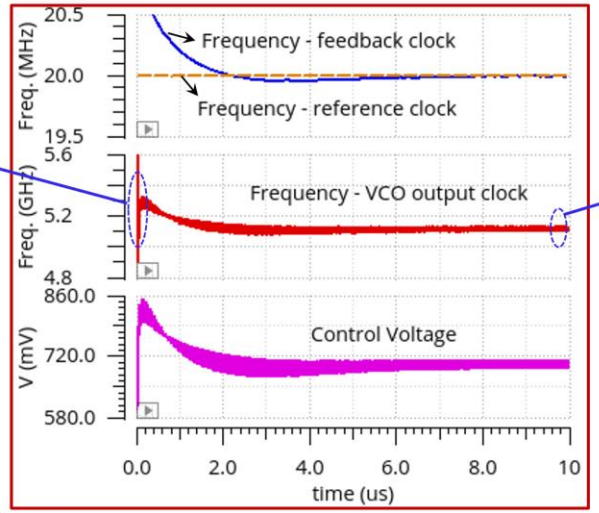
(a) Phase noise of VCO

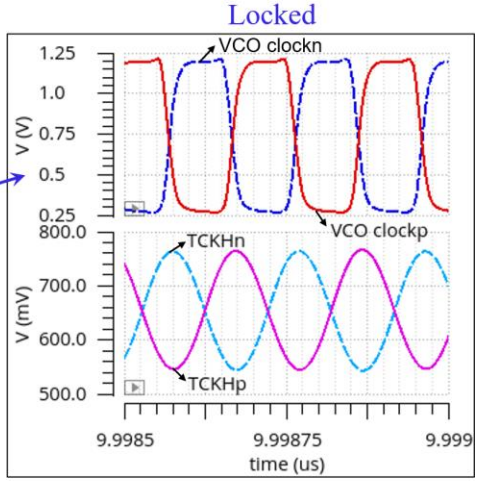


(b) Phase noise of others (PFD+CP+LPF+DIVs)



*VCO clock is the clock after several CML buffers





*TCKH is the output clock of the CML driver

(c) Transient simulations