

A 2.56 Gbps Clock and Data Recovery (CDR) ASIC

Design for High-Energy Physics Experiments

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On behalf of the ASIC design group in Central China Normal University 华中师范大学



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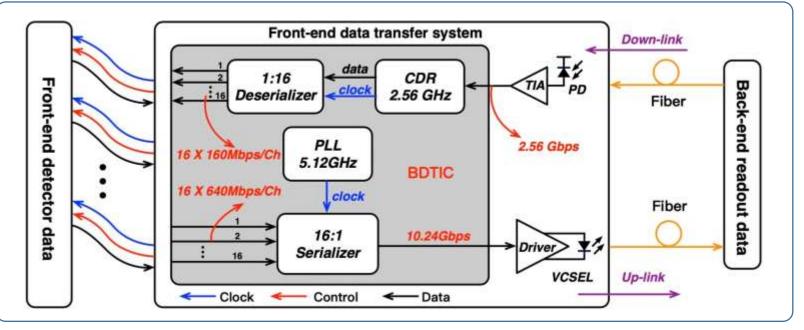
CDR ASIC design

DTest Results

Bi-directional Data Transmission system in HEP

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Simplified Bi-directional Data transmission system in HEP application

□ The proposed CDR design is one of the crucial sub-module of the

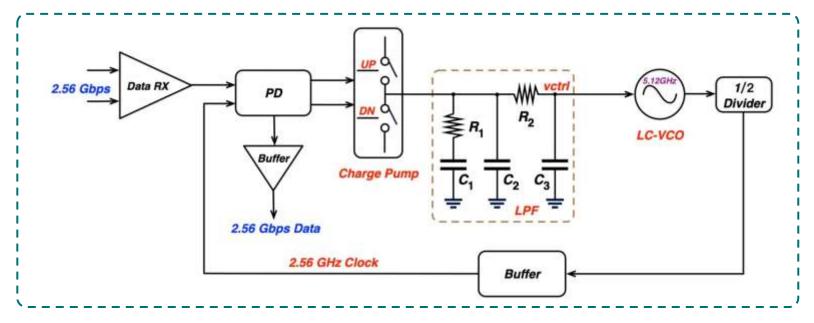
Bidirectinal Data InTerface Chip (BDTIC)

◆ work together with Xiaoting Li, Jingbo Ye's group in IHEP

□ CDR Data rate: 2.56 Gbps



CDR Overall Structure

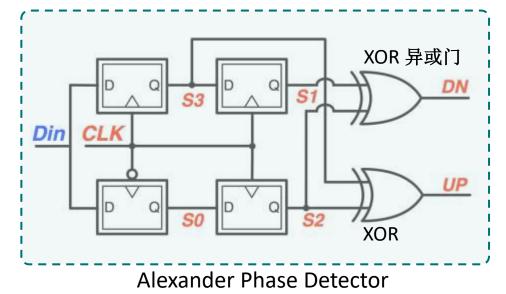


schematic block-diagram of the proposed CDR design

- □ PLL-based single-loop full-rate CDR.
- The proposed CDR is composed of high-speed Rx, Phase Detector (PD), Charge Pump (CP), Low-pass Filter (LPF) and the LC-based VCO.



Phase Detector (PD)

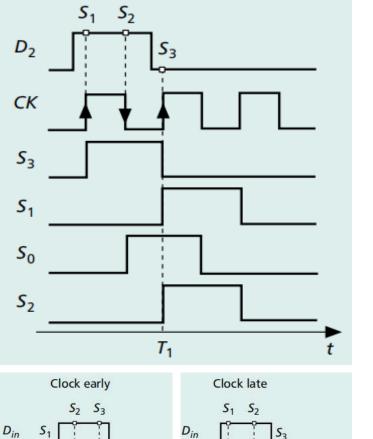


□ Full-rate Alexander PD structure

- □ Four DFFs and two XOR gates
- □ S1, S2, S3 : three data streams sampled by CK with different phases
- $\Box UP=S2\oplus S3, DN=S1\oplus S2$
- □ UP/DN: provides pulse with different widths proportional

to the phase difference between ck and data

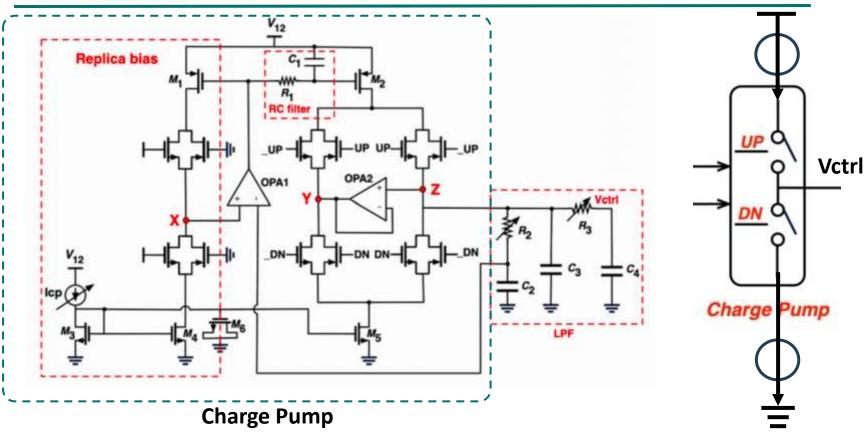
CK



CK



Charge Pump



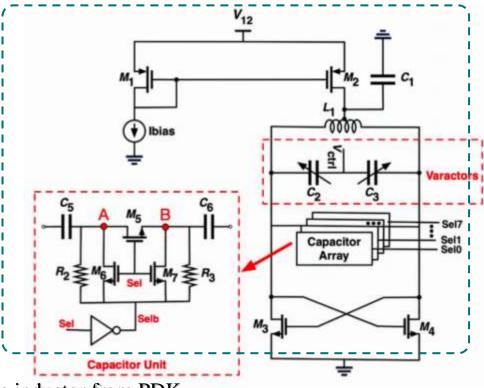
□ Use UP/DN signals as the current switch, charge and discharge the cap in LPF.

- Need accurate and precise current mirror design.
- □ Use two negative-feedback operational amplifier (OPA1, OPA2) to ensure X, Y,

Z at the same voltage during operation.



LC-based VCO



- □ L: passive inductor from PDK
- C: Varactors (C2 and C3) controlled by the Vctrl
 - + Capacitor Array (MOM cap array) configurable by SPI to adjust KVCO curve to ensure functionality in all PVT combinations
- In capacitor array unit, M5, M6, M7 related switch, reduce equivalent resistor of the cap to get higher Q factor.



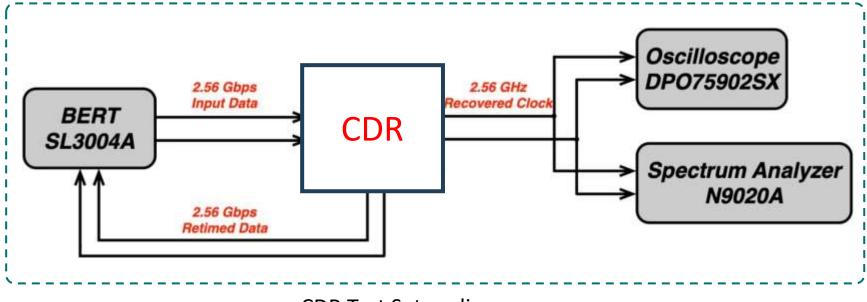
CDR ASIC design

Test Results

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CDR Test Set-up Diagram

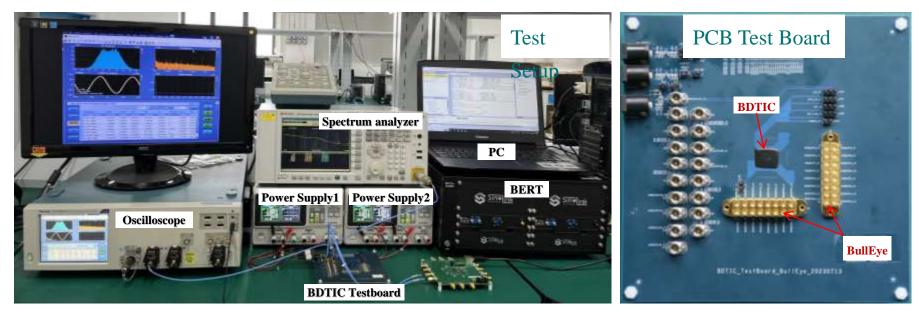


CDR Test Setup diagram

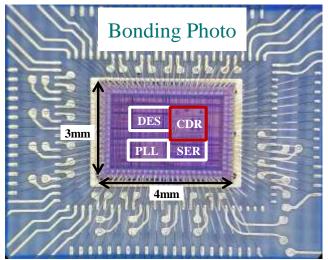
- BERT provides 2.56 Gbps PRBS7 data with a differential amplitude of 200mV.
- CDR outputs recovered clock, sent to the oscilloscope for jitter analysis, and sent to the spectrum analyzer for the phase noise analysis.
- CDR also outputs retimed data (resample the input data with recovered clock), sent to BERT for BER test.



CDR Test Pictures



- □ Process: SMIC55nm CMOS RF
- **\Box** Chip Size: 3 mm × 4 mm
- □ CDR core size: 1000µm × 700µm
- CDR power consumption:200 mW including Rx and CML driver





CDR Test Results

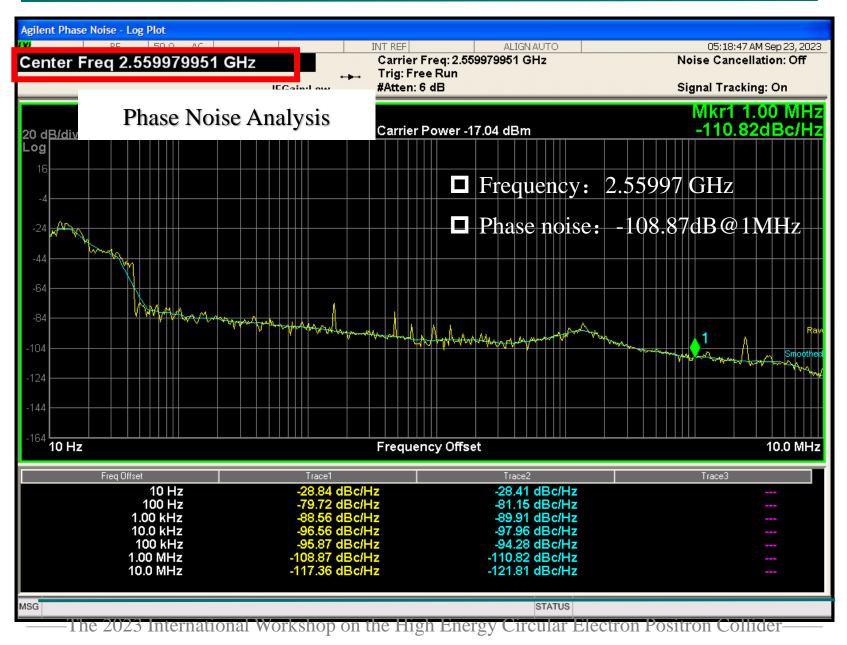
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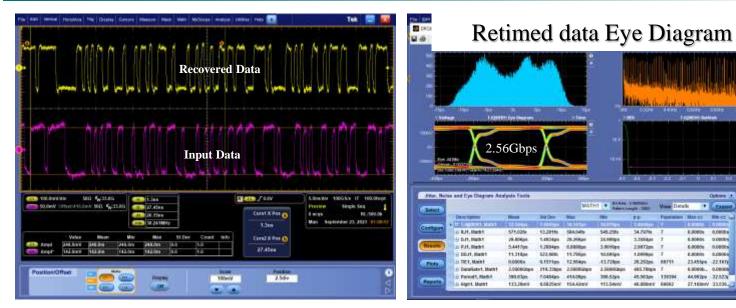


CDR Test Results





CDR Test Results



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Retimed 2.56 Gbps data output

12

Bill CT

0.0808+

0.00054

0.0000

0.08004

from the CDR

- □ Data rate: 2.56 Gbps
- \square RMS Jitter: 571.02 fs
- □ Total Jitter: 32.54 ps
- **BER runing time:** 20 minutes

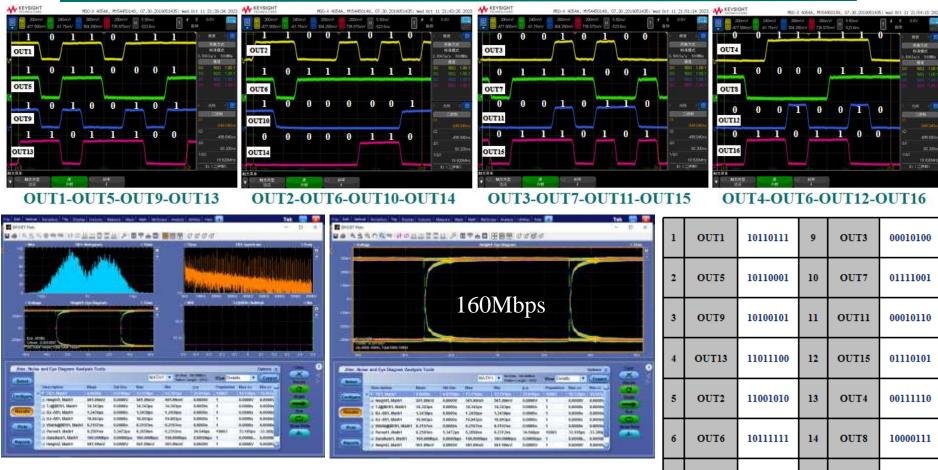
not a single error





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CDR + Deserializer Test Results



1: 16 Deserializer uses the 2.56 GHz recovered clock and retimed data from CDR

□ The logic function of the deserializer is proved in the test.

OUT10

OUT14

8

10000001

00000110

15

16

OUT12

OUT16

00010010



THANKS!