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A 2.56 Gbps Clock and Data Recovery (CDR) ASIC Design for High-Energy Physics Experiments

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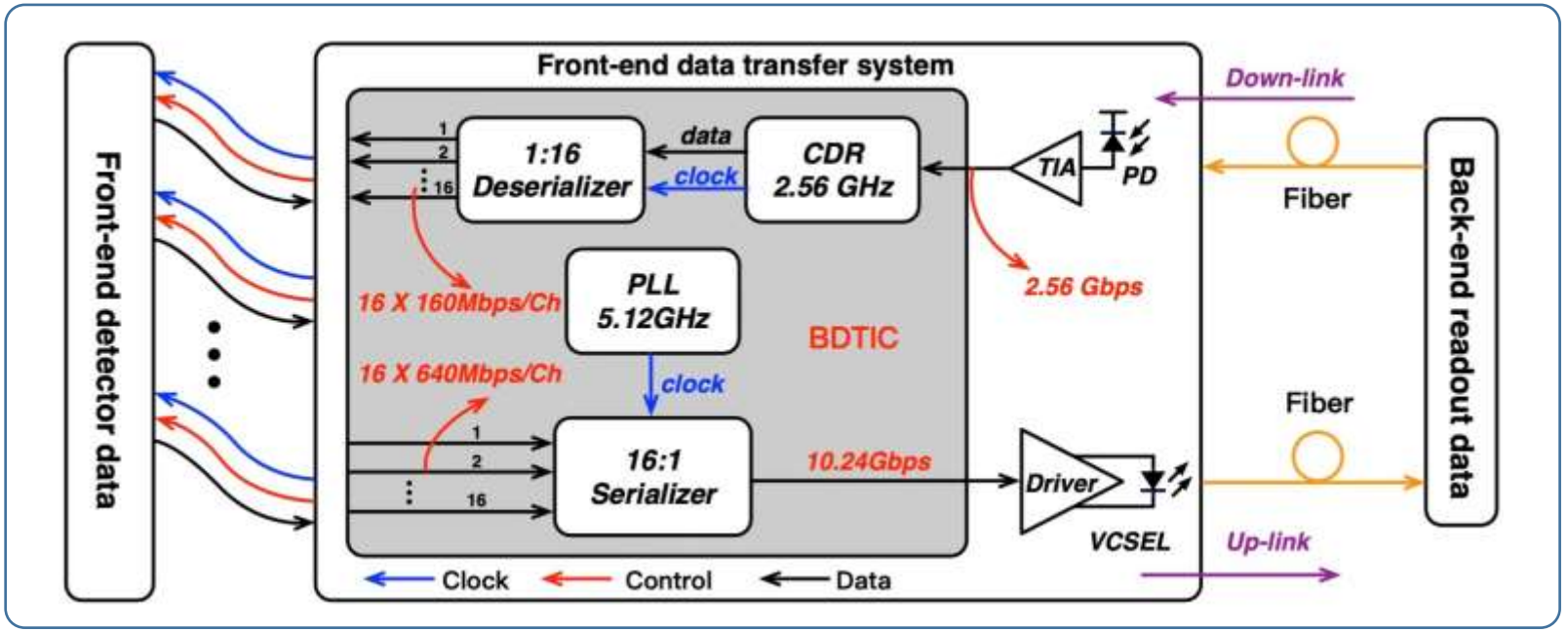
Data Transmission system

- CDR ASIC design
- Test Results

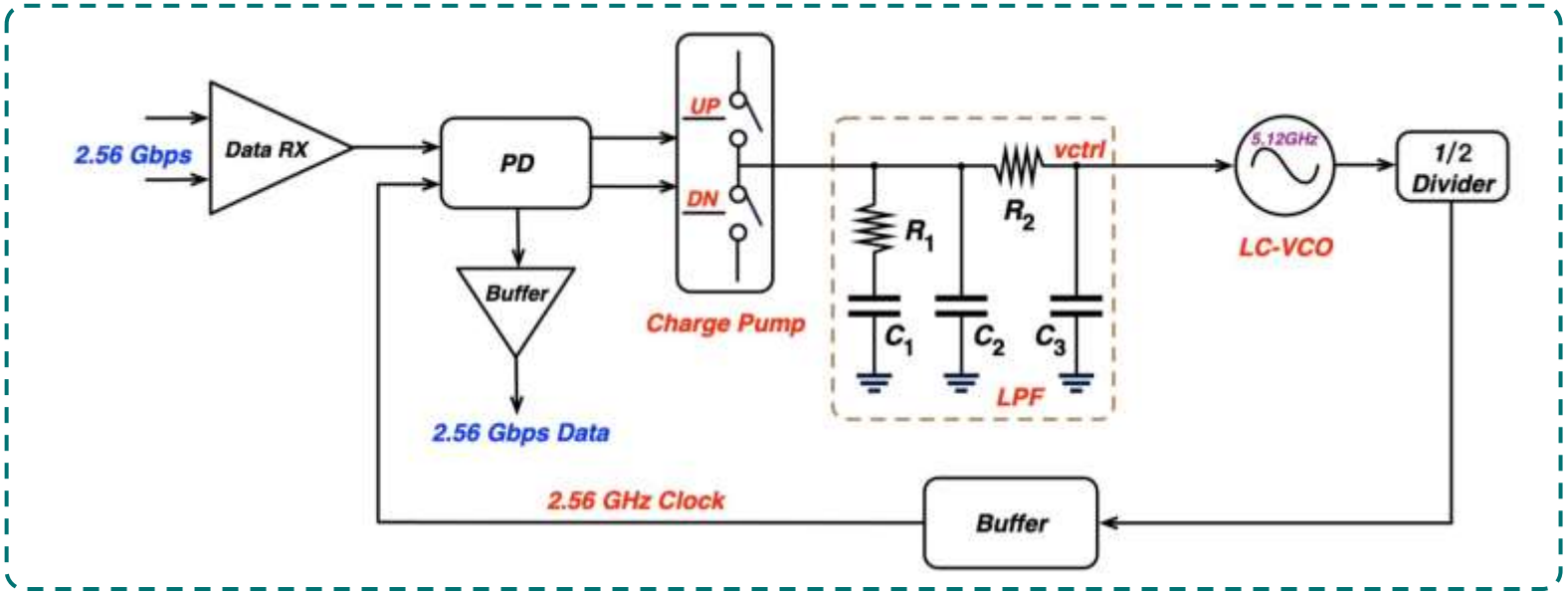
Bi-directional Data Transmission system in HEP



Simplified Bi-directional Data transmission system in HEP application

- The proposed CDR design is one of the crucial sub-module of the Bidirectinal Data InTerface Chip (BDTIC)
  - work together with Xiaoting Li, Jingbo Ye's group in IHEP
- CDR Data rate: 2.56 Gbps

CDR Overall Structure

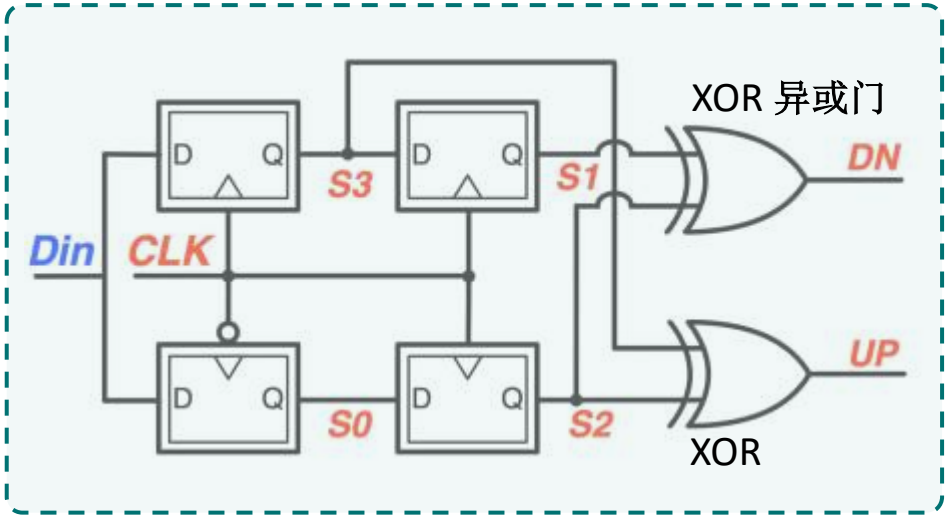


schematic block-diagram of the proposed CDR design

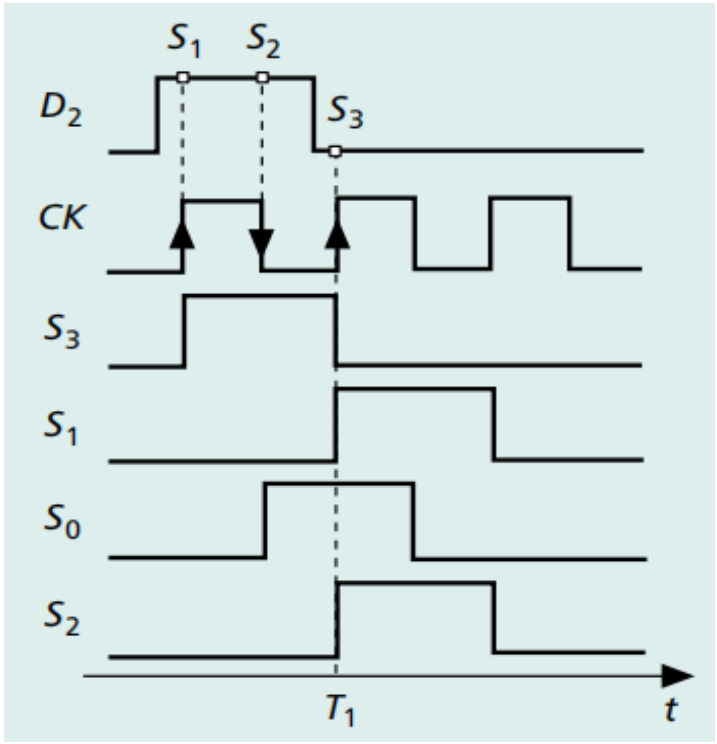
- PLL-based single-loop full-rate CDR.

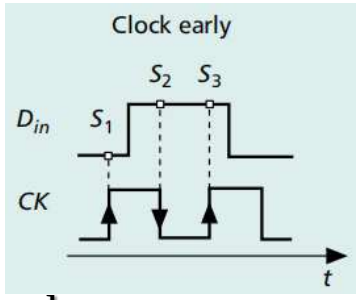
- The proposed CDR is composed of high-speed Rx, Phase Detector (PD), Charge Pump (CP), Low-pass Filter (LPF) and the LC-based VCO.

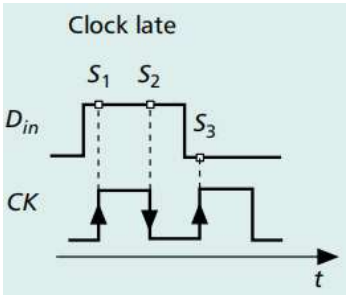
Phase Detector (PD)



Alexander Phase Detector

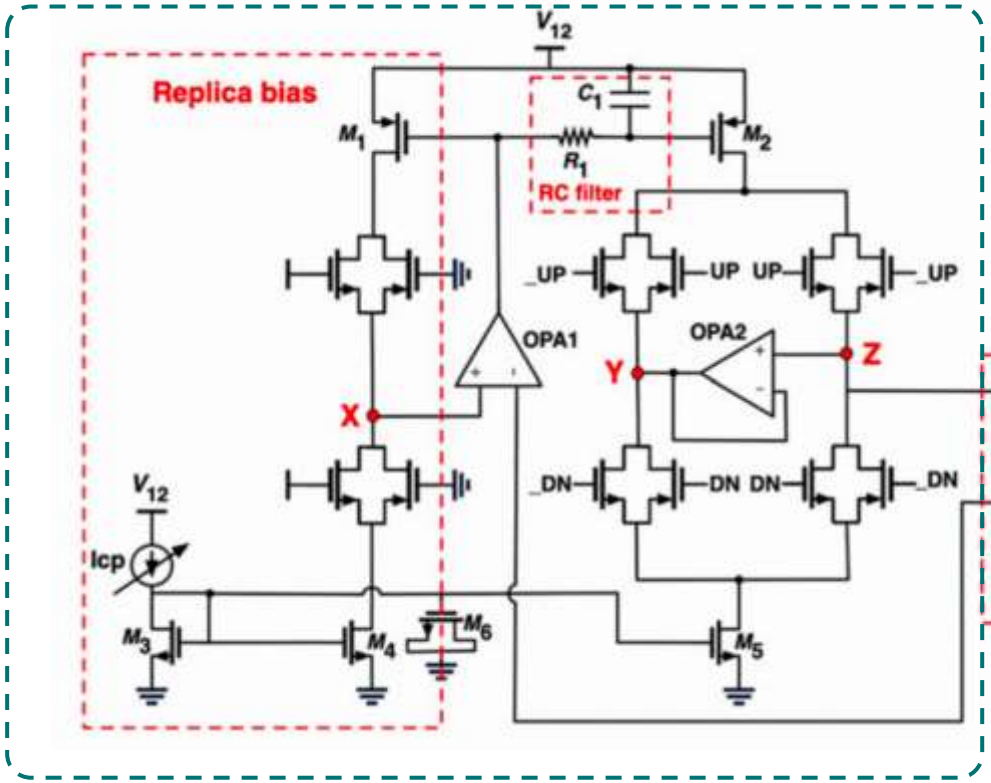




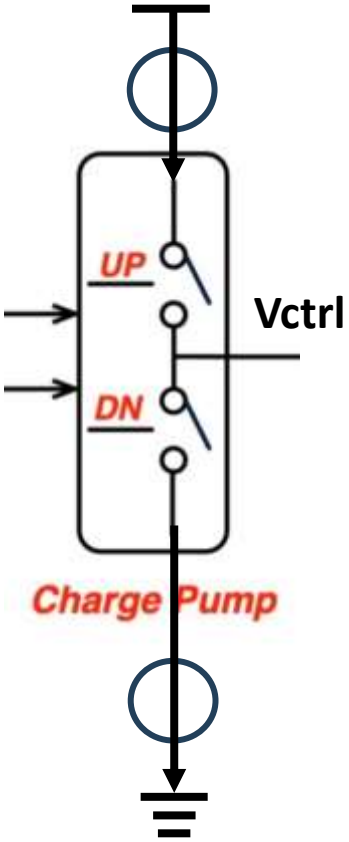


- Full-rate Alexander PD structure
- Four DFFs and two XOR gates
- S1, S2, S3 : three data streams sampled by CK with different phases
- UP=S2⊕S3, DN=S1⊕S2
- UP/DN: provides pulse with different widths proportional to the phase difference between ck and data

Charge Pump

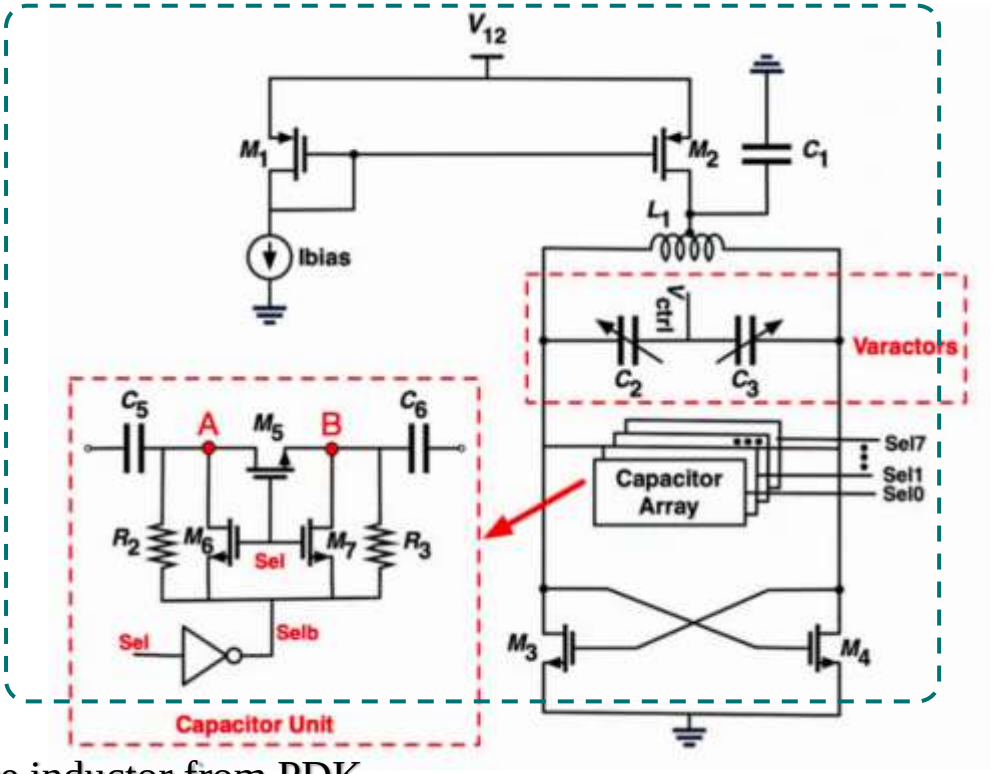


Charge Pump



- Use UP/DN signals as the current switch, charge and discharge the cap in LPF.
- Need accurate and precise current mirror design.
- Use two negative-feedback operational amplifier (OPA1, OPA2) to ensure X, Y, Z at the same voltage during operation.

LC-based VCO

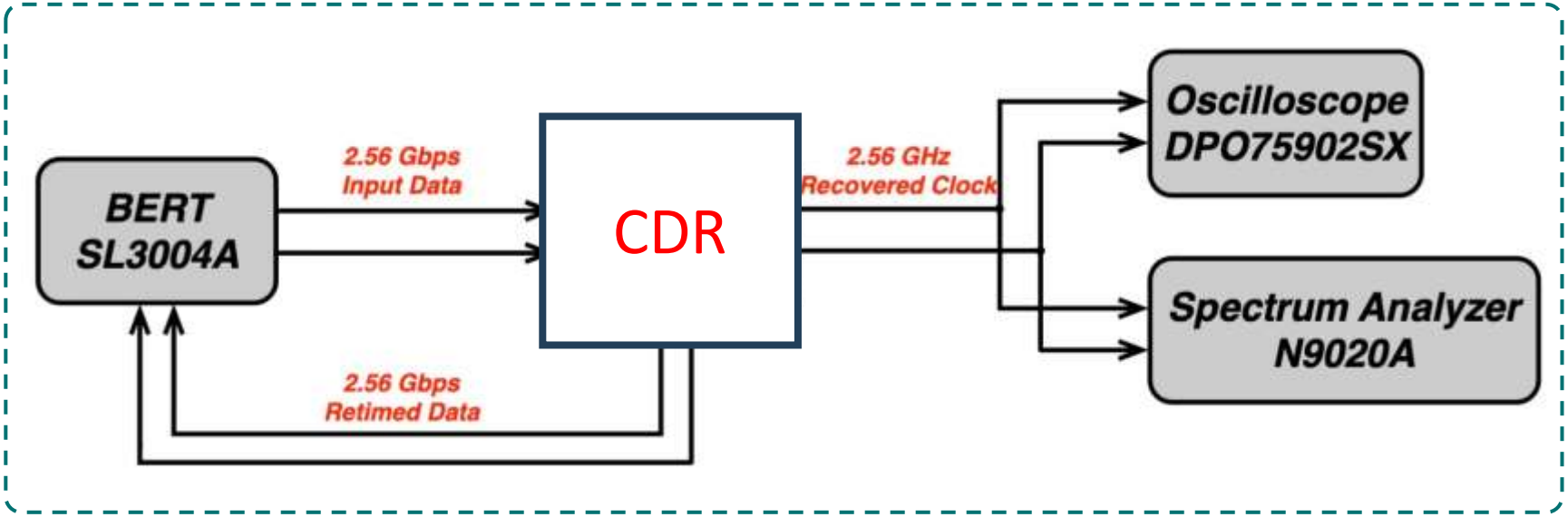


- L: passive inductor from PDK
- C: Varactors (C2 and C3) controlled by the Vctrl
  + Capacitor Array (MOM cap array) configurable by SPI to adjust KVCO curve to ensure functionality in all PVT combinations
- In capacitor array unit, M5, M6, M7 related switch, reduce equivalent resistor of the cap to get higher Q factor.

Data Transmission system

- CDR ASIC design
- Test Results

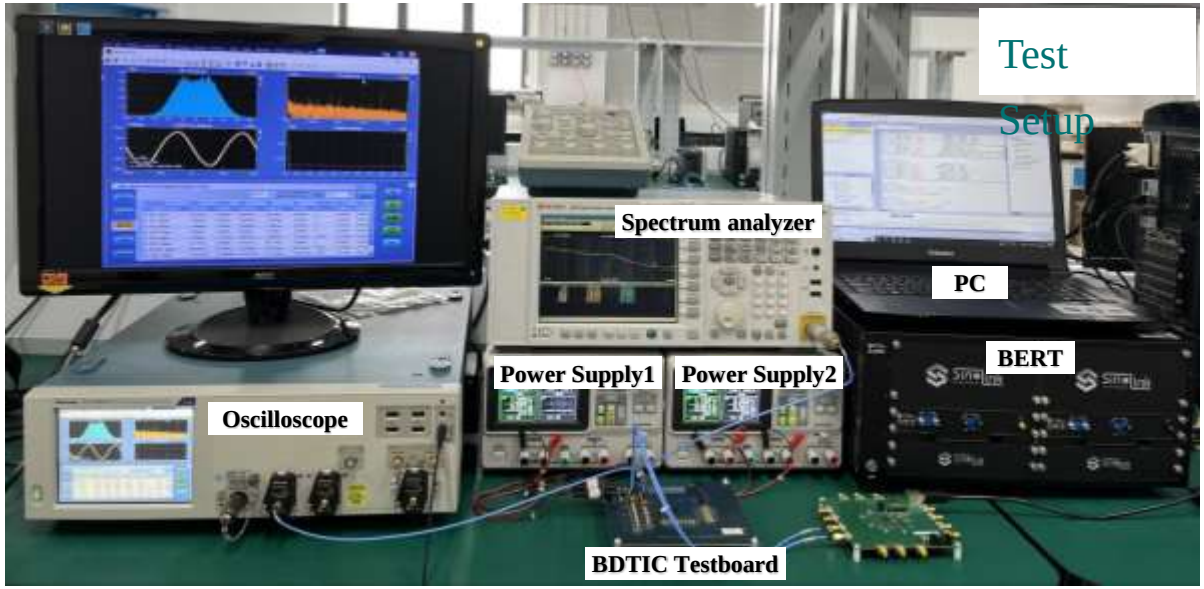
CDR Test Set-up Diagram

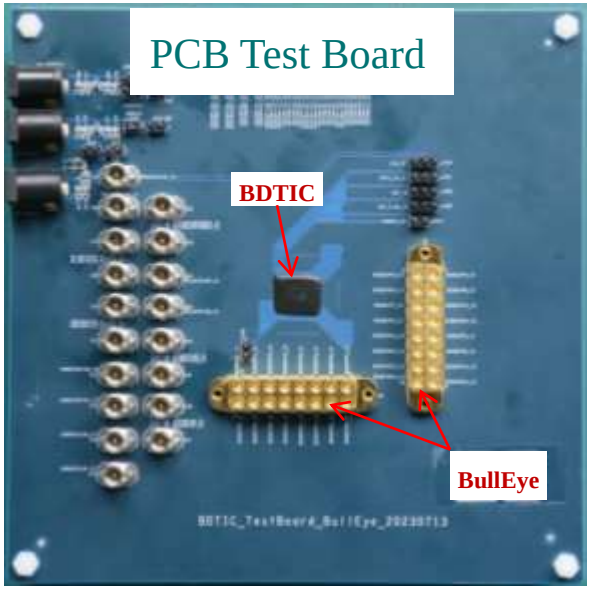


CDR Test Setup diagram

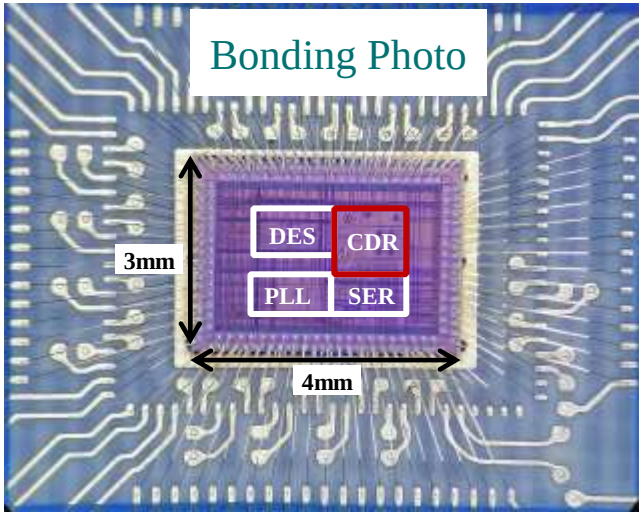
- BERT provides 2.56 Gbps PRBS7 data with a differential amplitude of 200mV.
- CDR outputs recovered clock, sent to the oscilloscope for jitter analysis, and sent to the spectrum analyzer for the phase noise analysis.
- CDR also outputs retimed data (resample the input data with recovered clock), sent to BERT for BER test.

CDR Test Pictures

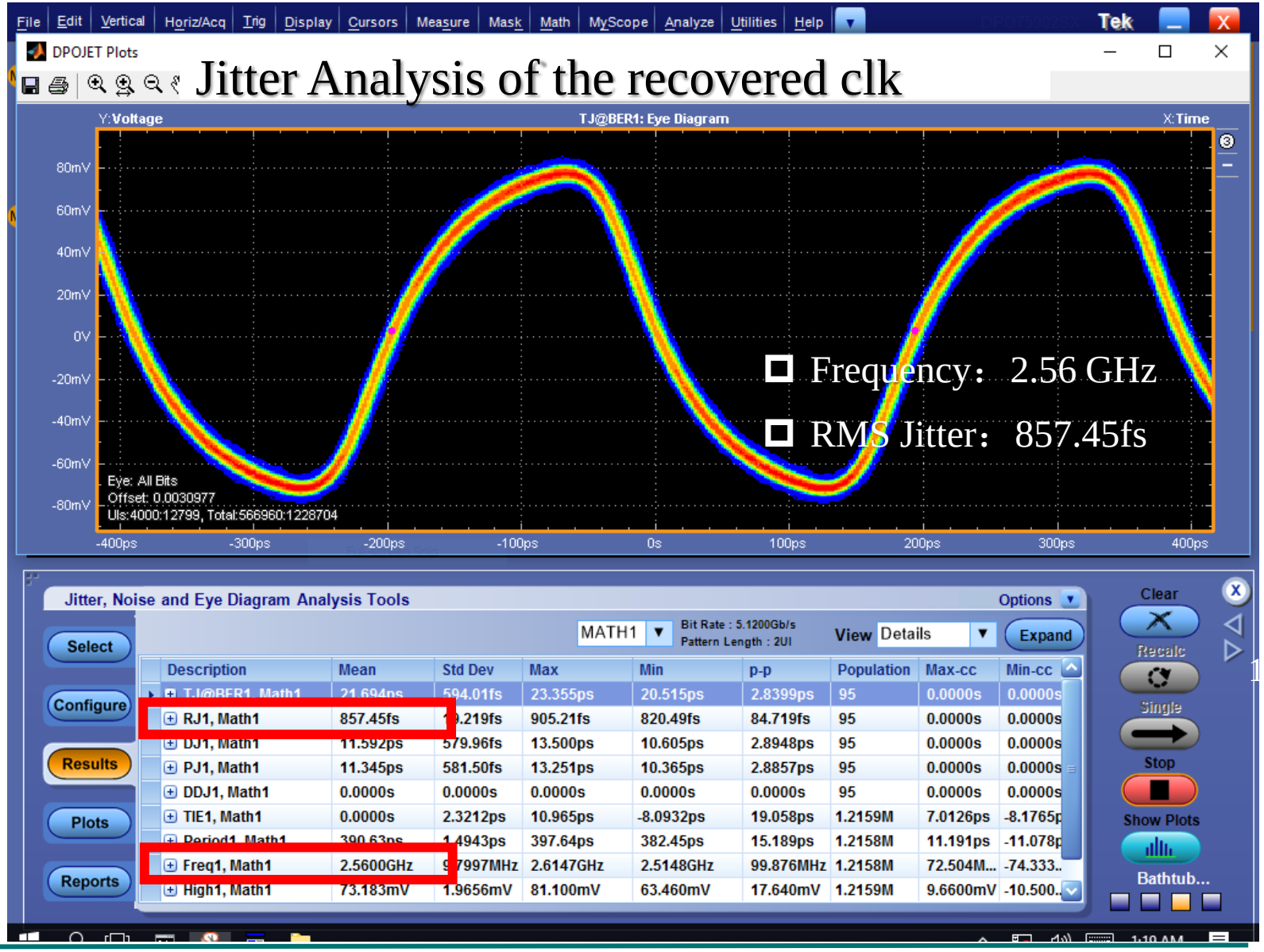




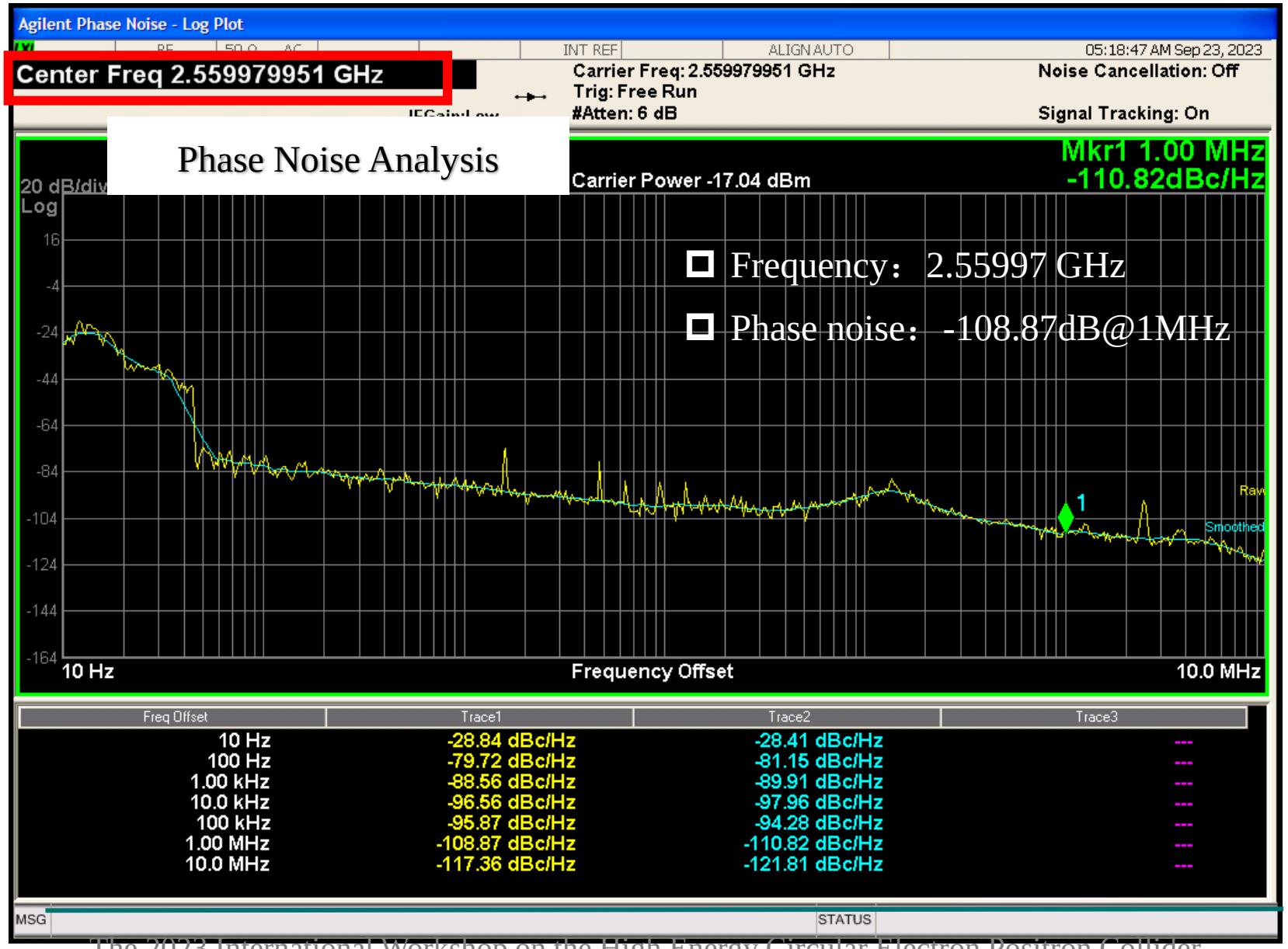
- Process：SMIC55nm CMOS RF
- Chip Size：3 mm × 4 mm
- CDR core size: 1000μm × 700μm
- CDR power consumption:200 mW
  including Rx and CML driver



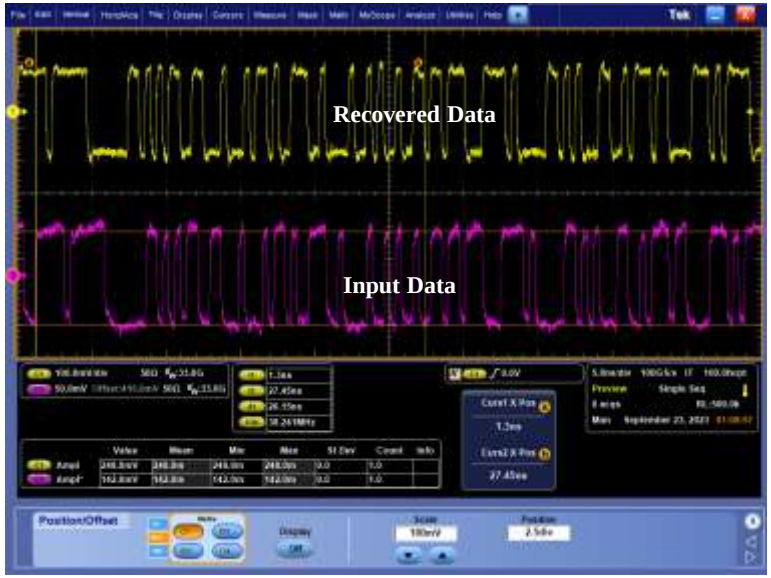
CDR Test Results

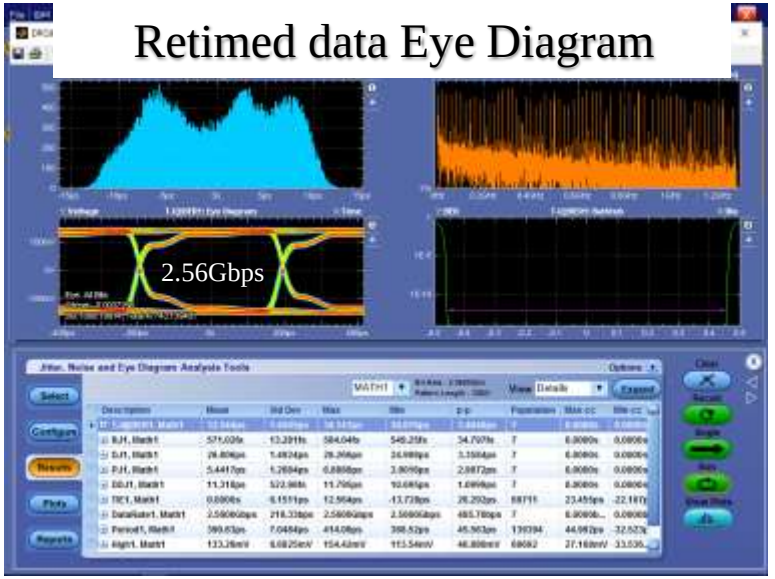


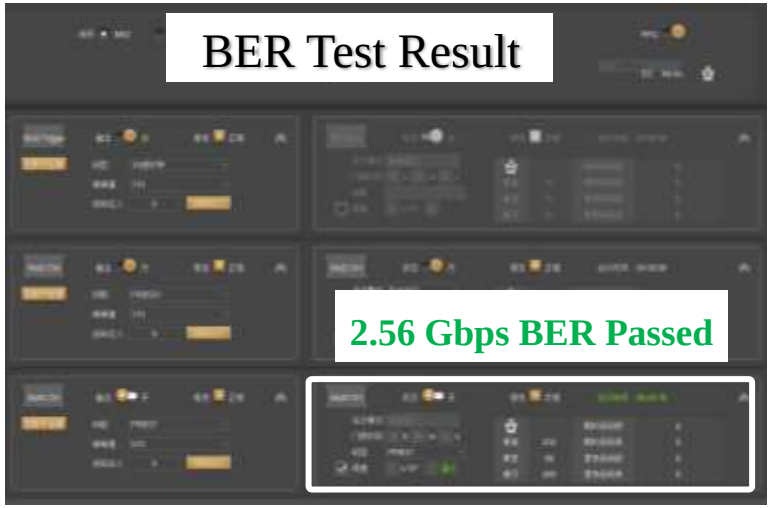
CDR Test Results



CDR Test Results



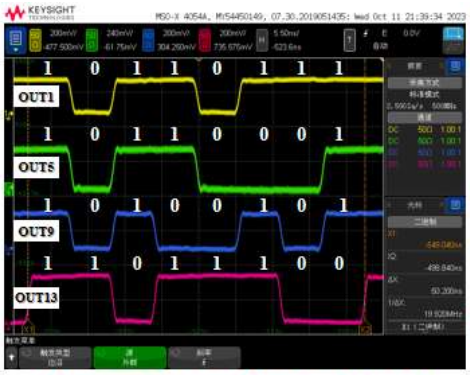




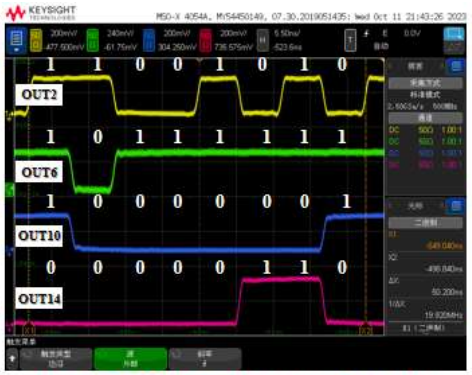
Retimed 2.56 Gbps data output from the CDR

- Data rate： 2.56 Gbps
- RMS Jitter： 571.02 fs
- Total Jitter： 32.54 ps
- BER runing time： 20 minutes not a single error

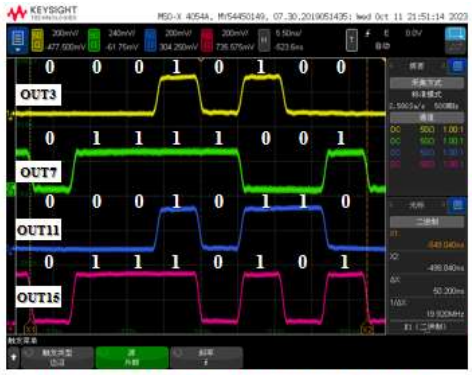
CDR + Deserializer Test Results



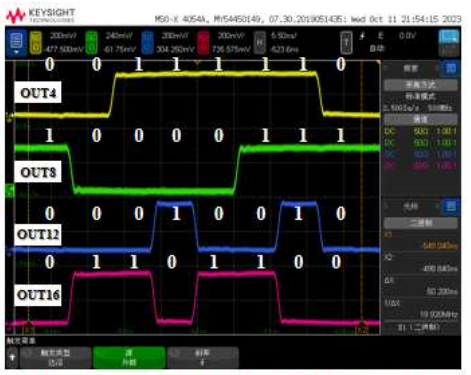
OUT1-OUT5-OUT9-OUT13



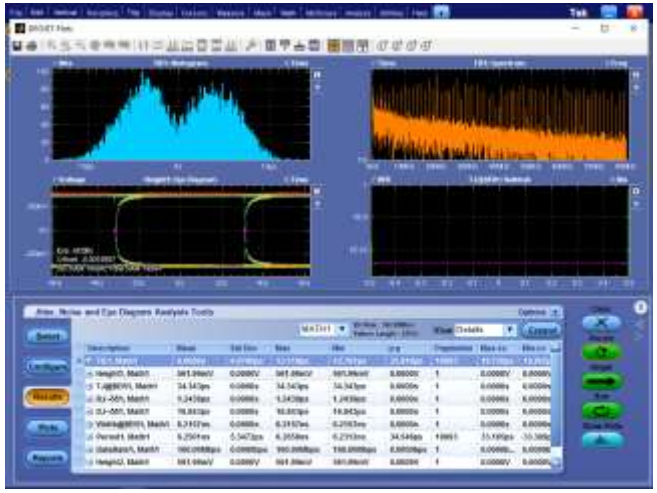
OUT2-OUT6-OUT10-OUT14



OUT3-OUT7-OUT11-OUT15



OUT4-OUT6-OUT12-OUT16



1	OUT1	10110111	9	OUT3	00010100
2	OUT5	10110001	10	OUT7	01111001
3	OUT9	10100101	11	OUT11	00010110
4	OUT13	11011100	12	OUT15	01110101
5	OUT2	11001010	13	OUT4	00111110
6	OUT6	10111111	14	OUT8	10000111
7	OUT10	10000001	15	OUT12	00010010
8	OUT14	00000110	16	OUT16	01101100

- 1: 16 Deserializer uses the 2.56 GHz recovered clock and retimed data from CDR
- The logic function of the deserializer is proved in the test.

THANKS!