Research Progress on Multichannel, High Precision TDC Based on VDL Technology

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/01

Introduction

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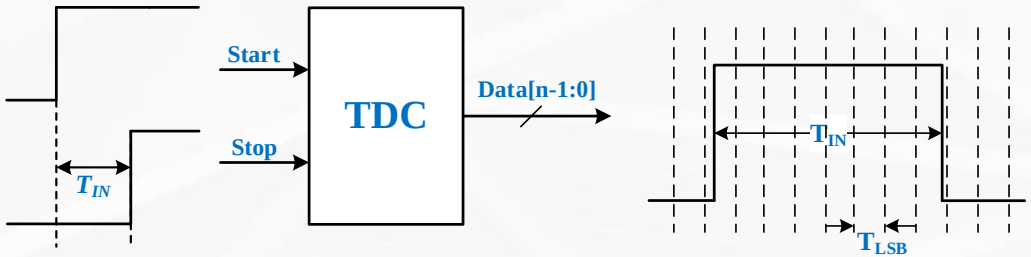
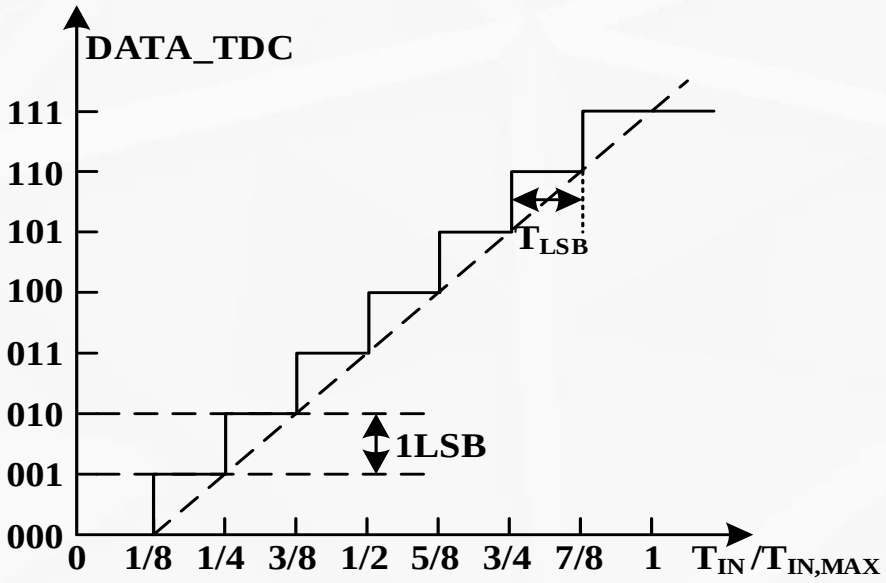
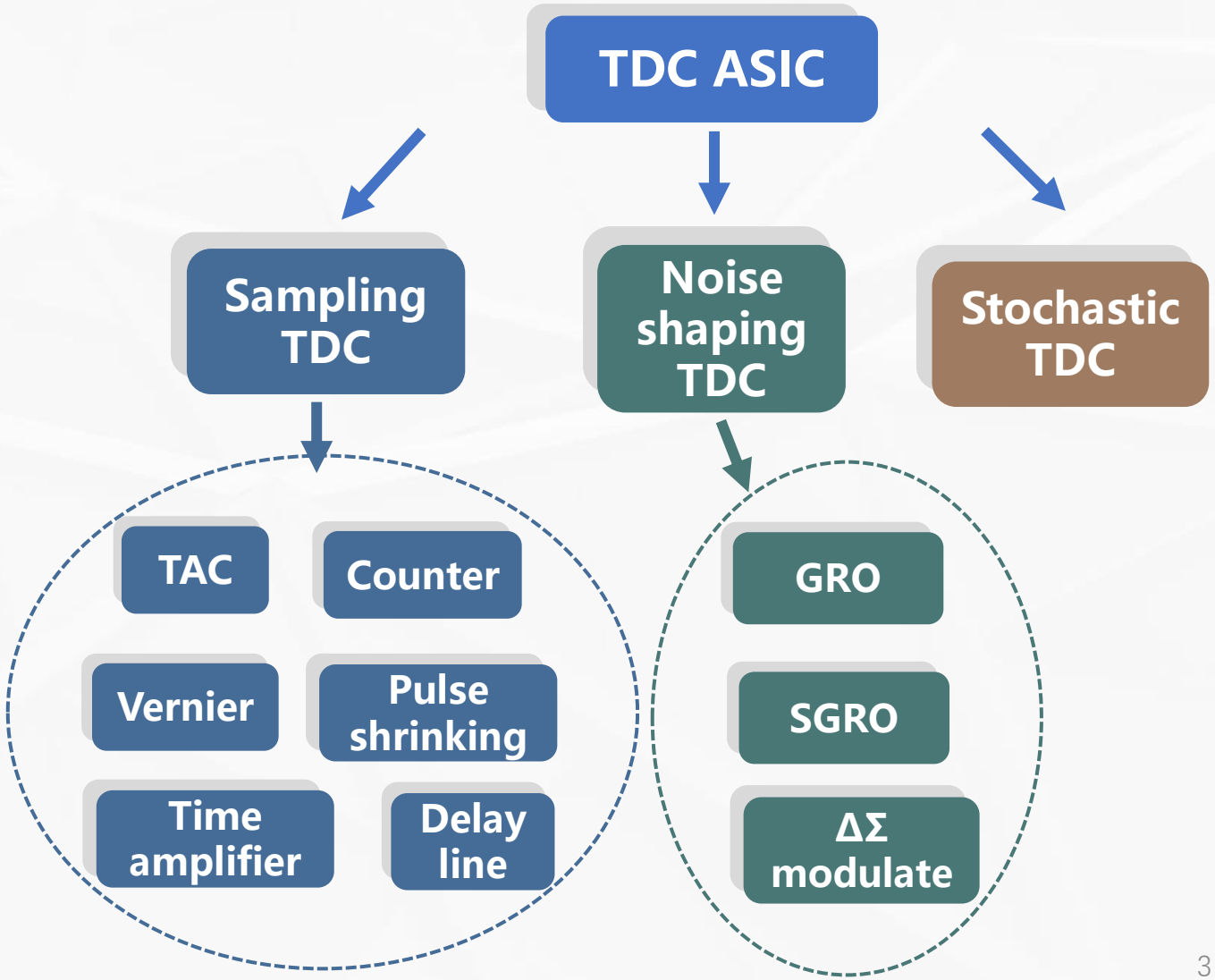
Principles and Classification of TDC

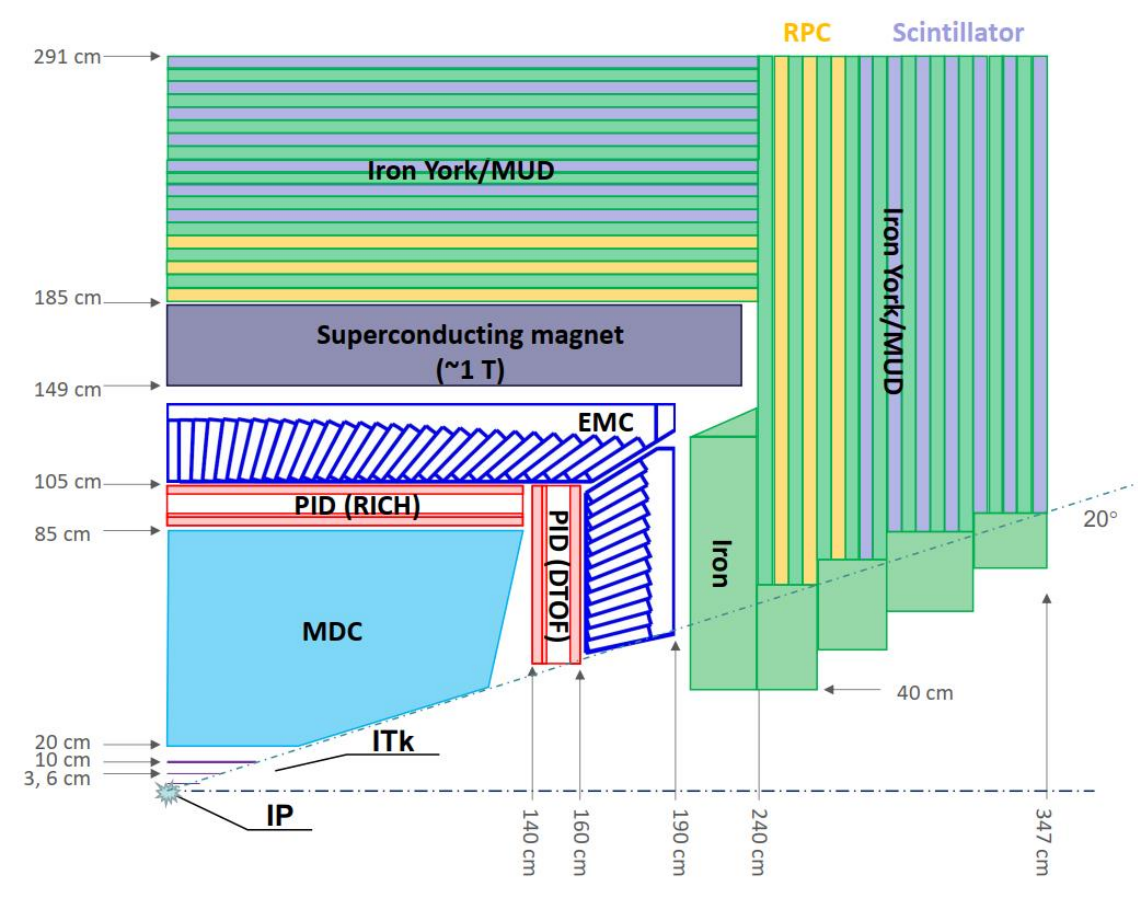




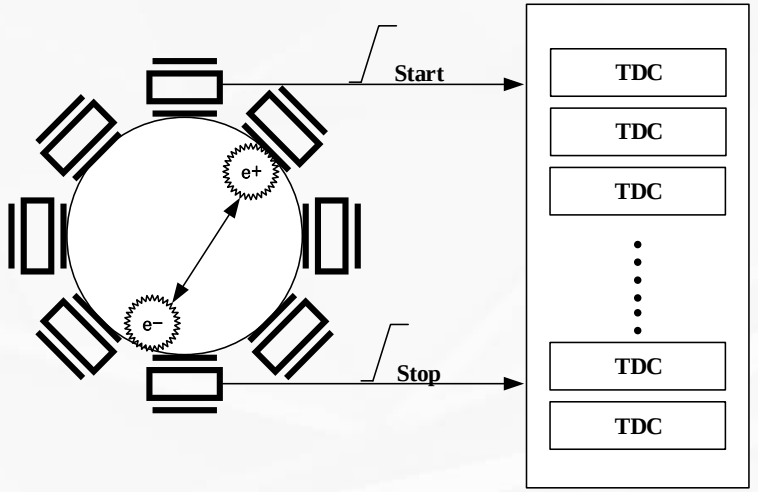
$$T_{IN} = T_{LSB} \times DATA\_TDC$$



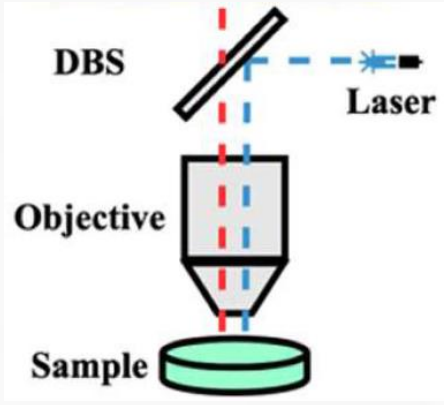
Applications in Radiation Detection



- High energy physical experiment (e. g. STCF)



- Positron emission tomography (PET)



- Fluorescence lifetime imaging microscopy (FLIM)

Architectural Considerations

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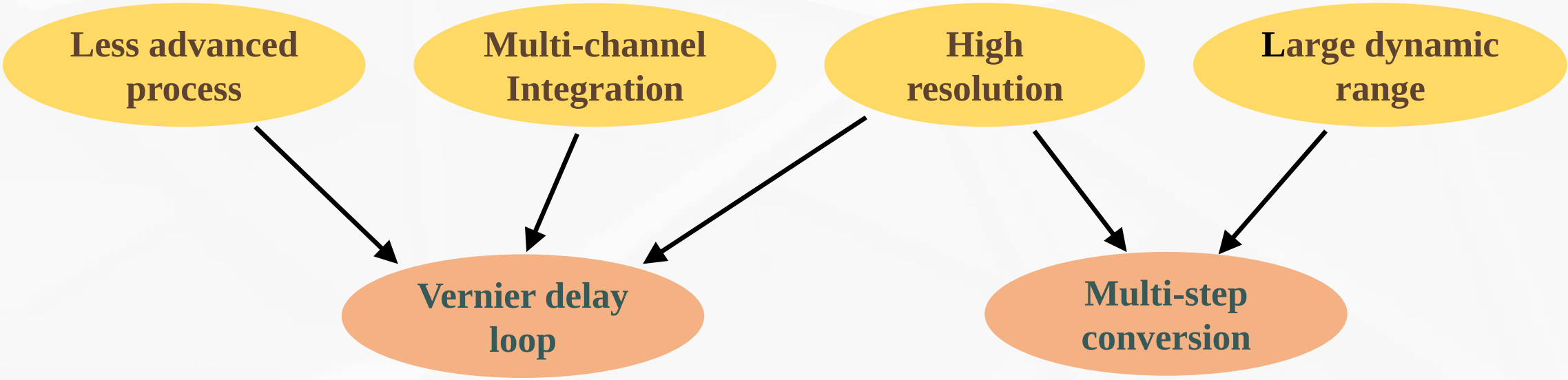
Design requirements (for the EMC in STCF)	
Process	CMOS 180 nm
Number of channels	≥ 6
Resolution	< 100 ps
Dynamic range	> 1 μs
Linearity	DNL < 1 LSB, INL < 1.5 LSB
Sample rate	> 4 MHz



/02

An 8-channel 3-step VDL based TDC ASIC designed in 2022

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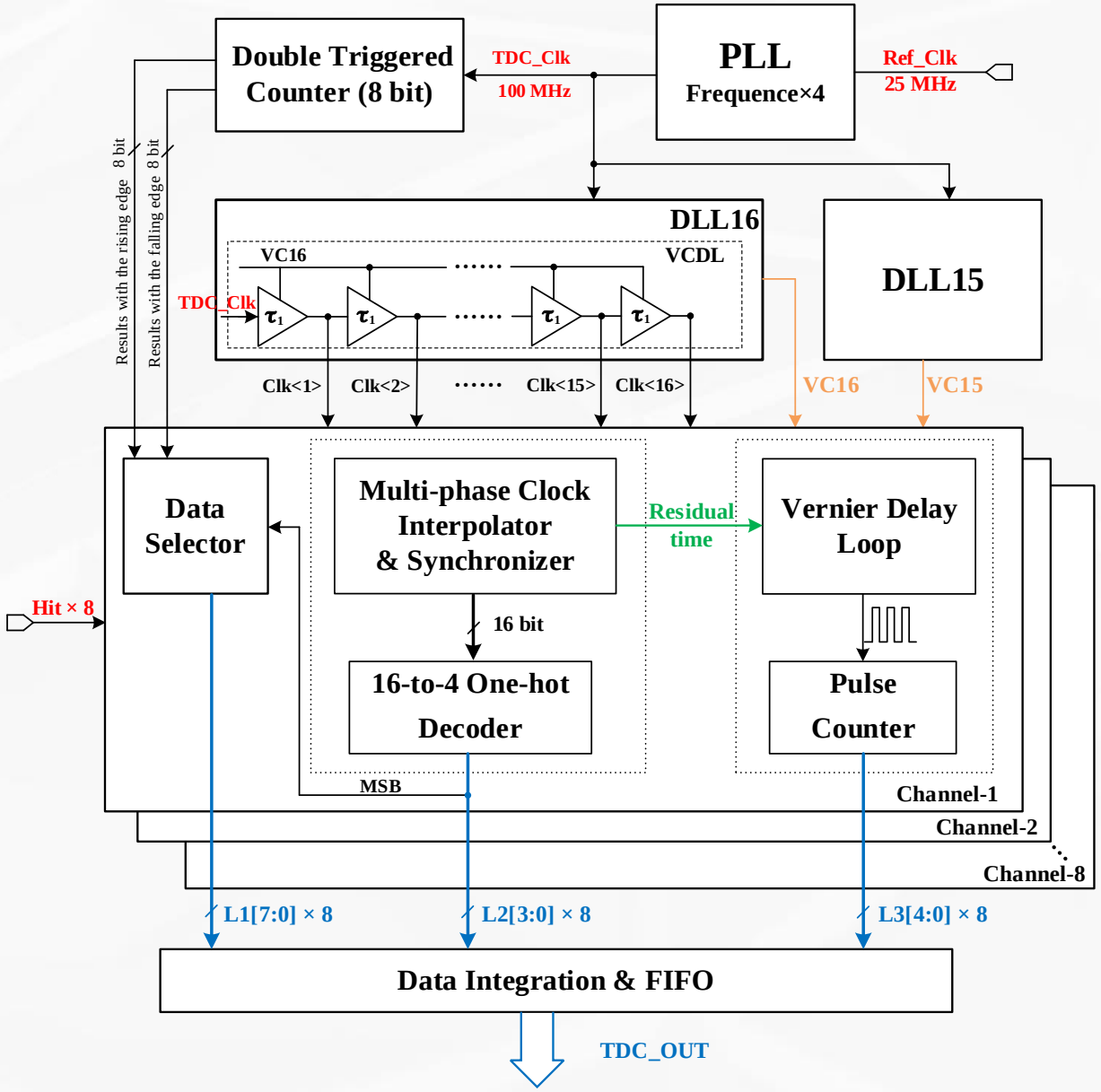
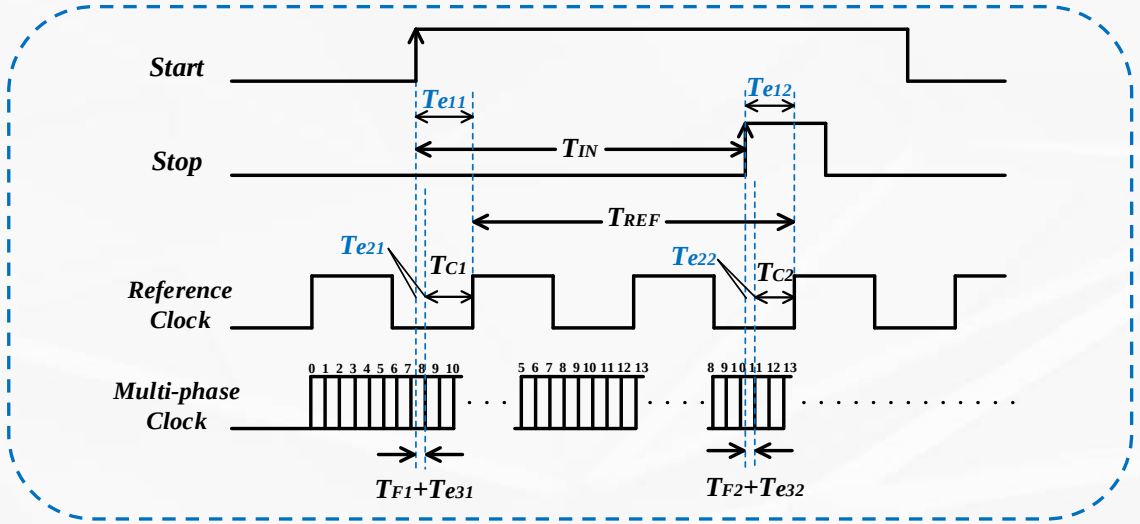
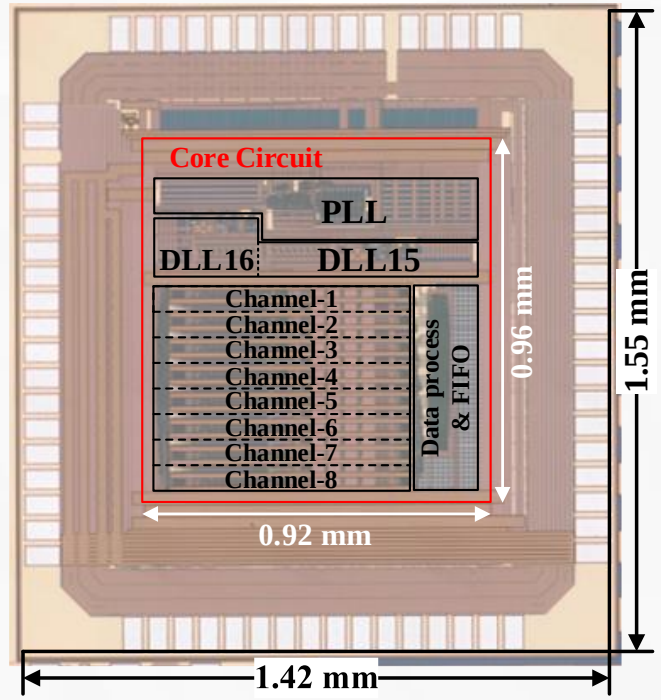
The Structure and Working Principle







The Design of DLL and PLL

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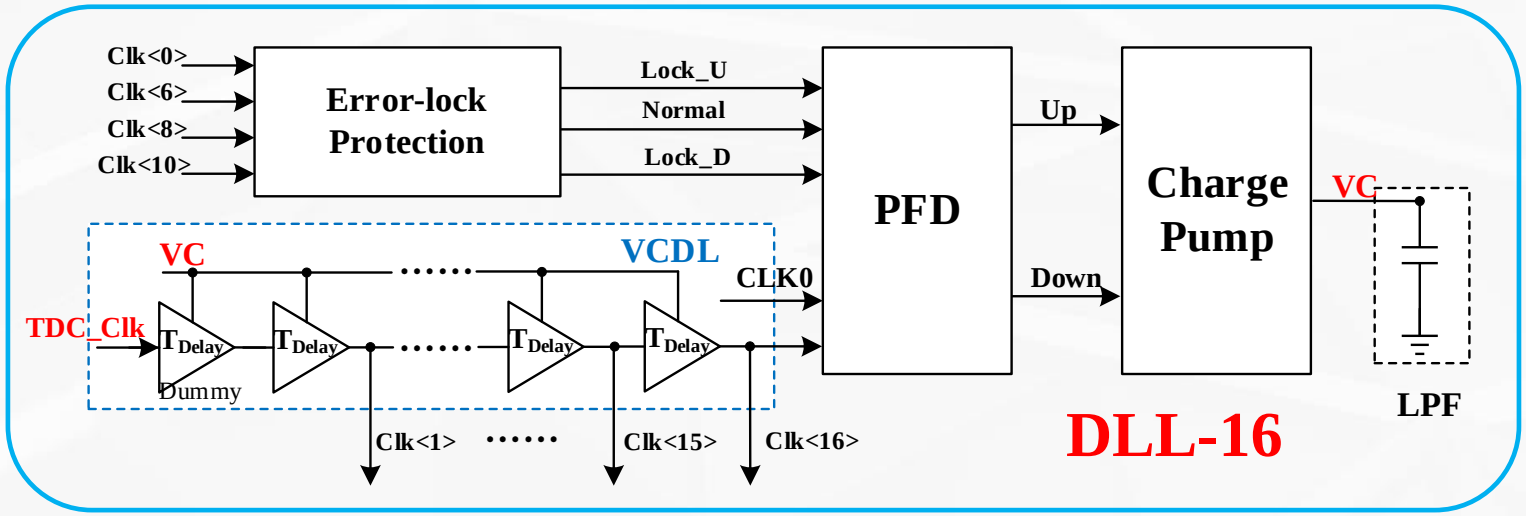
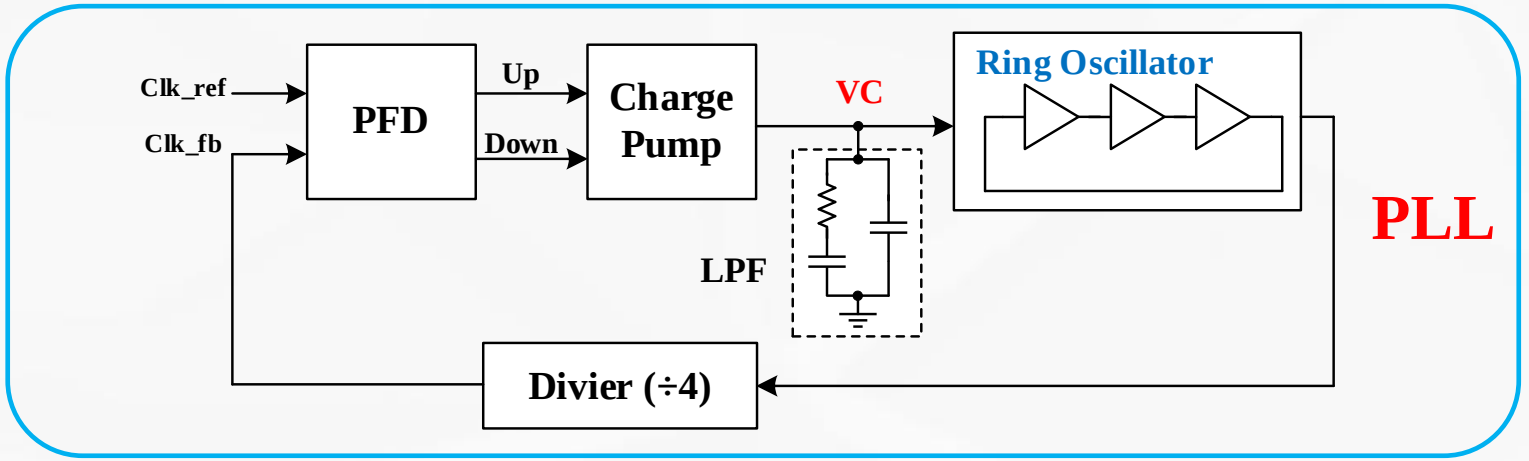
$$LSB = \frac{T_{Ref}}{n-1} - \frac{T_{Ref}}{n}$$

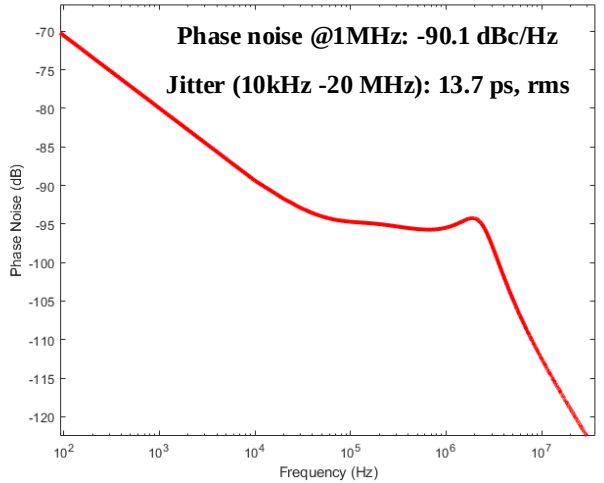
n =16
T_{Ref} = 10ns
LSB = 41.7 ps

Power consumption $\propto 1/T_{Ref}$



DLL Performance	
Operating frequency range	45 – 200 MHz
Error-lock protection	Yes
Locked phase error	< 10 ps
Jitter (rms)	< 5 ps





The Design of 3-Step TDC

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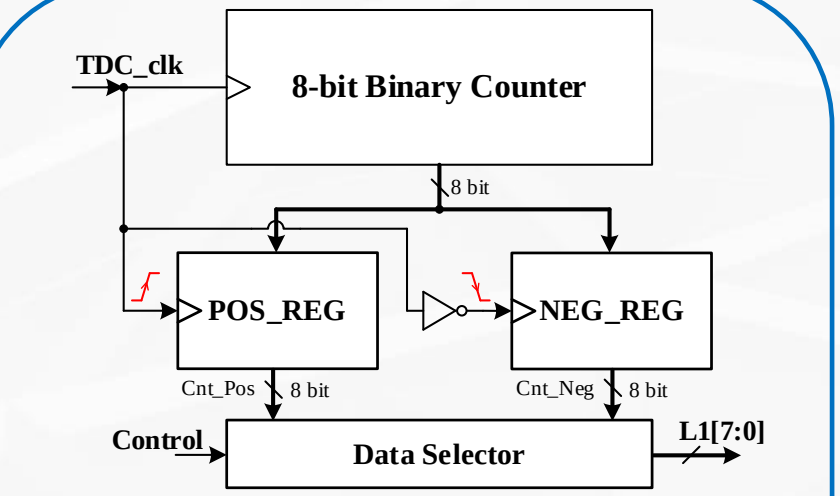
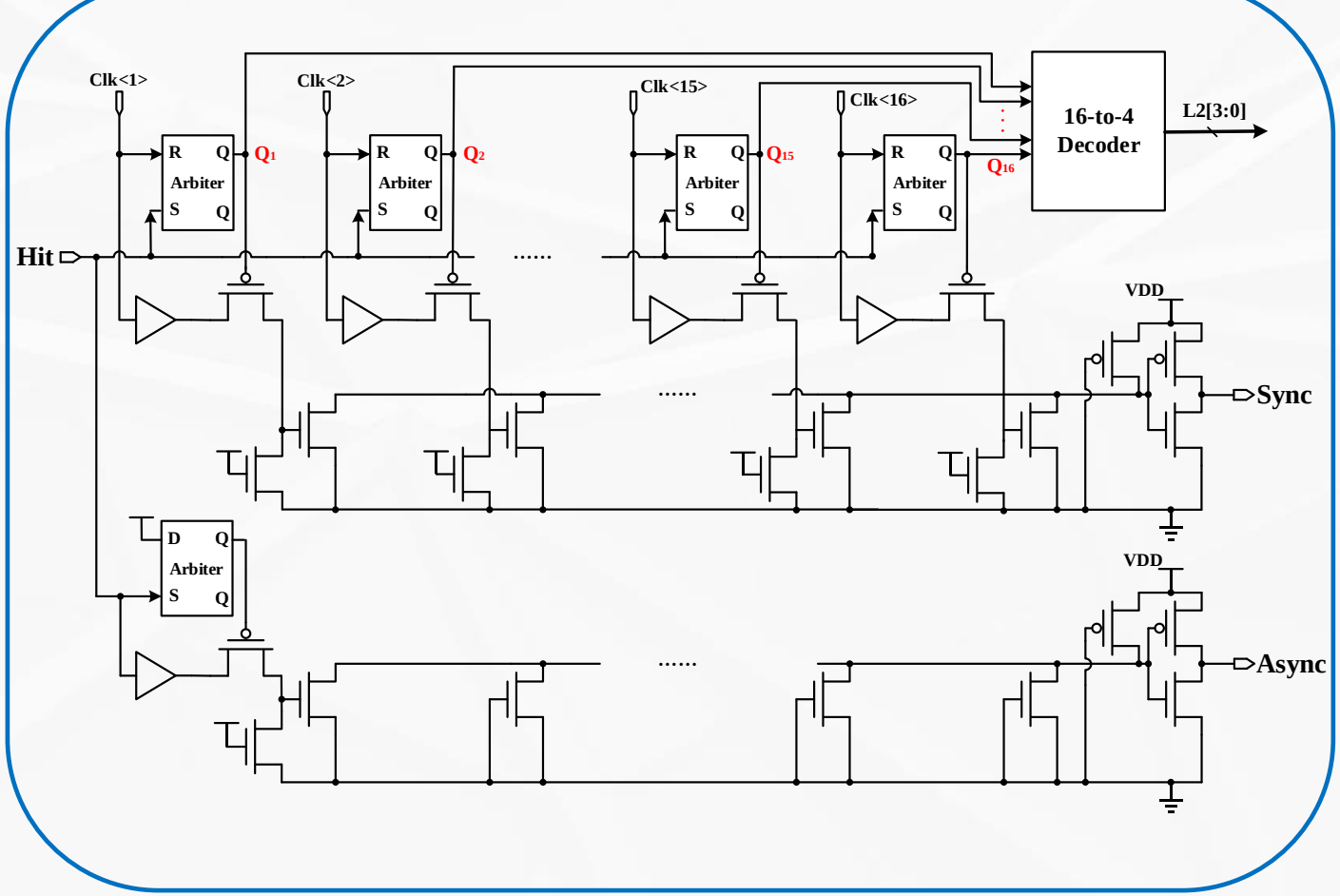
- The 1st step: Double Triggered Counter.



- The 2nd step: Multi-phase Clock Interpolator & Synchronizer



The Design of 3-Step TDC

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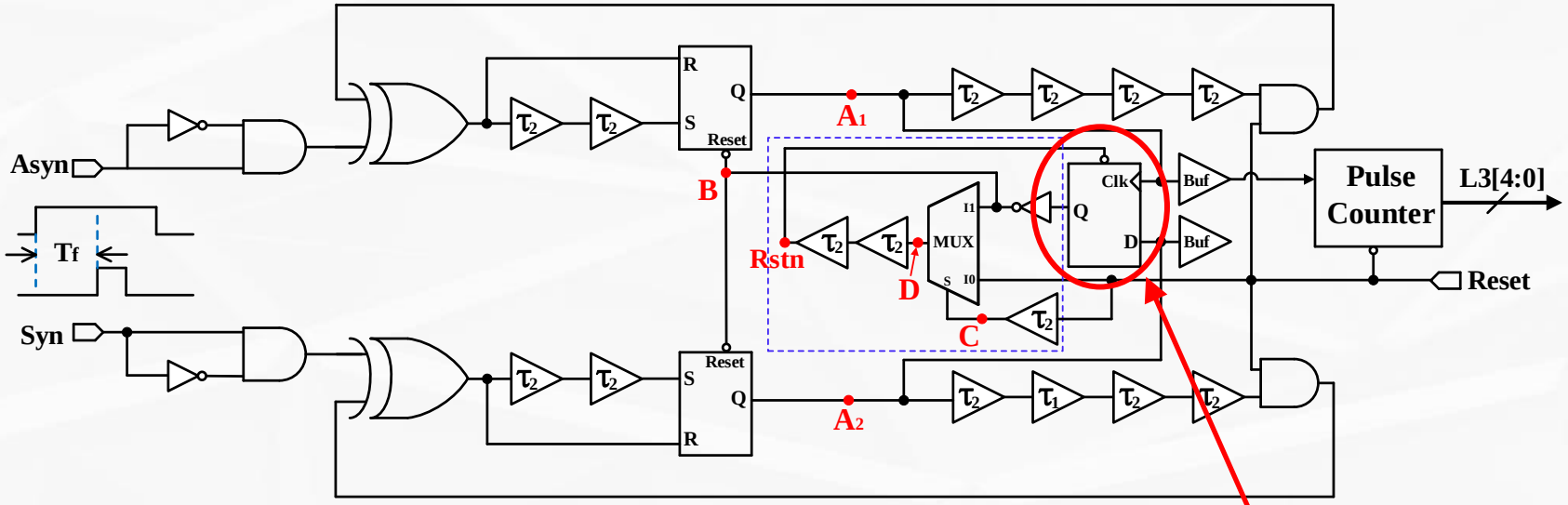
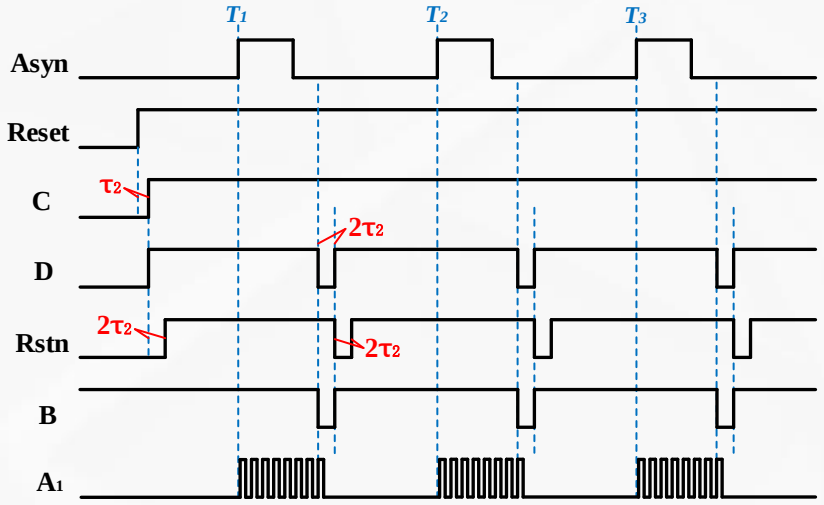
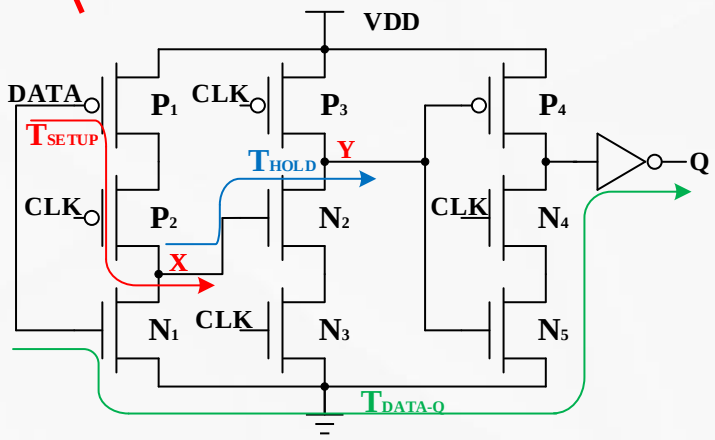
- The 3rd Step: Vernier Delay Loop







- ✓ Reduced mismatch—— improved linearity
- ✓ Automatic reset in single channel.
- ✓ Recovery time: 3.7 ns
- ✓ Dead time (max): 51.4 ns.
- ✓ Counting rate (min): ~19.5 MHz.

Testing Results

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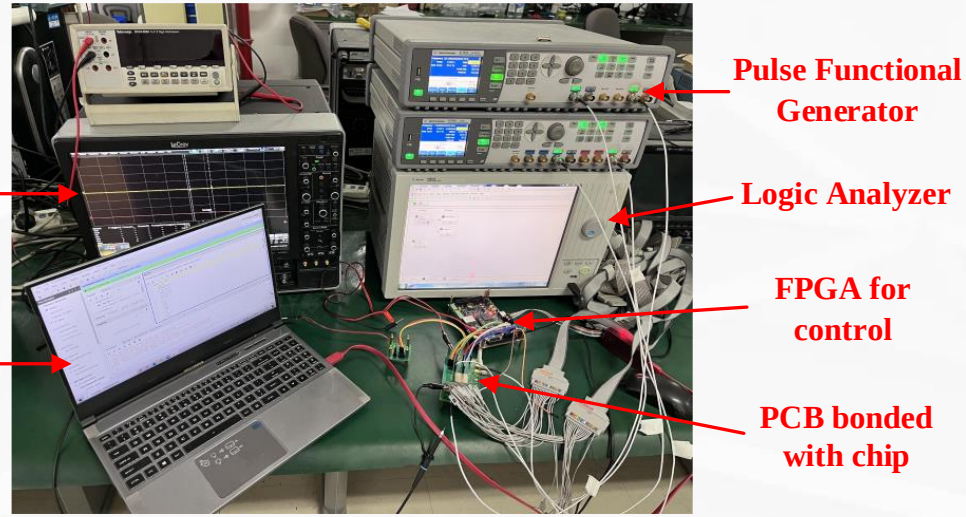
- **Testing System**



- **Linearity** (@Fref=100MHz, with code density test)

	DNL (max)	INL (max)
Channel 1-2	0.30 LSB	-0.91 LSB
Channel 1-3	0.32 LSB	-1.00 LSB
Channel 1-4	0.37 LSB	-1.26 LSB
Channel 1-5	0.34 LSB	-1.10 LSB
Channel 1-6	0.35 LSB	-1.16 LSB
Channel 1-7	0.30 LSB	-0.87 LSB
Channel 1-8	0.29 LSB	-0.70 LSB

- **Single Shoot Precision** (@Fref=100MHz)

The SSP results can be calibrated with the tested INL.

$$T_{CAL}(i) = T_{TEST}(i) - INL(i)$$

	Uncalibrated	Calibrated
Channel 1-2	93.5 ps	62.5 ps
Channel 1-3	91.7 ps	56.2 ps
Channel 1-4	98.6 ps	66.3 ps
Channel 1-5	116.1 ps	72.1 ps
Channel 1-6	96.3 ps	61.1 ps
Channel 1-7	90.4 ps	62.5 ps
Channel 1-8	104 ps	67.1 ps

- **Power Consumption** (@Fref=100MHz)

Counting Rate	Total Power Consumption
0	18 mW
1 KHz	88.2 mW
4 MHz	93.6 mW

Performance Comparison

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Year, ref	Process size (nm)	Number of channels/pixels	Type	Dynamic Range (ns)	LSB (ps)	SSP (ps)	DNL/INL (LSB)
2012, [1]	130	16	GRO	3700	56.5	325 (system)	-
2012, [2]	130	1024	Delay line	100	119	78.5	0.4/1.2
2014, [3]	350	48	GRO	51.8	3390	93.2	1.97/2.39
2019, [4]	150	128	GRO	81.8	80	196 (system)	0.2/2.4
2020, [5]	350	1	VDL	10	78	97.6	0.04/0.58
This work	180	8	VDL	2560	41.7	56.2	0.37/1.26

Reference:

[1] D. Tyndall et al. “A high-throughput time-resolved mini-silicon photomultiplier with embedded fluorescence lifetime estimation in 0.13 μm CMOS,” IEEE Trans. Biomed. Circuits Syst., vol. 6, no. 6, pp. 562–570, Dec. 2012.

[2] M. Gersbach et al., “A time-resolved, low-noise single-photon image sensor fabricated in deep-submicron CMOS technology,” IEEE J. SolidState Circuits, vol. 47, no. 6, pp. 1394–1407, Jun. 2012..

[3] S. Mandai et al. “A 780 × 800 μm2 multichannel digital silicon photomultiplier with column-parallel time-to-digital converter and basic characterization,” IEEE Trans. Nucl. Sci., vol. 61, no. 1, pp. 44–52, Feb. 2014.

[4] E. Manuzzato et al.,“A16×8 digital-SiPM array with distributed trigger generator for low SNR particle tracking,” IEEE Solid-State Circuits Lett., vol. 2, no. 9, pp. 75–78, Sep. 2019.

[5] E. Conca et al., “Large-area, fast-gated digital SiPM with integrated TDC for portable and wearable time-domain NIRS,” IEEE J. Solid-State Circuits, vol. 55, no. 11, pp. 3097–3111, Nov. 2020.

Prospects and Thoughts

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- **How to improve resolution ?**
  - ✓ Higher clock frequency: less accumulated jitter but more power consumption.
  - ✓ More delay units in DLL: more accumulated jitter and more power consumption.
  - ✓ Auxiliary circuits like time-amplifier: more complicated and worse linearity

- **How to improve SSP ?**
  - ✓ Frequency synthesizer with low noise: LC-VCO based PLL, fully differential delay unit.
  - ✓ Attenuated noise from power supply: noise filtering, LDO integrated on chip.
  - ✓ Multi-channel averaging for a single event: SSP downsized to $1/\sqrt{n}$.

- **How to balance the performance of multi-channels ?**
  - ✓ More symmetrical channels: axial symmetry, central symmetry.
  - ✓ In-situ calibration: like that in HPTDC [1].
  - ✓ Calibration techniques: digital scrambling technique[2], histogram-based approach [3], genetic algorithm [4], delay offset calibration [5] .

Reference:

[1] Christiansen J. HPTDC High Performance Time to Digital Converter. 2004.
[2] M. Zanuso, et al. Time-to-digital converter with 3-ps resolution and digital linearization algorithm, Proc. ESSCIRC (2010) 262–265.
[3] J. Wu, Several key issues on implementing delay line based TDCs using FPGAs, IEEE Trans. Nucl. Sci. 57 (3) (2010) 1543–1548.
[4] H. Chung, et al. A 360-fs-time-resolution 7-bit stochastic time-to-digital converter with linearity calibration using dual time offset arbiters in 65nm CMOS, IEEE J. Solid-State Circuits 56 (3) 940–949.
[5] H. Chung, et al. A 10-Bit 80-MS/s decision-select successive approximation TDC in 65-nm CMOS, IEEE J. Solid-State Circuits 47 (5) (2012) 1232–1241.

/03

A 6-channel TA-based TDC ASIC designed in 2023

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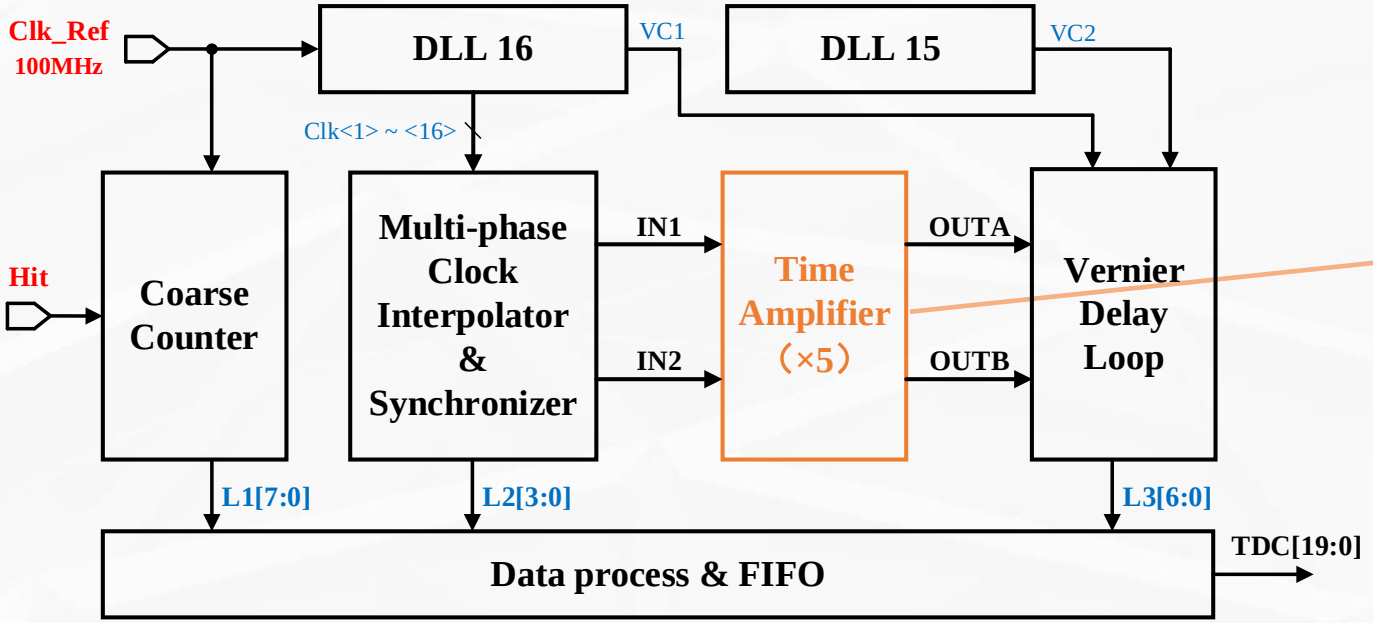
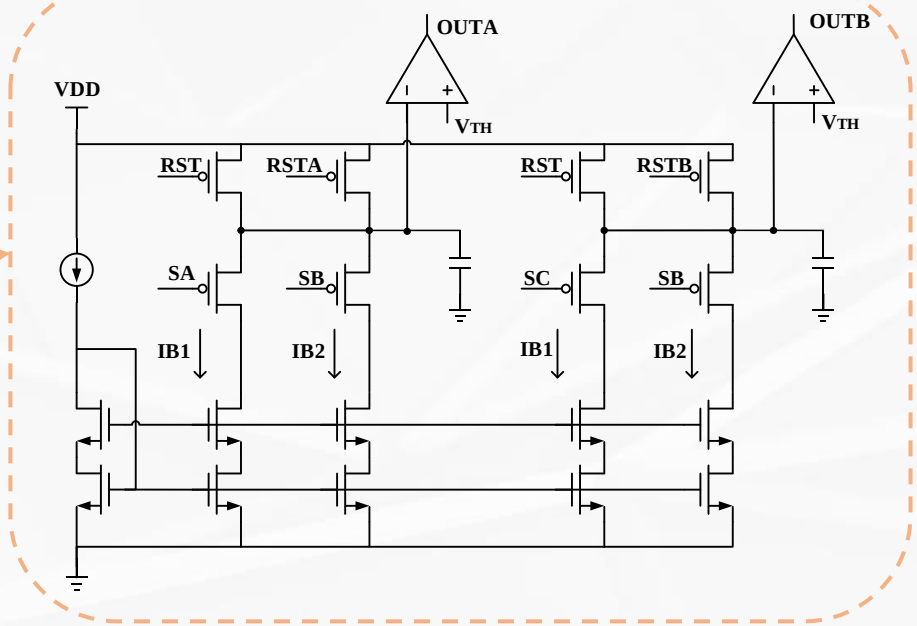
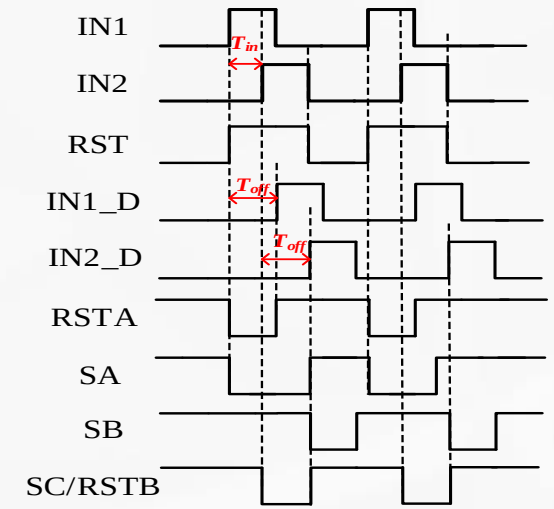
The Design of TA-based TDC







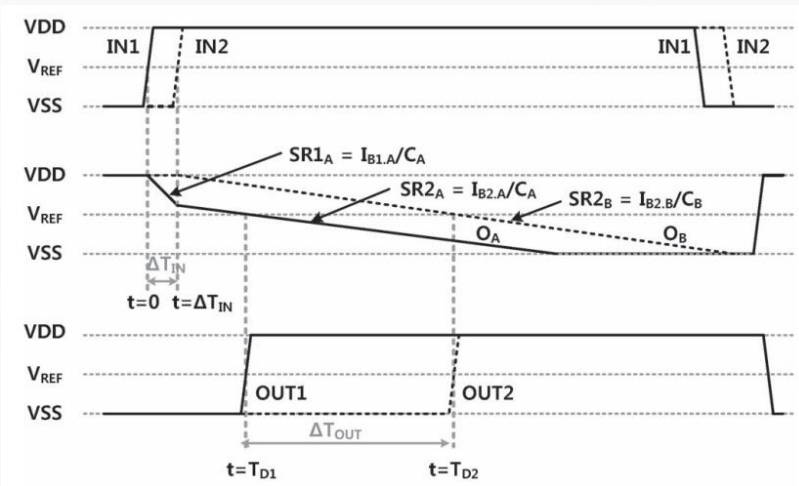
RST=~(IN1 NOR IN2)

RSTA=~(IN1⊕IN1_D)

SA=~(IN1⊕IN2_D)

SB=(IN2⊕IN2_D)

SC/RSTB=~(IN2_D)



The Layout and Simulation Results

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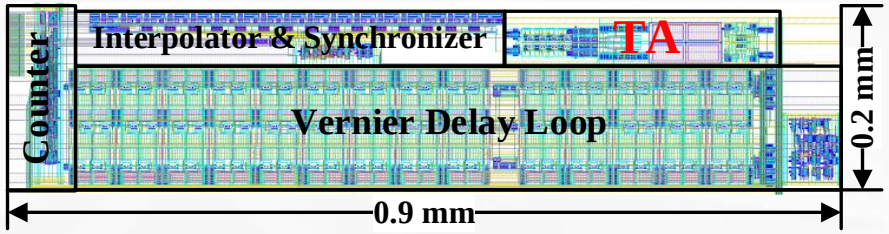
- The layout of single channel.



- The chip Photograph

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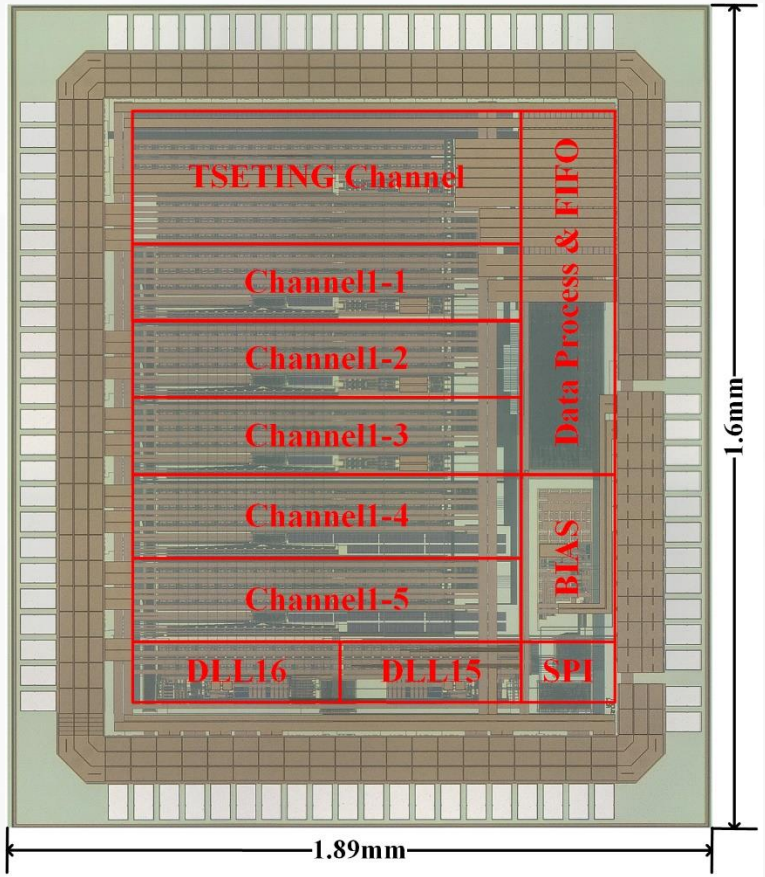
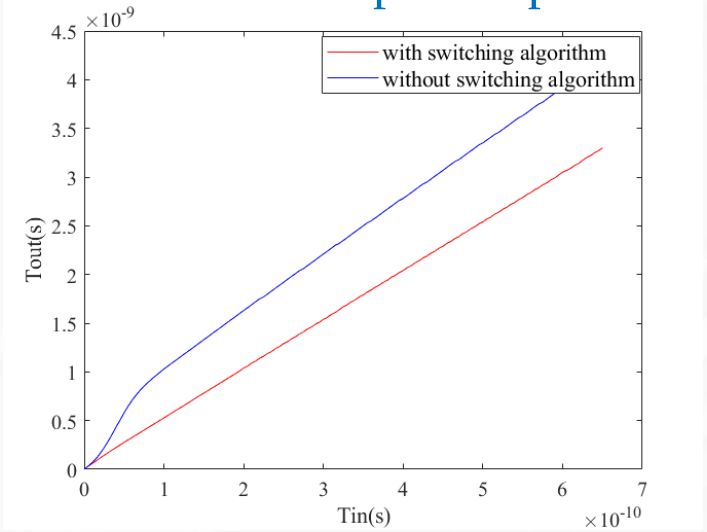
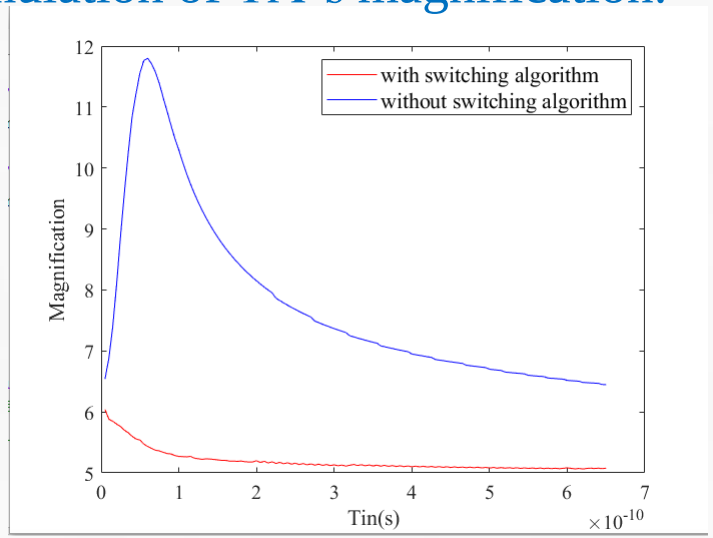
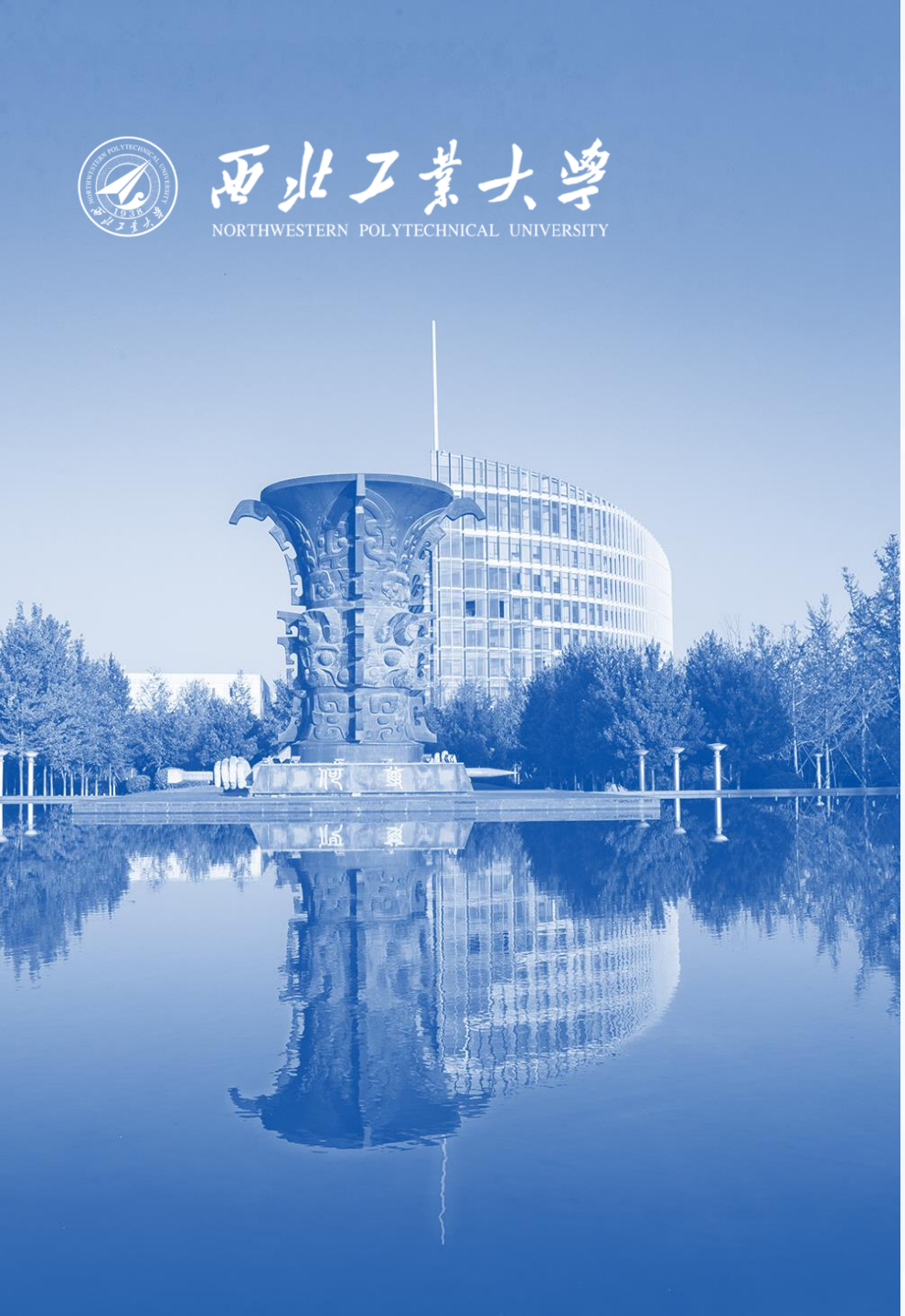


- Simulation of TA's input-output curve.



- Simulation of TA's magnification.





Thanks for Your Attention