GOBIERNO DE ESPAÑA

MINISTERIO DE CIENCIA E INNOVACIÓN

Ciemat
Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

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UE 23

2023 international workshop on the high energy Circular Electron Positron Collider (CEPC)

Oct 23-27, 2023 Nanjing, China

SEMI-DIGITAL HCAL WITH RPC AND MRPC

MARY-CRUZ FOUZ
CIEMAT

AIDA innova

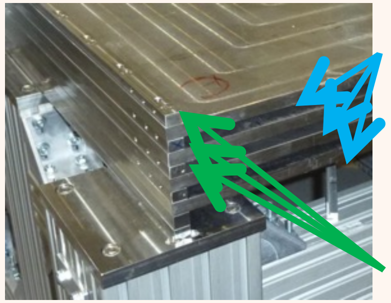
CALICE

SDHCAL – MAIN CHARACTERISTICS

Sampling calorimeter. Absorber: Stainless Steel + Detector: Glass Resistive plate Chambers

***Absorber*: Stainless steel**

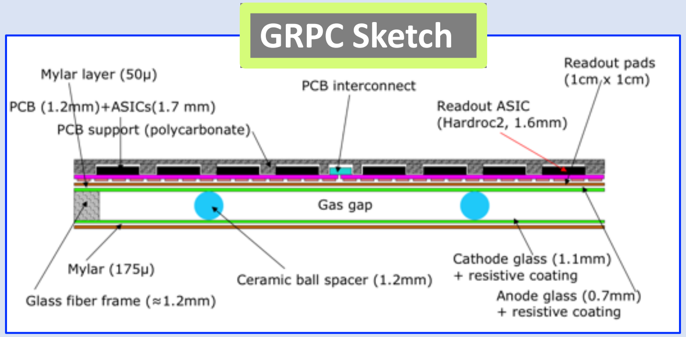
Absorber **plates up to ~3x1 m^2 .**
Surface **planarity < 1mm** ,
Thickness 15mm, tolerance **50µm**



Plates (15mm) assembled together by using an intermediate **spacer** insuring the place for introducing the detectors

Detail after assembly the **first 4 absorber plates of a 1.3m^3 prototype (plates ~1x1m^2)**

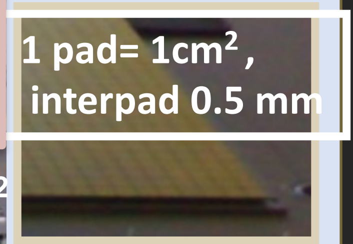
***Detector*: GRPC (Glass Resistive Plate Chambers)** operating in **avalanche mode**



1x1 cm^2 pads. Semi-Digital Readout, 2bits **- 3 thresholds**
➔ It counts **how many** and **which pads** have a **signal larger than one of the 3 thresholds**

Embedded electronics:
PCB separated from the GRPC by a mylar layer (50µm).
➔ Bottom: **1x1cm2 pads**
➔ Top: **HARDROC** (**HA**dronic **R**pc **R**ead**O**ut **C**hip) & related connections

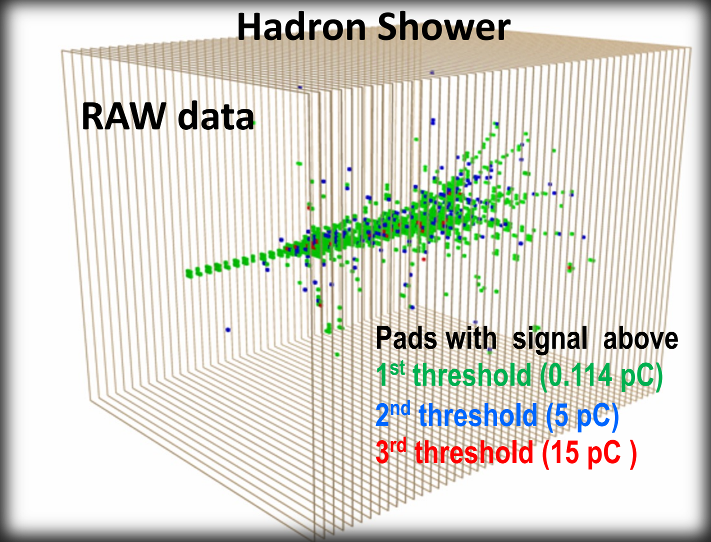
Power-pulsed electronics (only for linear colliders): In **stand-by during dead time** in between collisions or spills in beam tests



1M³ SDHCAL PROTOTYPE

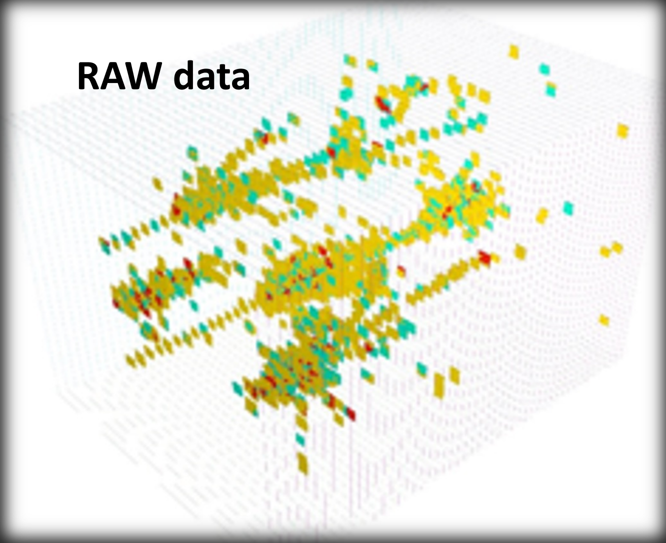
SDHCAL ~1.3m³ prototype
At Test Beam @ CERN

~ half million channels!!
(More than in the full calorimeter systems of the LHC experiments)



Excellent detailed view of shower development

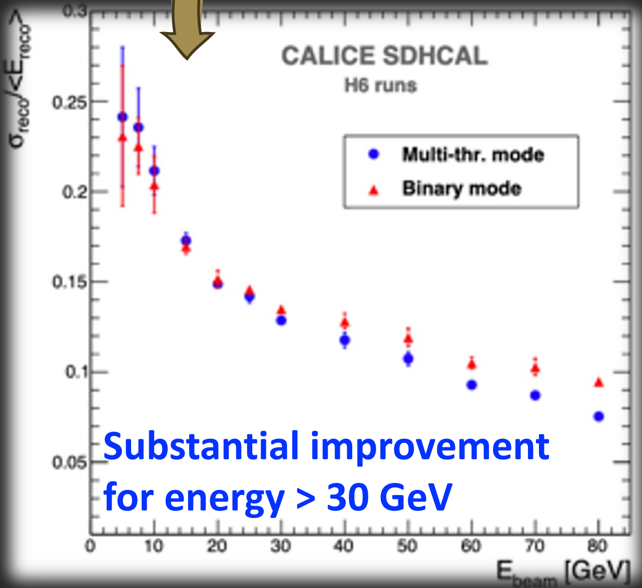
TRACKER-CALORIMETER



SNAPSHOT ON PERFORMANCE & RECONSTRUCTION

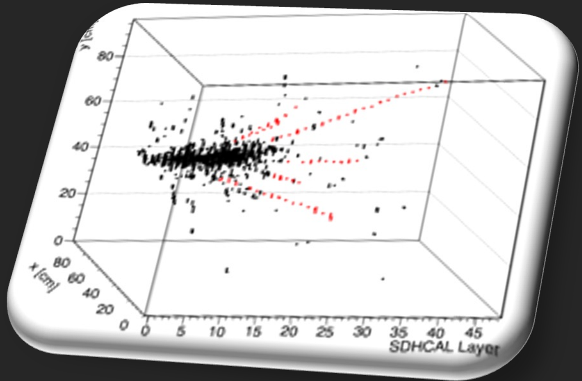
Advantage of (semi)-digital vs analog ➔ It allows a higher granularity at lower costs.
Granularity is crucial to improve the jet energy resolution using Particle Flow Algorithms.

Advantage of semi-digital vs digital
➔ Multi-threshold improves resolution

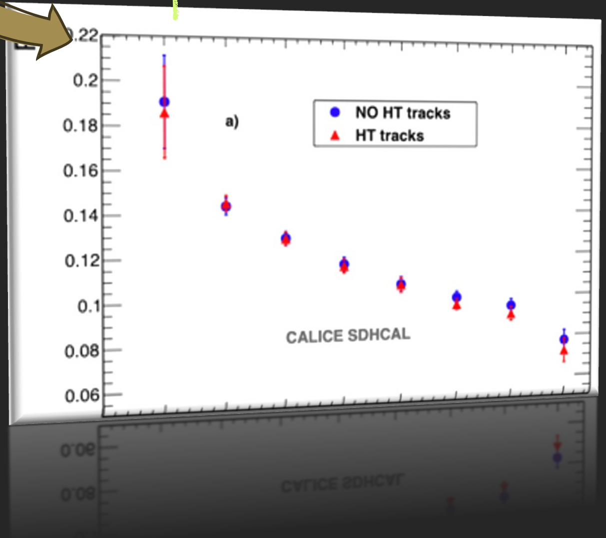


When increasing energies the binary produces saturation (mainly in the core of the shower). The number of particles crossing a single pad increases

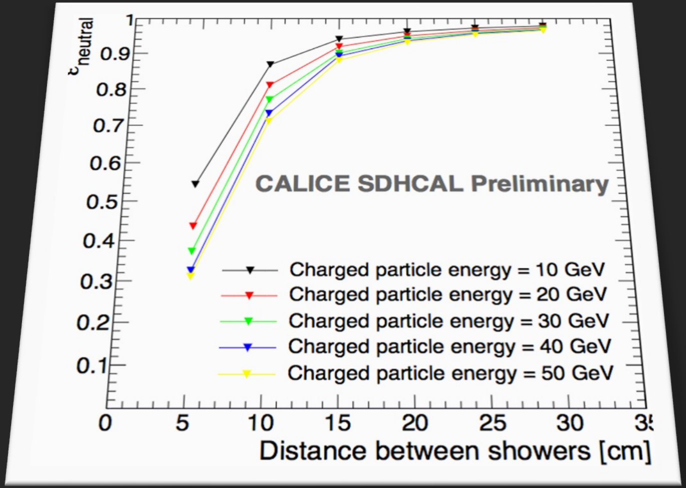
Single track reconstruction with Hough transform techniques



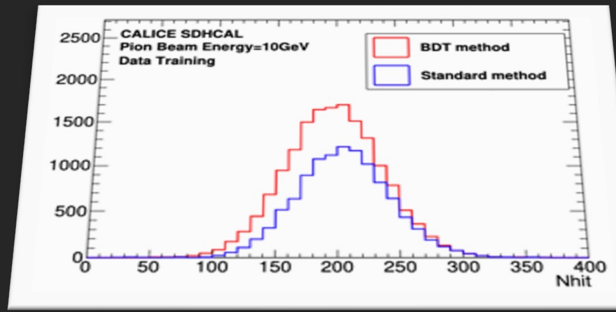
Improved resolution



Nearby hadronic showers separation



PID: BDT & MVA technique



TOWARDS FULL SIZE CALORIMETERS - CHALLENGES

Some general Challenges

- High precision mechanics
- Embedded electronics
- Low power consumption
- Very uniform response despite the large number of channels

Partially addressed with the $1m^3$ prototype but a step forward needed

Circular vs linear colliders extra difficulties

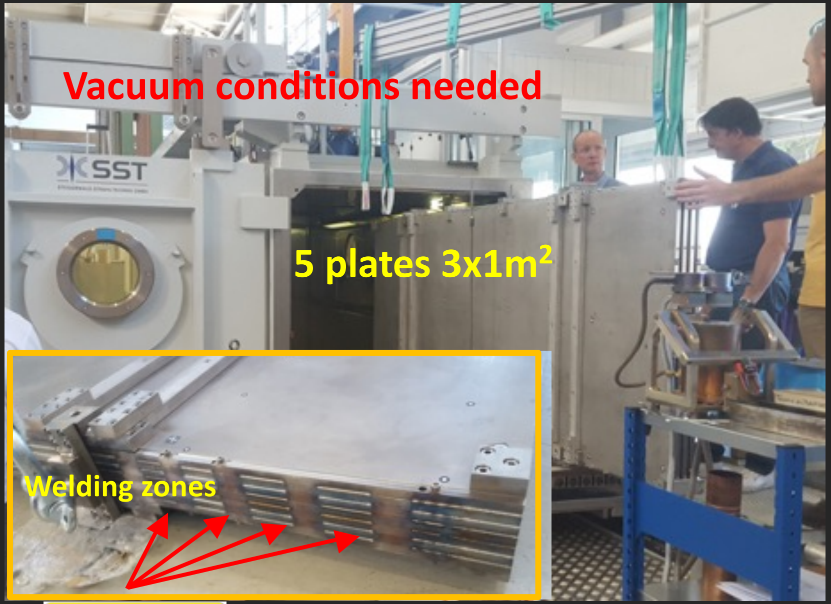
- Continue readout
- Higher rates

In addition coolling system must be considered

CHALLENGES – HIGH PRECISION MECHANICS

Procedures developed with roller leveling for improving planarity of absorber plates ($1x3m^2$) from several mm to ~500 microns

Development of Electron Beam Welding assembly protocols to reduce deformations introduced by welding procedures below mm level (600 microns in this test with 5 plates 3x1 m^2)



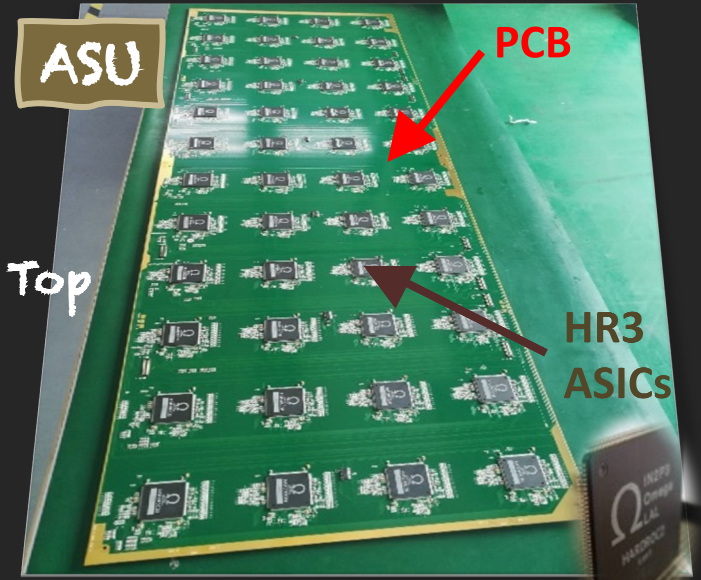
Larger modules (more plates) ➔ bigger machine needed & complicated handling (heavy structure to be moved an rotated several times)

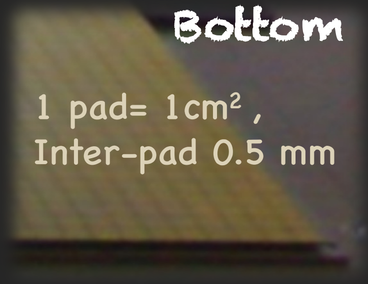
Possible option ➔ build sub-modules and after weld them using laser welding. The procedure should introduce reasonable deformations (the rigidity of the modules is much higher than for individual plates)

CHALLENGES - ELECTRONICS

- Electronics must be compact despite the huge number of channels ➔ Embedded in the calorimeter
- Homogeneous response➔ Stringent planarity requirements for PCBs to insure homogeneous contact of pads with RPCs
- Lower power consumption ➔ Power pulsing for linear colliders, more developments needed for circular

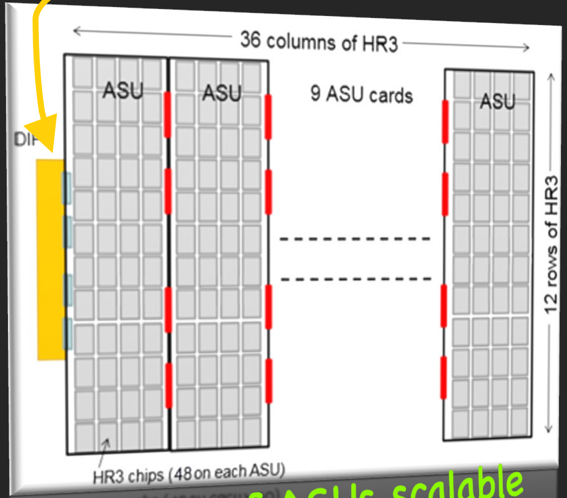
Best 13 layer PCB option found up to 1x0.33 m²





HADROC3

Independent channles
Zero suppress
Extended dynamic range (15fC to 50 pC)
I2C link with triple voting for SC parameters
packaging in QFP208, die size ~30 mm2

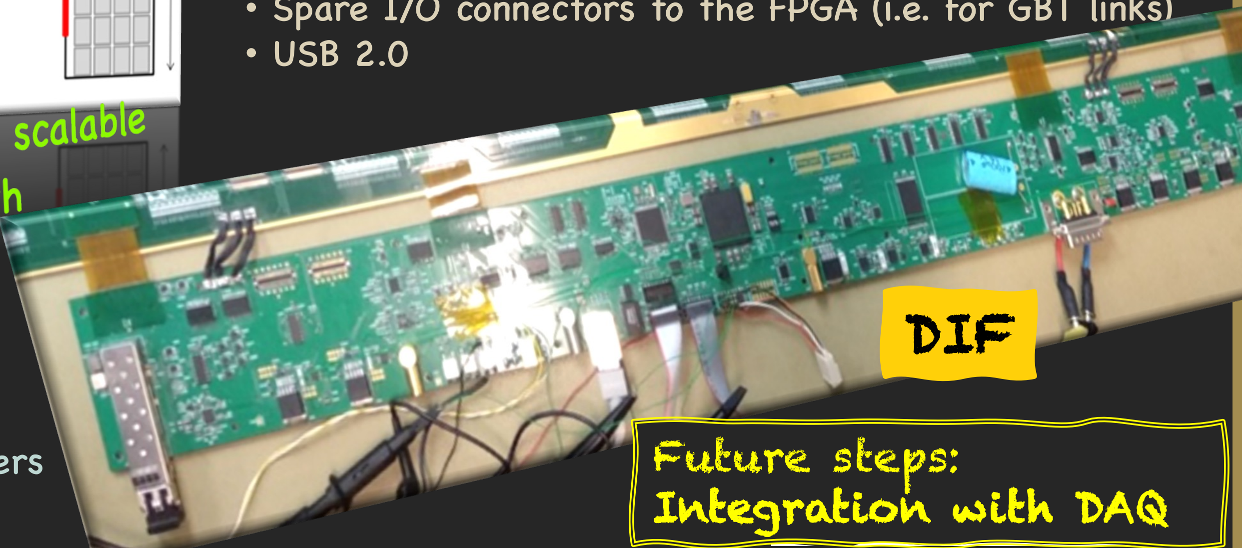


Number of ASUs scalable with GRPC length

DIF (Detector InterFace)

Sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ.

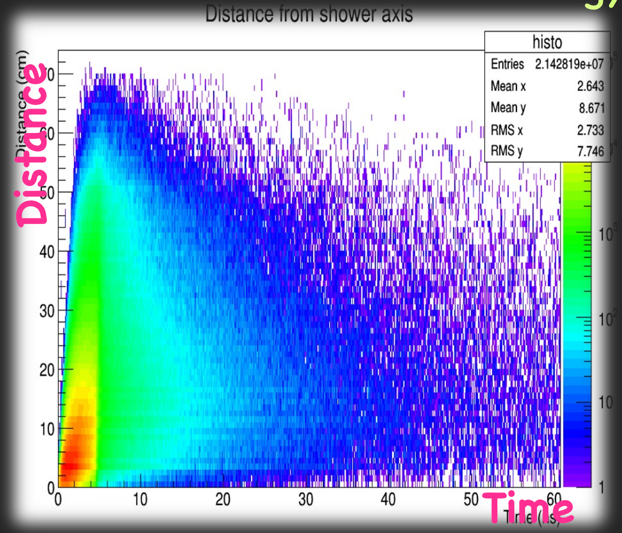
- 1 DIF per RPC plane handle up to 432 HR3 chips
- HR3 SC through I2C bus (12 IC2 buses).
- Data DAQ transmission by Ethernet
- Clock and synchronization by TTC (also used in LHC)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- USB 2.0

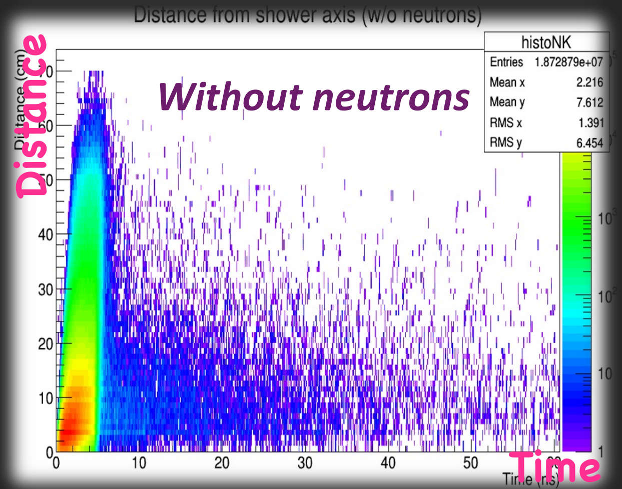


Future steps:
Integration with DAQ

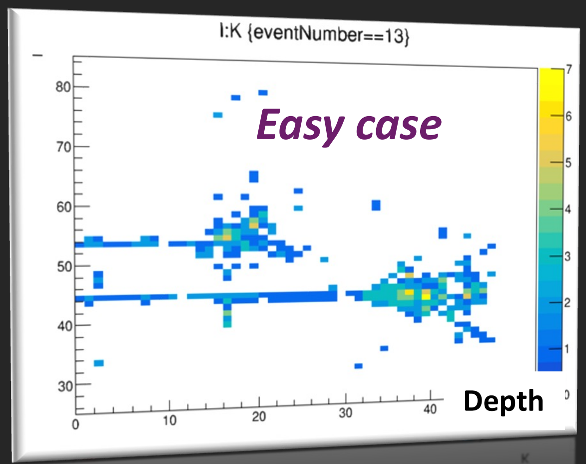
INCLUDING PRECISION TIME MEASUREMENTS 5D CALORIMETER - WHY?

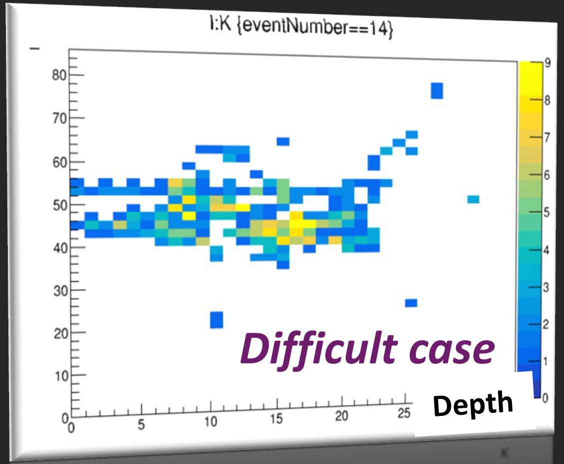
Timing could be an important factor to identify delayed neutrons and better reconstruct their energy



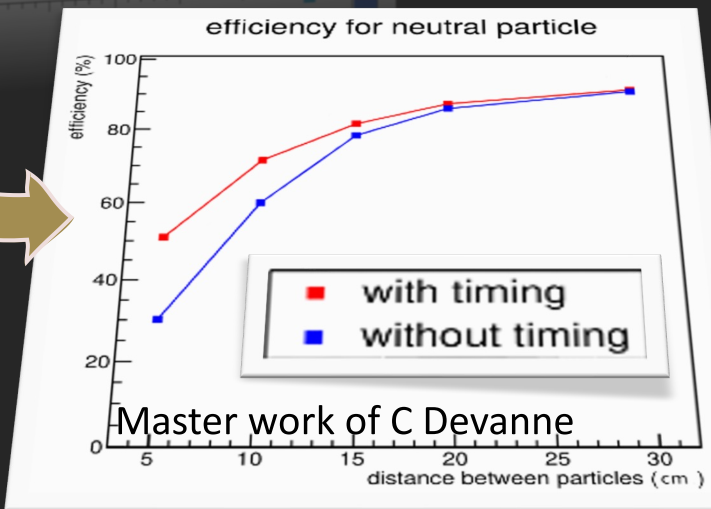


Time information can help to separate close by showers and reduce the confusion for a better PFA application.
Example: pi-(20 GeV), K-(10 GeV) separated by 8 cm.





Recent studies show time information could improve significantly hadronic showers separation at lower distances.



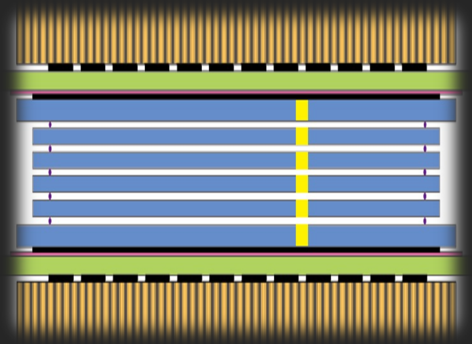
Master work of C Devanne

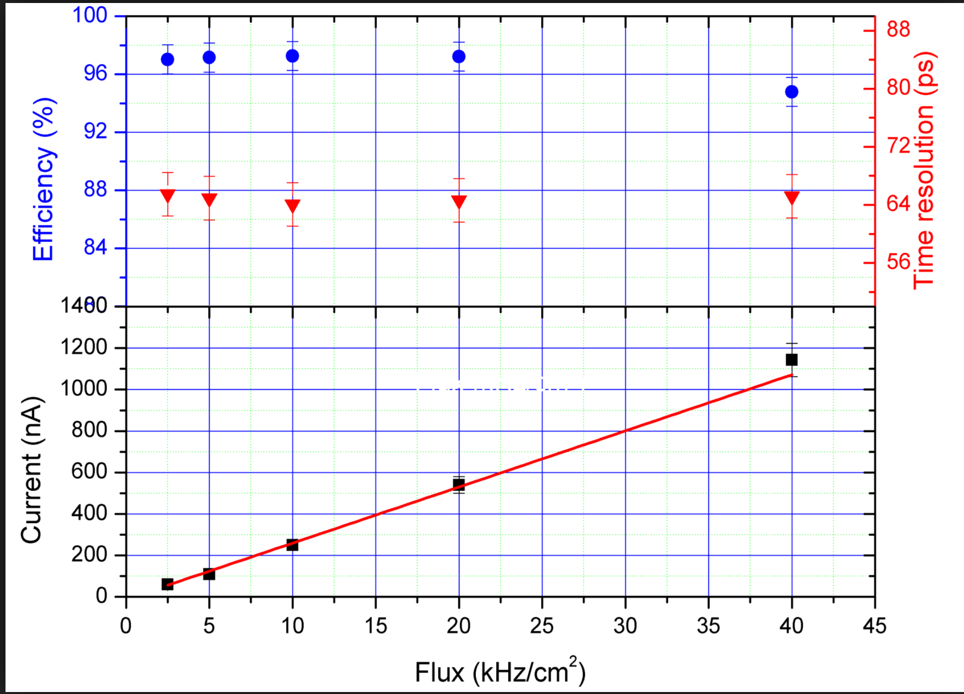
INCLUDING PRECISION TIME MEASUREMENTS 5D CALORIMETER - HOW?

❖ Chambers: GRPC ➔ MultiGap – GRPC

will improve the intrinsic timing of the calorimeter

Time resolution of ***better than 100 ps*** was obtained with **5-gap RPC** by Tsinghua group





Low resistive materials could /should be used to increase the rate capability

❖ Electronics: An ASIC with a fast preamplifier, precise discriminator and excellent TDC

DEVELOPMENTS ON MULTIGAP GRPC CHAMBERS

SEVERAL PROTOTYPES IN DIFFERENT INSTITUTES

Glass resistivity ~10^{12} - 10^{13} Ωcm

two times 4-gap
PCB inserted
between the two

1cm Strip width

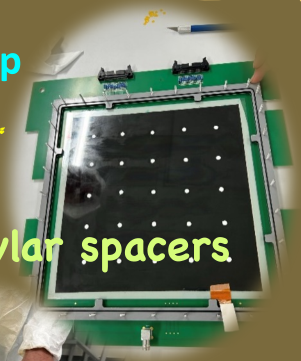
Mylar spacers

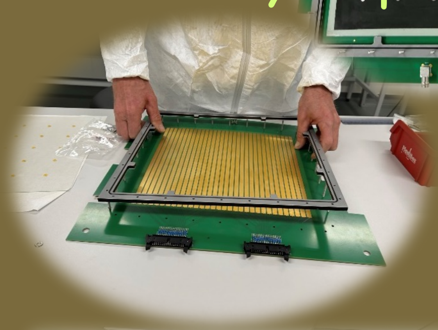
1x1m² chamber

two times 3-gap

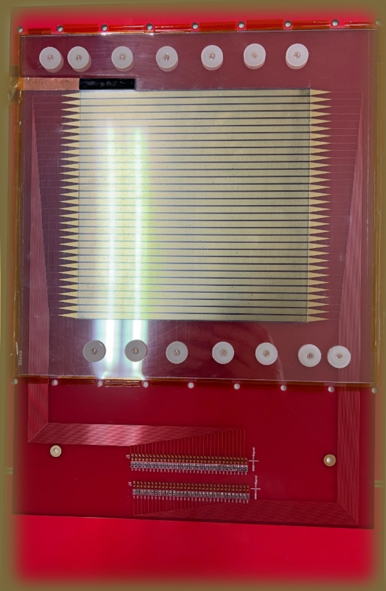
30x30cm²

Mylar spacers





Glass resistivity ~ 5x10^{12} Ωcm



Single stack 5 gaps

X-Y Strip
4mm Strip width

20cm x 20cm

Ø 230 µm ceramic fishing line

Expecting less charge going to the fishing line

DEVELOPMENTS ON MULTIGAP GRPC CHAMBERS FOR HIGH RATES

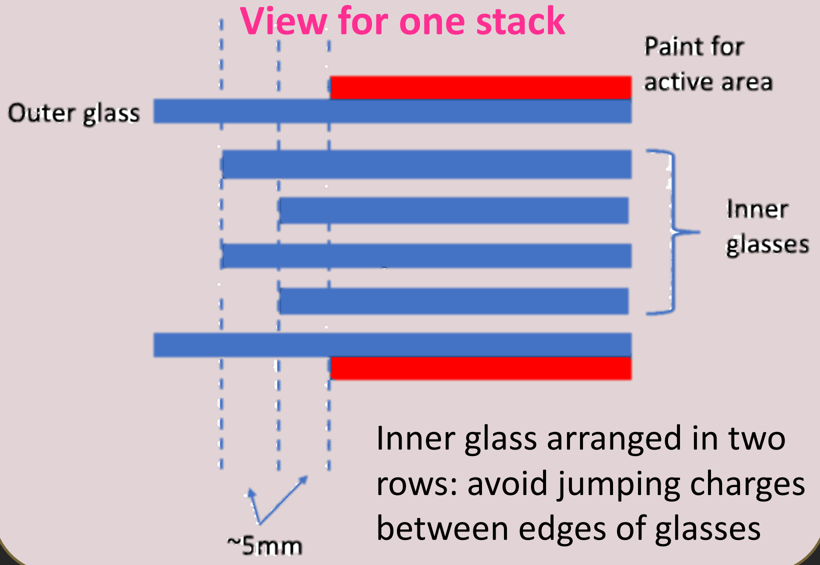
Low resistivity glass for high rates

Glass resistivity ~ 10^{10} **Ωcm**

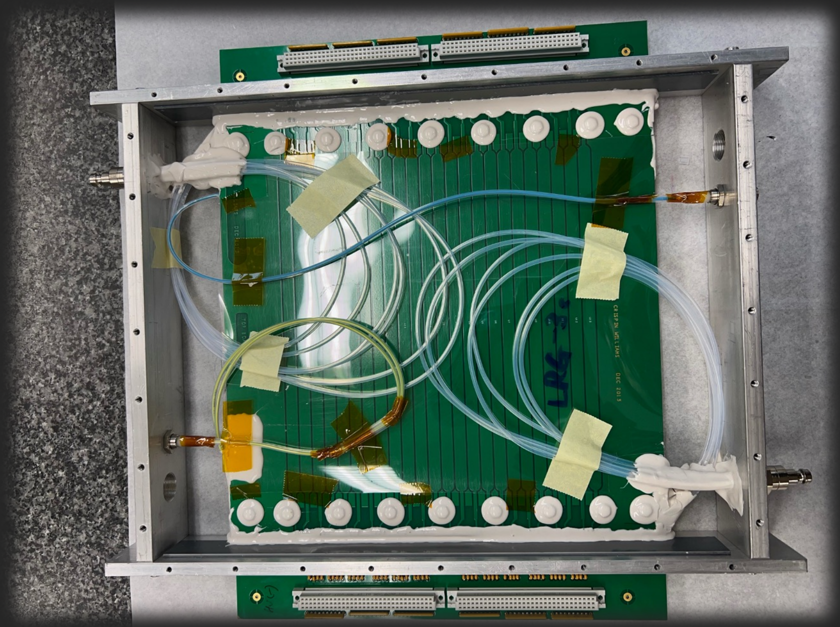
Glass thickness : 500 µm

2 stack 5 gaps

Ceramic fishing line



Inner glass arranged in two rows: avoid jumping charges between edges of glasses



ELECTRONICS FOR PRECISION TIME CALORIMETER – ASICS -

"Present" BaseLine

- 32 channels
- on-chip TDC
- Time resolution below 40ps

Pros: Embeds the preamp, the TDC , a QDC

Con: Limited digital logic, difficult to chain, deadtime

Developed at CNRS-OMEGA partially thanks to AIDA2020 for CMS-muon upgrade

It is not the ASIC for the long term,
only for exploring the RPC capabilities.
Must be substituted in the future due to its limitations

Other option being used

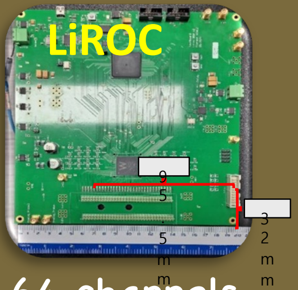
NINO Designed for the ALICE MRPC (TOF array)
- 8 channels
- Time resoltion ~50 ps

Medium/long term possible option

weeroc

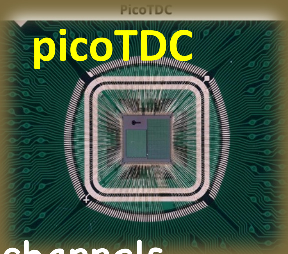
Board is under development by the WEEROC company

Based on



64 channels

+



64 channels
Time resolution <12 ps

ELECTRONICS FOR PRECISION TIME CALORIMETER – READOUT -

Two different Active Sensitive Unit (ASU) under development

- For small prototypes
- For Larger prototypes

ELECTRONICS FOR PRECISION TIME CALORIMETER – READOUT -

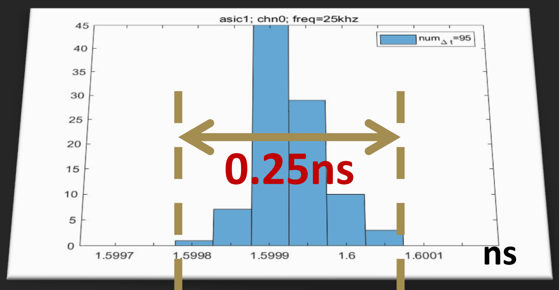
Two different Active Sensitive Unit (ASU) under development

- For small prototypes
- For Larger prototypes

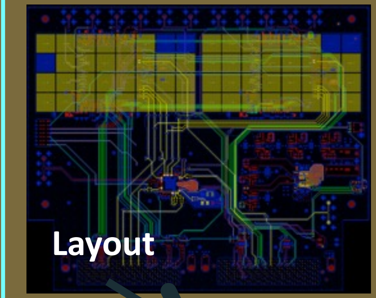
Validation performed

- Reference voltage checks
- Thresholds tests
- No crosstalk
- Timing by injecting signal
  - between neighbor channels $\sigma(\Delta t_{12})$ = 45.8ps
  - between 2 chips $\sigma(\Delta t_{12})$ = 53.6ps

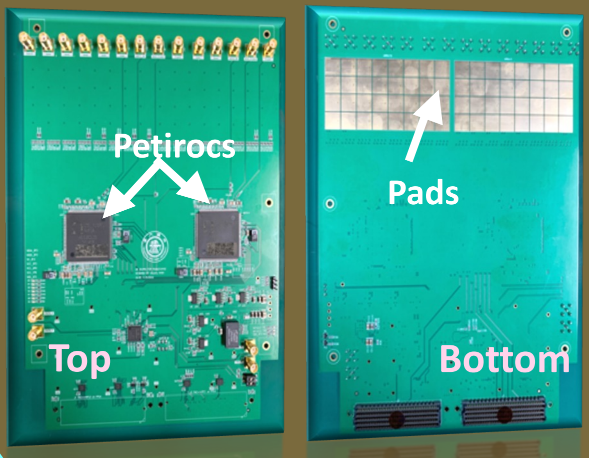
asic1; chn0; freq=25khz



Hosting **2 Petiroc ASICs**
to readout 64 **1cm x 1cm pads** for **16x16 cm²** detector



Board (version2)



Board Test Setup

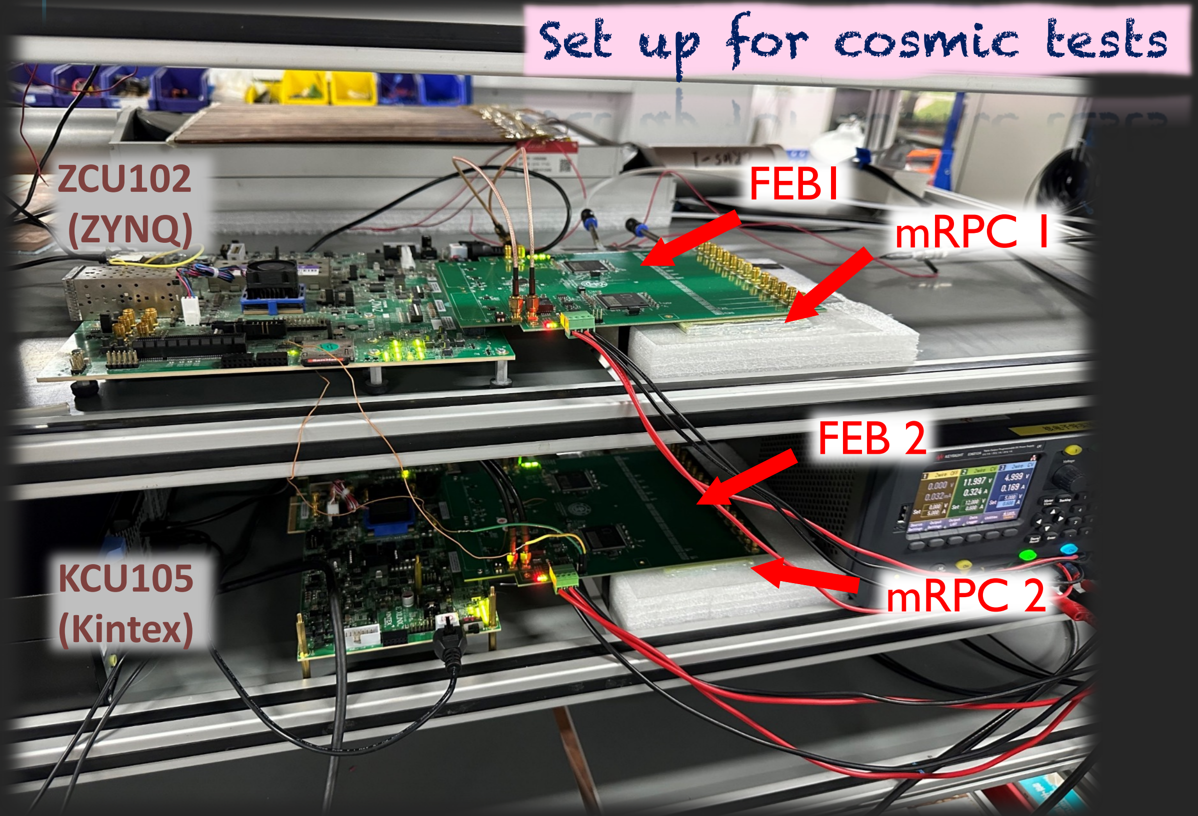
Using ZCU102 evaluation board

M.C Fouz Ciemat

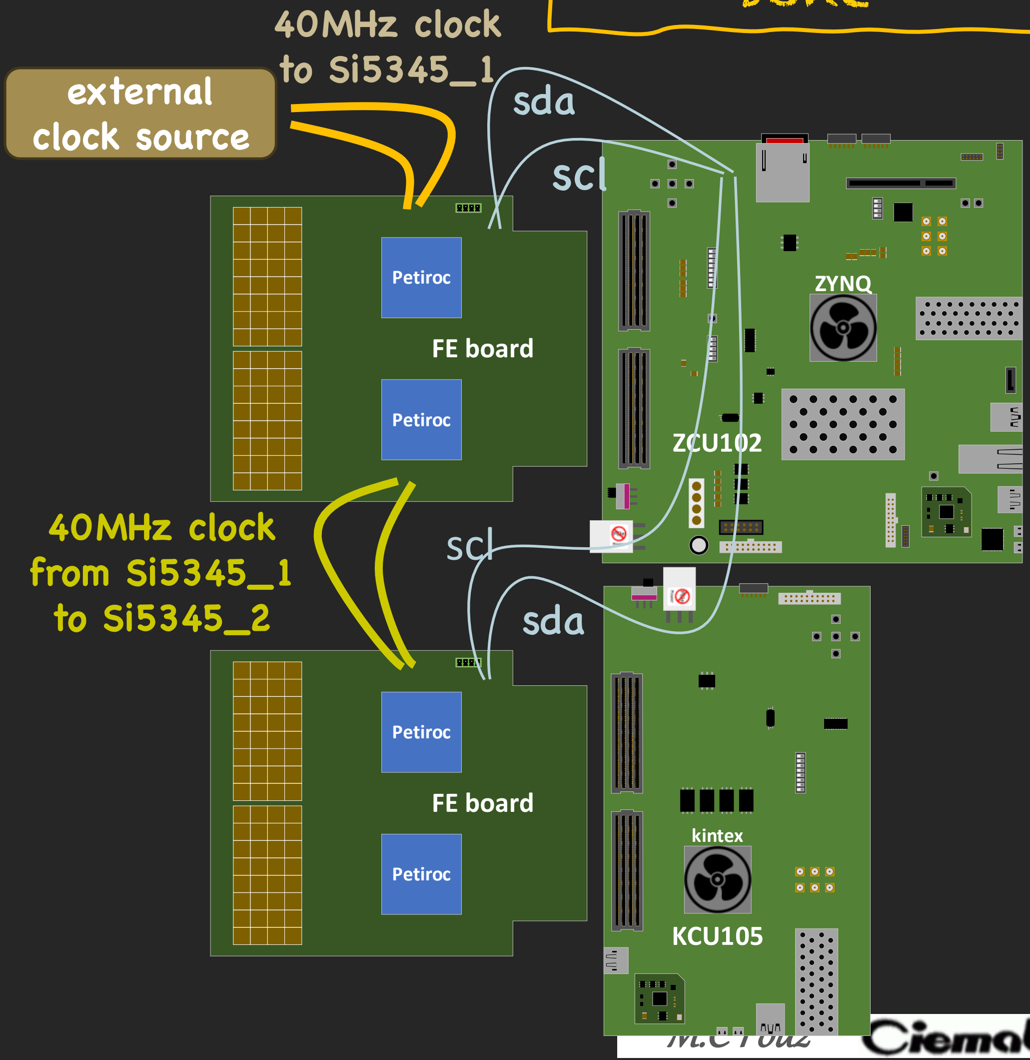
ELECTRONICS FOR PRECISION TIME CALORIMETER – READOUT -

Two different Active Sensitive Unit (ASU) under development

→ For small prototypes



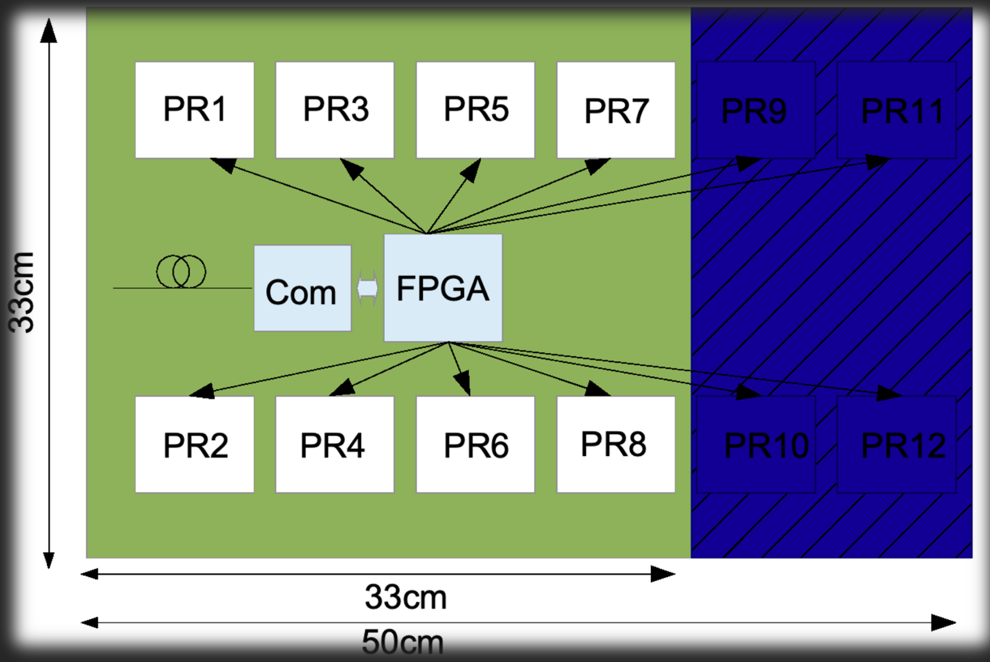
Synchronization Done

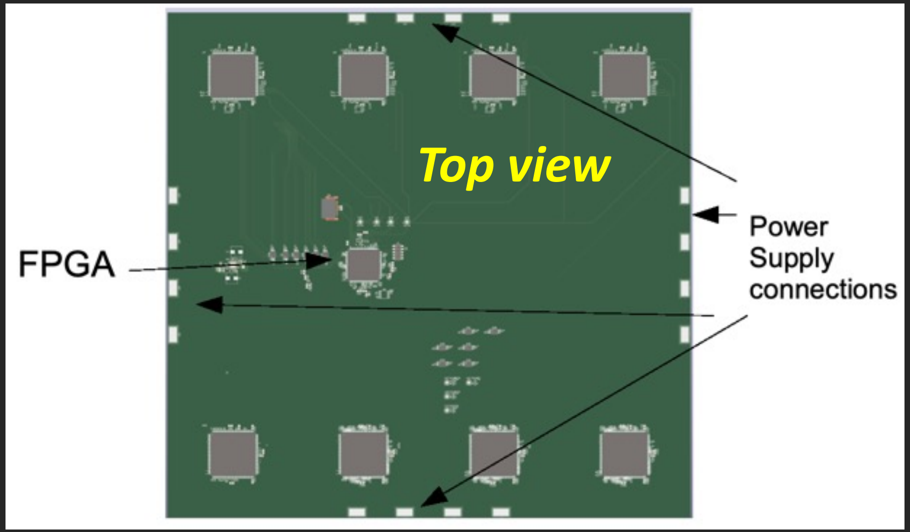


ELECTRONICS FOR PRECISION TIME CALORIMETER – READOUT -

Two different Active Sensitive Unit (ASU) under development

- For small prototypes
- For Larger prototypes





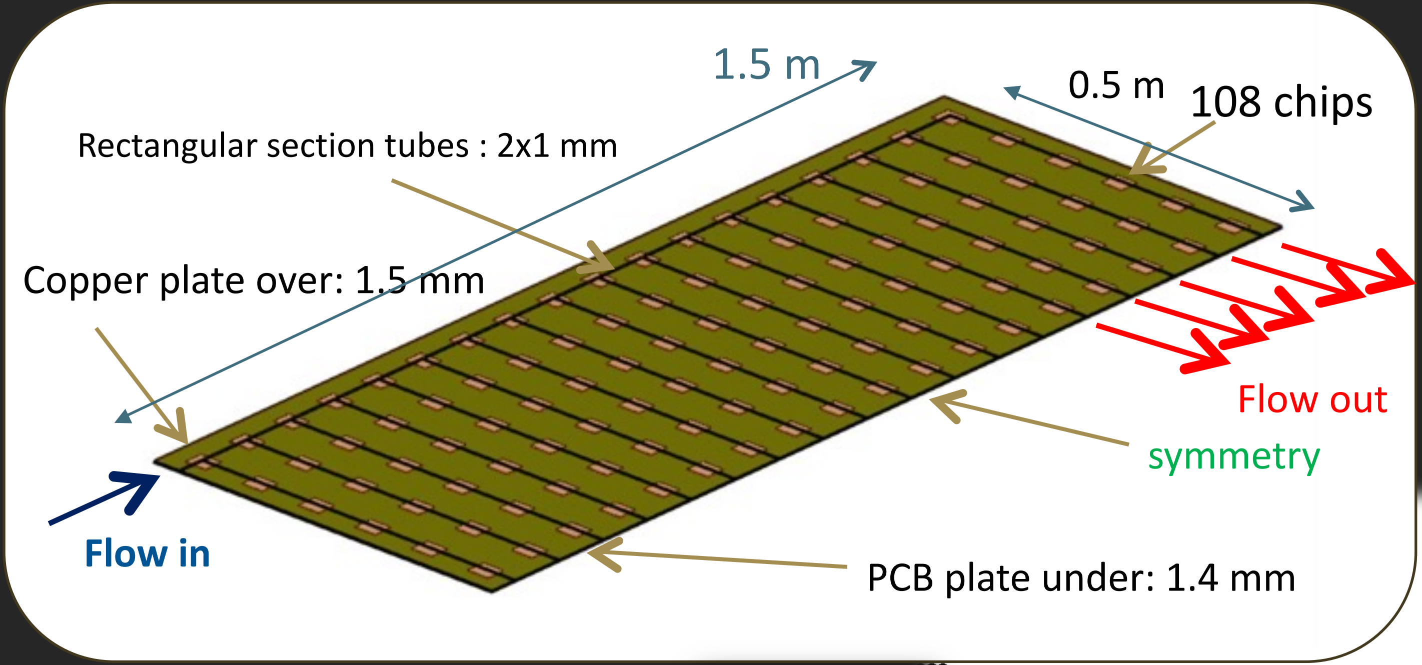
Local FPGA embedded on board

POWER CONSUMPTION AND COOLING

The duty cycles of CEPC/FCCee are different from that of ILC and no power pulsing is possible.

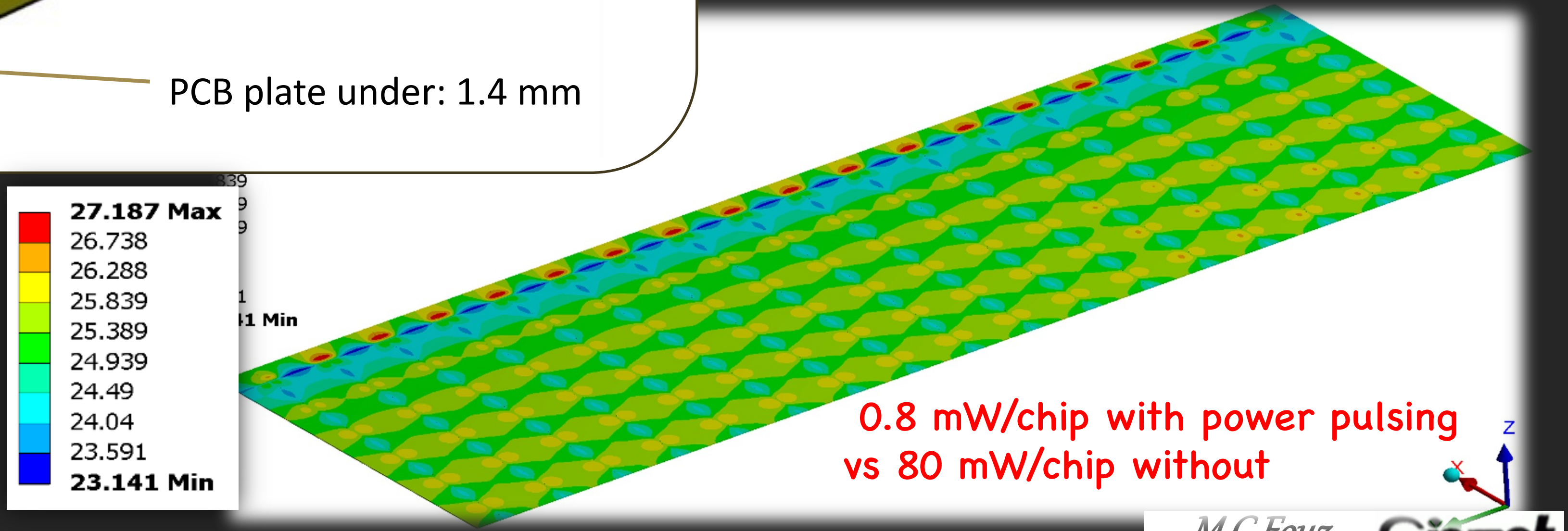
➔ Power consumption increases by a factor of 100-200 ➔ Active cooling is needed

But it should not add too much dead zone.



A simple cooling system based on water circulating into copper pipes designed

Simulation with HADROC electronics
To be done with the new ASICs



0.8 mW/chip with power pulsing vs 80 mW/chip without

M.C Fouz Ciemat

GROUPS INVOLVED

CIEMAT (SPAIN)
CNRS - IP2I (FRANCE)
CNRS - LPC (FRANCE)
CNRS - OMEGA (FRANCE)
GANGNEUNG-WONJU UNIVERSITY (SOUTH KOREA)
SHANGHAI JIAO TONG UNIVERSITY (CHINA)
VRIJE UNIVERSITEIT BRUSSEL (BELGIUM)
YONSEI CANCER CENTER (KOREA)

Extra material

FROM 1M3 TO LARGER PROTOTYPES-ELECTRONICS: ASIC,PCB,DIF

➢ **New ASIC**

HADROC3 (HR3)

Zero suppress
Extended dynamic range (up to 50 pC)
I2C link with triple voting for slow control parameters
packaging in QFP208, die size ~30 mm2

➢ **New ASU**

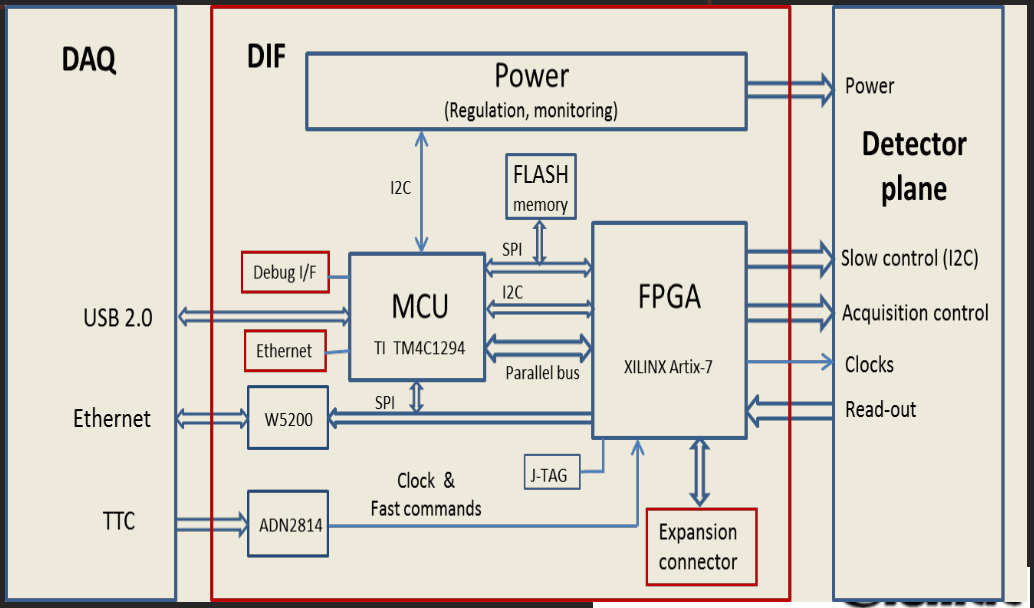
The **ASU** (**A**ctive **S**ensor **U**nit) hosts the ASICs and connect them to the rest of electronics

1m X 0.33 m2, **12 layers ASU** with **new rooting design**

➢ **New DIF & DAQ**

DIF (Detector InterFace) sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ. It controls also the ASIC power pulsing

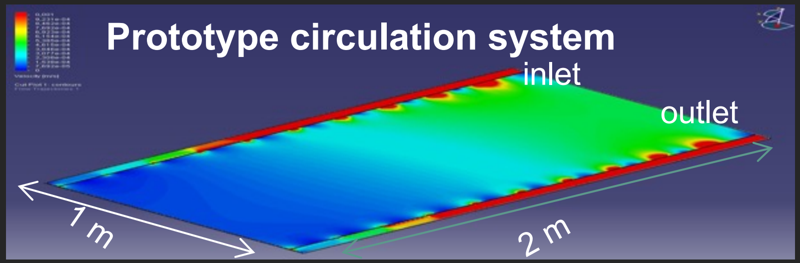
- Only **one DIF per plane** (instead of **three**)
- DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
- HR3 **slow control** through **I2C bus (12 IC2 buses)**.
  Keeps also **2 of the old slow control buses as backup & redundancy**.
- **Data transmission to/from DAQ** by **Ethernet**
- **Clock and synchronization** by **TTC** (already used in LHC)
- **93W Peak power supply** with super-capacitors (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**

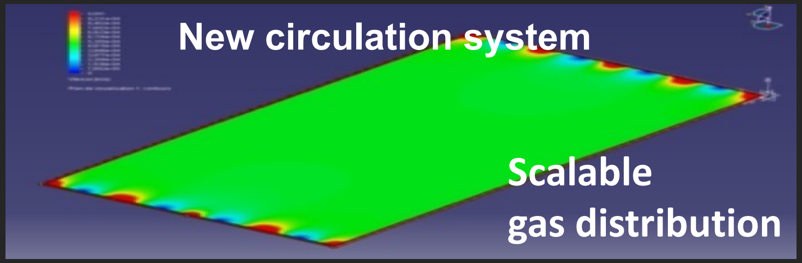


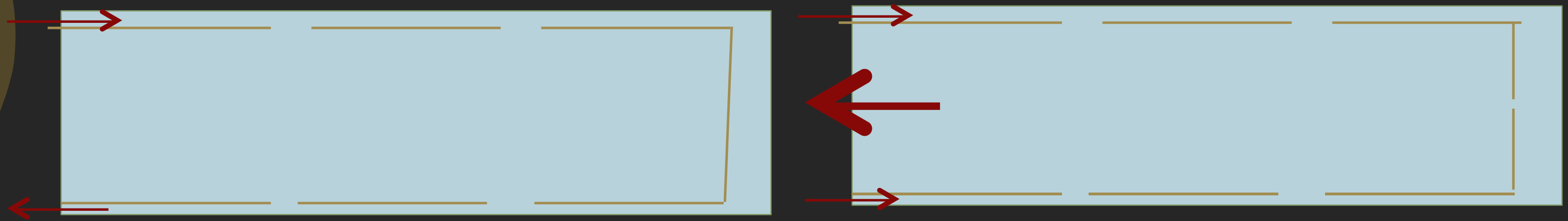
FROM 1M3 TO LARGER PROTOTYPES GRPC CHAMBERS

Construction and operation of large GRPC needs some improvements with respect to the $1m^2$ used at the $1m^3$ SDHCAL prototype.

Gas distribution







Energy reconstruction

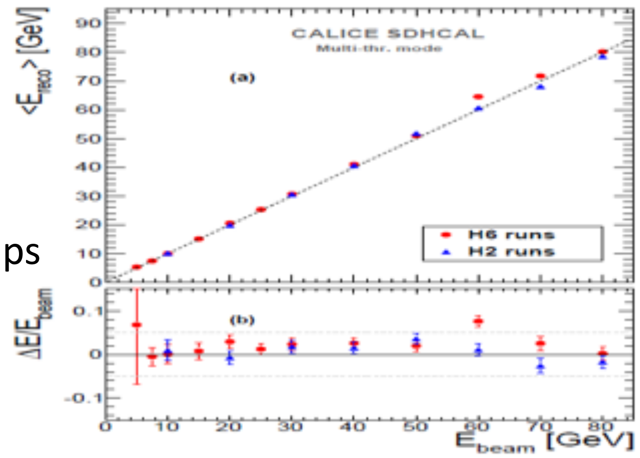
$E_{rec} = \alpha (N_{tot}) N_1 + \beta (N_{tot}) N_2 + \gamma (N_{tot}) N_3$

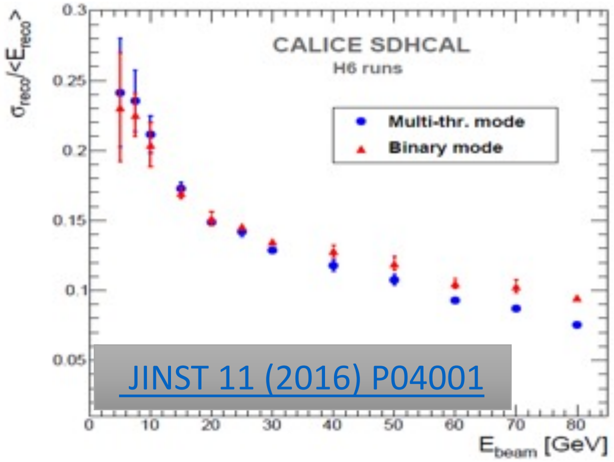
N_1= Nb. of pads with first threshold <signal < second threshold
N_2 = Nb. of pads with second threshold <signal < third threshold
N_3 = Nb. of pads with signal> third threshold

$N_{tot} = N_1 + N_2 + N_3$

α , β , γ are **quadratic functions** of
They are computed by minimizing :

$\chi^2 = (E_{beam}-E_{rec})^2/E_{beam}$





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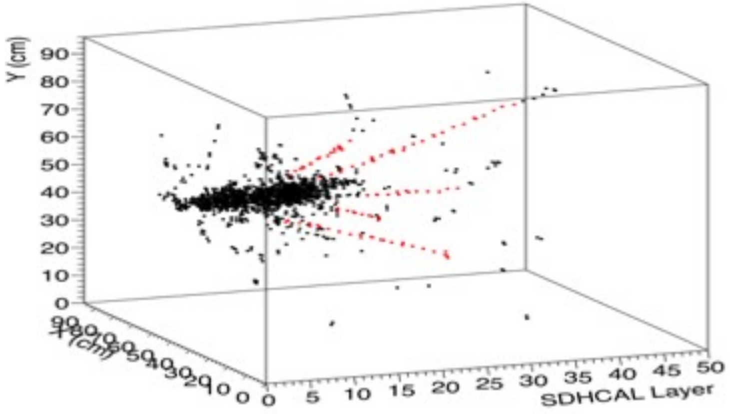
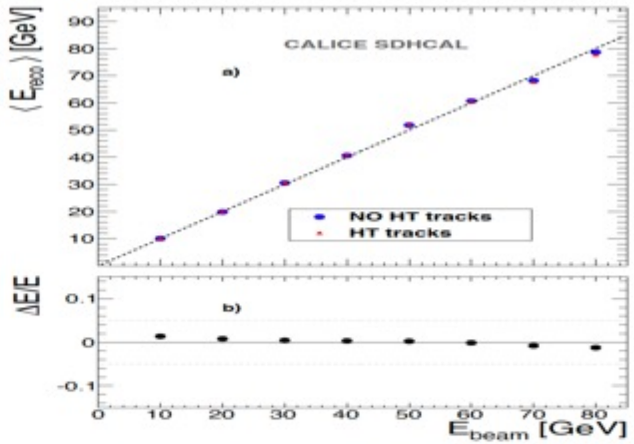
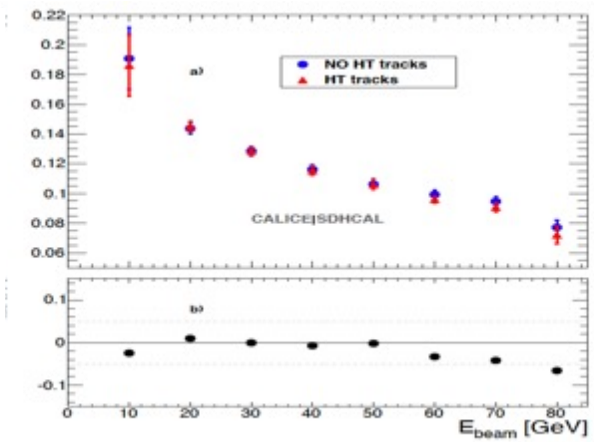
Hough-Transform

Track segments reconstruction using 3D-Hough Transform helps to apply different treatment to the hits of these segments.







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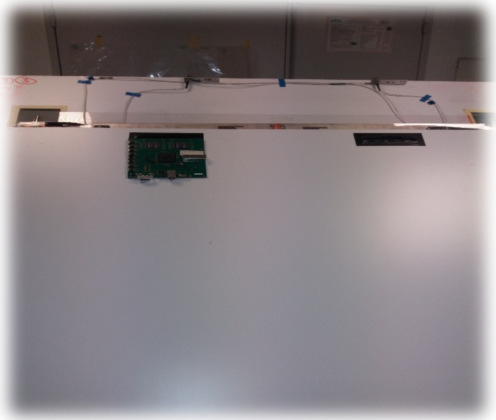
$E_{rec} = \alpha (N_{tot}) N'_1 + \beta (N_{tot}) N'_2 + \gamma (N_{tot}) N'_3 + c \; N_{HT}$

$N_{tot} = N'_1 + N'_2 + N'_3 + N_{HT}$

In addition track segments will be used as in-situ calibration and monitoring tools

Chamber + Electronic tests
“Standard” glass 1x1m2 chamber



Readout by: PETIROC+ external TDC
Same cards as the ones developed for upgraded CMS RPC
2 PETIROC2 + FPGA Cyclone V + ethernet

At the moment 64 strips in total can be read out but can be extended on future if needed.

Some tests to be done in incoming weeks