Highly granular Si-ECAL

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GENERALITAT VALENCIANA Conselleria d'Innovació, Universitats, Ciència i Societat Digital
Financiado por la Unión Europea NextGenerationEU
Gen-T

IJCLab
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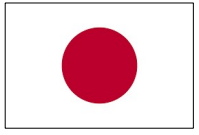
Laboratoire de Physique des 2 Infinis

LPSC Grenoble

LPNHE PARIS

ΩMEGA Microelectronics

cnrs IN2P3 Les deux infinis



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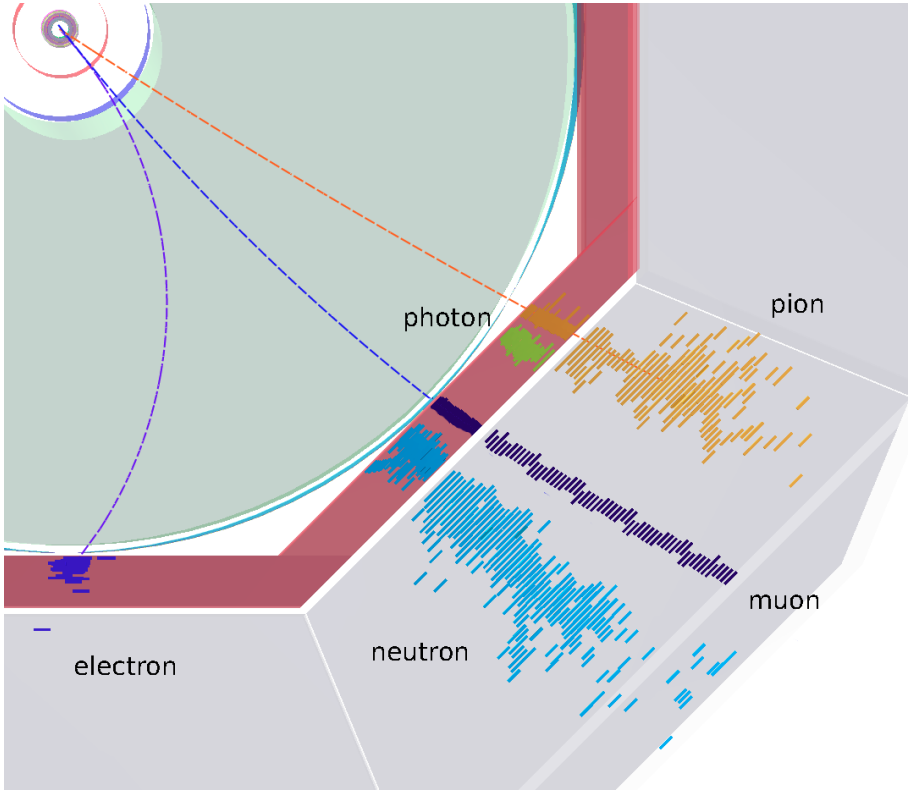
Particle Flow Algorithms



Concept

- Base the measurement on the subsystem with best resolution for a given particle type (and energy)
- Separation of signals by charge and neutral particles in the calorimeters
- **Maximal exploitation** of precise **tracking** measurement
  - **“no” material in front of calorimeters → very low material budget for trackers**
- Single particle separation

Calorimetry requirements

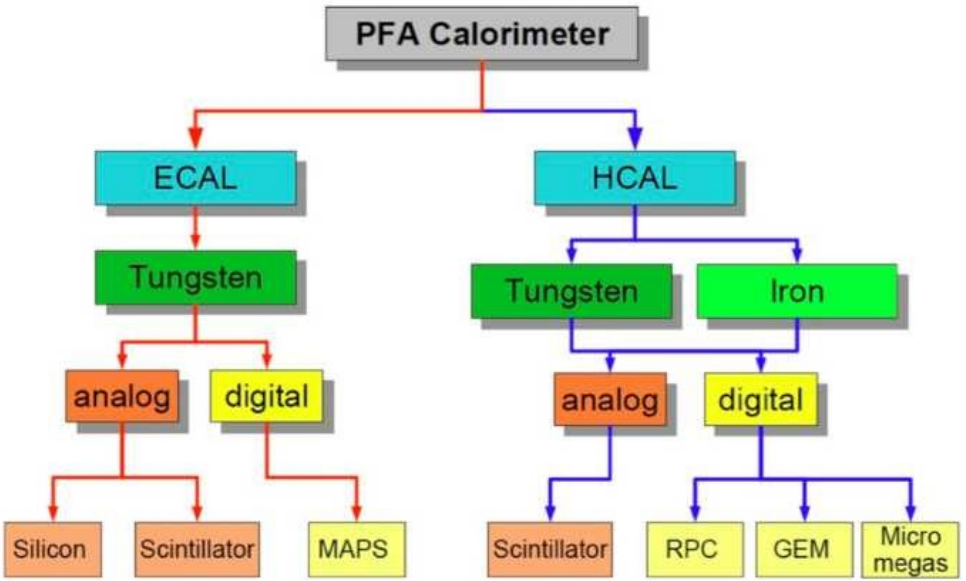
Ultracompactness: small Molière radius of calorimeters to minimize shower overlap

Extreme high granularity

Full coverage

Particle Flow Calorimetry R&D

Mainly organised within the CALICE



More than 300 physicists/engineers from ~60 institutes and 19 countries coming from the 4 regions (Africa, America, Asia and Europe)

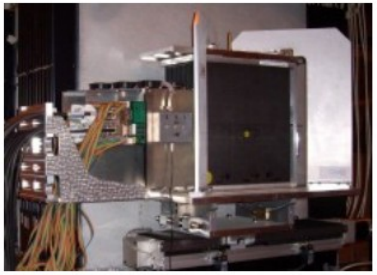
All projects of current and future high energy colliders propose highly granular calorimeters

Technological prototypes

Physics Prototype

Proof of principle

2003 - 2011



Number of channels : 9720

Pixel size: 1x1 cm2

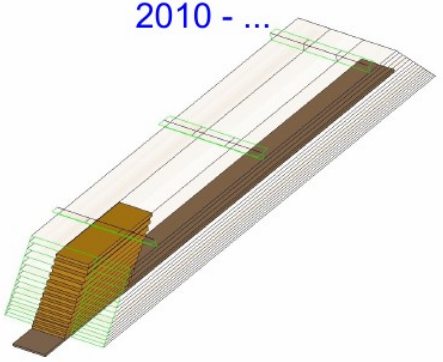
$R_{M,eff}$: ~ 1.5cm

Weight : ~ 200 Kg

Technological Prototype

Engineering challenges

2010 - ...



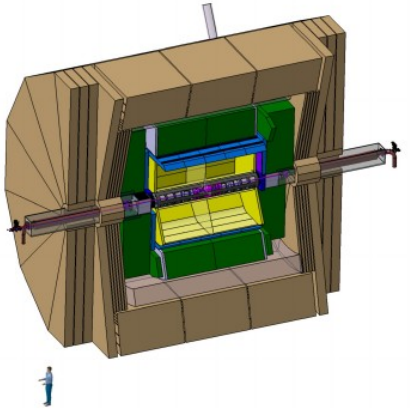
Number of channels : 45360

Pixel size: 0.55x0.55 cm2

$R_{M,eff}$: ~ 1.5cm

Weight : ~ 700 Kg

LC detector



ECAL :

Channels : ~100 10^6

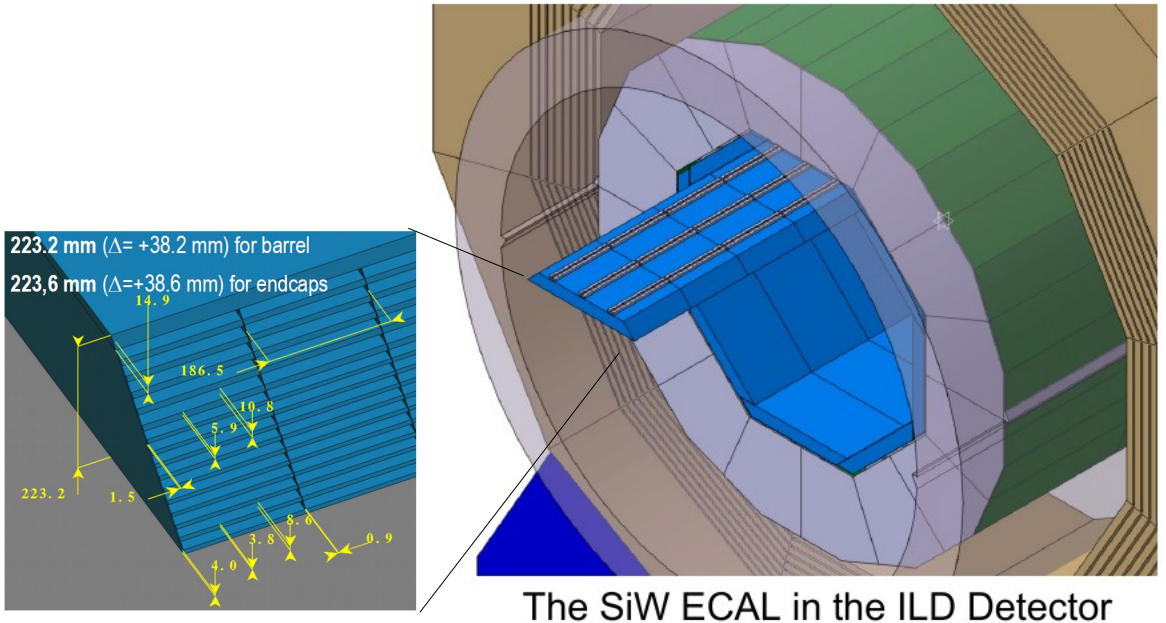
Total Weight : ~130 t

Towards a real detector

SiW-ECAL for future LC

- **Tungsten** as absorber material
  - **Narrow showers**
  - Assures **compact** design
  - Low radiation levels forseen at LC
  - X_0=3.5 mm, R_M=9mm, I_L=96mm

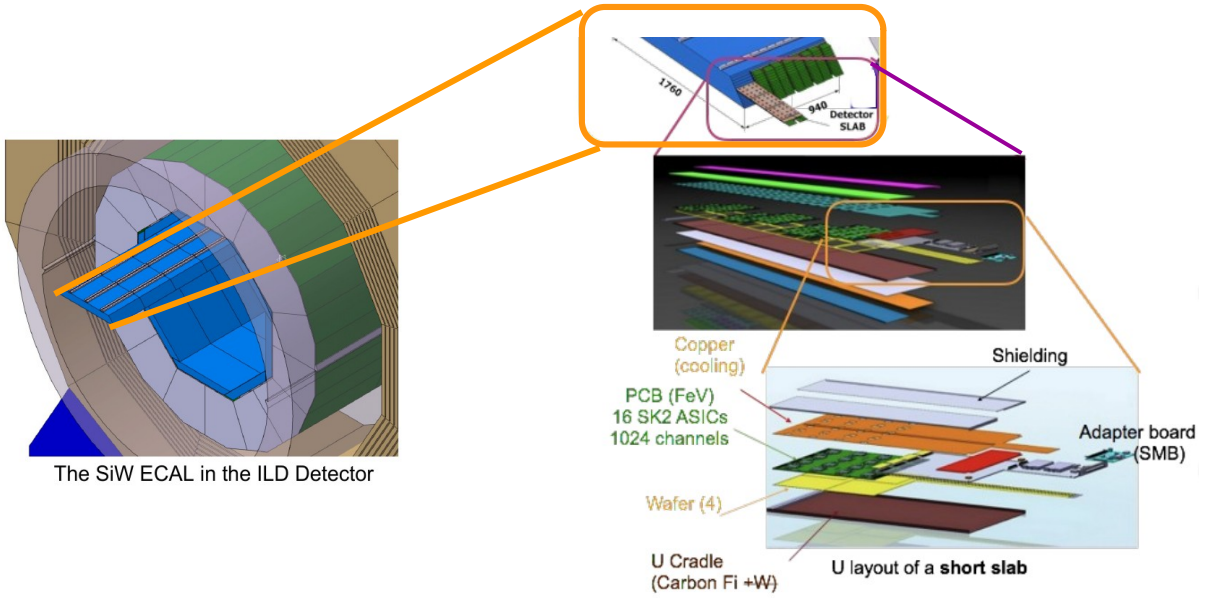
- **Silicon** as active material
  - Support **compact** designs
  - Allows **pixelisation**
  - **Robust technology**
  - **Excellent signal/noise** ratio



The SiW ECAL in the ILD Detector

The **SiW ECAL R&D** is tailored to meet the specifications for the **ILD** ECAL **baseline** proposal

SiW-ECAL for the ILD



The SiW ECAL in the ILD Detector

- O(10^4) long modules
- O(10^5) ASUs (PCB+wafer+ASIC)
- O(10^{6-7}) ASICS
- O(10^8) cells
  - 2000 m^2 of Si
- 130 T of tungsten

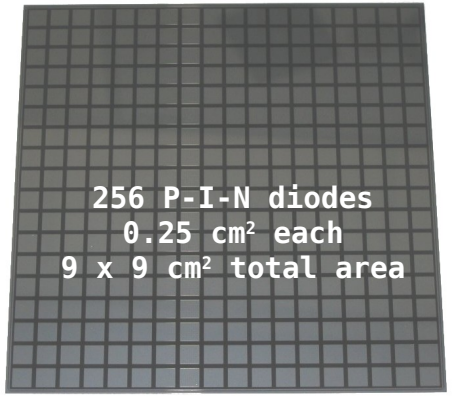
Cell size of 5x5 mm → all cells are self triggered + zero suppression

Successful application of PFA requires calorimeters to be placed insided the magnetic coil

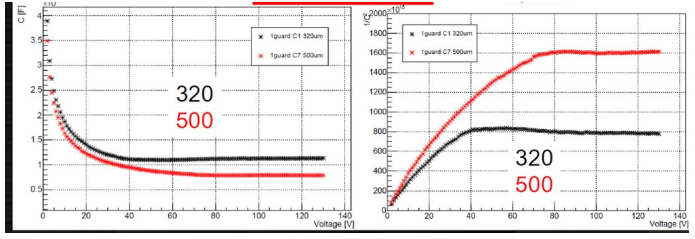
- Very compact design: Thickness of **20 cm for 20-30 active layers + 24X0 tungsten**
- Very limited space for inactive material (PCB, electronic components) → **No active cooling but Power Pulsing**

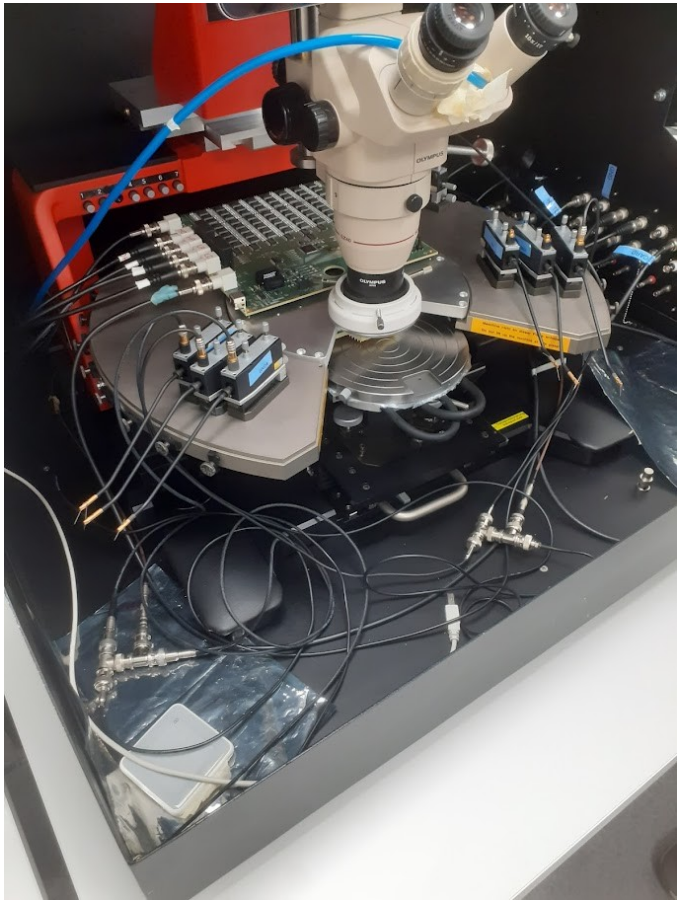
Sensors: Silicon P-I-N diodes wafers

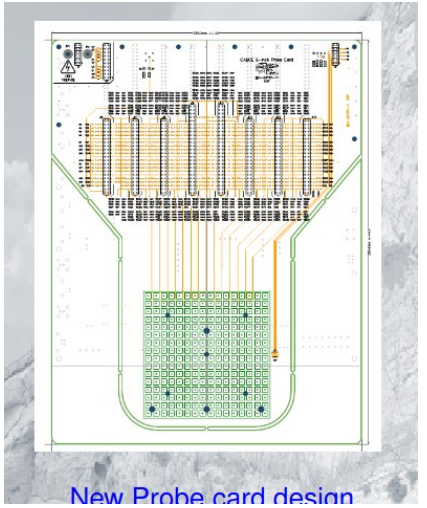
Designed for ILC : **Low cost, ~2000 m2**
Minimized number of manufacturing steps
Target is 2.5 EUR/cm2
Now : ~10 EUR/cm2 (Japan)



EUDET layout
Prototype from Hamamatsu





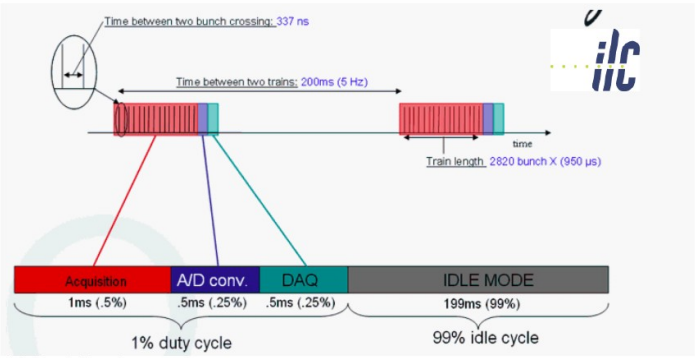


Probe-card designed by CERN for CALICE.

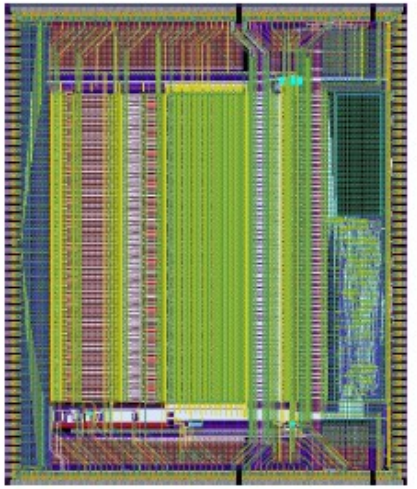
Switch card: designed for CMSHGCAL

Very Front End electronics

- **SKIROC** (Silicon Kalorimeter Integrated Read Out Chip)
  - SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels
  - High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)
  - **Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)**
  - **Dual readout: high and low gain**
  - **Auto-trigger at ~0.5 MIP**
  - Low Power: (25µW/ch) **power pulsing** switch off electronics bias currents during bunch trains



N.B. Final numbers may vary



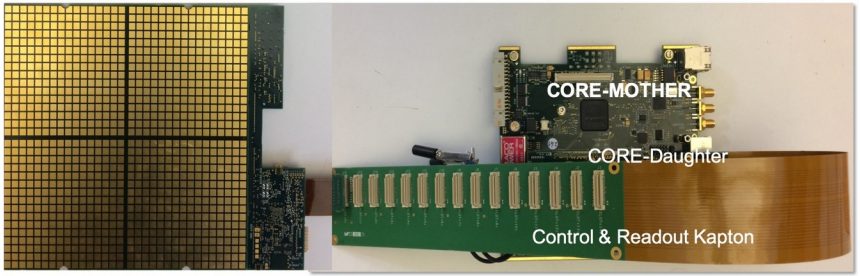
OMEGA Microelectronics

- Prototype version (Skiroc 2 and 2a) for R&D and beam tests
- Definitive version will be optimized for ILC and work in zero suppression conditions.

Ultra compact Digital Readout

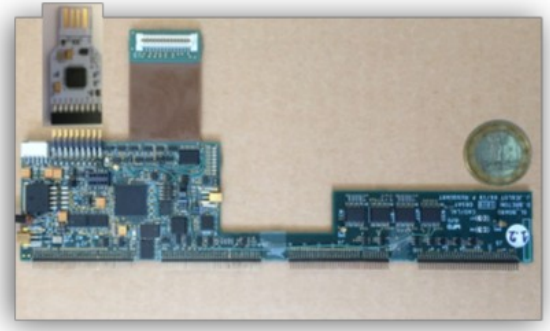
▶ Core Mother / Daughter system

- Controlling /reading up to 30 Slboards

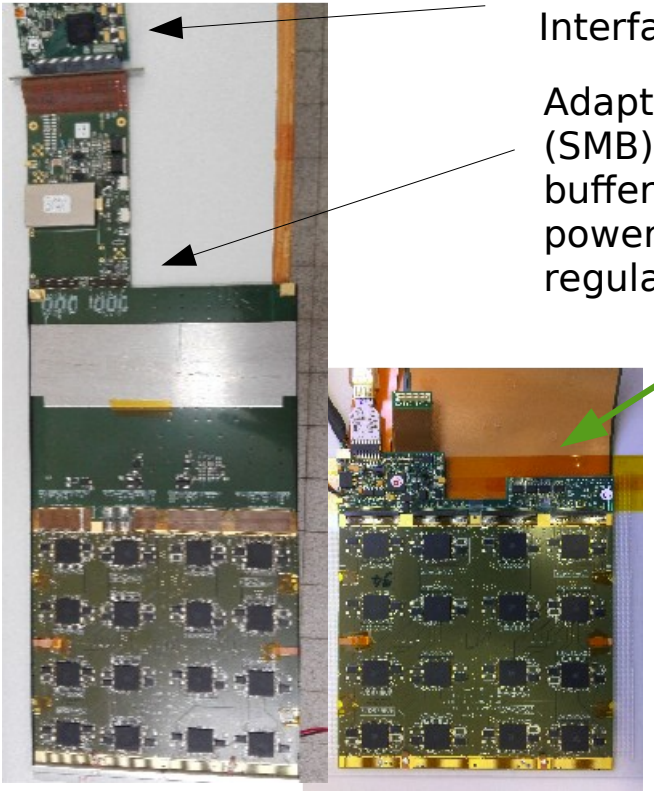


▶ The SL-Board

- **the sole interface for the ~10,000 channels of a 2m slab**



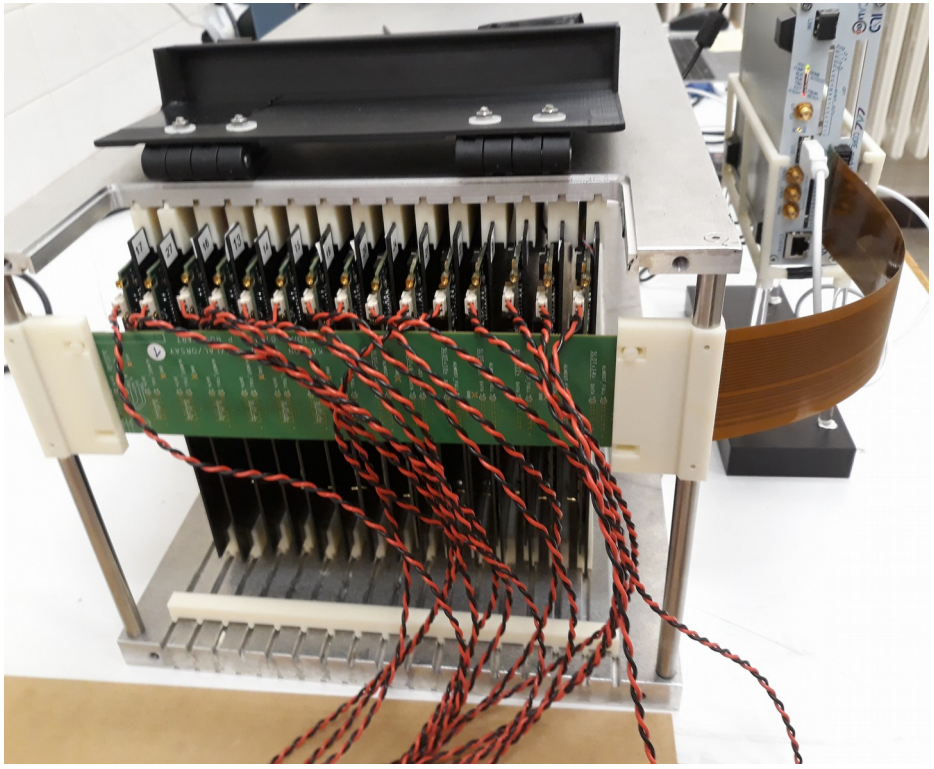
IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis



<2019 **≥2019**

The new DAQ fits the tight space requirements of the ILD

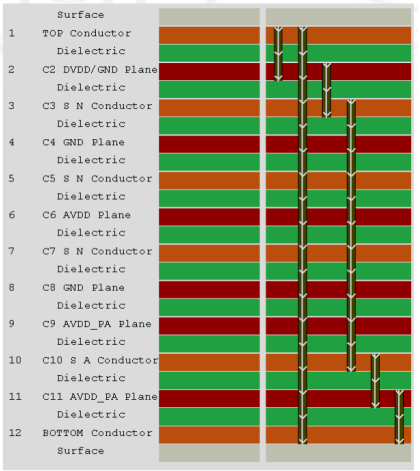
Ultra compact Digital Readout

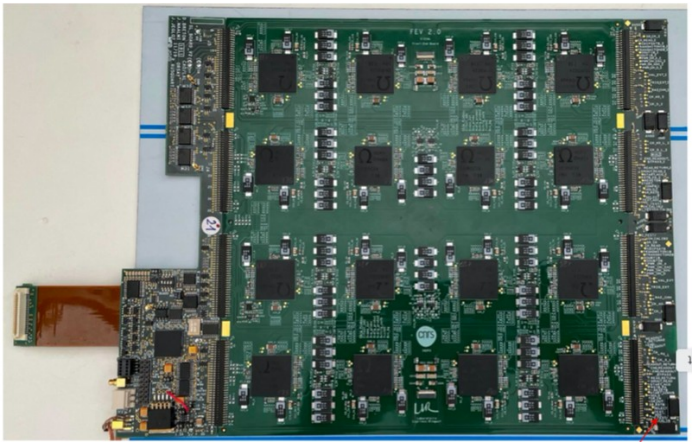


The new DAQ fits the tight space requirements of the ILD

New generation of PCBs

- Dimensions: 180mm x 180mm
  - Thickness: 1.6mm
- New features:
  - Locally buffered clock for configuration the system
  - New connector for interconnexion
  - Add connector & HV filter for individual wafer
  - New system with individual HV kapton
  - Analog probe to check connection to pixel connectivity



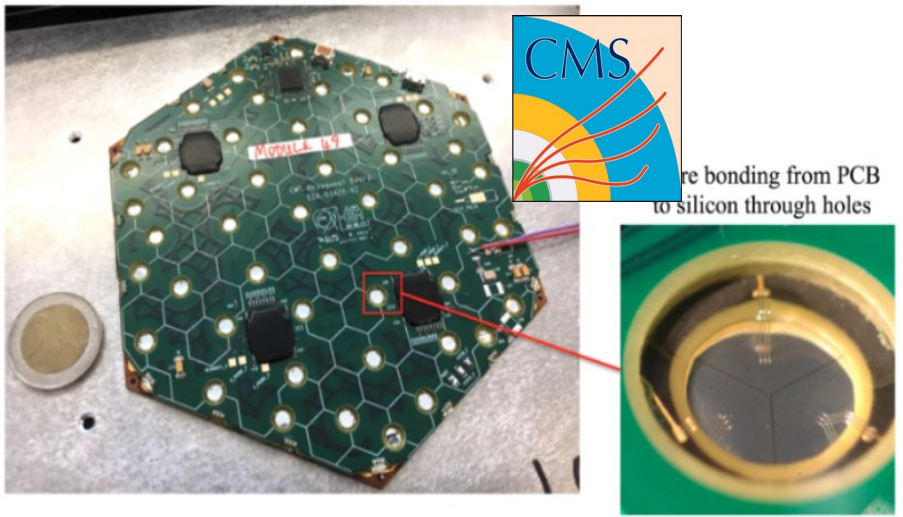


Power Pulsing Mode: new philosophy

- we limit the current through the Slab (current limiter present on the SL Board) which:
  - avoid driving high currents through the connectors and makes the current peaks local around the SKIROCs chips.
  - avoid voltage drop along the slab.
  - permits temperature uniformity
- We add large capacitors with low ESR for local energy storage (around each SKIROC chip)
- Generate local power supply with LDO (Low Drop Out) to remove voltage variations

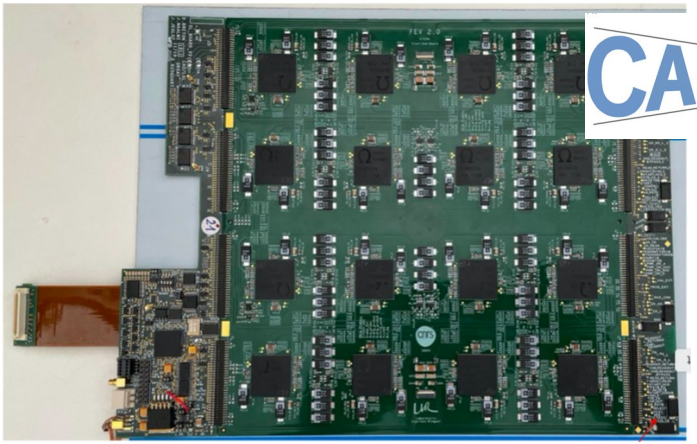
Sensor integration – high density channels

- Very dense **PCBs:**
  - i.e. at SiW-ECAL they are known as featuring 1024 readout channels (with digital, analogue, clock signals) in a 18x18 cm^2 board



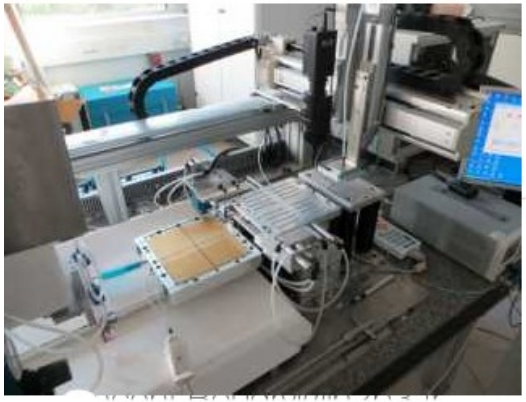
CMS HGCAL Hexaboard

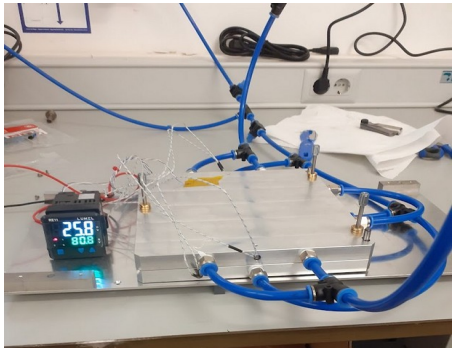
Wire bonding from PCB to silicon through holes



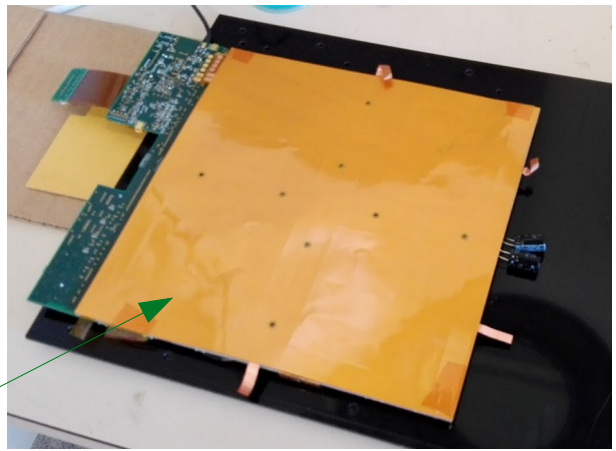
SiW-ECAL current prototype solution. --> 5x5mm² cells

Sensor integration – high density channels





Wafers are glued to PCB (robot at LPNHE & Kyushu U. & **IFIC 2023-2024)**



Sensor polarization through HV deliver via a copper/kapton sheet

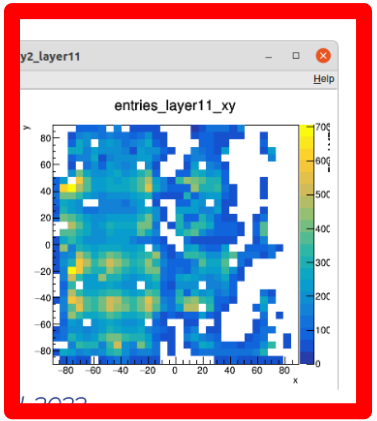
No space for wirebonding

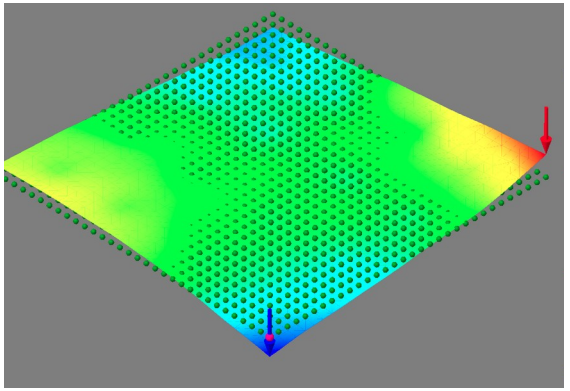
Glue with conductive epoxys epoxy+silver mixes

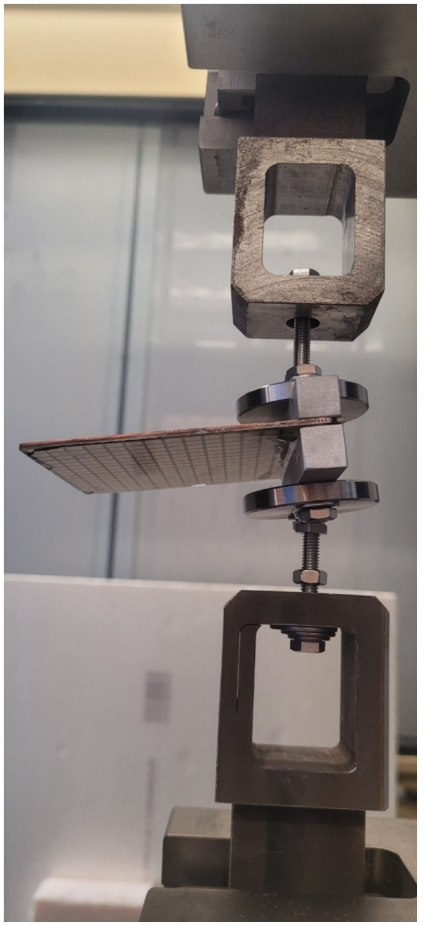
Low temperature curing (40-80 degrees)

Sensor connectivity degradation

- Since 2022: observation of partial delamination of several sensors



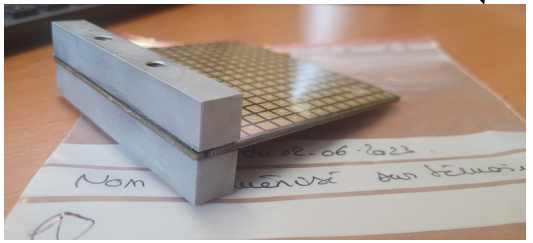




- Degradation? Mechanical stress due to PCB deformations ?
- Under investigation

Ongoing studies:

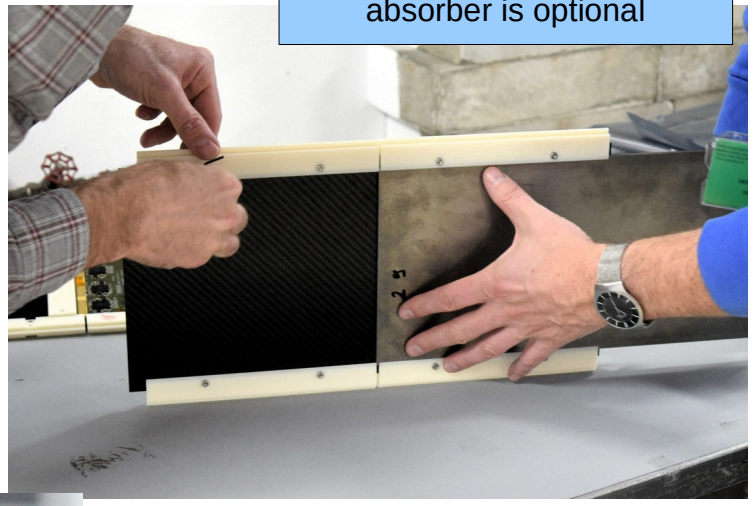
Testing different glues, underfill, tape solutions

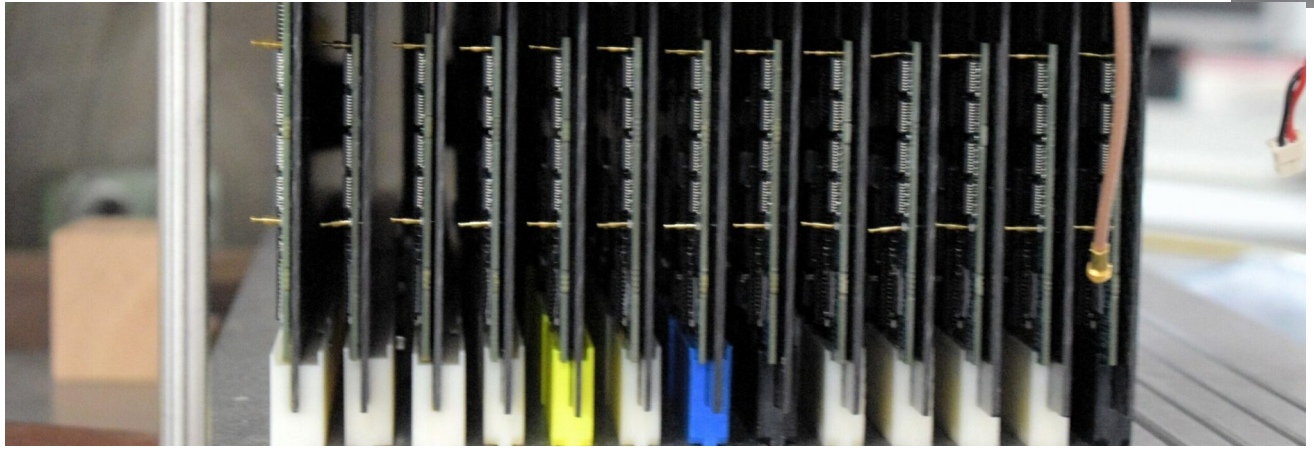


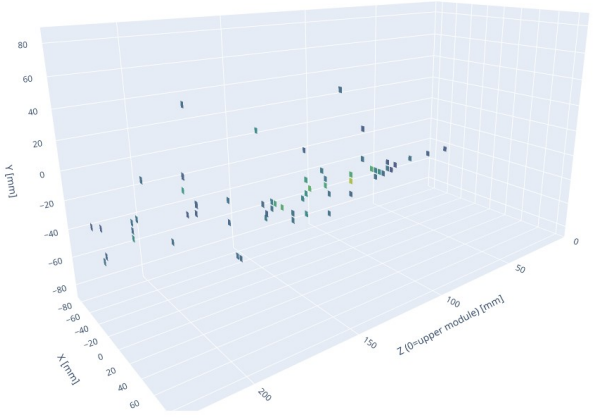
Test Beams End 2021-2022

- **15 layers with 1024 readout cells each**
  - **5.5mm si pads**
  - LHC calorimeter scale
  - But it fits in a suitcase
- **2 periods at DESY for commissioning and DAQ developments**
- **2 weeks at CERN**

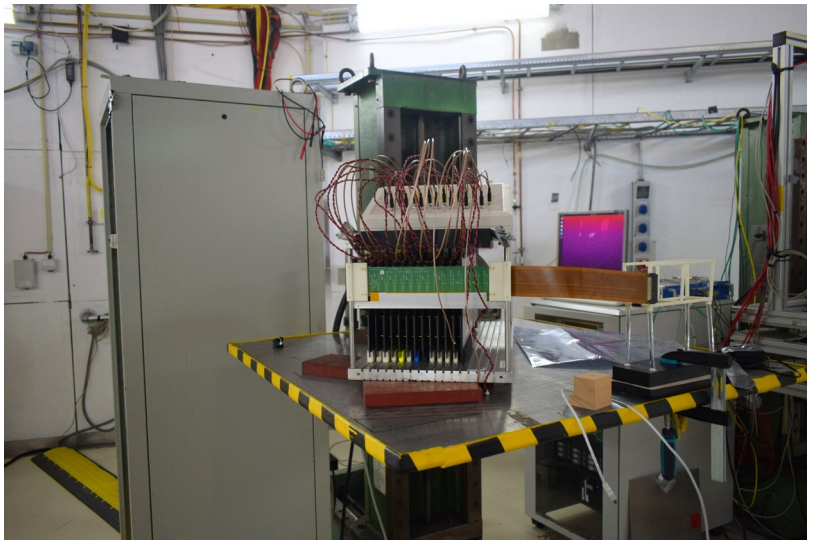
Flexible stack:
absorber is optional

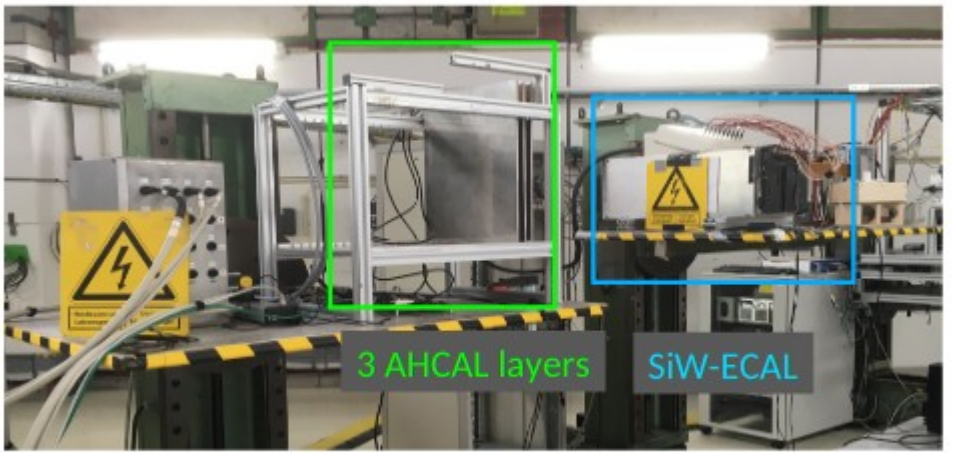




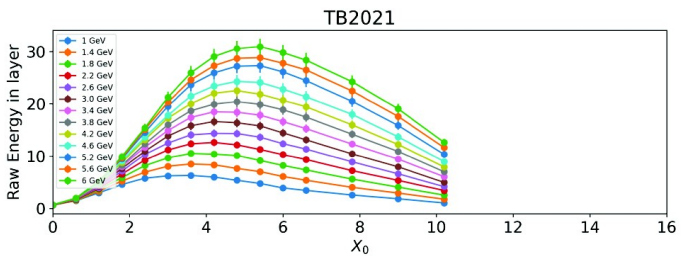


Test Beams DESY 2021-2022

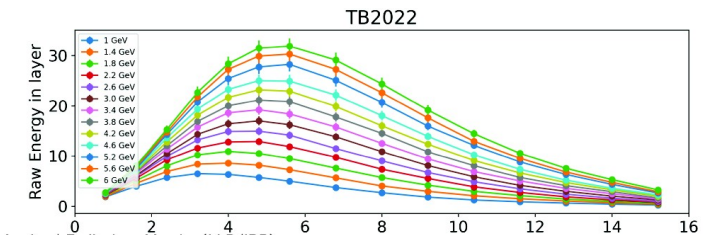




SiW-ECAL + AHCAL DAQ test @ DESY in March 2022



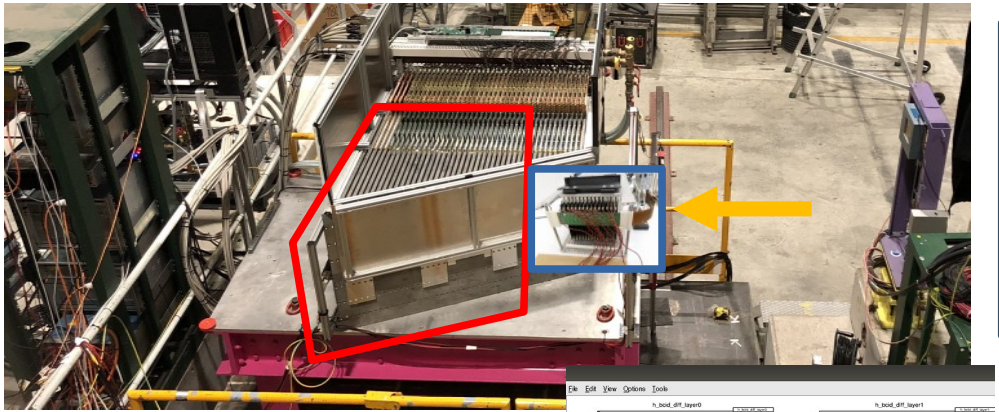
Preliminary simulation



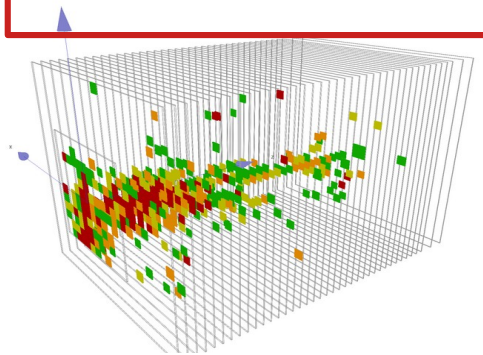
Preliminary simulation

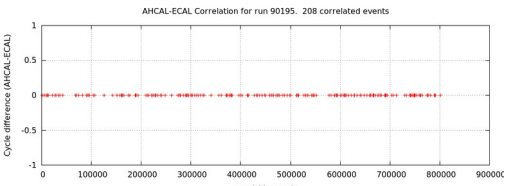
Common beam test CERN SPS 06/2022

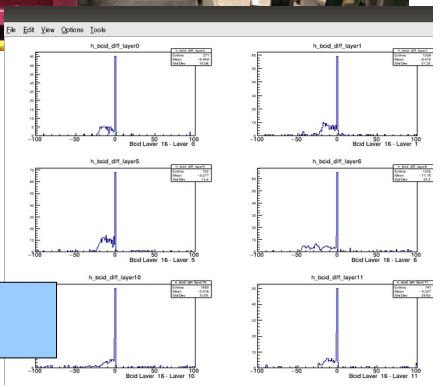
AHCAL :
- **38 layers 72×72 cm²**
- 3×3 cells scintillator + SiPM
- 1.7 cm Stainless Steel (~4λ)
- **6t, 1×1×1.5 m³**
- **20k channels**



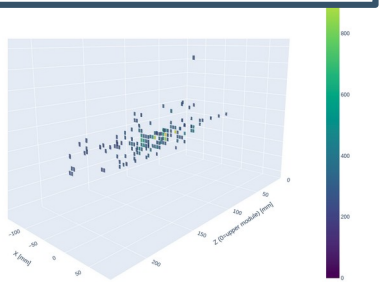
SiW-ECAL
- **15 layers 18×18 cm²**
- 0.5×0.5 cm² Si cells
- 2.8+5.6 mm W (21 X_0)
- 100 kg, 0.4×0.4×80 cm³
- **15k channels**







Synchronization checked online



Muons (150GeV), electrons (10-100GeV) and pions (10-150GeV)

Data analysis in progress: stay tuned

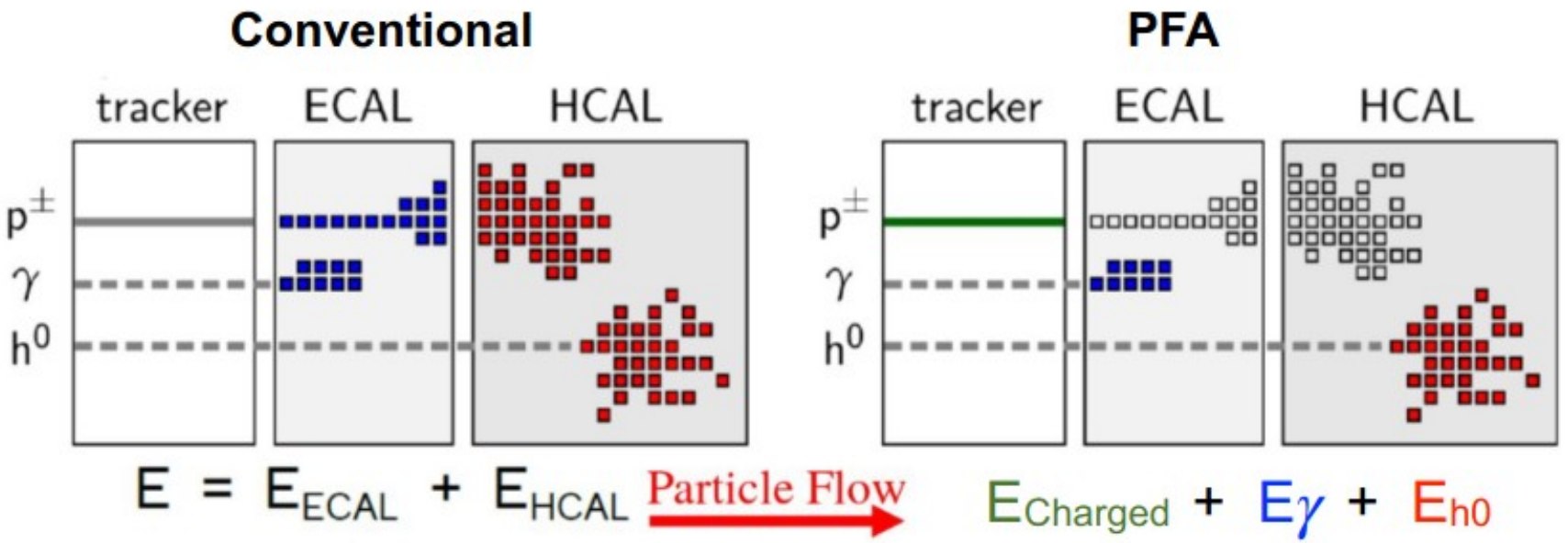
The path to Large Scale prototypes

- **Ongoing R&D** phase with the goal of **the construction of multilayer scale SiWECAL PF prototypes** → (within the new DRD collaborations)
  - With **high granularity** (up to 5x5mm²) → **15 new layers in construction**
  - **Extreme compactness** to ensure the smallest moliere radius
  - Fully implementing **power pulsing**!
  - To be tested in **beam facilities** in order to ensure a proper integration/interplay of the two sections (ECAL+HCAL) which is **crucial for PFA**
- **Adaptation** of the concepts to **different projects**
  - Lineal-vs-circular → low or high rates → Power pulsing or not, self trigger or not
  - e+e- vs hadron → no strict radiation hardness requirement vs the opposite
  - First phase of simulation studies required.
- Application of **new ideas**
- **Intermediate applications: LUXE**

Particle Flow Algorithms

Lepton Collider goal is around dE_{jet}/E_{jet} - 3-4%

(e.g. 2x better than ALEPH / ATLAS)



Example: jet created by a proton

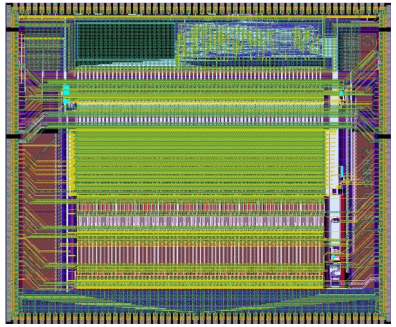
"traditional" detector : $E = E_{ECAL} + E_{HCAL}$

Particle Flow detector: $E = E_{track}$

Technological premises

Highly integrated (very) front end electronics

e.g. SKIROC (for SiW Ecal)



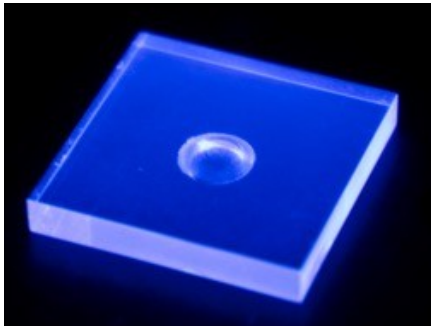
Size 7.5 mm x 8.7 mm,

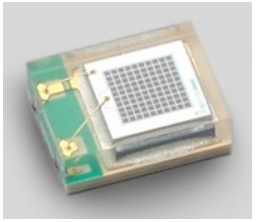
64 channels

- **Analogue measurement**
- **On-chip self-triggering**
- **Data buffering**
- **Digitisation**

  ... all within one ASIC

Miniaturisation of r/o devices





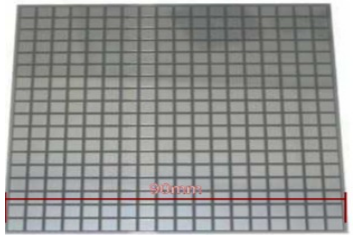
- Small scinitllating tiles
- (Low noise) SiPMs

Power pulsed electronics
to reduce power consumption…
Compactness –> no space left for active cooling systems

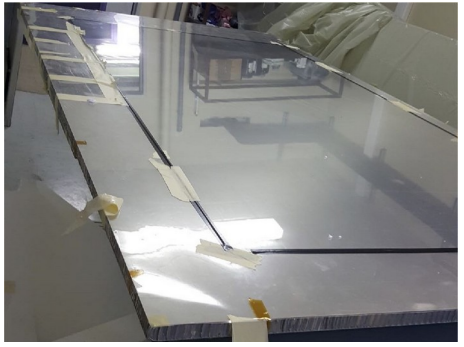
Self trigger of individual cells below MIP level

Large surface detectors

Si Wafer

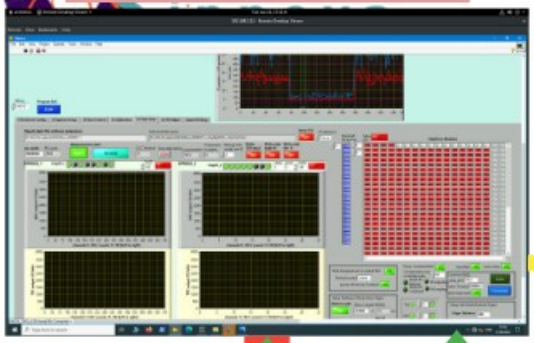


RPC layers



Many things that look familiar to you today were/are pioneered/driven by CALICE

AHCAL LabView



Clocks, Busy

LDA

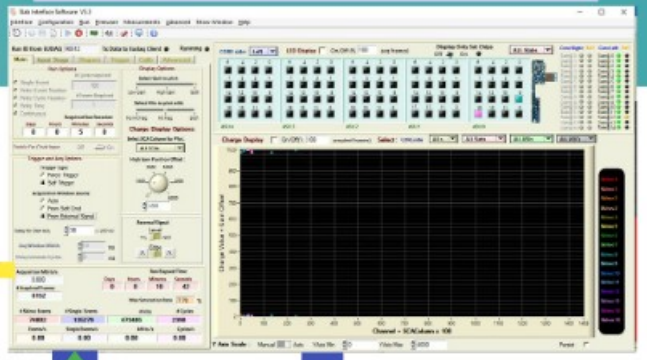
CCC

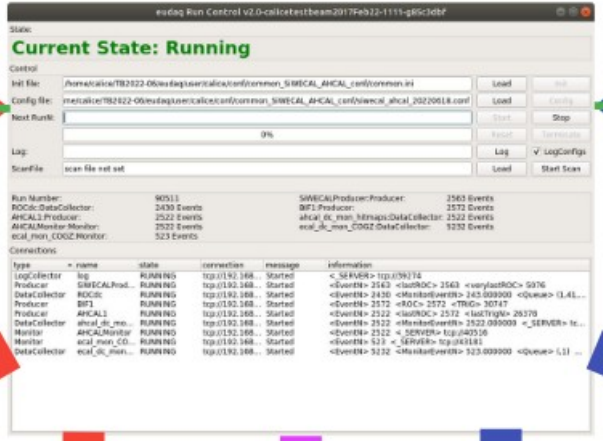
CORE

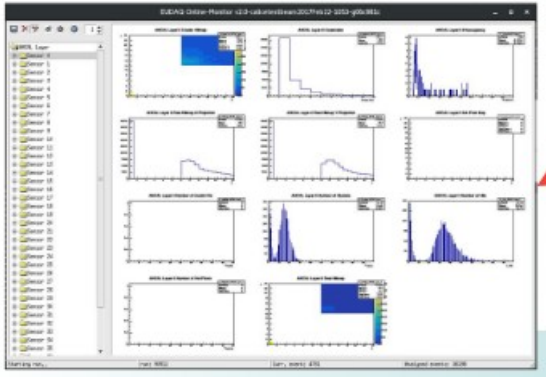
Command

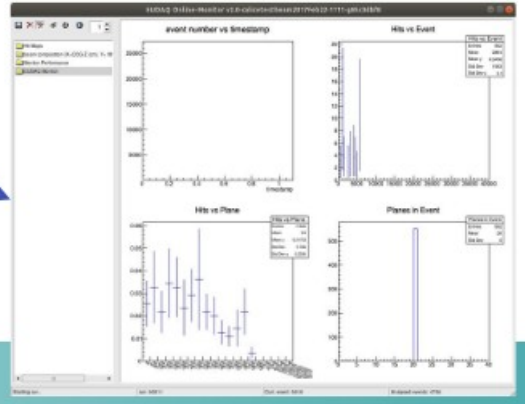
Configs

SiW-ECAL LabWindows









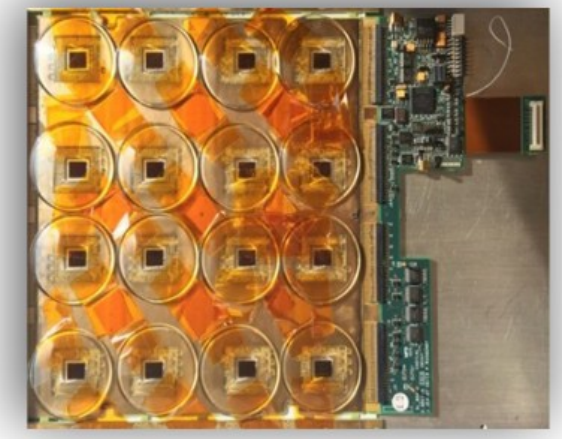
Readout modules

- Very dense **PCBs *aka* FEV** with 1024 readout channels (with digital, analogue, clock signals) in a

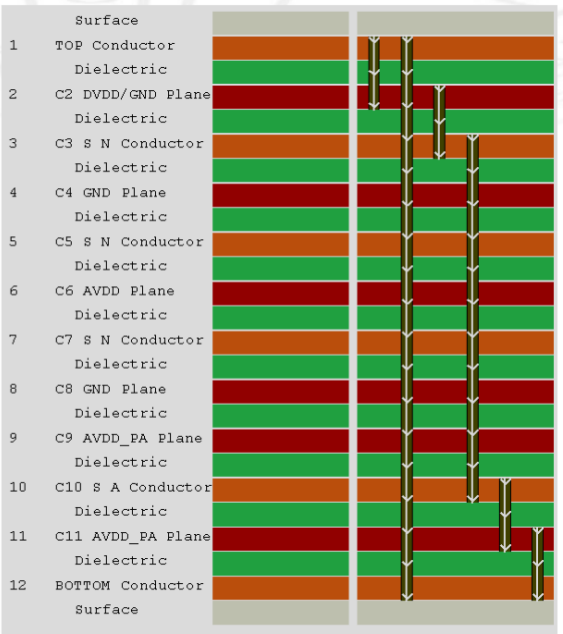
FEV10-12

- ASICs in BGA Package
- Incremental modifications
  - From v10 -> v12
  - **Main “Working horses” since 2014**

FEV_COB



- ASICs wirebonded in cavities
- COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12



The FEV zoo (from 2014)

- Very dense **PCBs *aka* FEV** with 1024 readout channels (with digital, analogue, clock signals) in a

FEV10-12

Validation of the technology concept "culminated" in 2017-18 with a series of test beams

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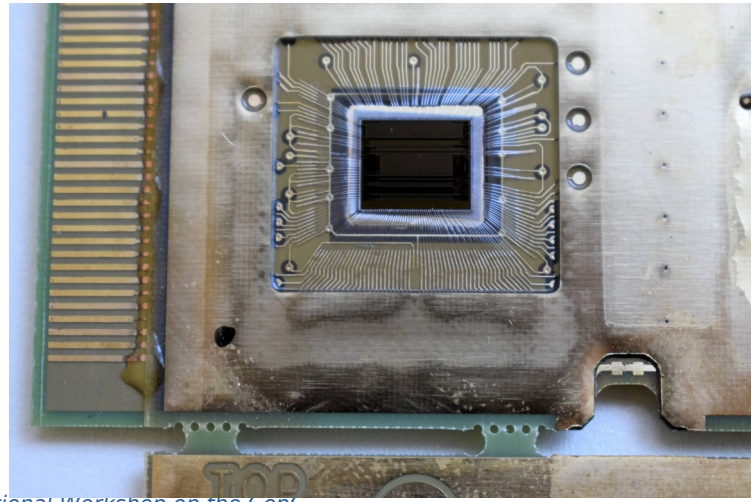
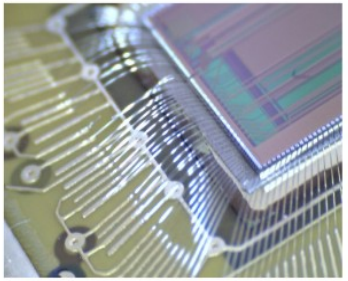
- ASICs in BGA Package
- Incremental modifications
  - From v10 -> v12
  - **Main "Working horses" since 2014**

Ultra thin PCBs

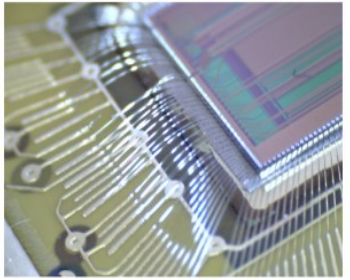
- **PCB with naked die placed in carved cavities and wirebonded to the board**
- Very thin board ~1.2mm (ILD requires 1.8mm for board and comp.)
  - 10 layers (+ gnd cupper layer)
  - To be compared with 2.8-3mm of the FEV10-13
  - but they include BGA SKIROCs and extra components as decoupling capacitances...!!



Zoom into ASIC cavities



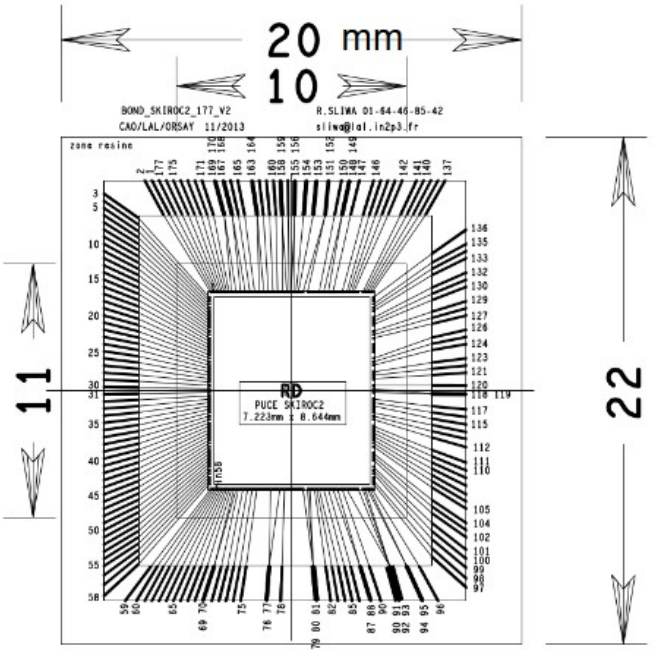
Before application of epoxy



After application of epoxy

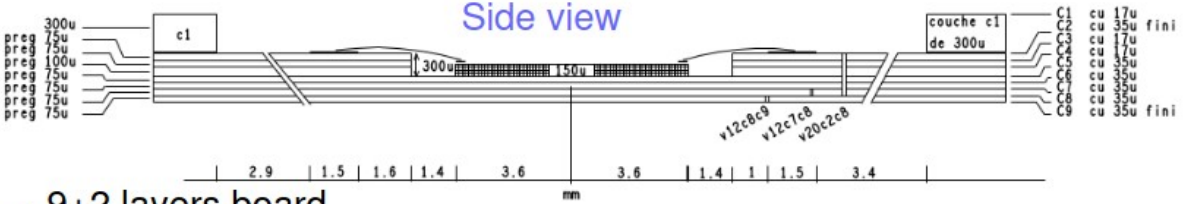
FEV11_COB – Some Technical Details

Bonding scheme

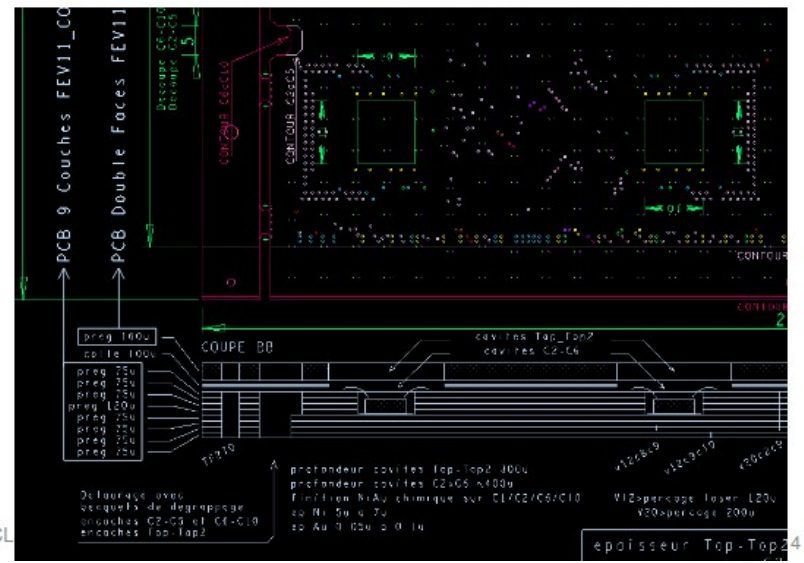


- ~177 Bonding wires
- Bonding by CERN Bondlab
- Regular exchange allowed to iron out early shortcomings

Side view

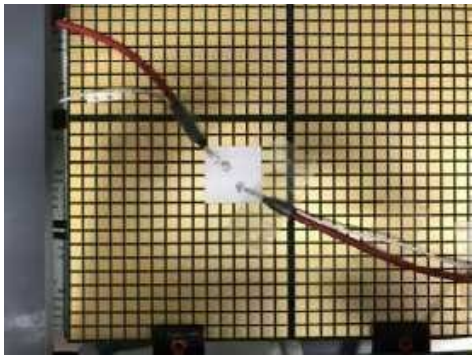


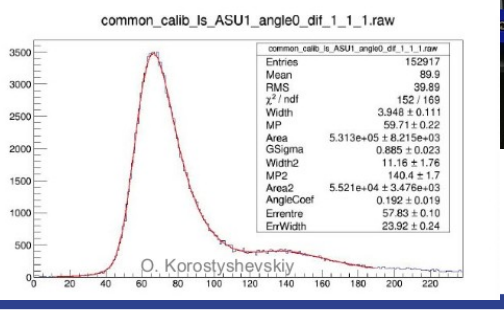
- 9+2 layers board
- Overall height ~1.2mm
- ASICs buried in cavities to ensure overall flatness
  - Need to make sure that bonding wires don't pass board surface



Electrical prototype of Long Slab

- Daisy chain of 8 ASU (extendable to 12)
- Corresponding to typical barrel length
  - 2m long !
- Electrical, electronic and mechanical challenges
  - Power delivery through the full length
  - Very long signal, control, clock lines
  - Very thin and long modules... wit silicon wafers glued in the back



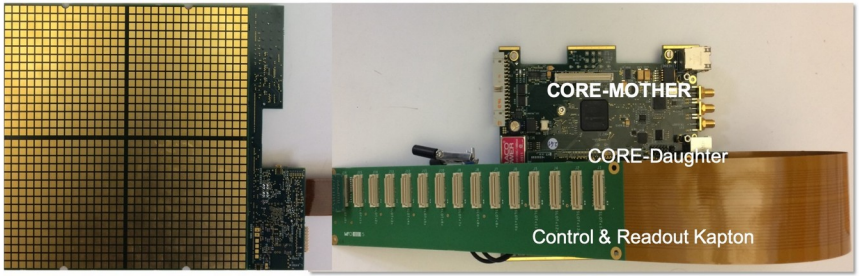


DESY@2018

Ultra compact DAQ

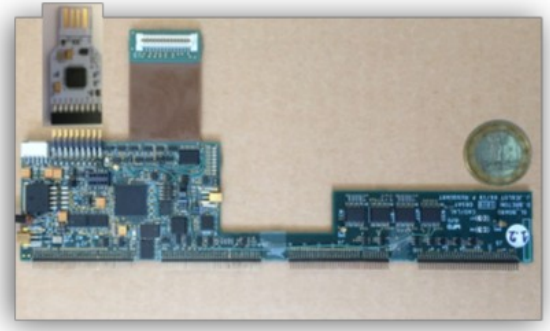
▶ Core Mother / Daughter system

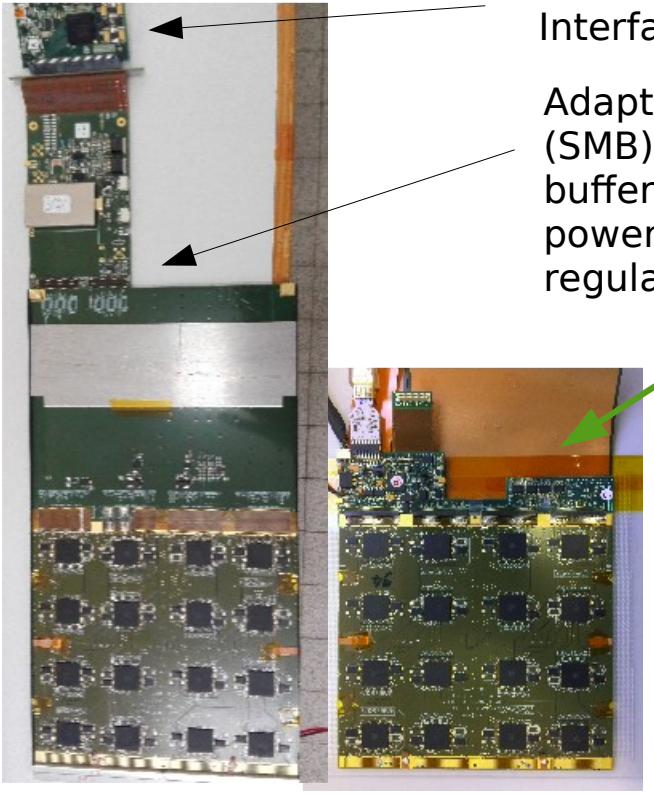
- Controlling /reading up to 30 Slboards



▶ The SL-Board

- the sole interface for the ~10,000 channels of a 2m slab





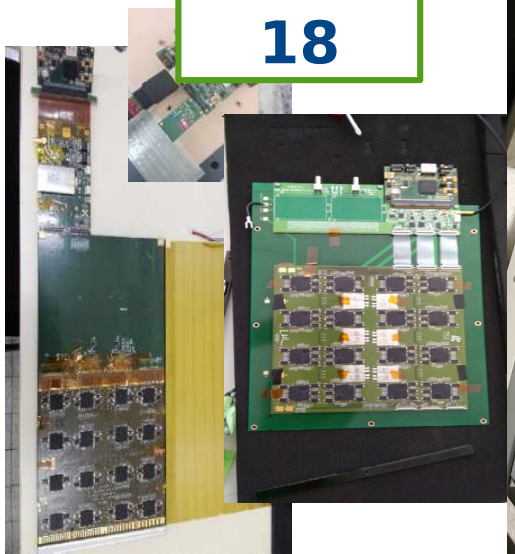
<2019 ≥2019

The new DAQ fits the tight space requirements of the ILD

Technological prototype: time travel

2010-2015

2010-18



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2018-22