CEPC vertex detector prototype status

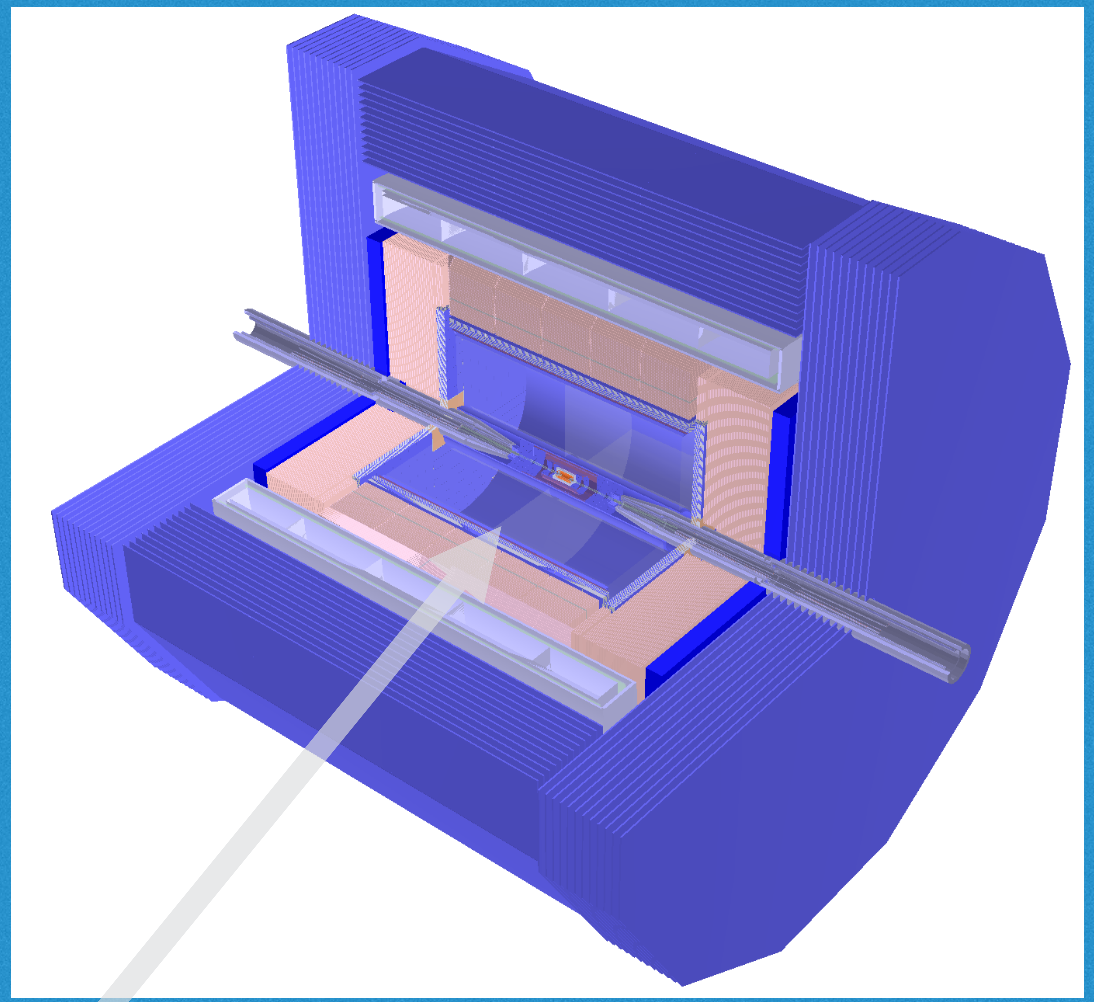
Zhijun Liang (IHEP)
For the CEPC vertex detector prototype team

CEPC detector concept

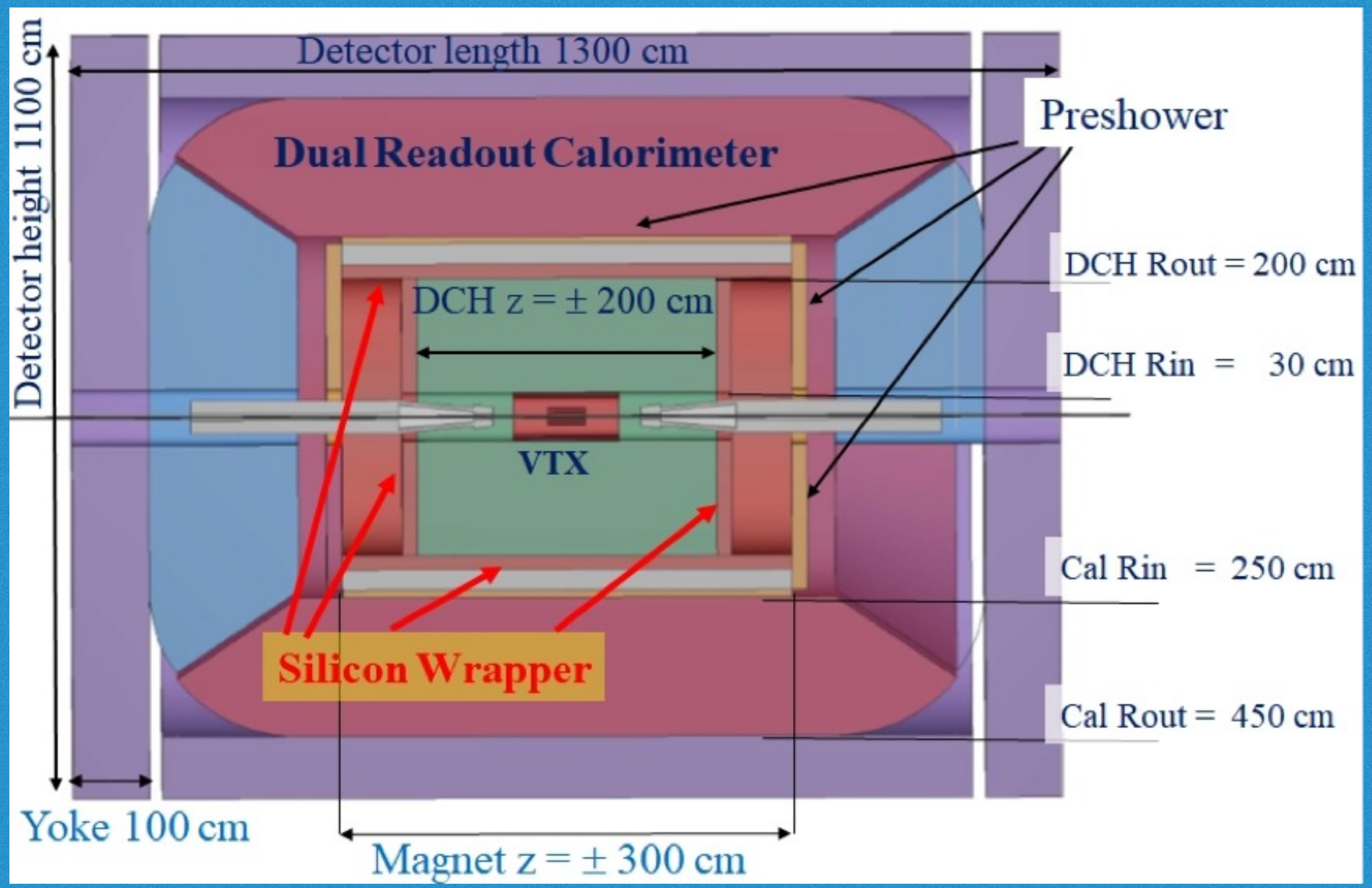
CEPC plans for 2 interaction points

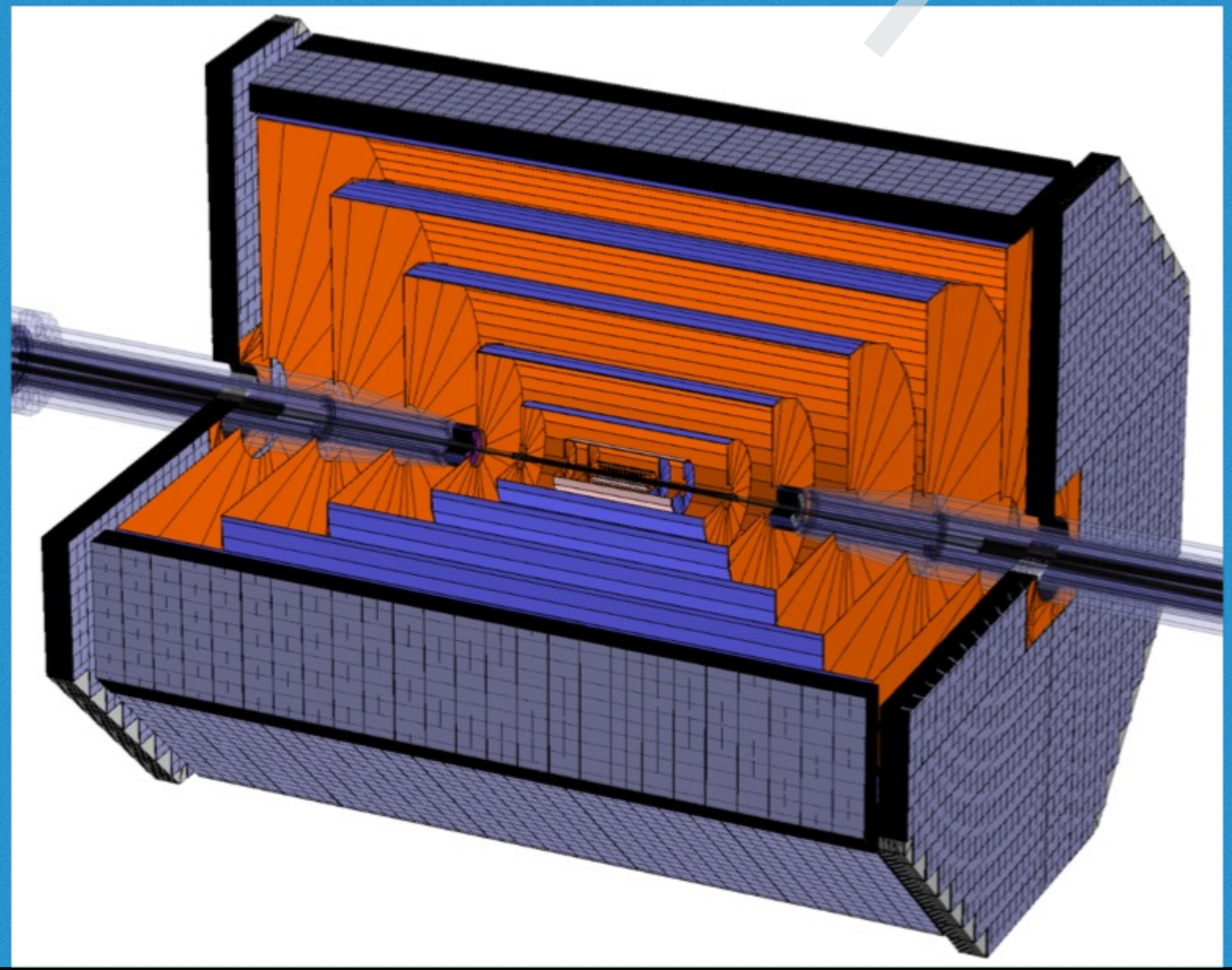
➢ **All four detector concepts require high-precision silicon vertex detectors**

ILD-like detector (3 Tesla)



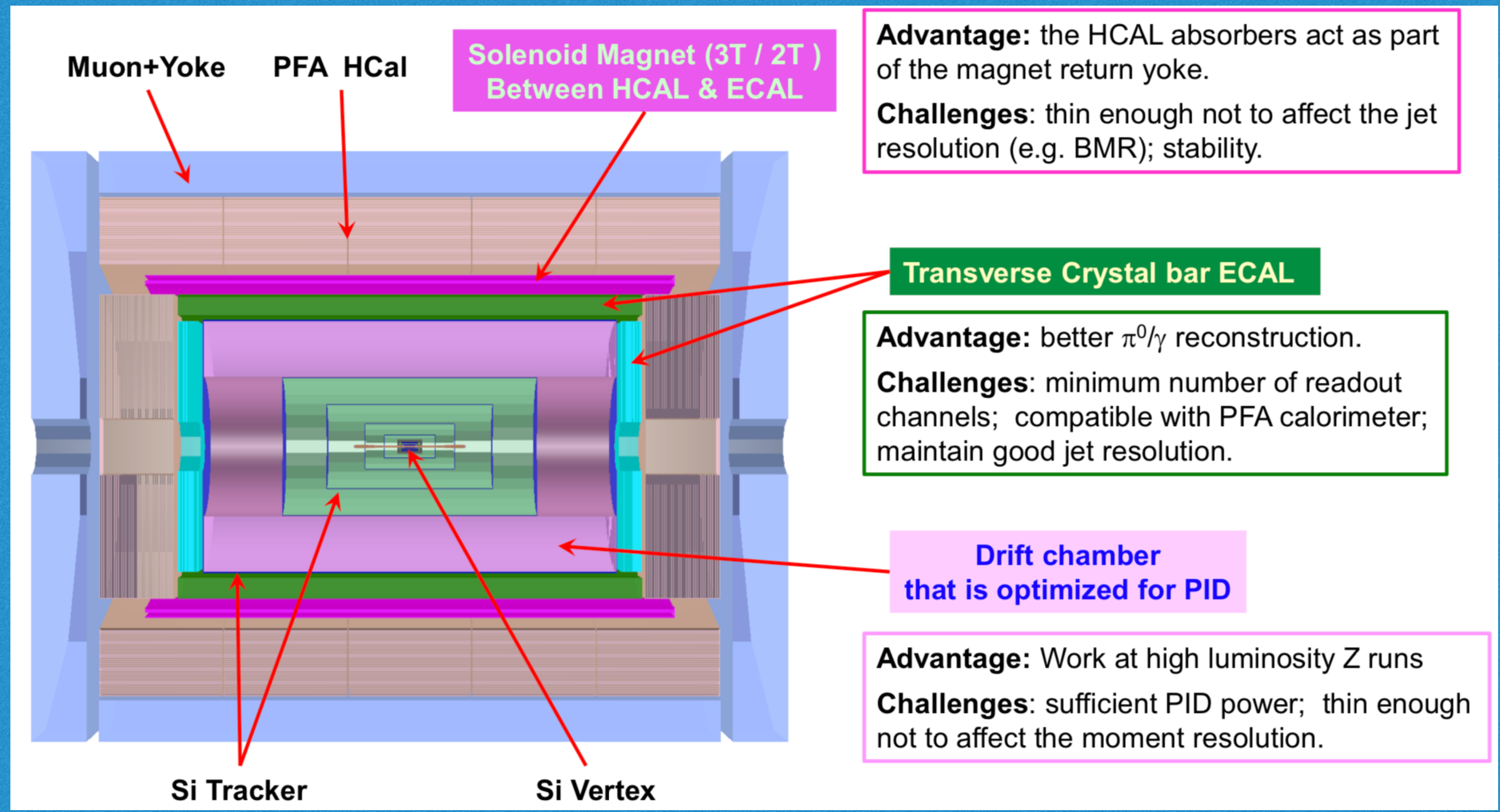
Low magnetic field concept (2 Tesla)





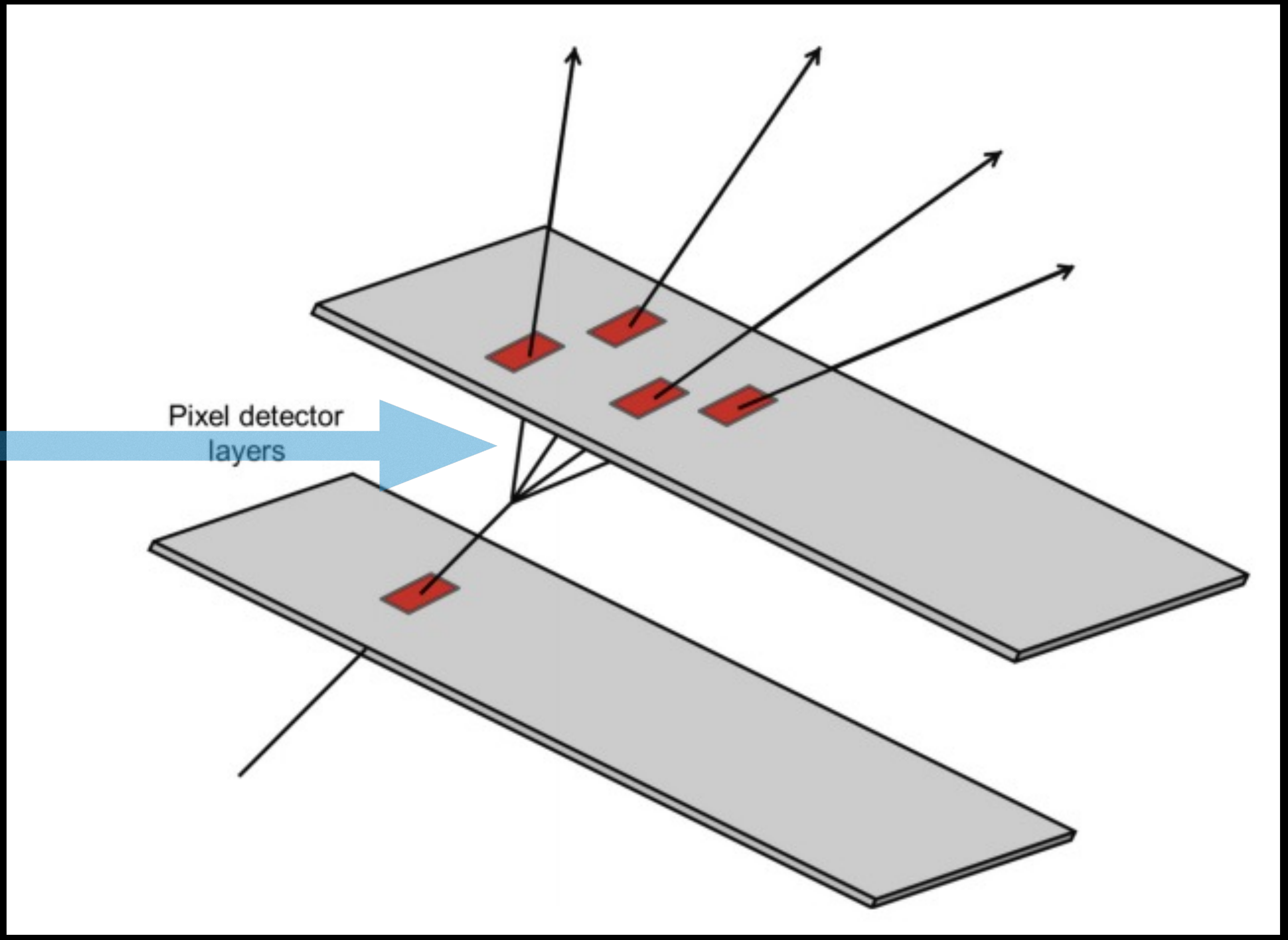
Full silicon tracker concept

4th concept



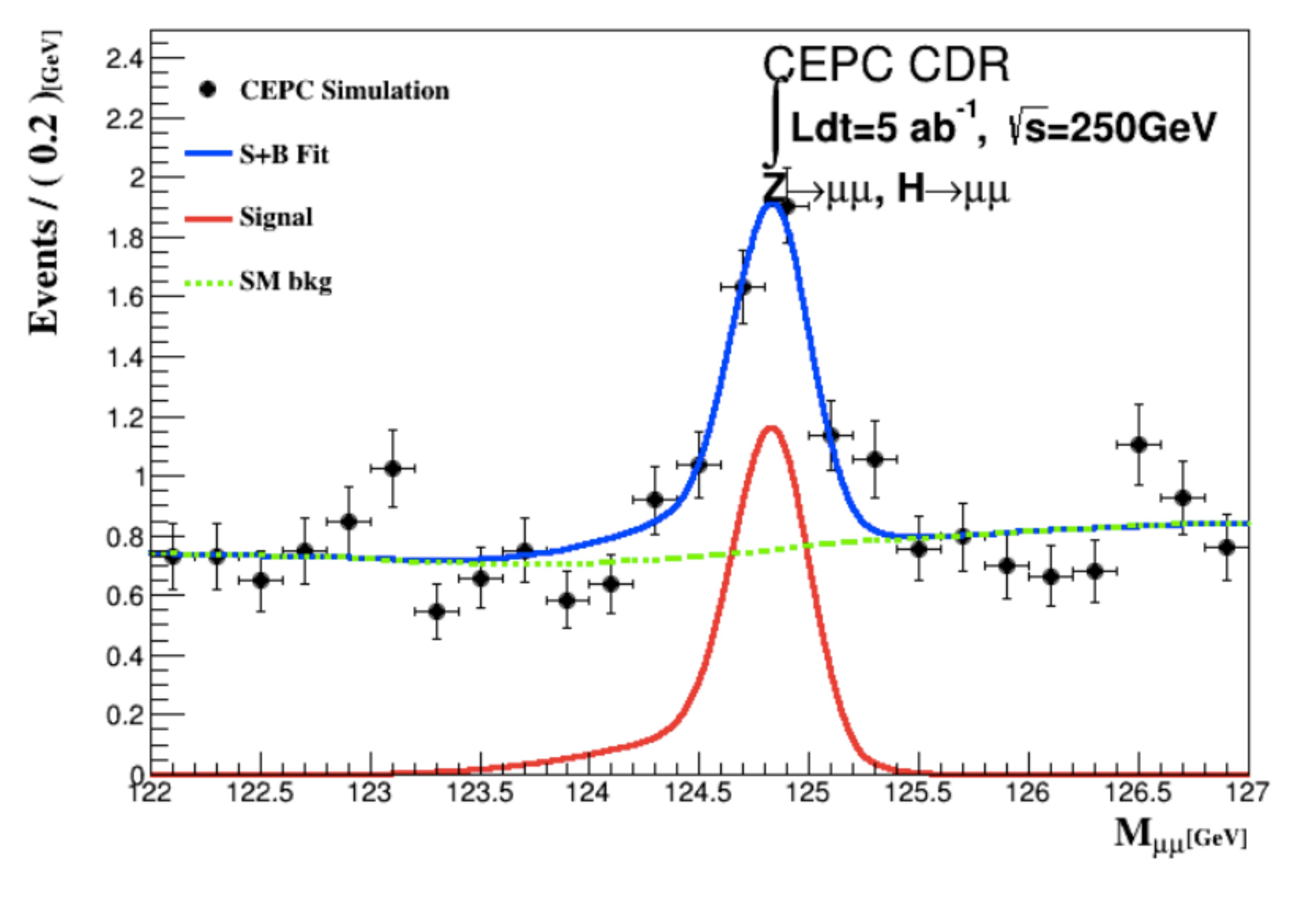
Vertex detector: Physics goal

- Produce a world-class vertex detector prototype
  - Small inner radius, close to beam pipe
  - Spatial resolution: 3~5 μm (pixel detector)
  - Low material budget <0.15% X0 per layer
  - Timing resolution: ~25ns (40MHz collision @ Z pole)



- Physics motivation
  - Higgs precision measurement
  - $H \to bb$ precise vertex reconstruction
  - $H \to \mu\mu$ (precise momentum measurement)

Need tracking detector with high spatial resolution

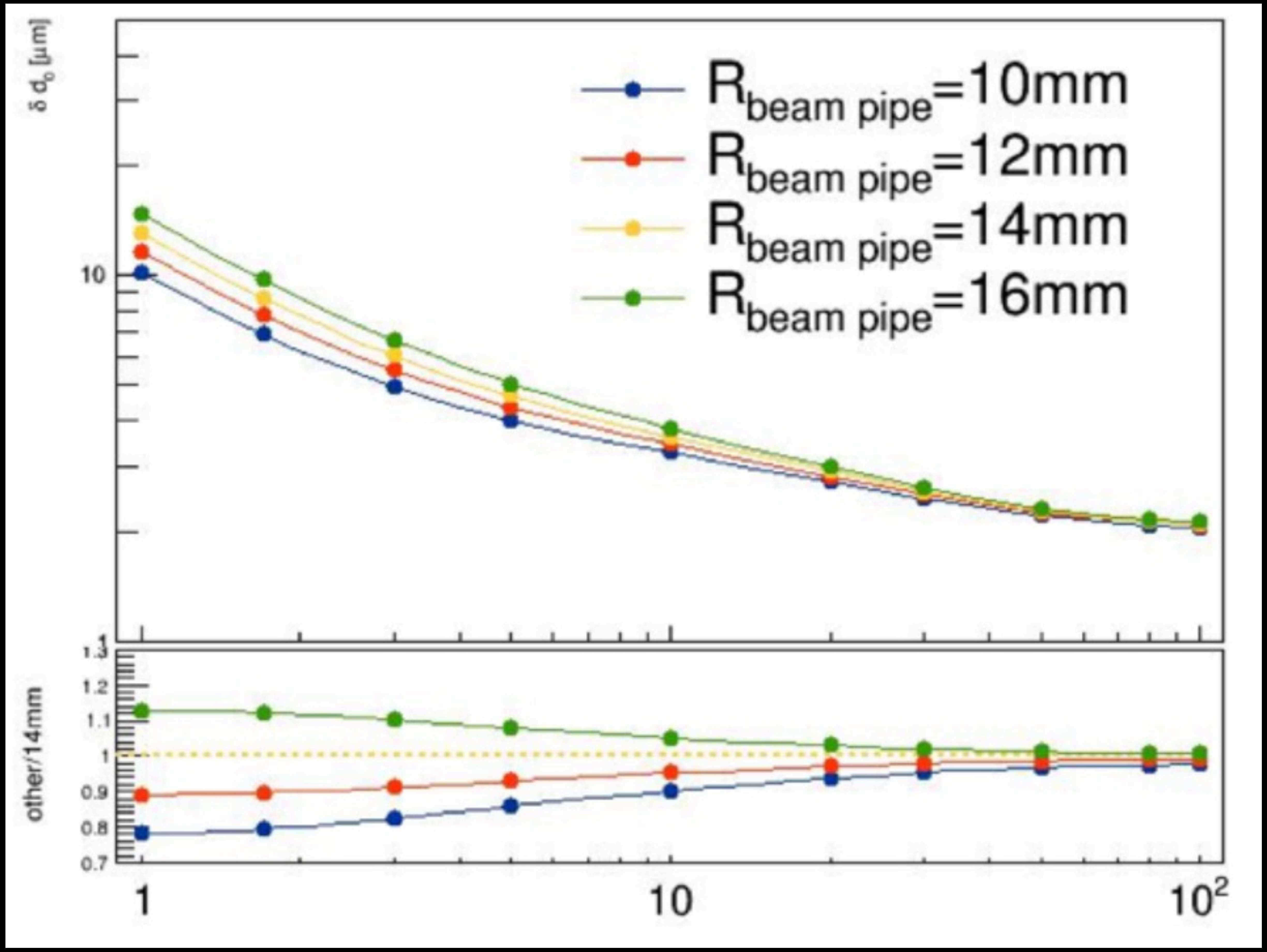


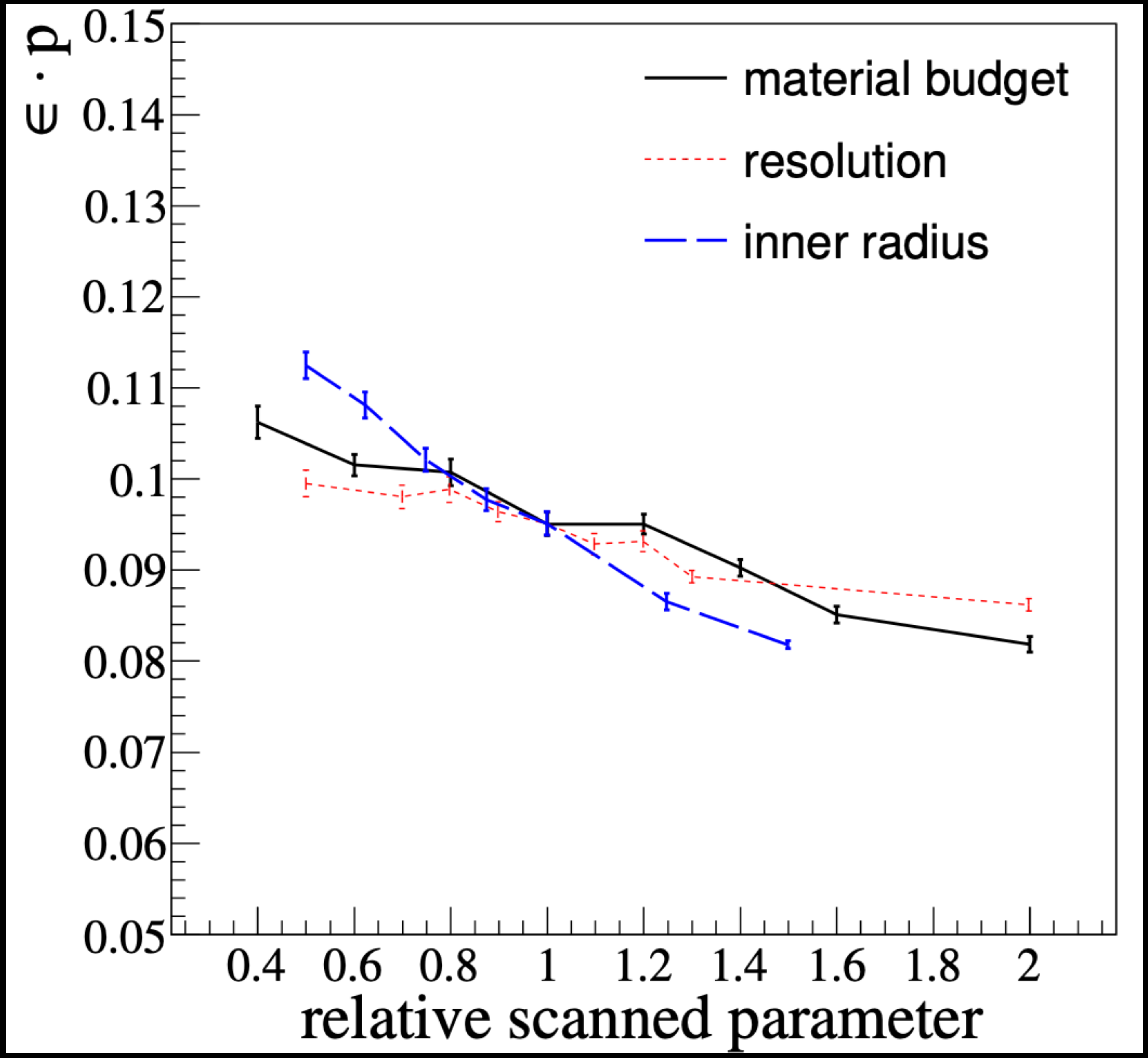
- Main technology
  - Develop the know-how in China to build such detector
  - High spatial resolution technology → pixel detector
  - Radiation resistance technology

Requirement on vertex detector

C-tagging performance

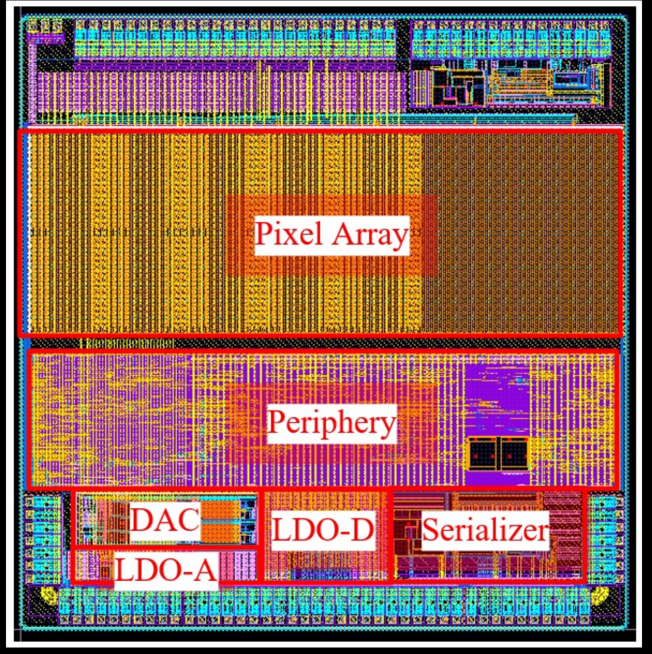
- 1st priority: Small inner radius, close to beam pipe (new baseline beam pipe radius=10um)
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor： 3~5 μm
- Global Timing resolution of CEPC tracker: ~25ns (40MHz collision @ Z pole)

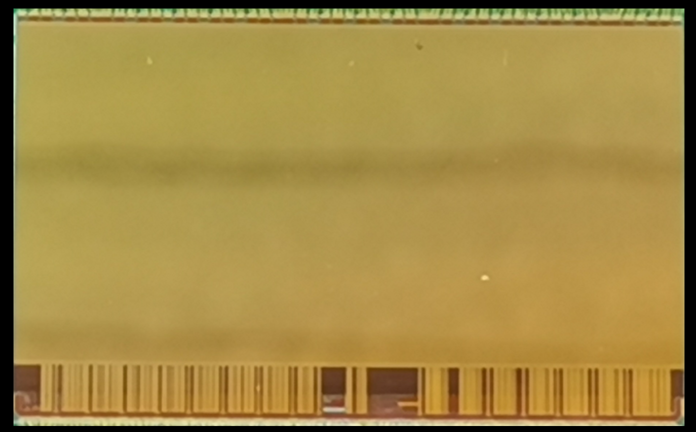




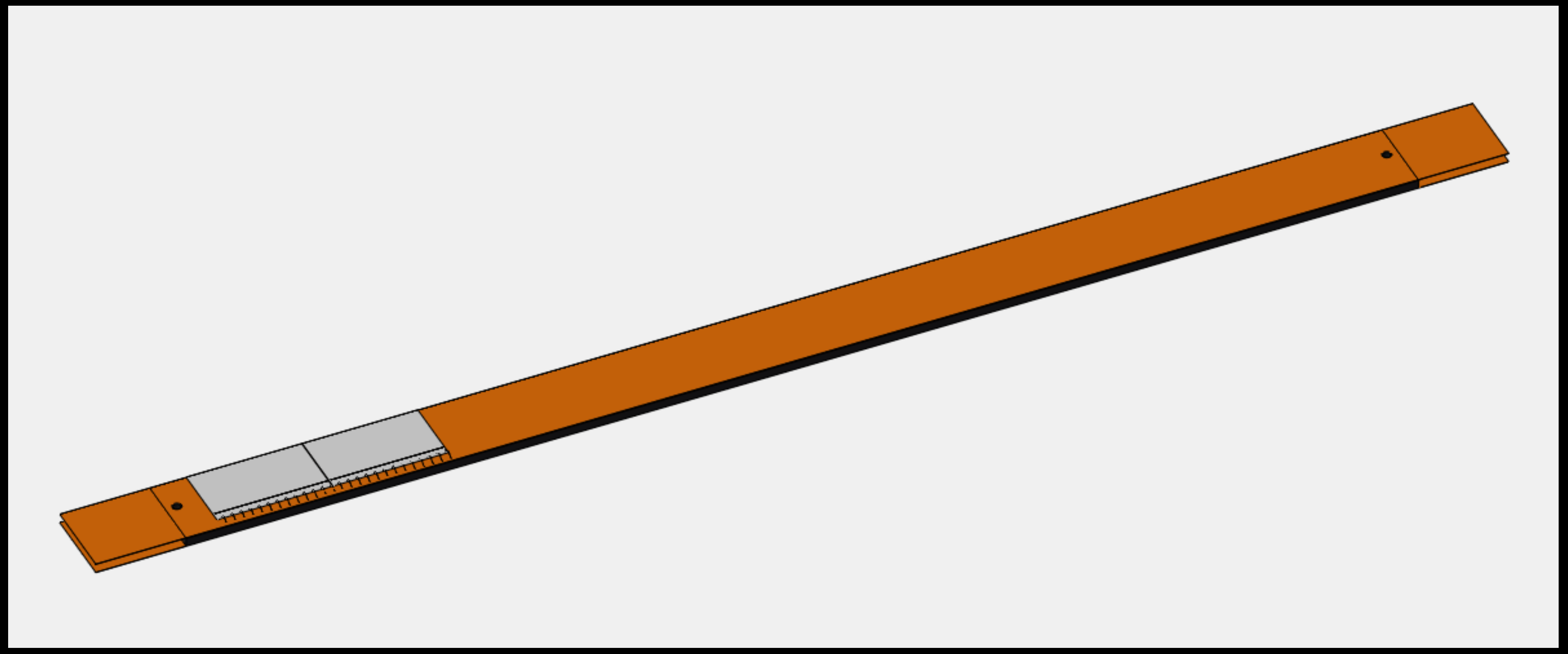
Overview of CEPC vertex detector R & D

CMOS imaging sensor prototyping

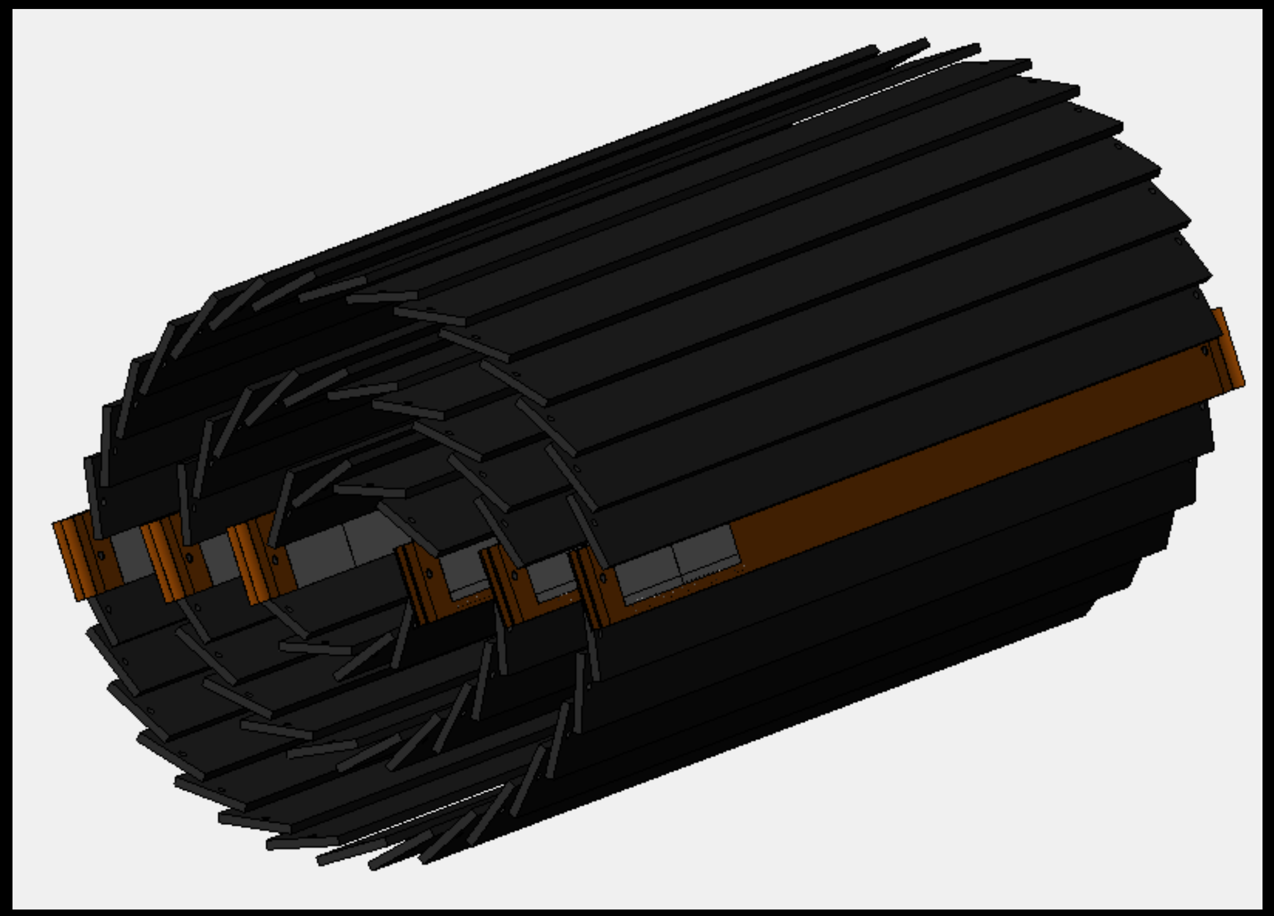


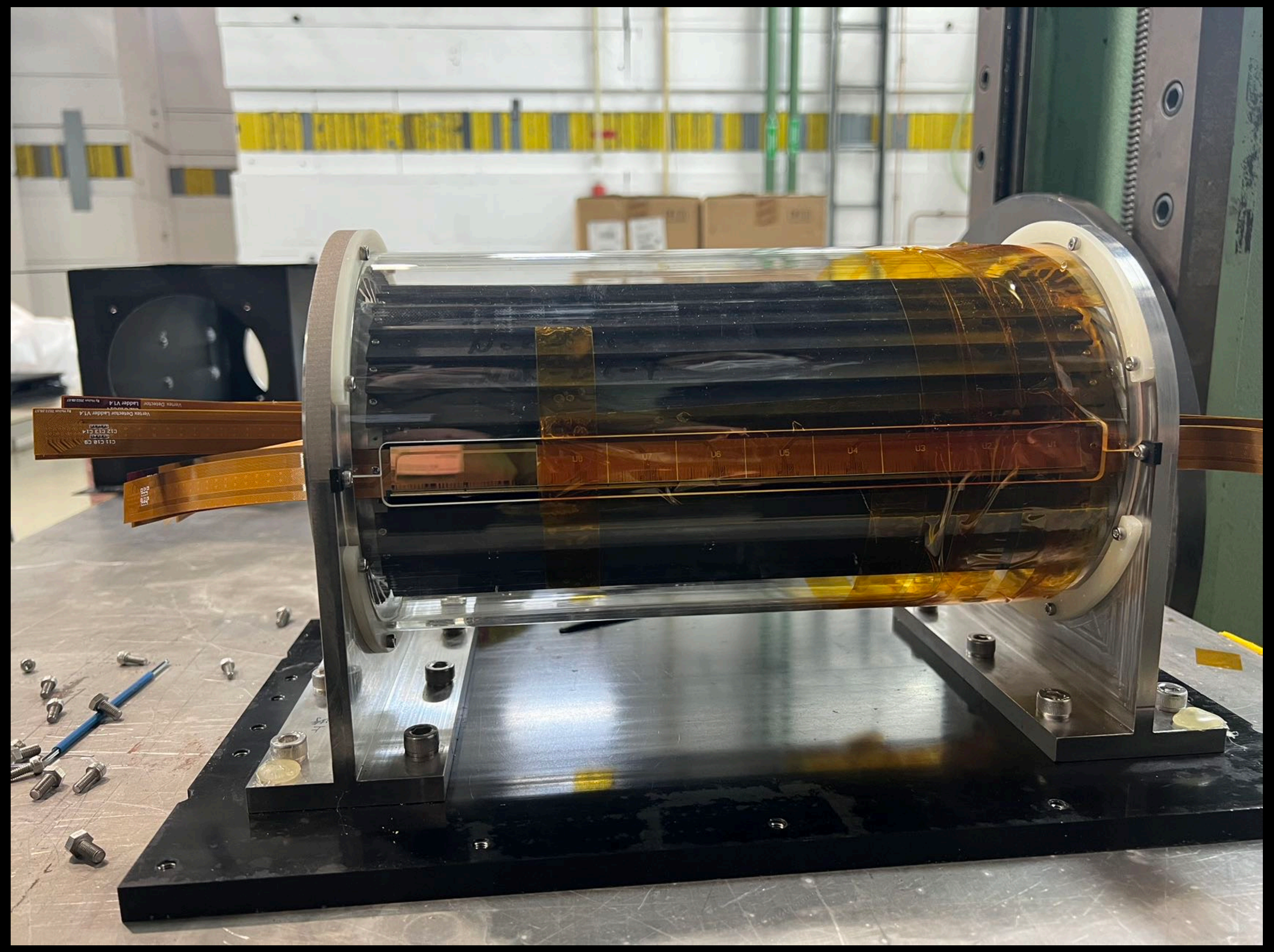


Detector module (ladder) Prototyping



Vertex detector Prototype for beam test





- Design CMOS imaging sensor chip
- Detector Module prototyping
- Vertex Detector assembly and testbeam

Road map of sensor R & D

- This talk focus on more TaichuPix based CEPC vertex detector prototype
- More details chip development in talks tomorrow in electronics section
- 3D-integrated pixel circuit for a low power and small pitch SOI sensor, Yunpeng LU
- Development of TaichuPix pixel chips for the first CEPC vertex detector prototype, Ying Zhang

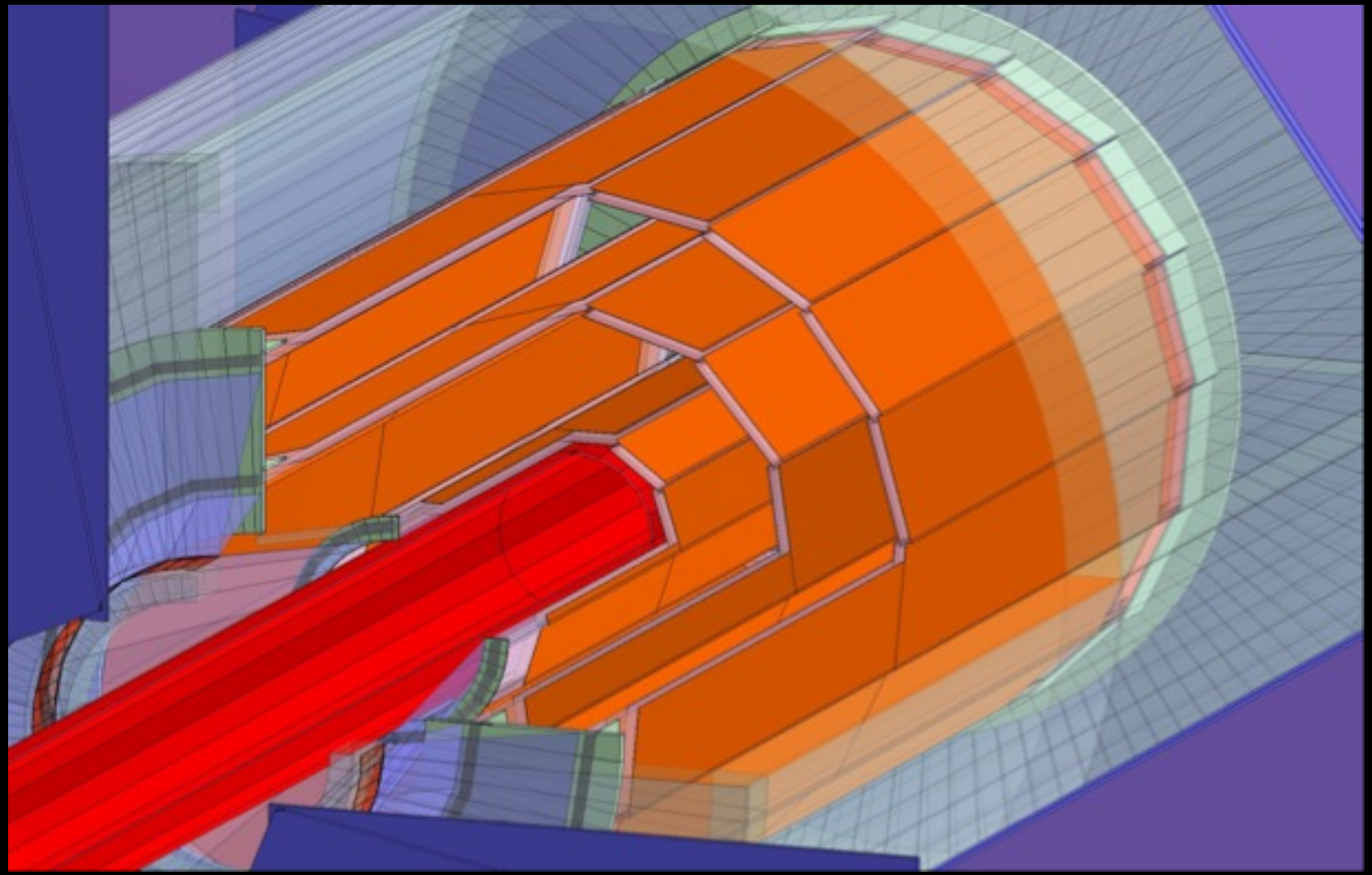
Research Team in MOST2 silicon project

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning Irradiation, test beam organization
IFAE(Spain)/CCNU	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
ShanDong University	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
Nanjing University	Irradiation, test beam

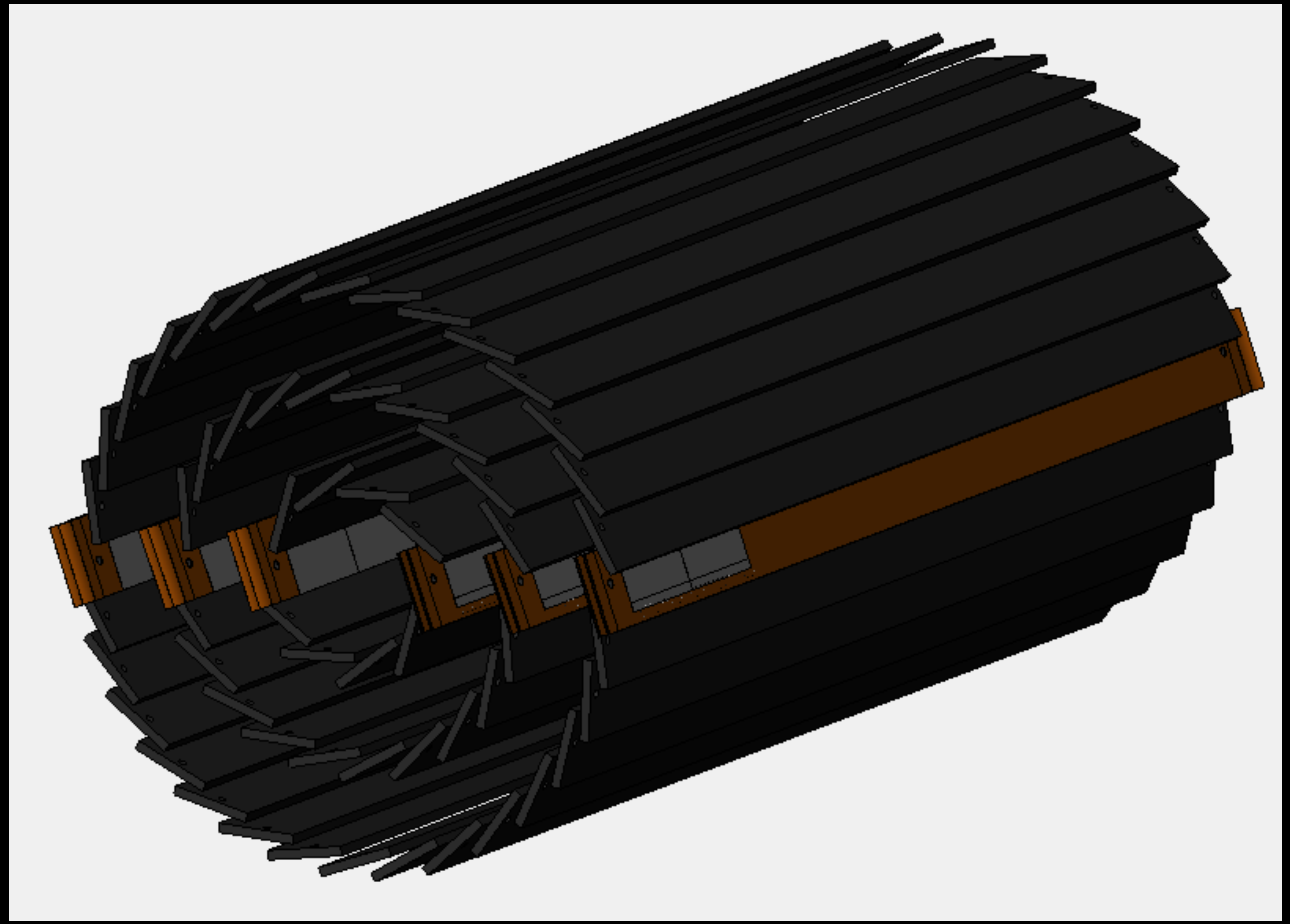
Vertex detector prototype structure optimization

- Based on CEPC vertex detector conceptual design → Three double-layer barrel detector
  - This project plan to prototype the important part of vertex detector (CDR design)
  - The cost for the full vertex detector is high (eg: ~50 M CHF for ATLAS ITk pixel detector)
    - → Plan to build full mechanical part of the detector
    - → install a sector of ladders in prototype , not necessary to build full vertex for R & D
- Optimize the geometry based on real ASIC and electronics dimension
  - Optimize geometry based on its physics performance from simulation
  - Engineering design of prototype structure

CEPC Vertex detector
Conceptual design (2016)

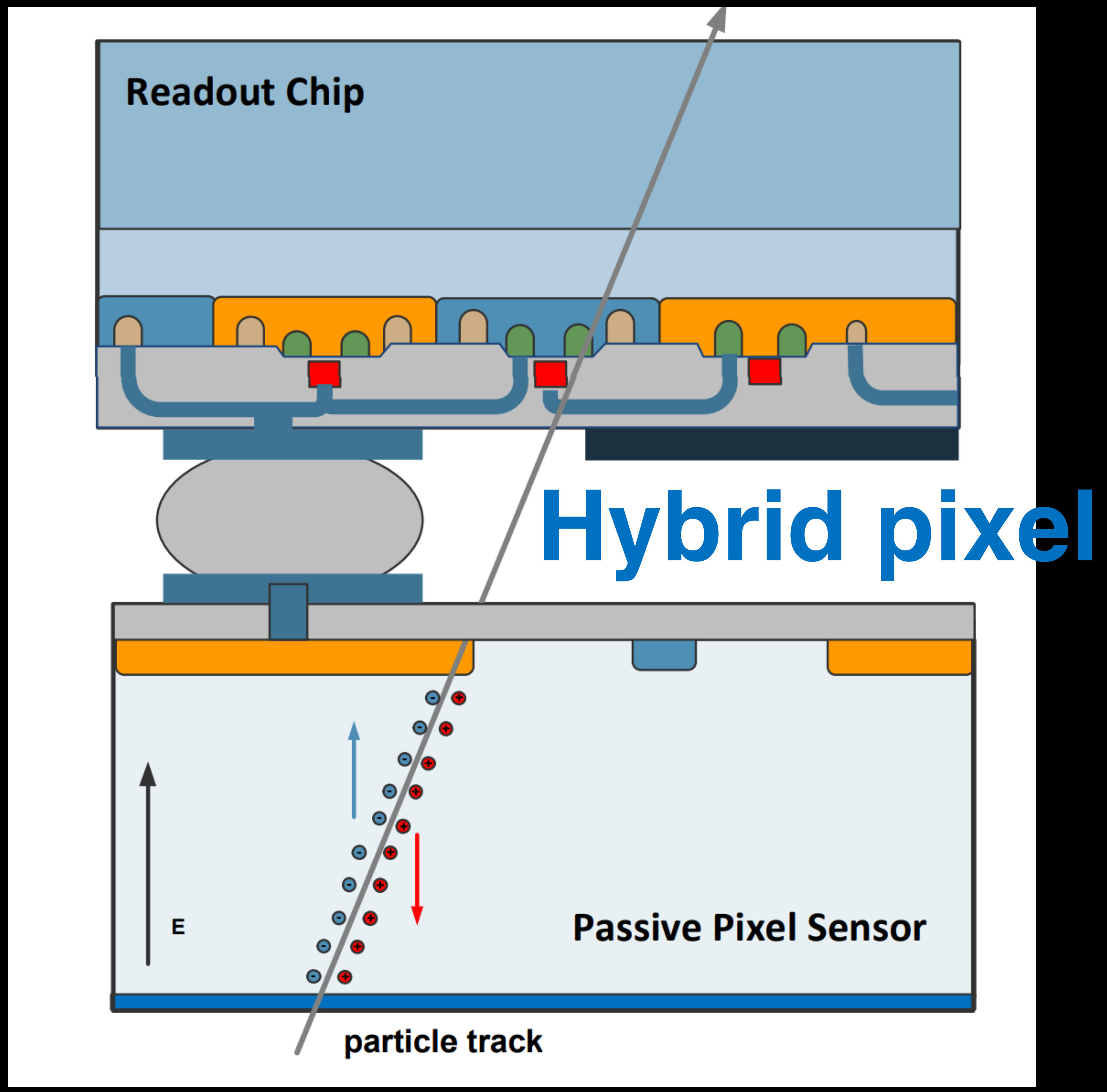


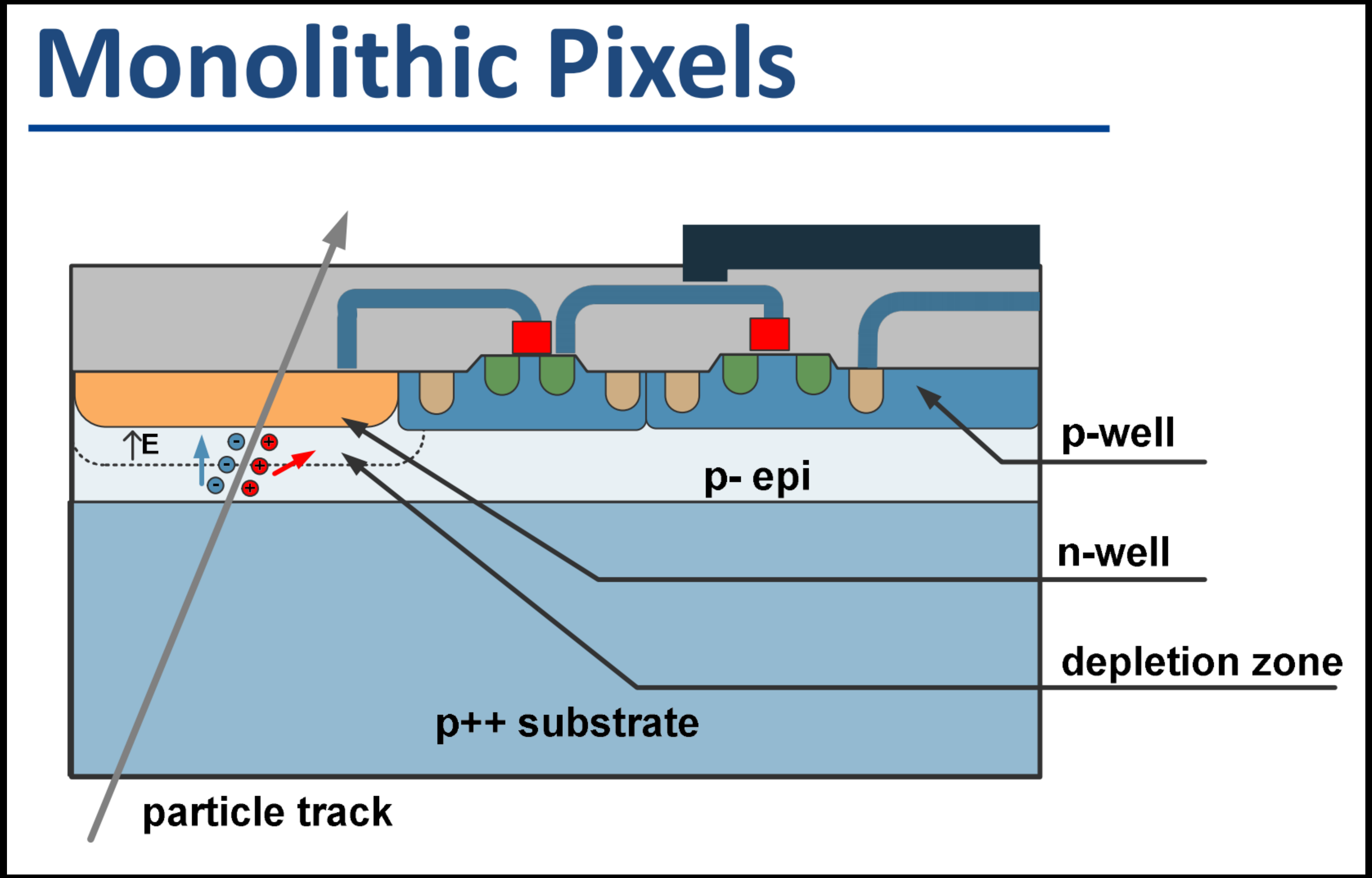
This project
Vertex detector prototype design



CMOS Monolithic pixel sensor

- Conventional Hybrid pixel technology at Large Hadron Collider
  - Need to bump bonding with readout ASIC
  - Typical pixel size >=50μm, much more difficult for bump bonding with smaller pixels
- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - Sensor and ASIC high integrated in one chip, easier for detector assembly
  - Can have compact structure in pixel array design.
    - Pixel size can be reduced to 25um or below → can achieve better spatial resolution





CMOS Sensor chip R & D

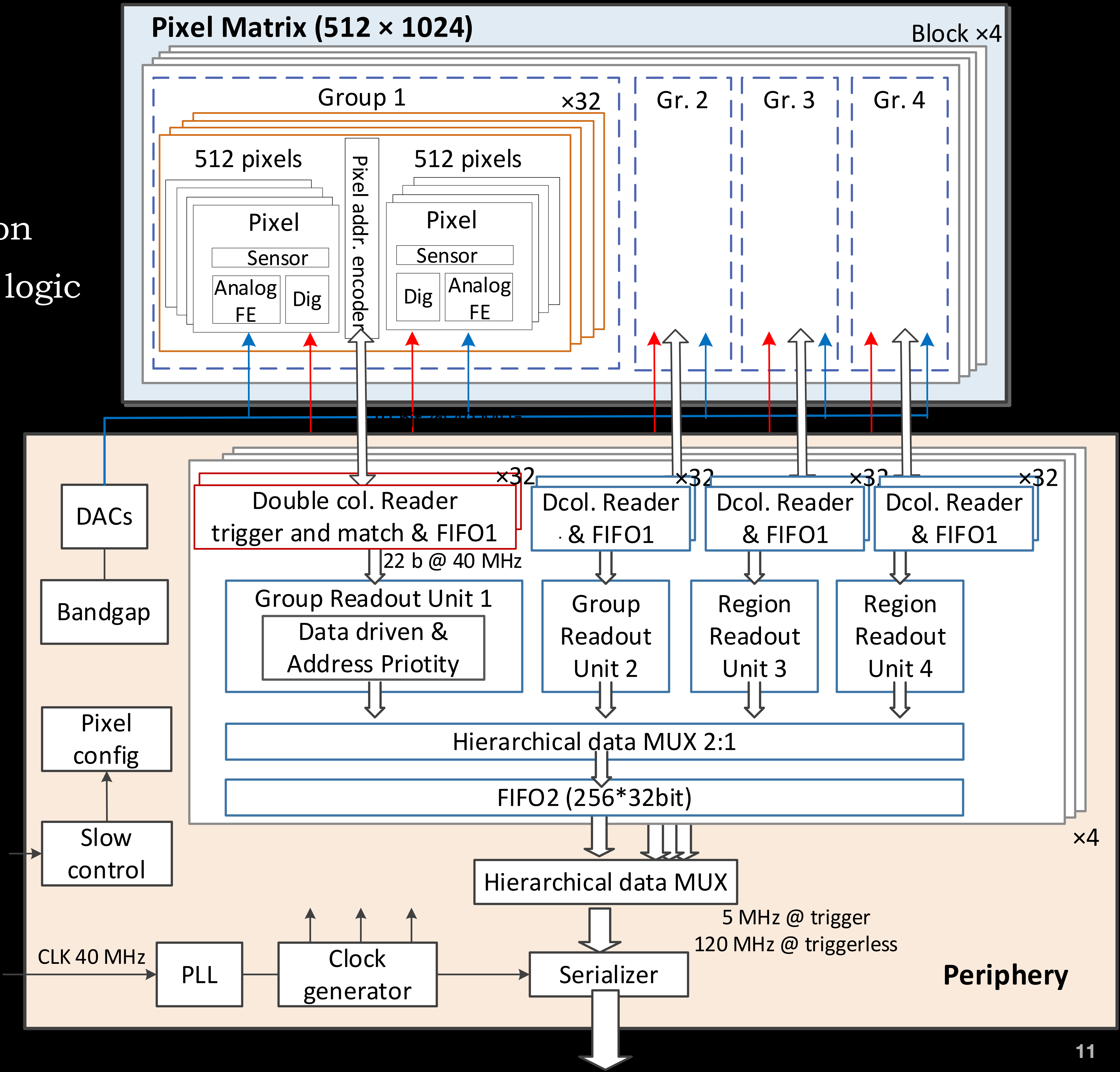
- The existing CMOS monolithic pixel sensors can't fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - Radiation tolerance **(per year):** **>**1 Mrad
  - High readout speed -> for high luminosity CEPC Z pole running (40MHz)

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

TaichuPix readout architecture

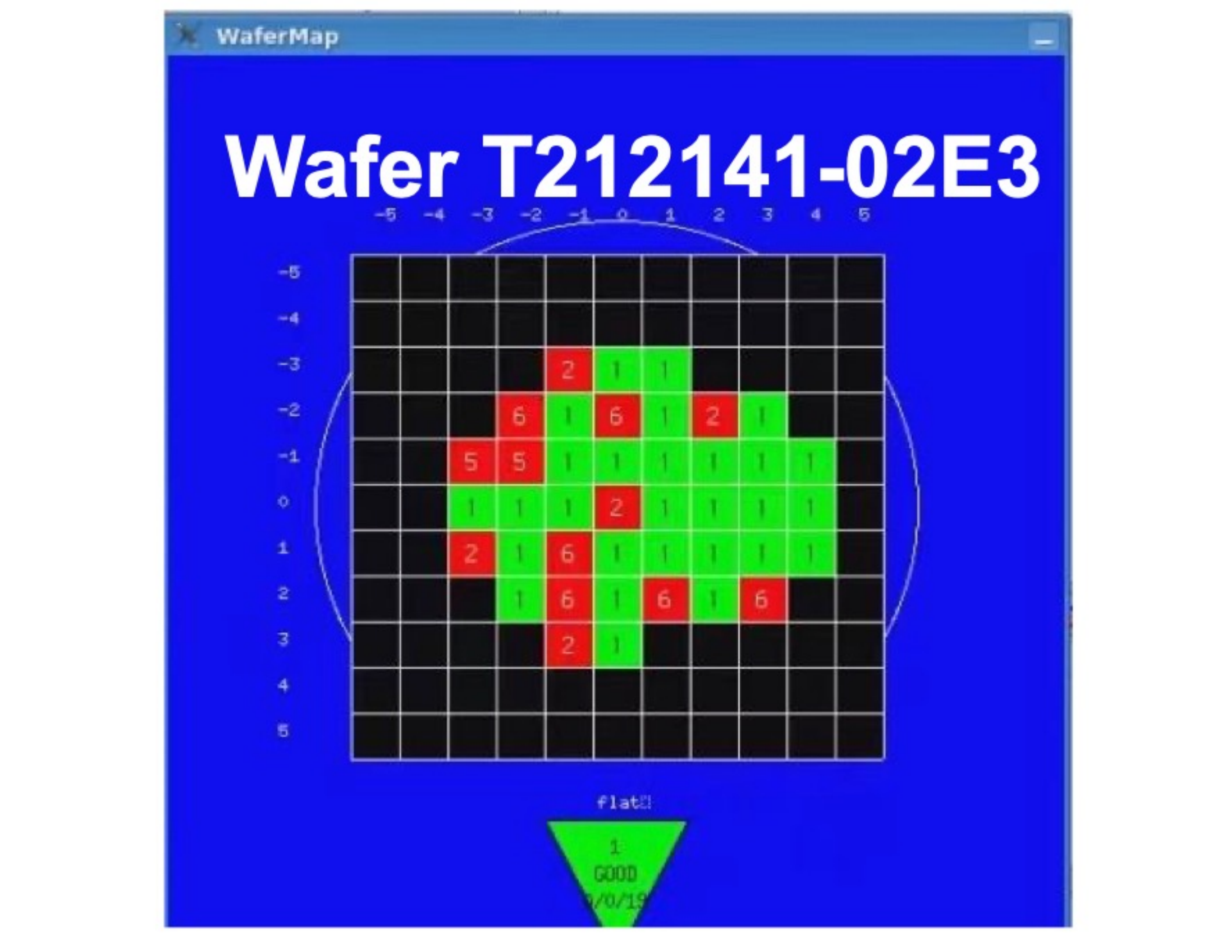
- **High resolution and high data rate**
- **Data-driven readout design**

- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Readout time: 50 ns for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

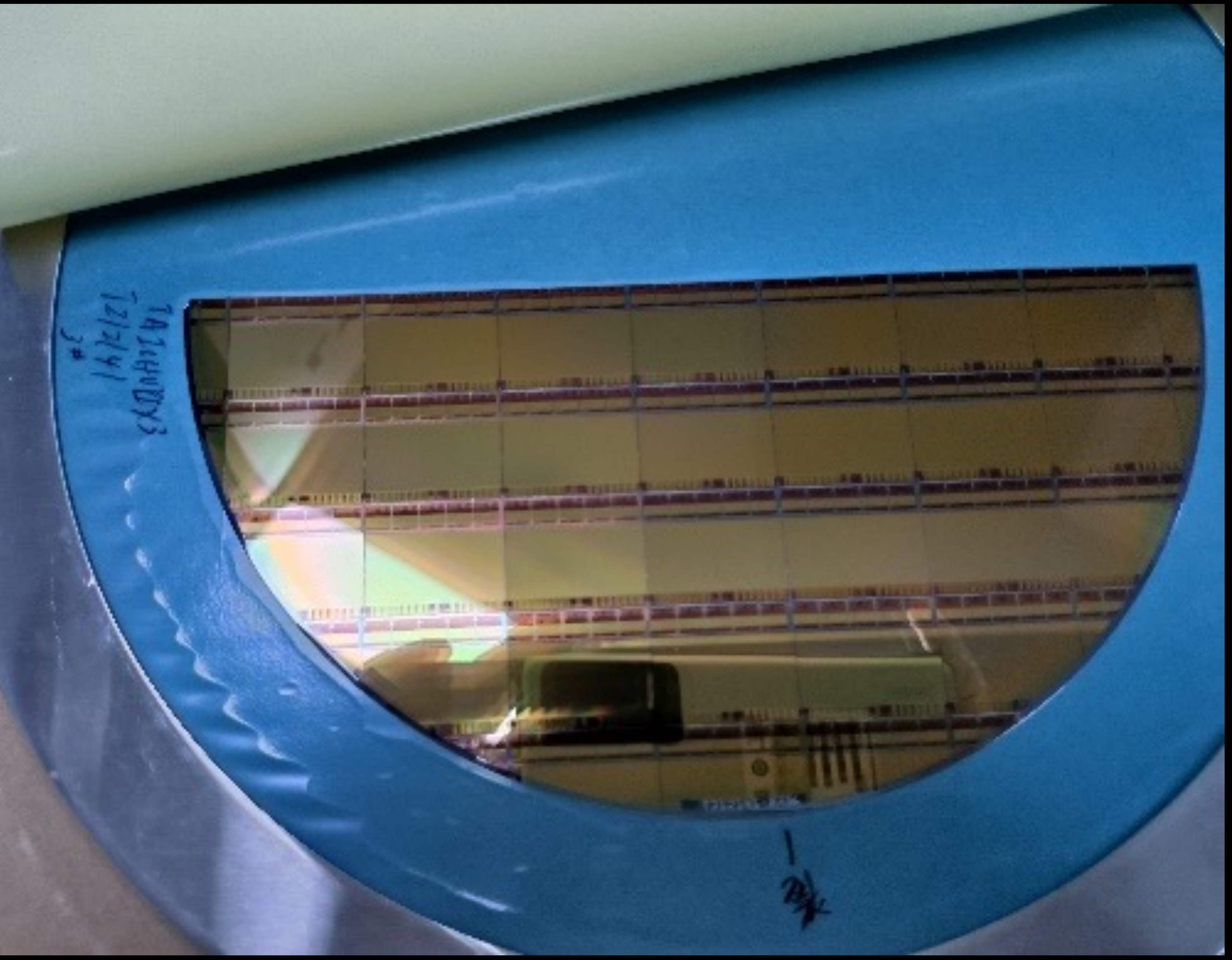


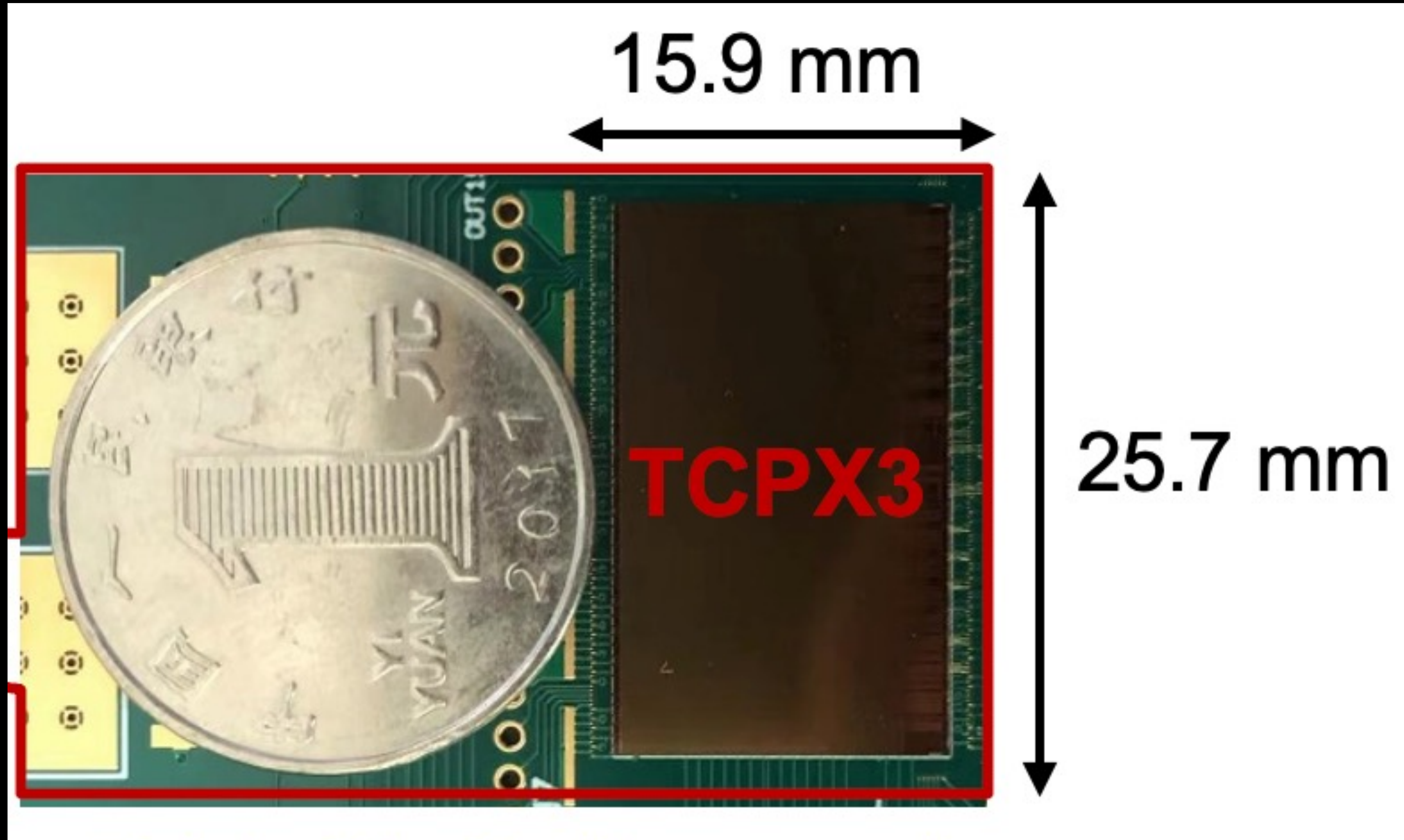
Full-size TaichuPix3 prototyping (engineering run)

- **Developed the first full-size CMOS pixel sensor for particle detector in China**
  - **Full size 1024×512 Pixel array, Chip Size： 15.9×25.7mm**
    - **25µm×25µm pixel size → high spatial resolution**
    - **Process: Towerjazz 180nm CIS process**
  - **Fast Periphery digital readout , high-speed data interface**

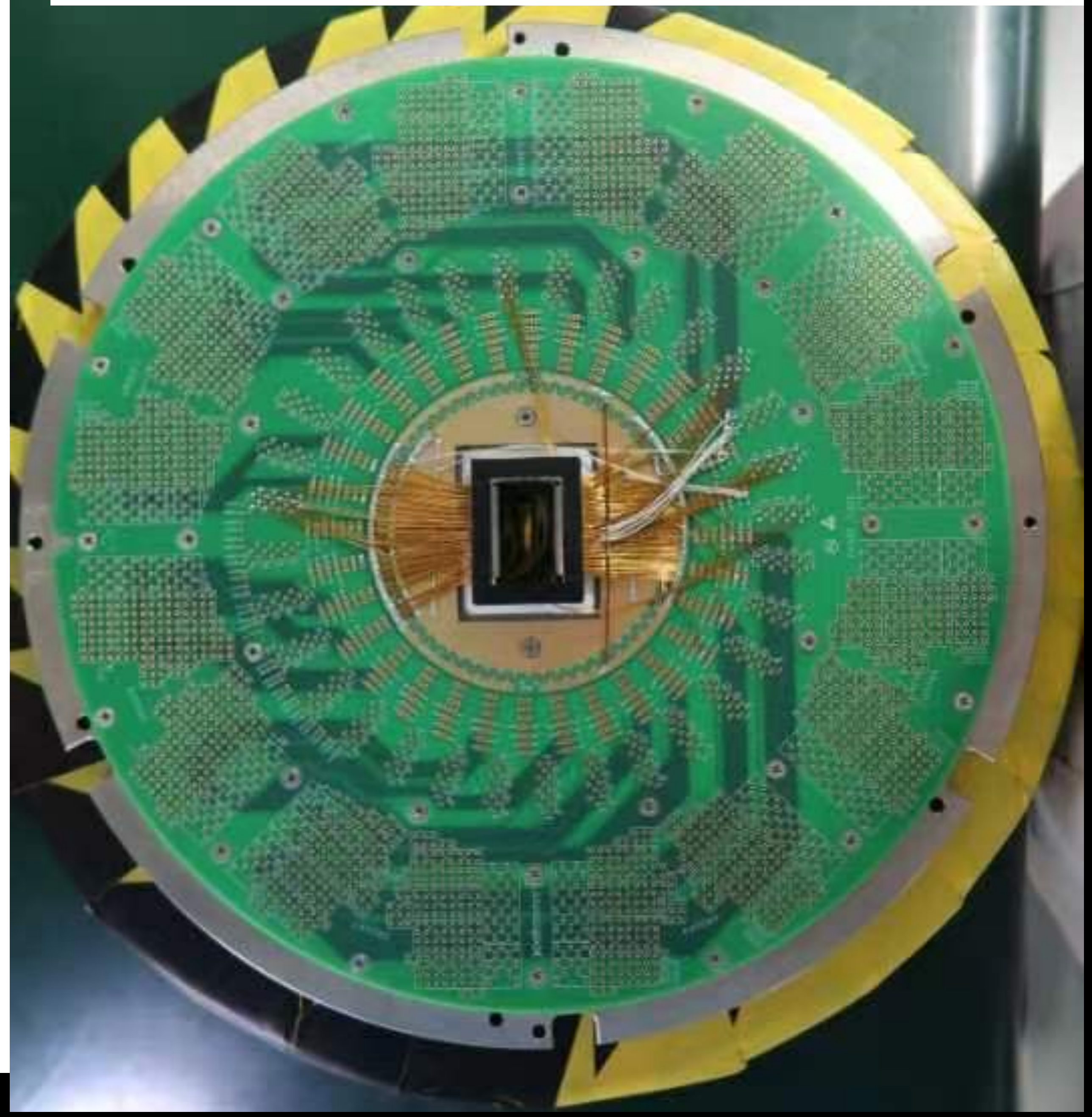


An example of wafer test result



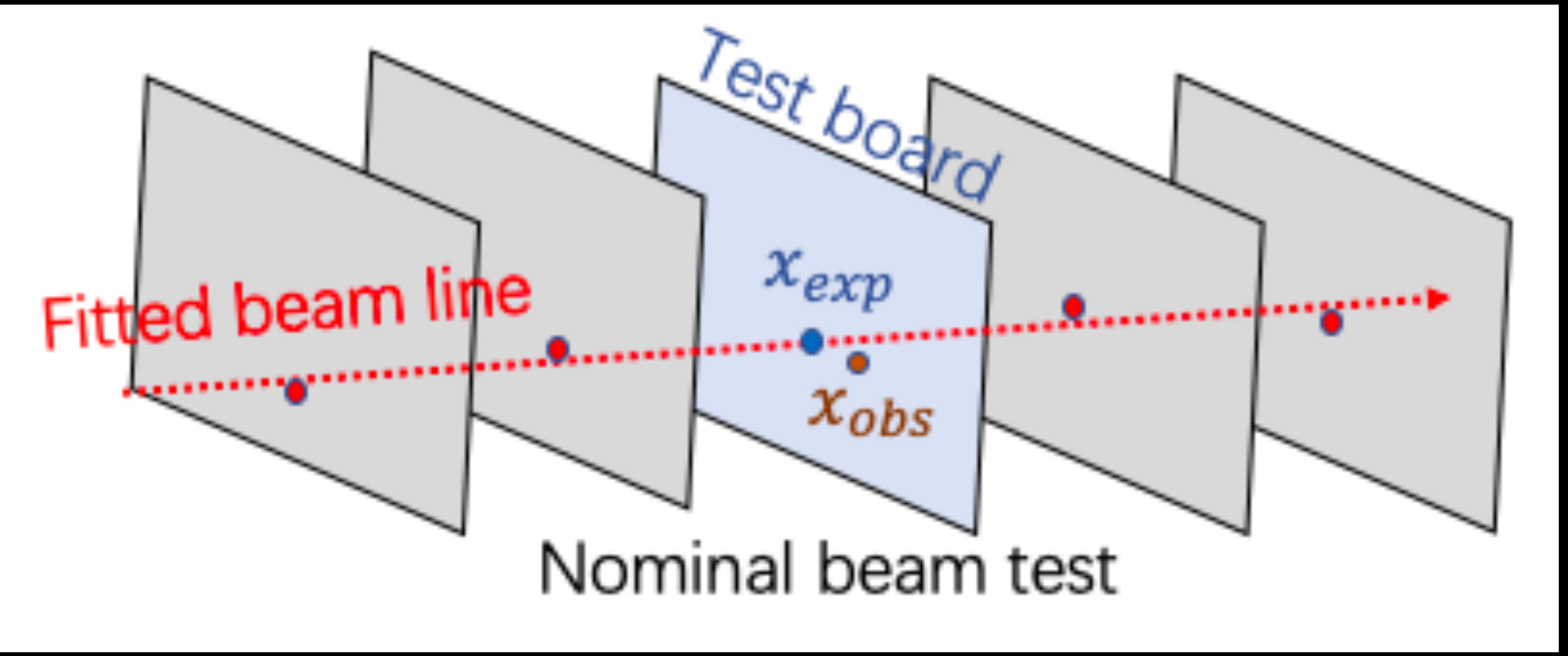


TaichuPix-3 chip vs. coin

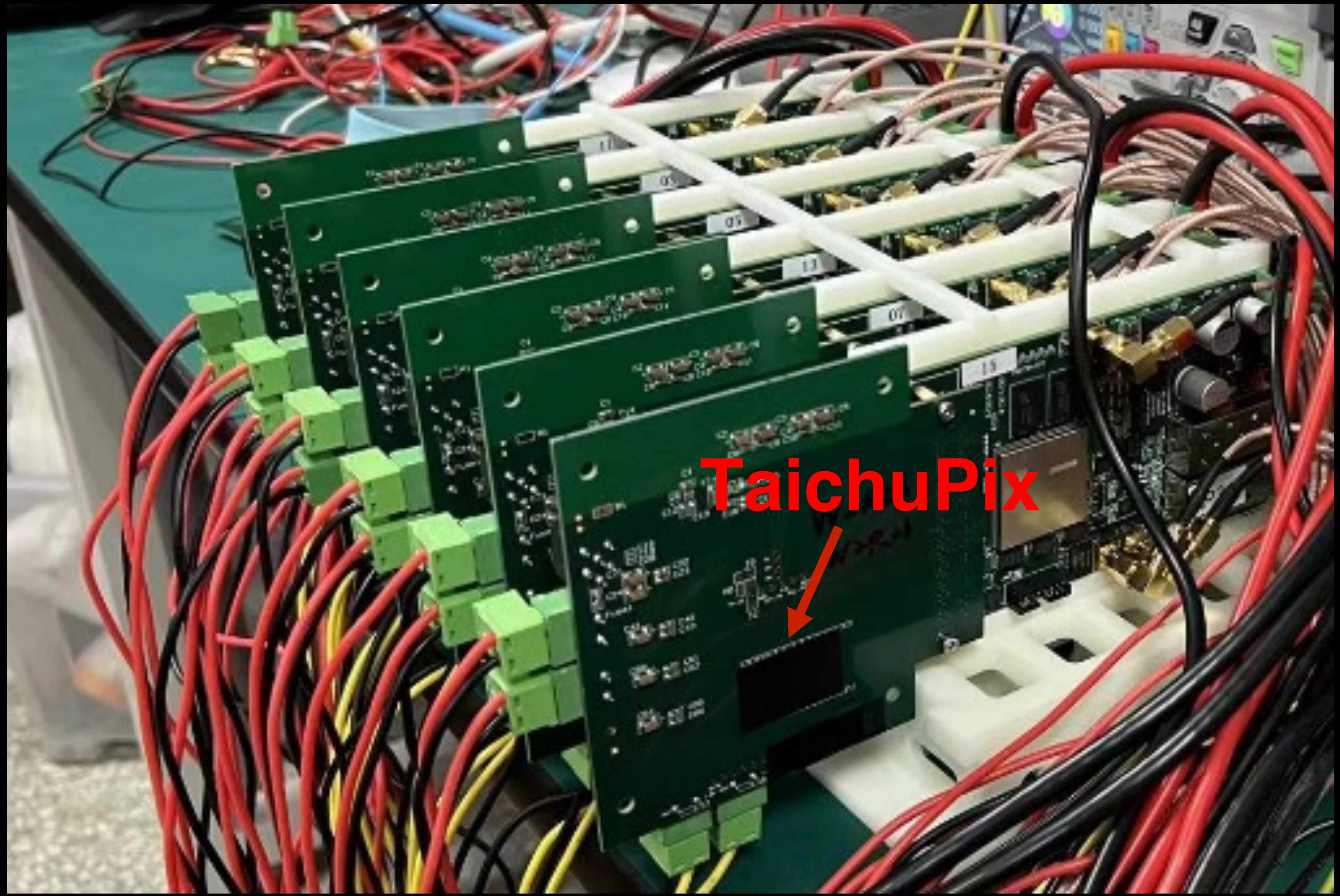


Spatial resolution measured by testbeam

- The 6-layer of TaichuPix-3 telescope built
  - Tested at DESY with 4-5 GeV electron beam, 1kHz rate
  - One layer of TaichuPix used as Detector-Under-Test (DUT)
  - Other five layers as beam telescope used for track fitting
  - Spatial resolution of TaichuPix reach 4.78 μm
    - Reach the goal of the project (3-5 μm)

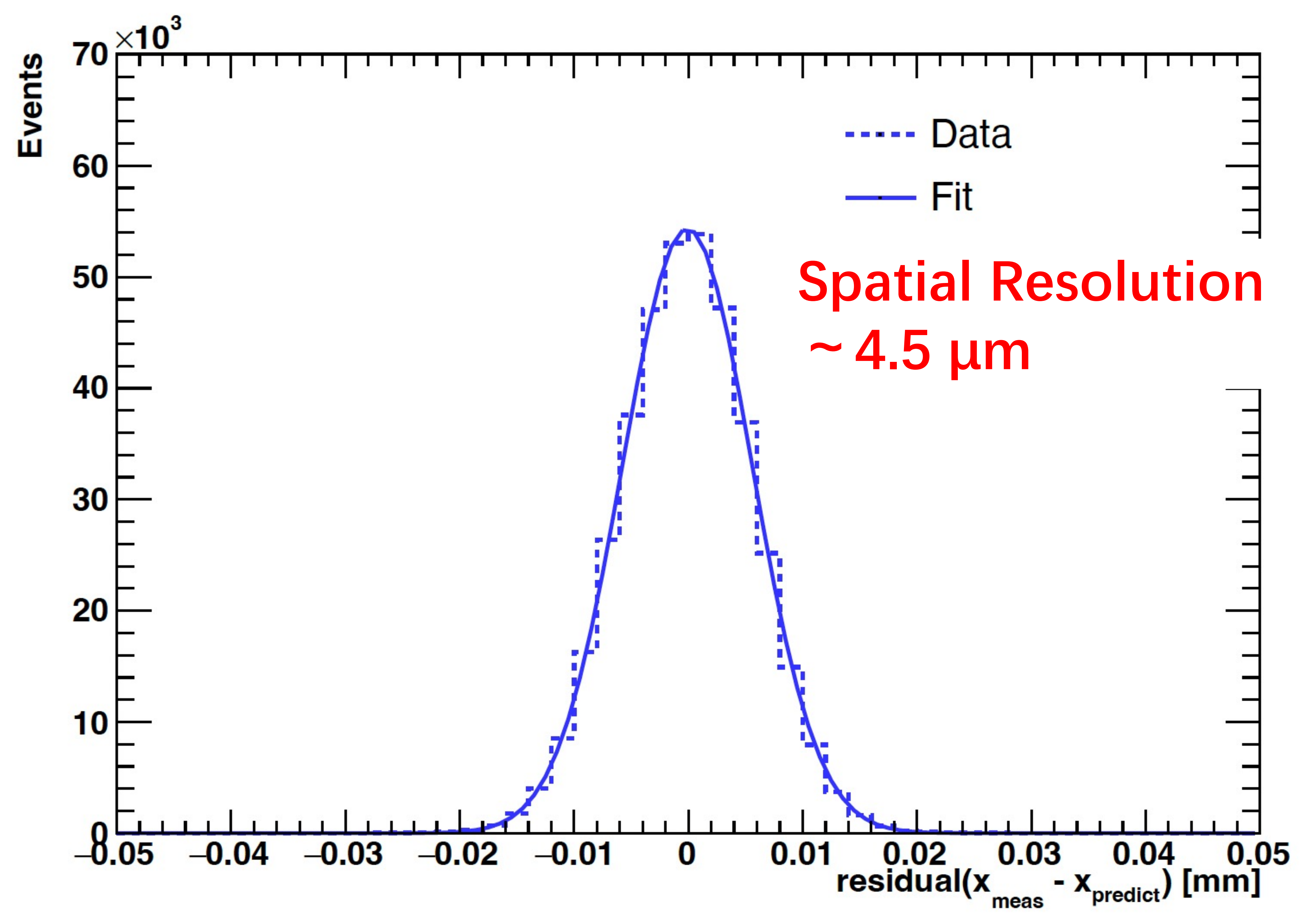


Setup for Taichupix beam telescope



Residual distribution

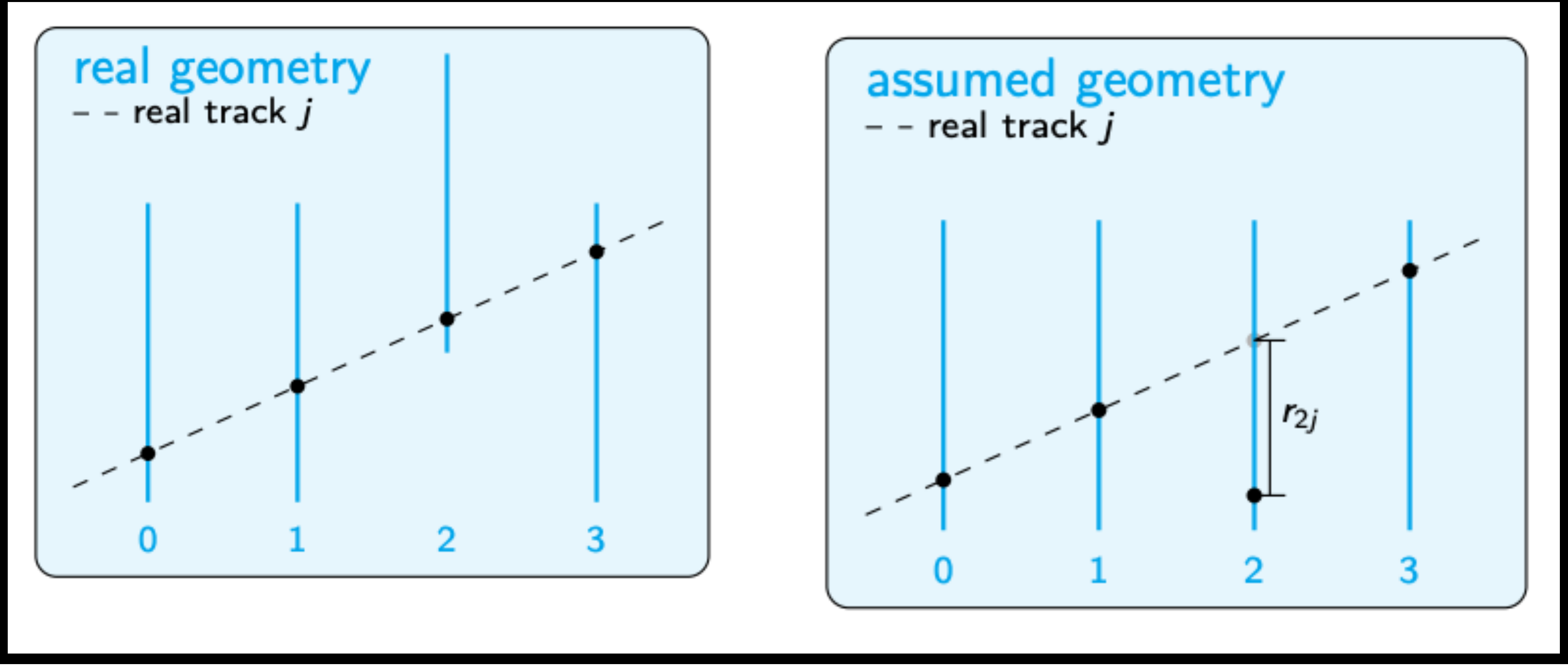
DUT measured position – expected position from track



Spatial resolution measured by testbeam : alignment

- The measured hits position misaligned due to non-ideal installation precision
- Method: Millepede matrix method

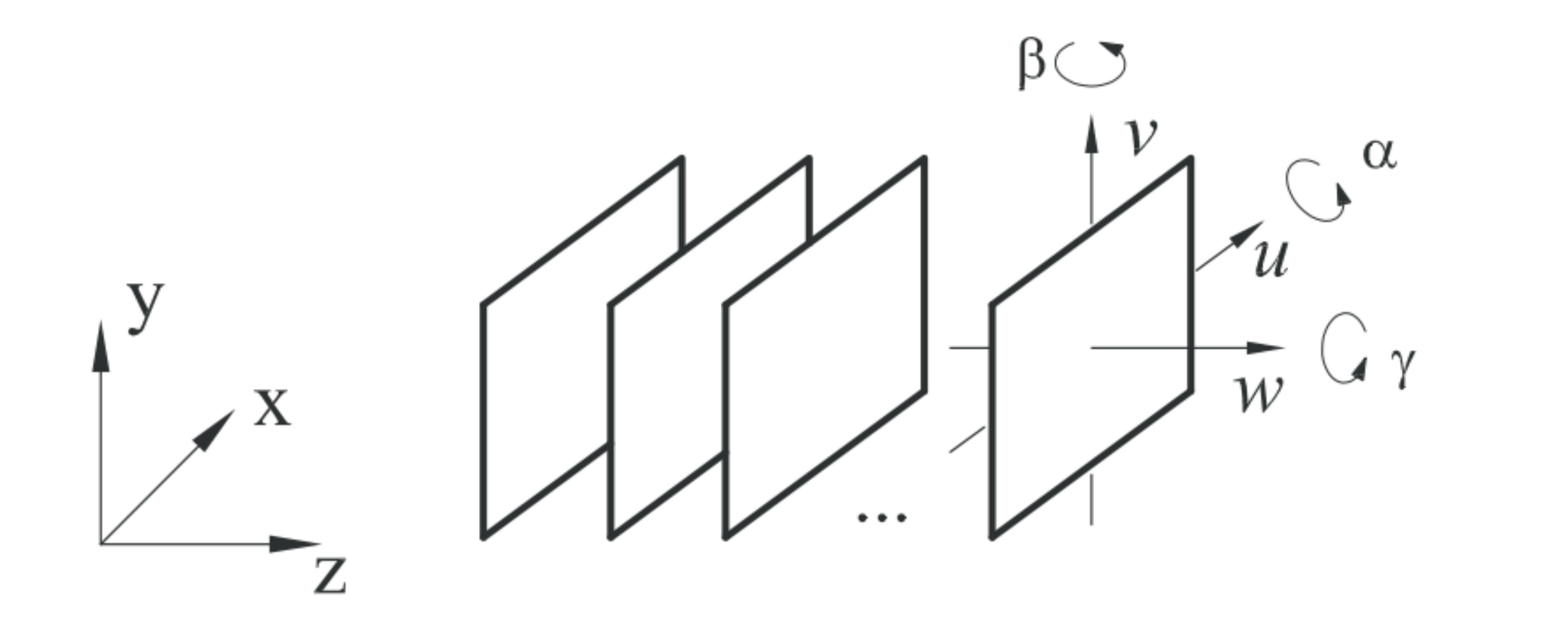
$$\chi^2 = \sum_{j \in tracks} \sum_{i \in hits} \vec{r}_{ij}^{T}(g, l_j) V_{ij}^{-1} \vec{r}_{ij}(g, l_j)$$



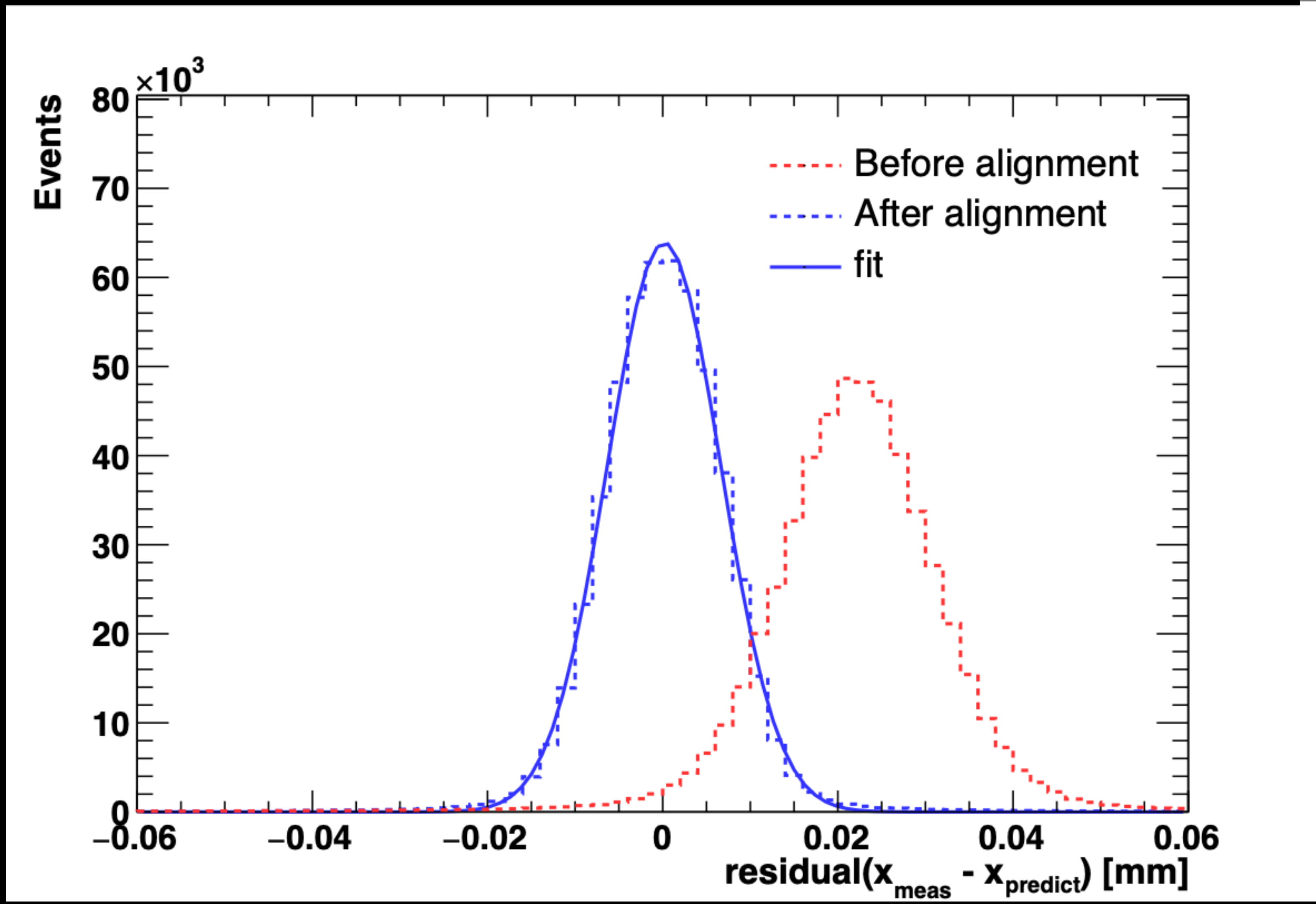
Six alignment parameters used for each chip position

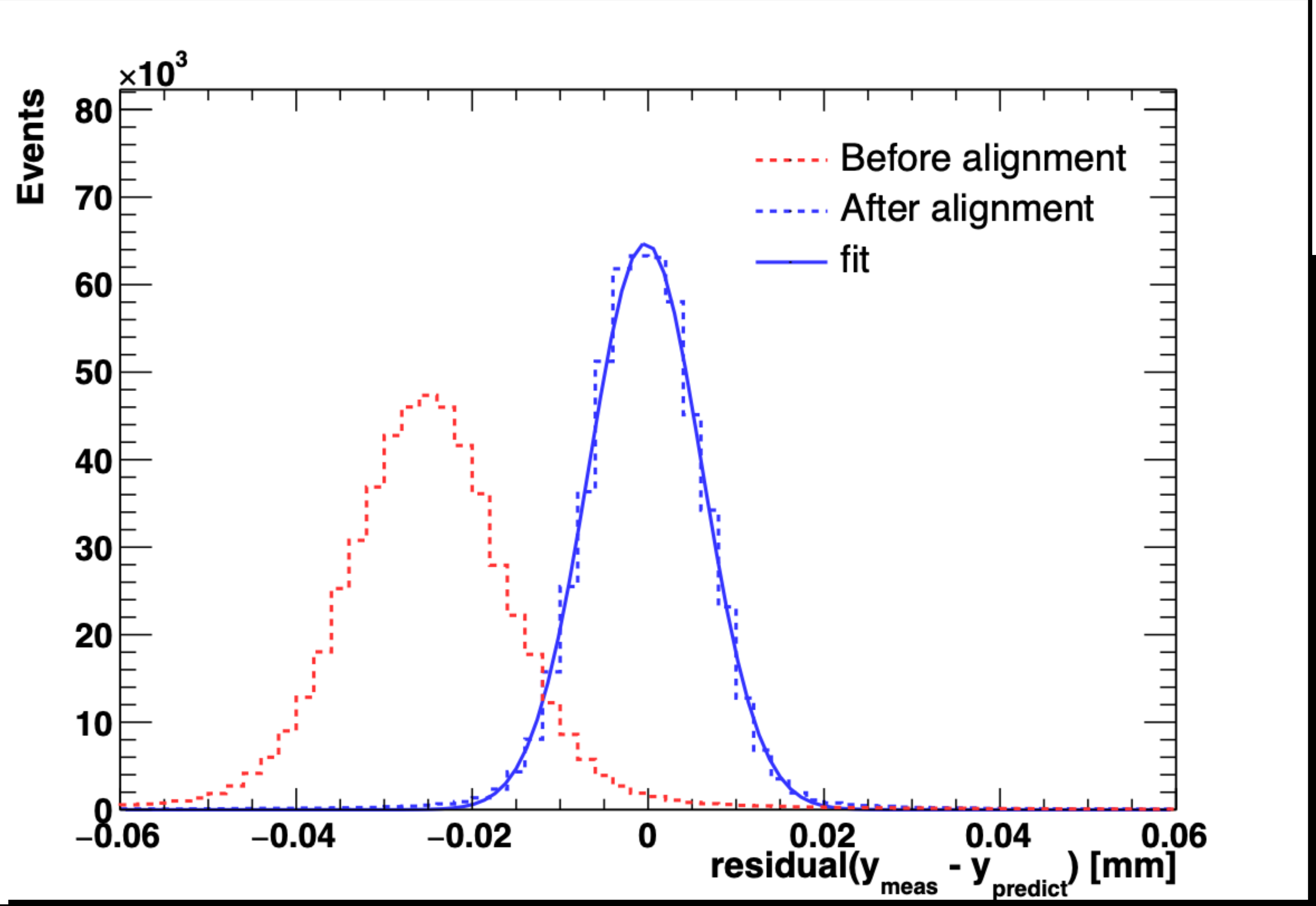
Translation along X, Y, Z direction

Rotation around X, Y, Z axis



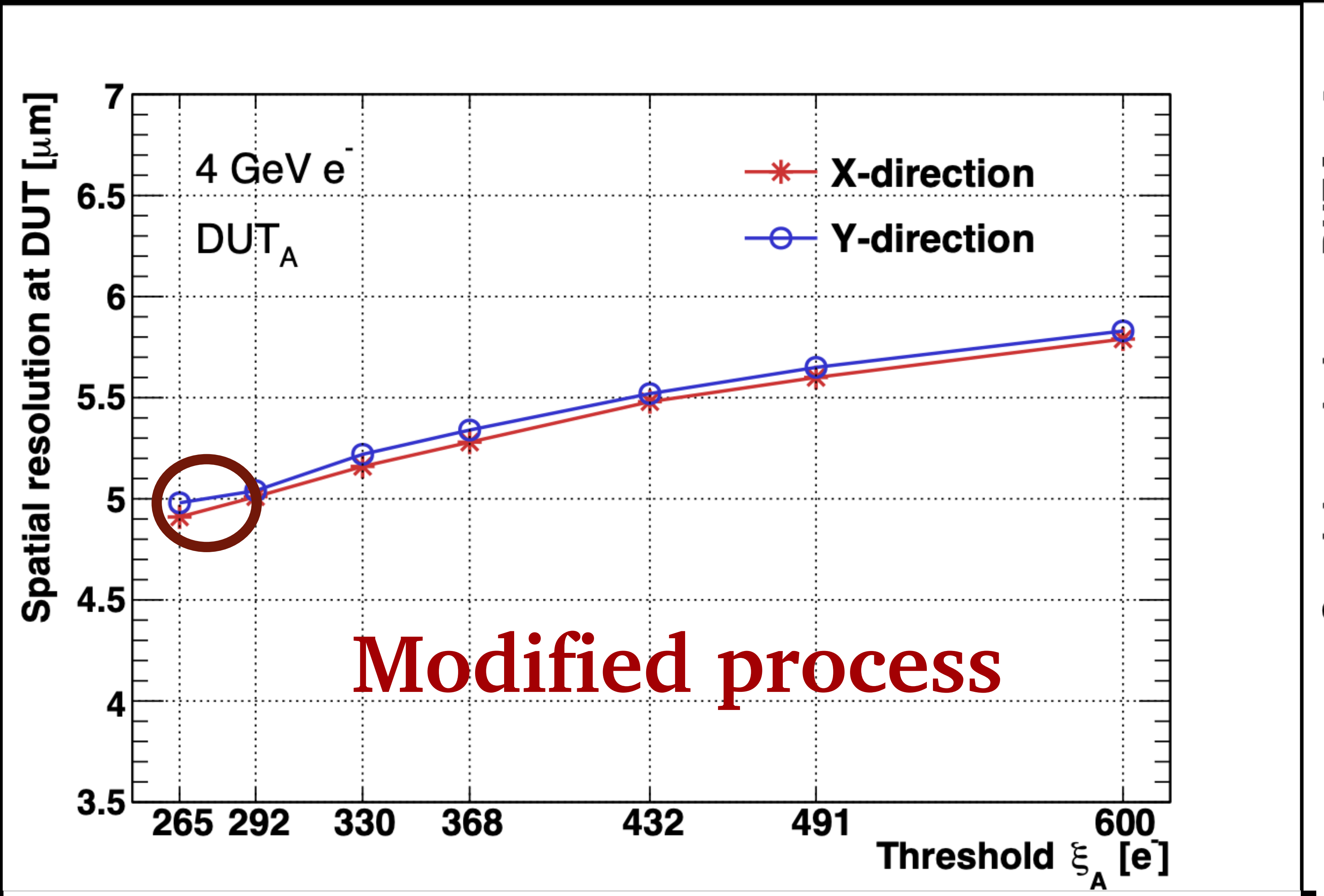
Impact of the alignment on residual distribution

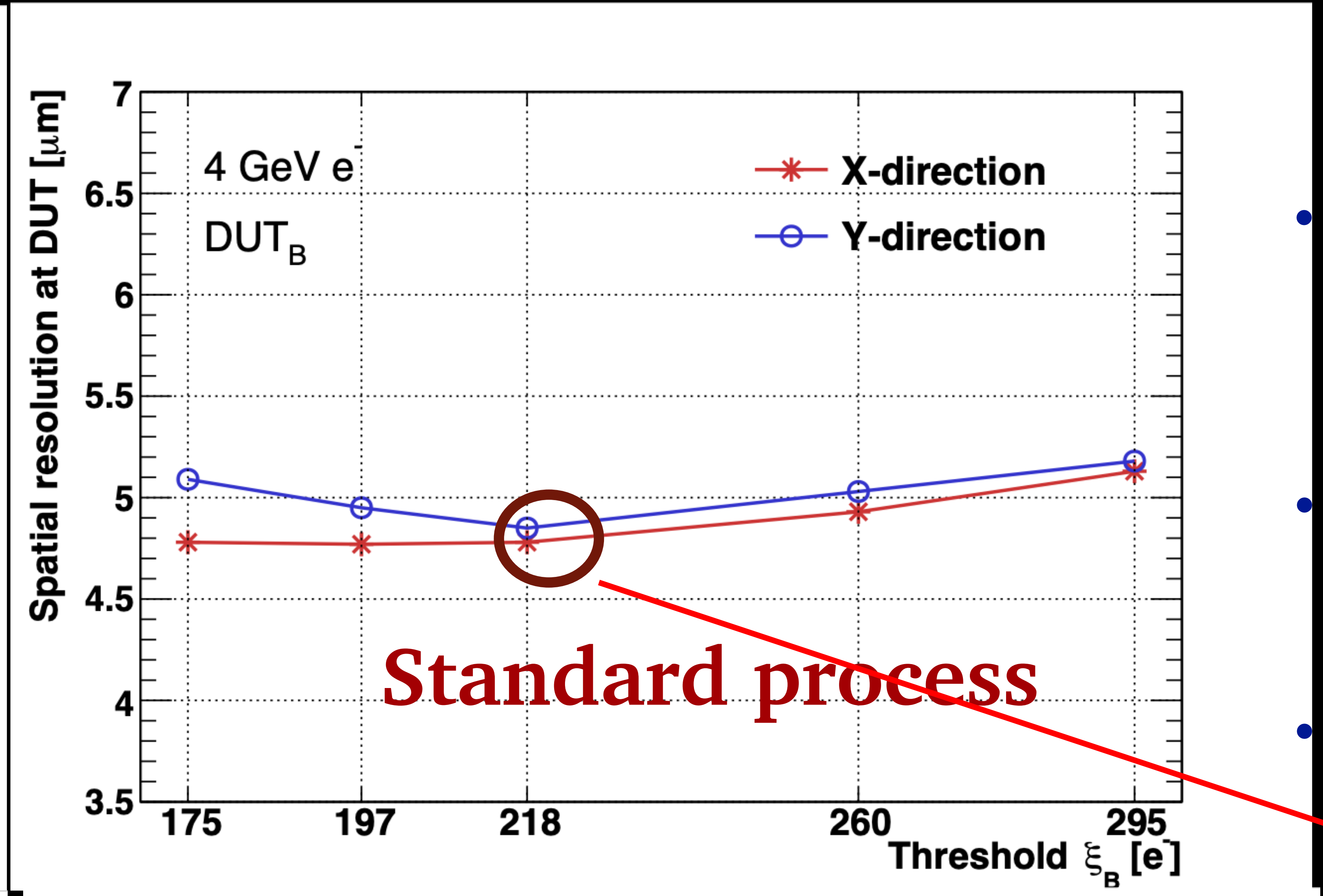


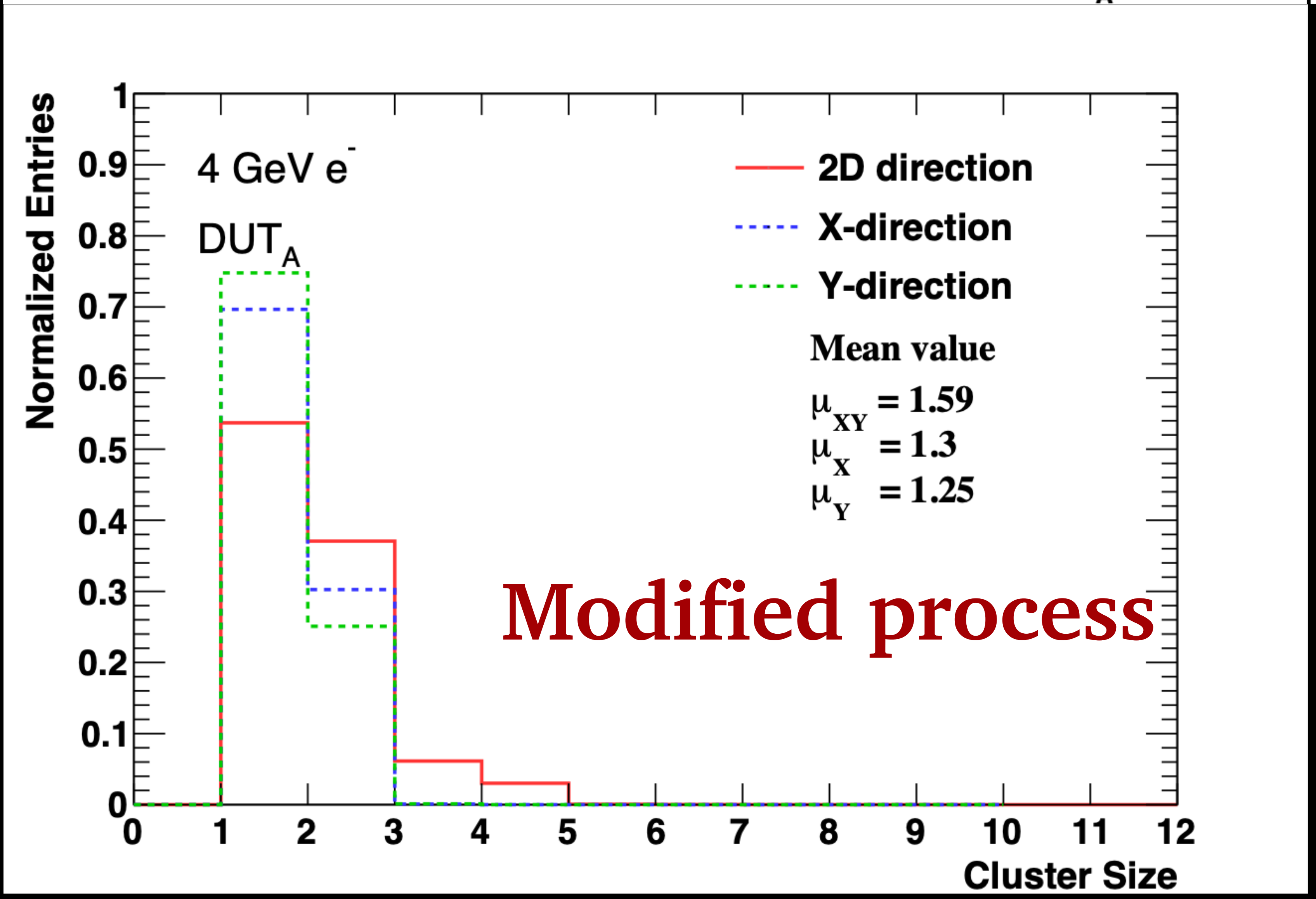


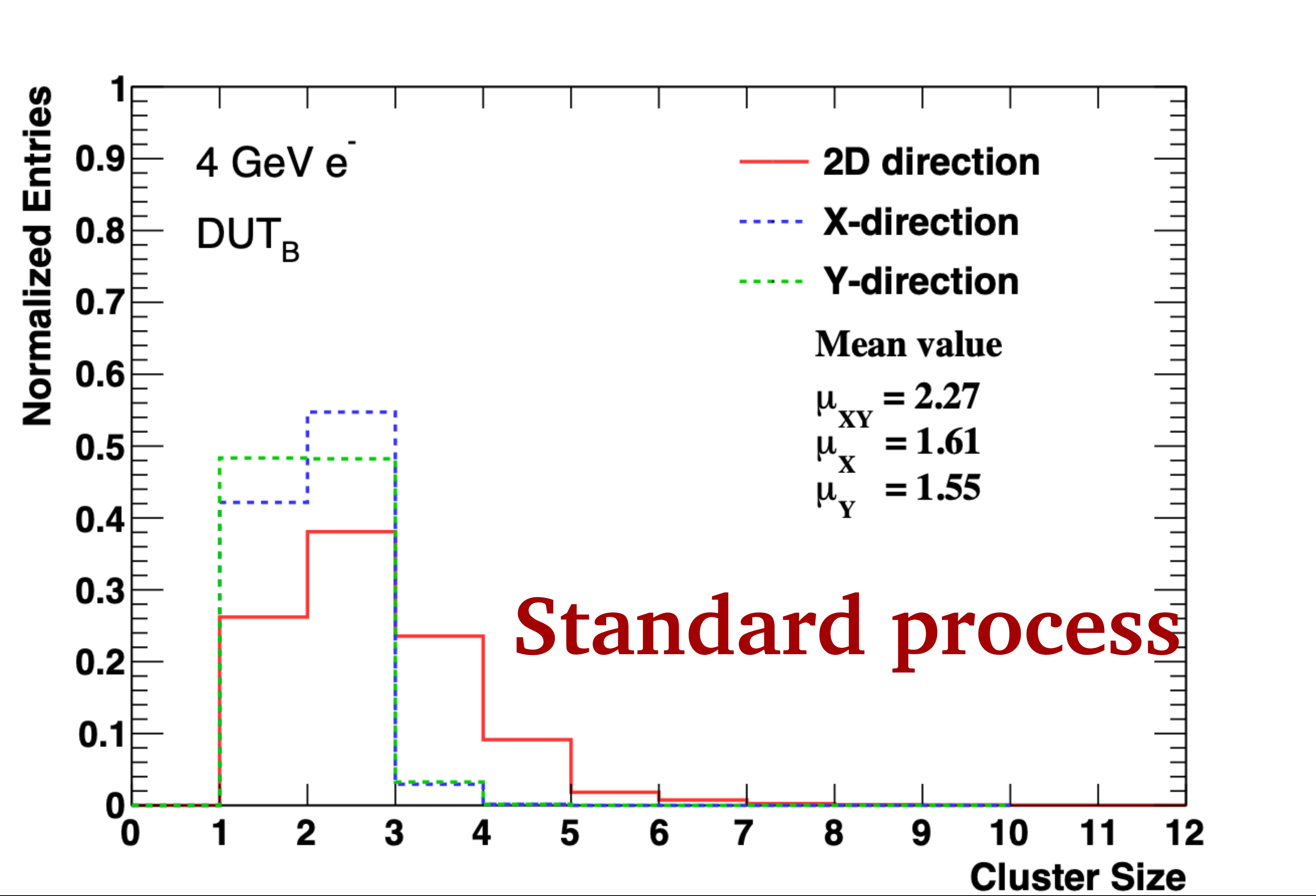
Spatial resolution and cluster size VS threshold

- The spatial resolution extracted by the unbiased residual distribution after substracting the track uncertainty→ **The spatial resolution less than 5 um**

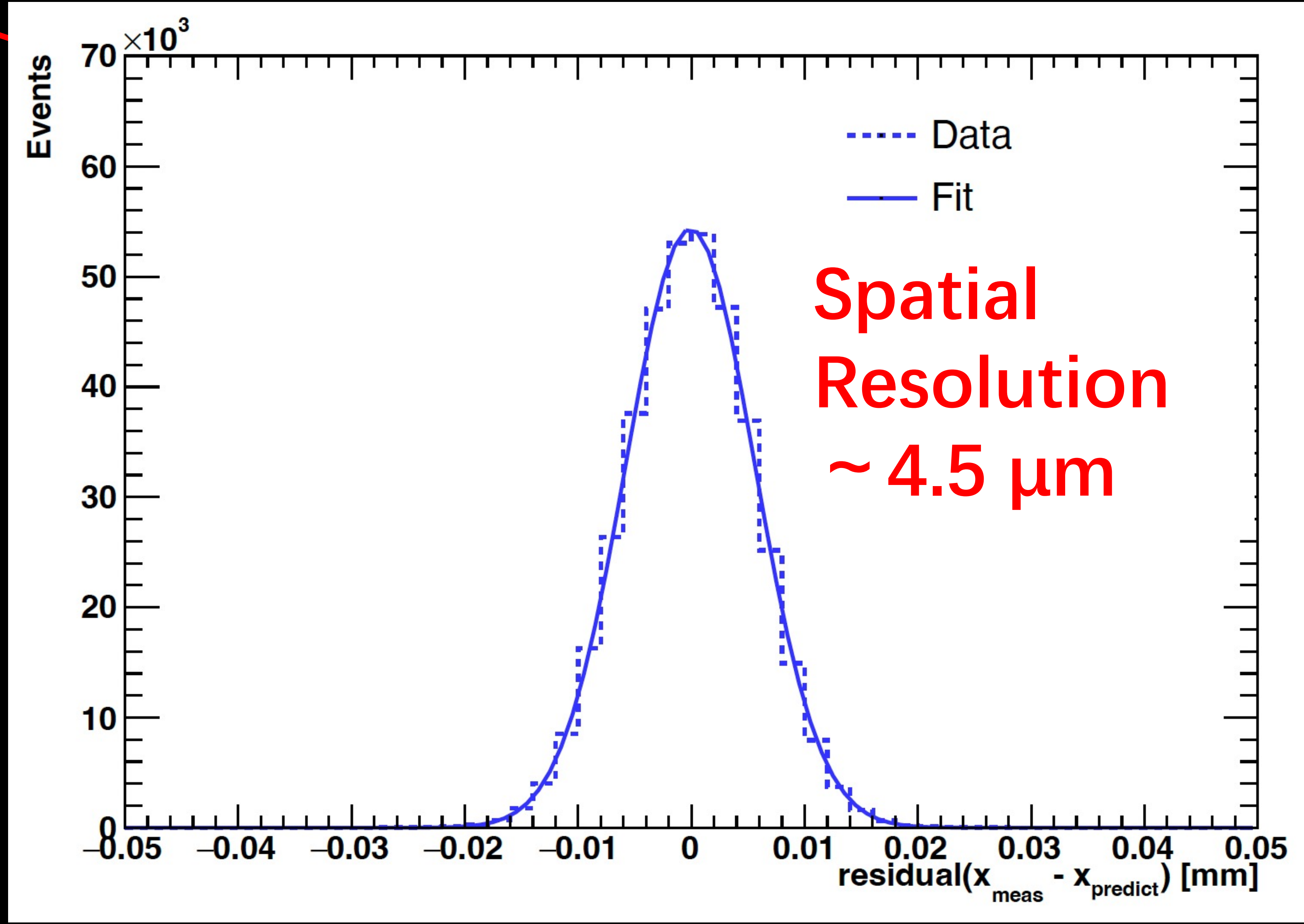








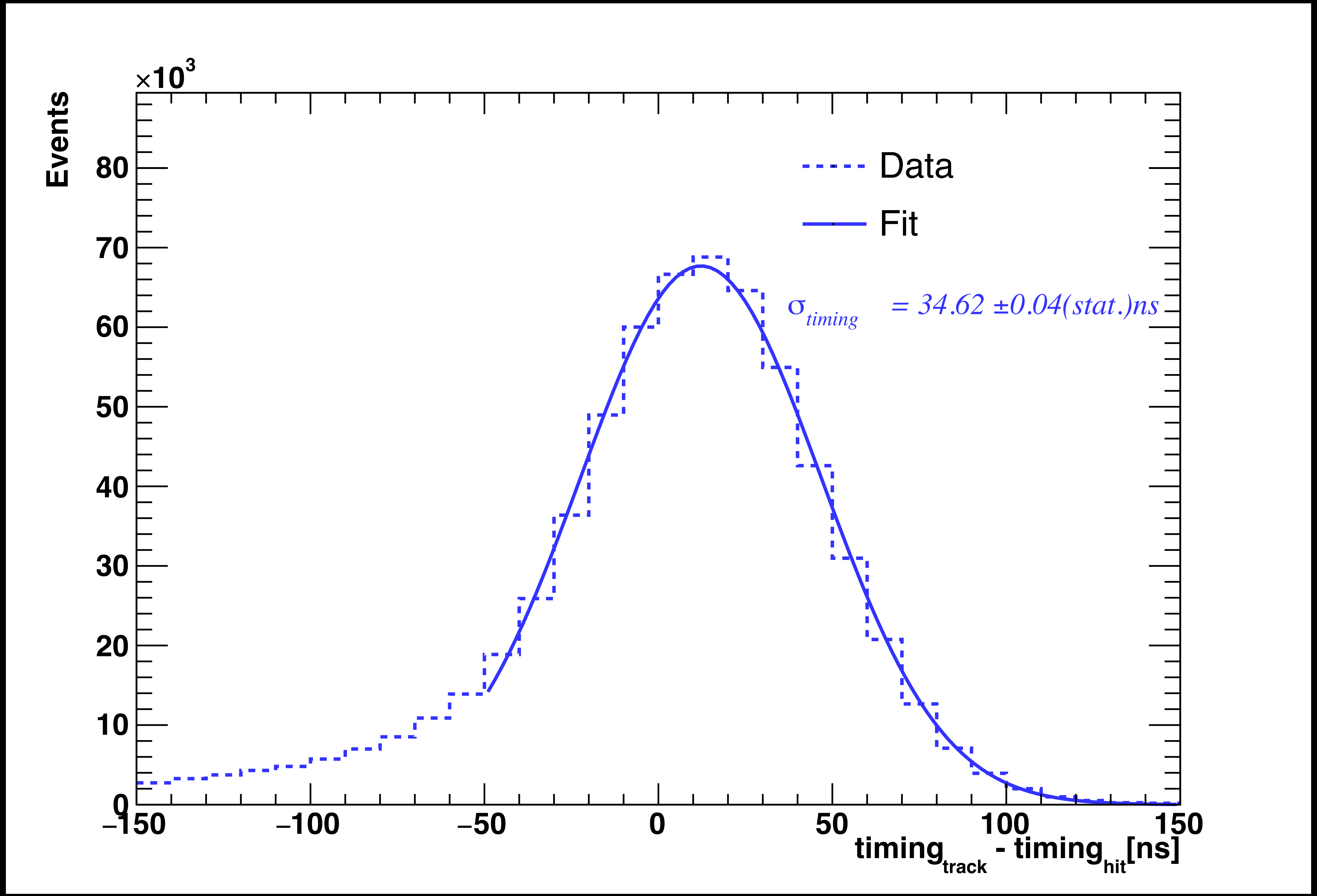
- **Less charge sharing effects in modified process with full depletion**
- **If lowering the threshold, cluster size will be dominated by noise**



Time resolution of Taichupix (Preliminary result)

- CEPC tracker resolution requirement: 25ns @40MHz Z pole collision
- Taichupix telescope have two time stamp:
  - Time stamp from FPGA (all 6 Taichu chip synchronized by FPGA)
  - Precise time stamp from Taichu chip
- Time resolution is ~35ns @20MHz clock
  - By comparing telescope track time Vs DUT time

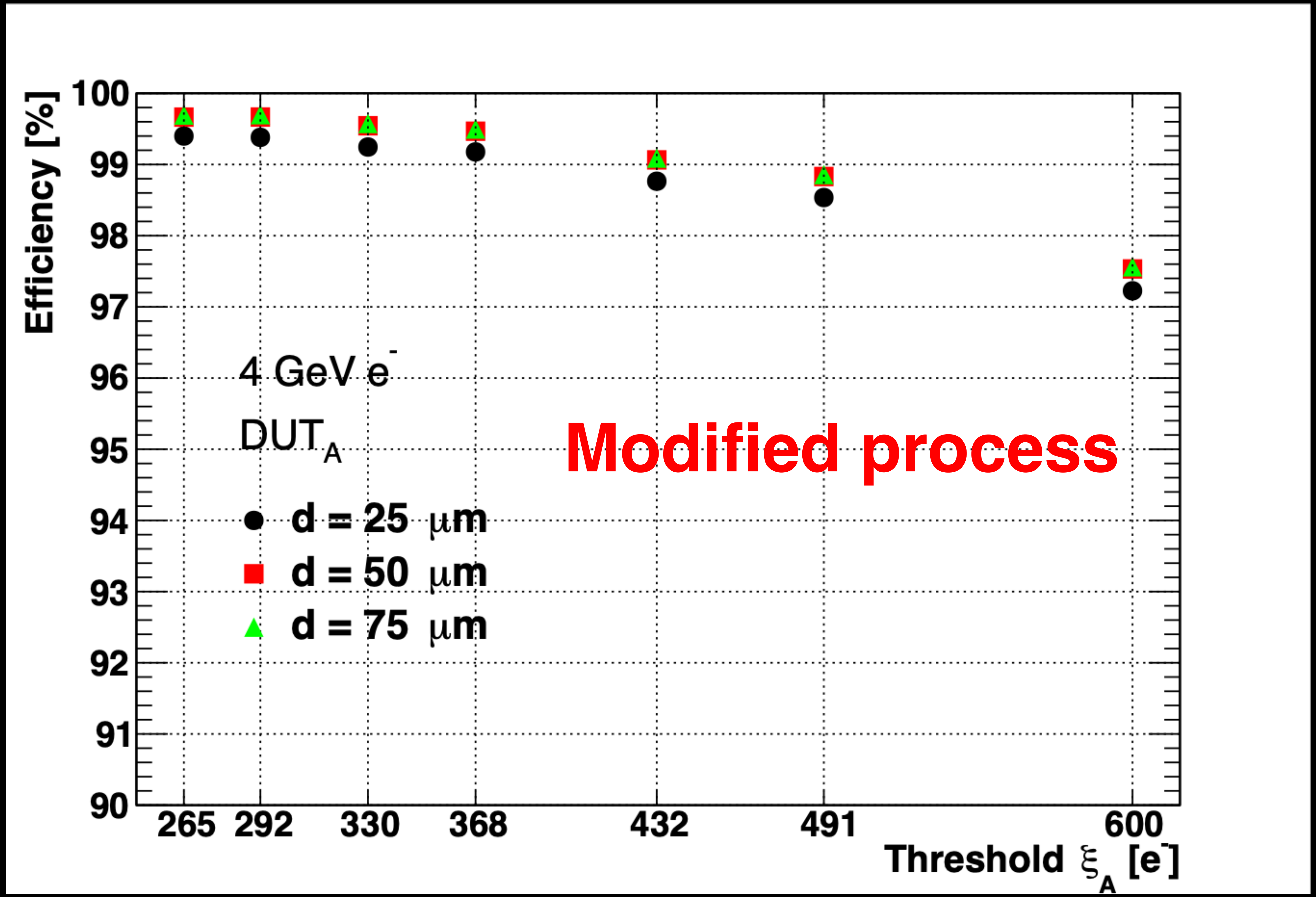
Track time - DUT time

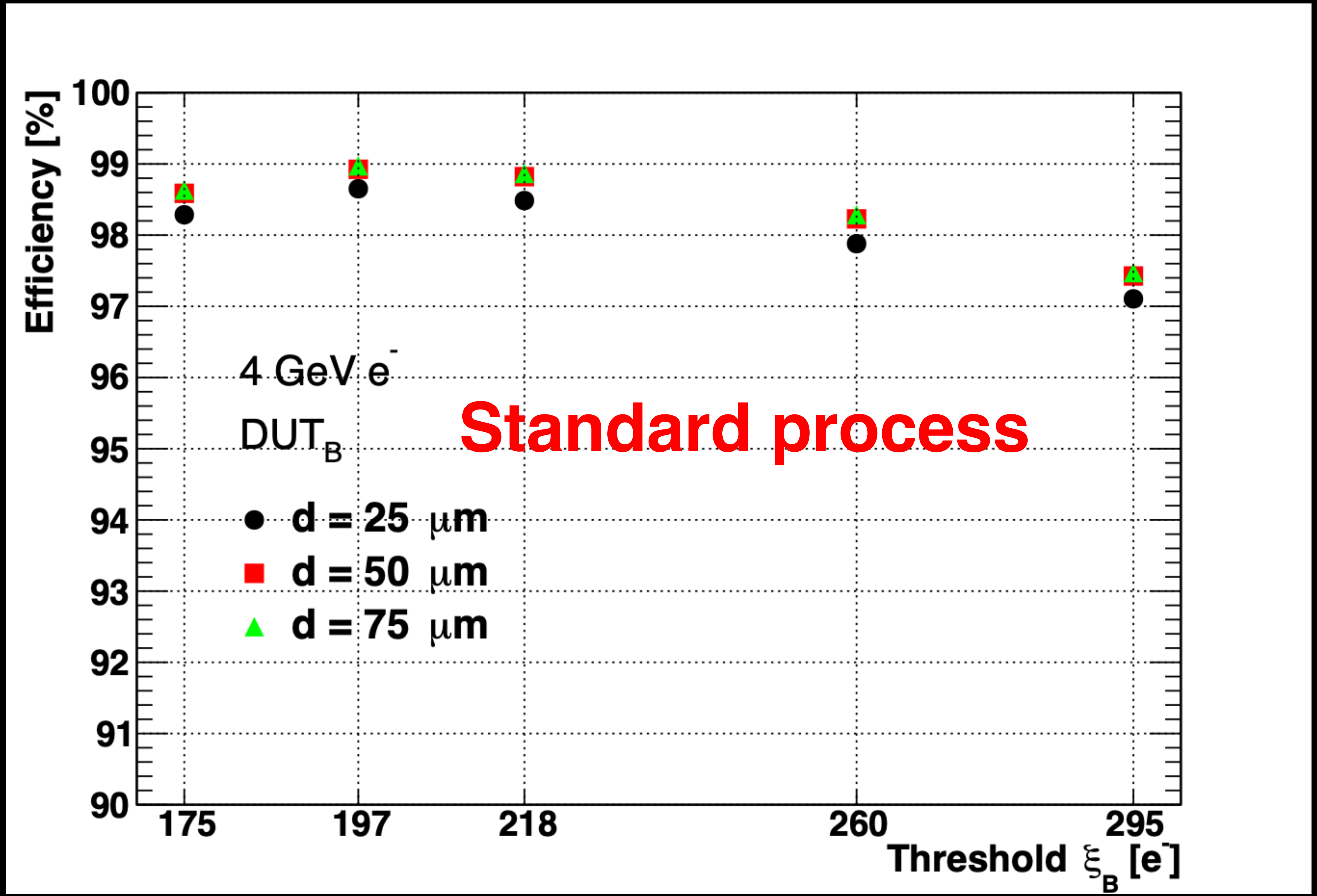


Efficiency Vs threshold

- Efficiency is the ratio of tracks that match the hit on the DUT within a distance around the predicted hit from the telescope to all tracks of the telescope
  - It can reach about 99% efficiency in optimized threshold

$$\epsilon = \frac{N^{matched\ Tracks}_{|x_{meas},y_{meas} - x_{pre},y_{pre}| < d}}{N^{Tracks}_{tel}}$$

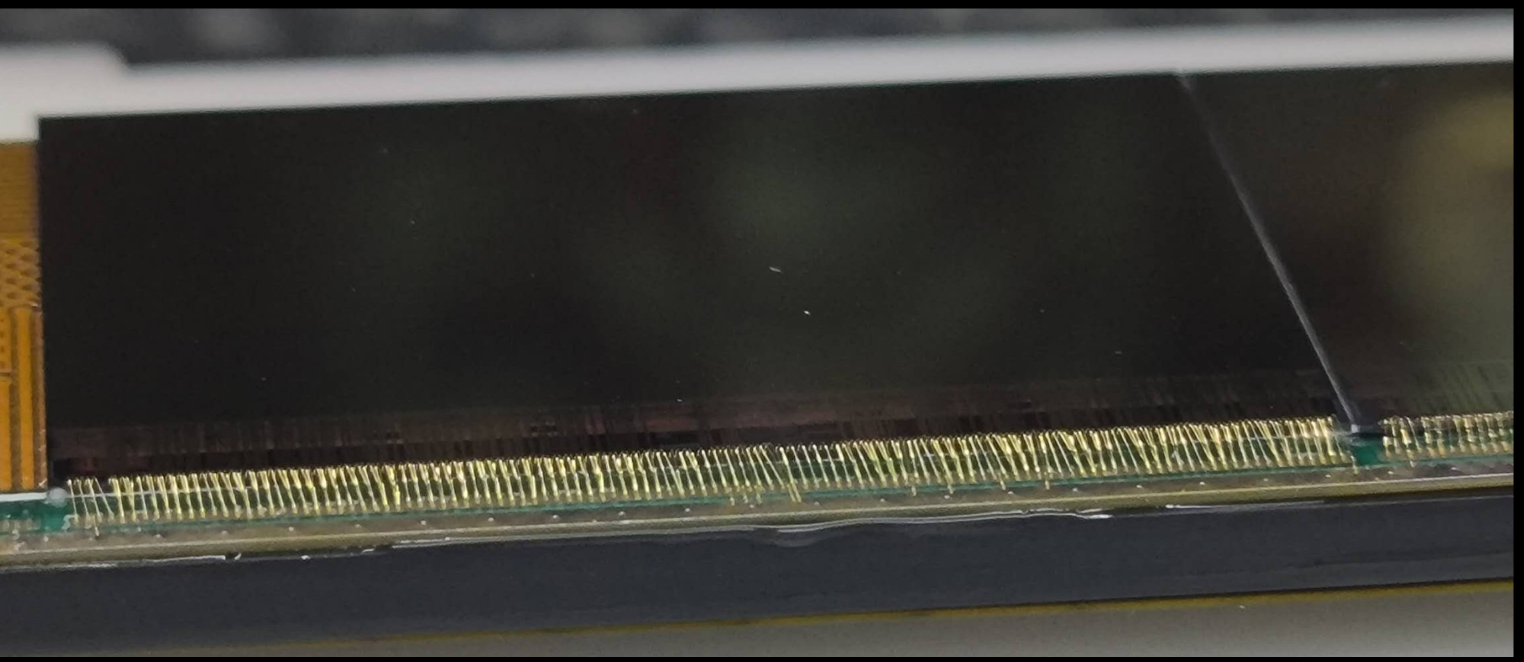


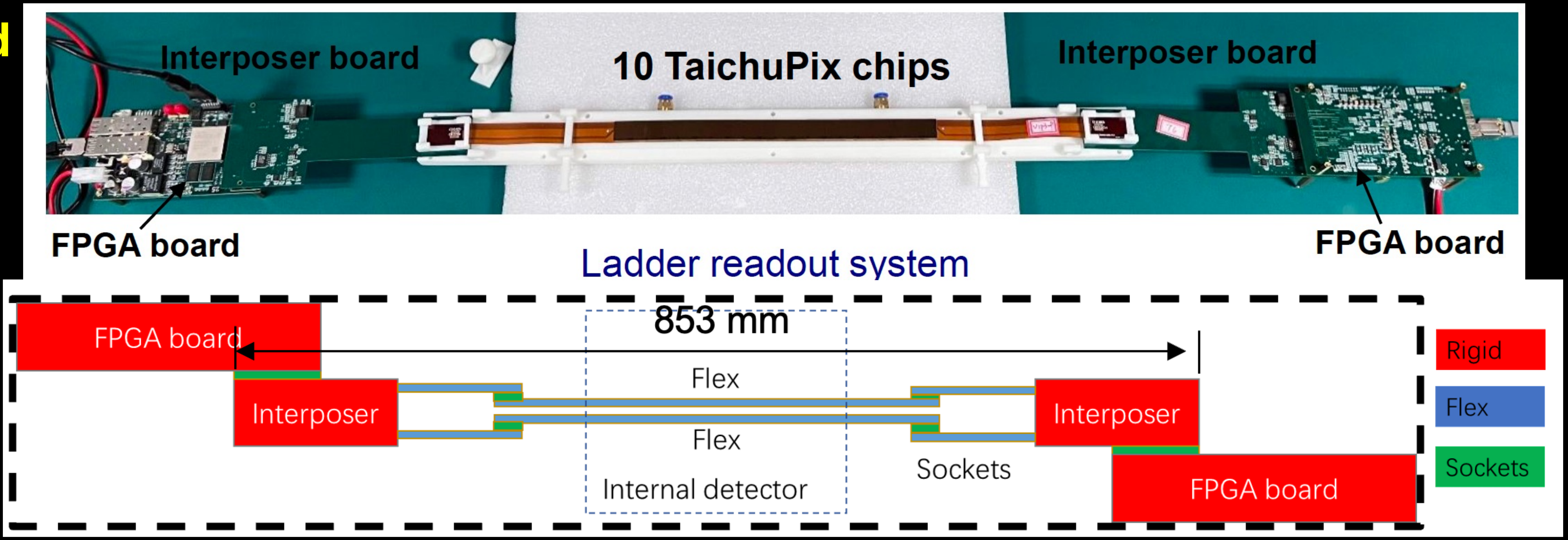


Detector module (ladder) R & D

- Completed detector module (ladder) design
  - Detector module (ladder) = 10 sensors + readout board + support structure + control board
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- Challenges
  - Long flex cable→ hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals

Taichupix chip wire bonded on FlexPCB





- Solutions
  - Readout from both ends, readout compose of three parts, careful design on power placement

Laser test result of ladder

- A full ladder includes two identical fundamental readout units
  - Each contains 5 TaichuPix chips, a interposer board, a FPGA readout board
- Functionality of a full ladder fundamental readout unit was verified
  - Scanning a laser spot on the different chips with a step of 50 μm,

  →Clear and correct letter imaging observed

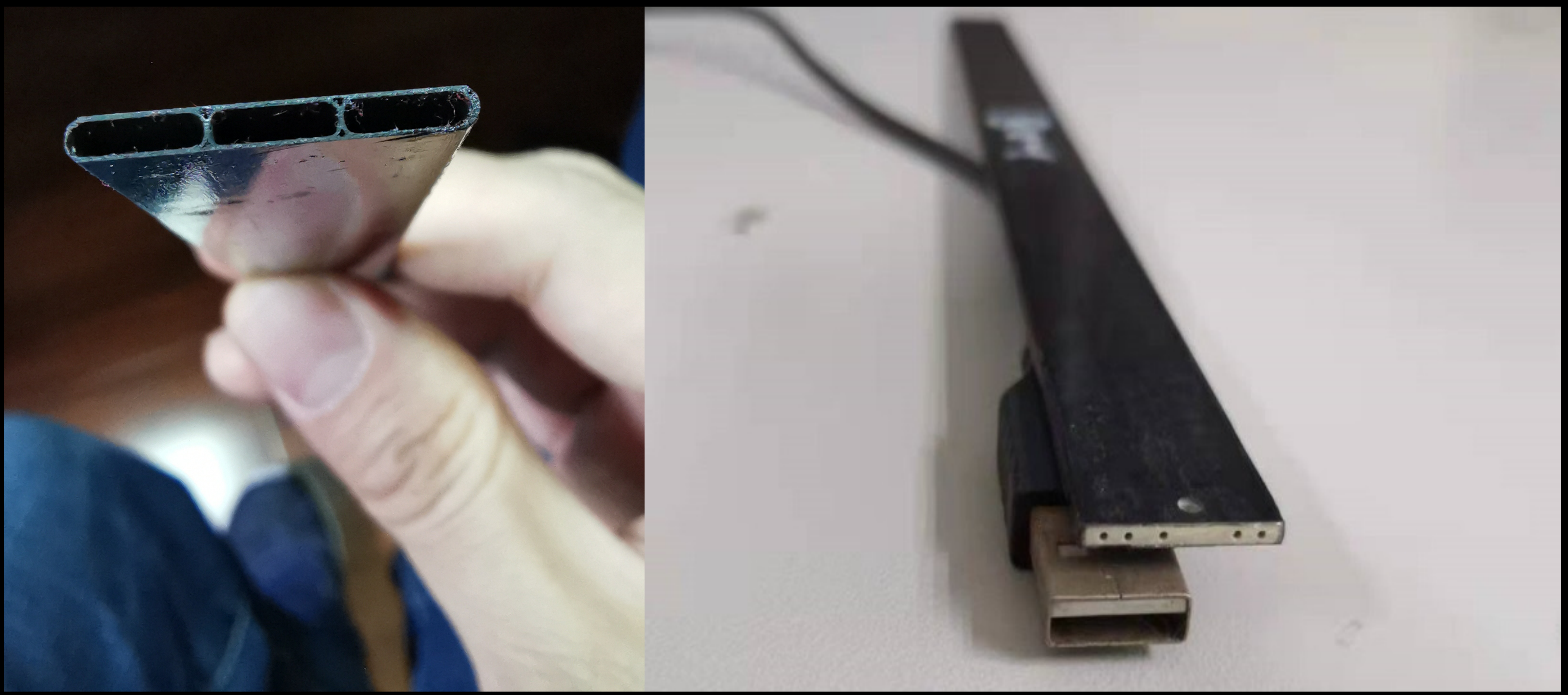
  →Demonstrating 5 chips working together → one ladder readout unit working

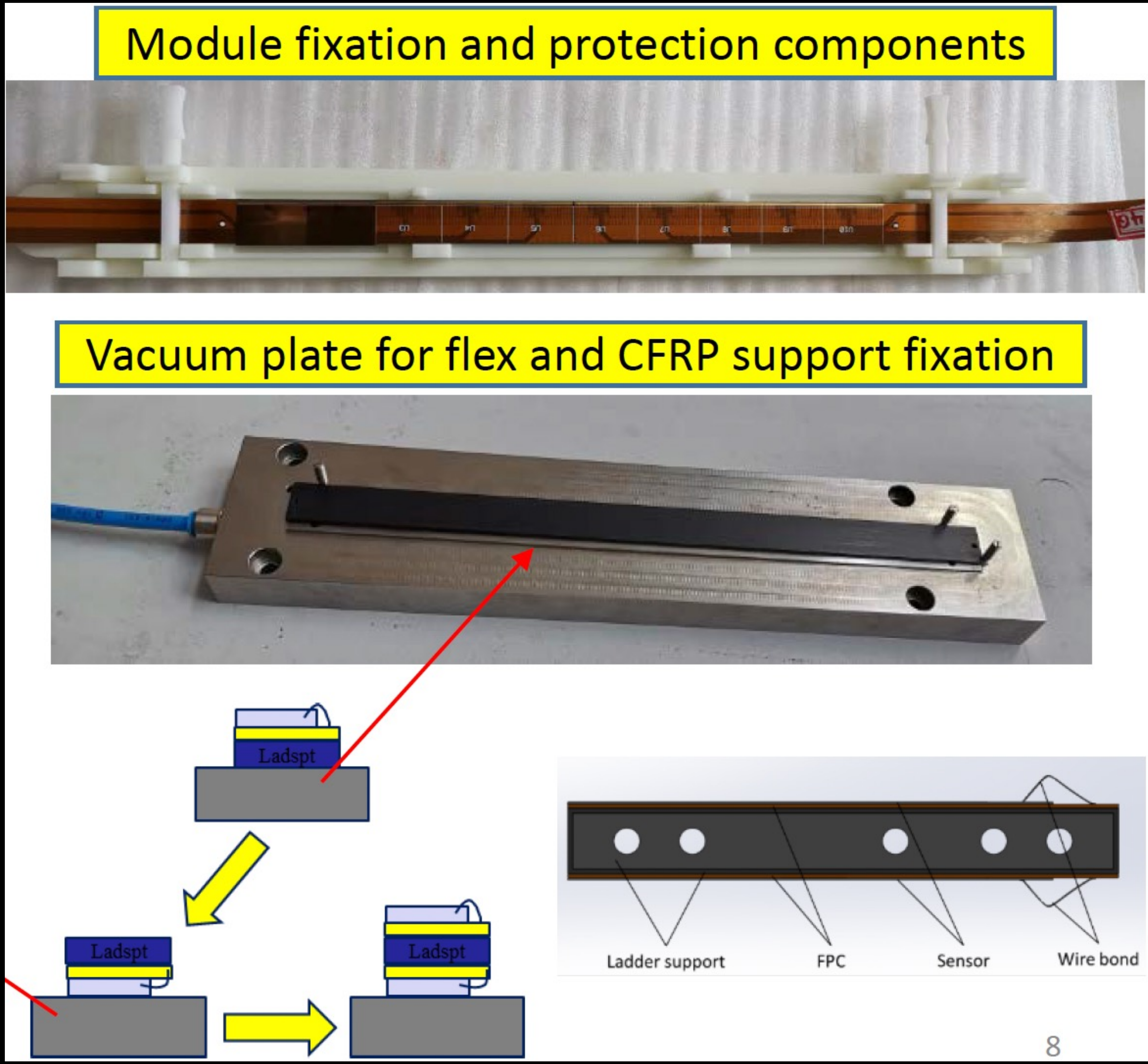
Laser tests on Taichupix chip on full ladder
（"CEPCV" pattern by scanning laser on different chips on ladder ）

Double-side ladder in CECP vertex detector

- Ladder in vertex detector is double-sided
  - Two flexible PCB + one carbon fiber support
- Both side has wire-bonding → Challenging
- Dedicated tooling for double-side assembly

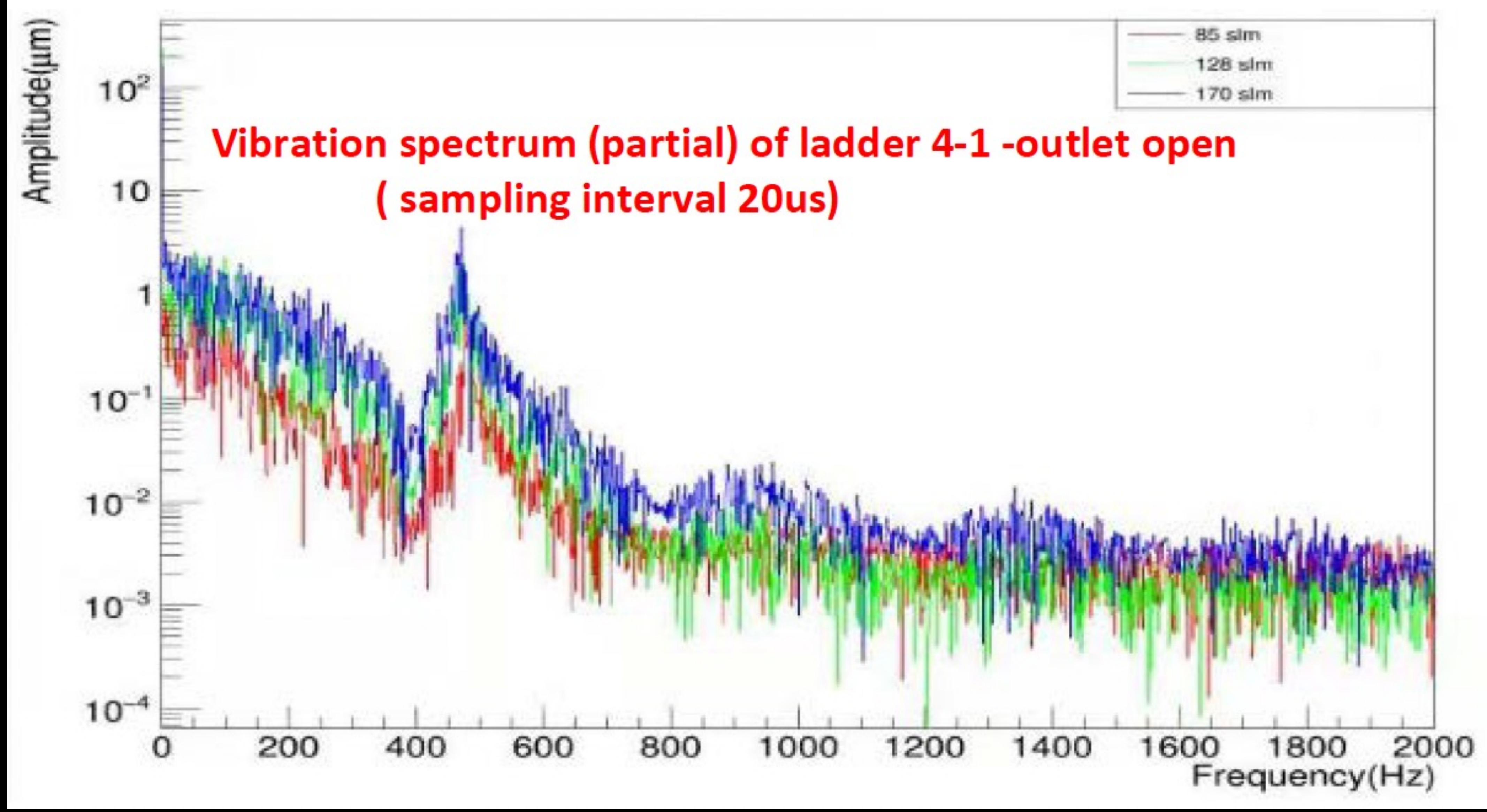
Designed and fabricate carbon fiber support



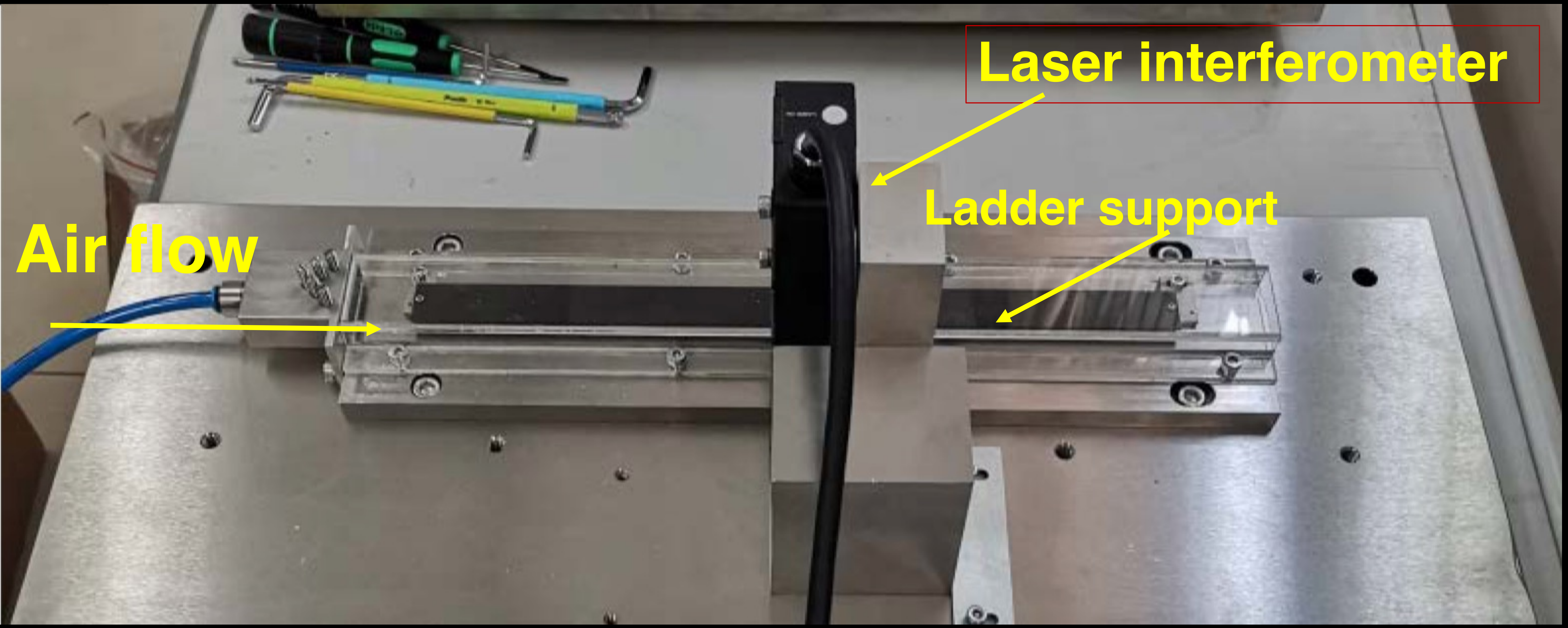


Air Cooling test on ladder

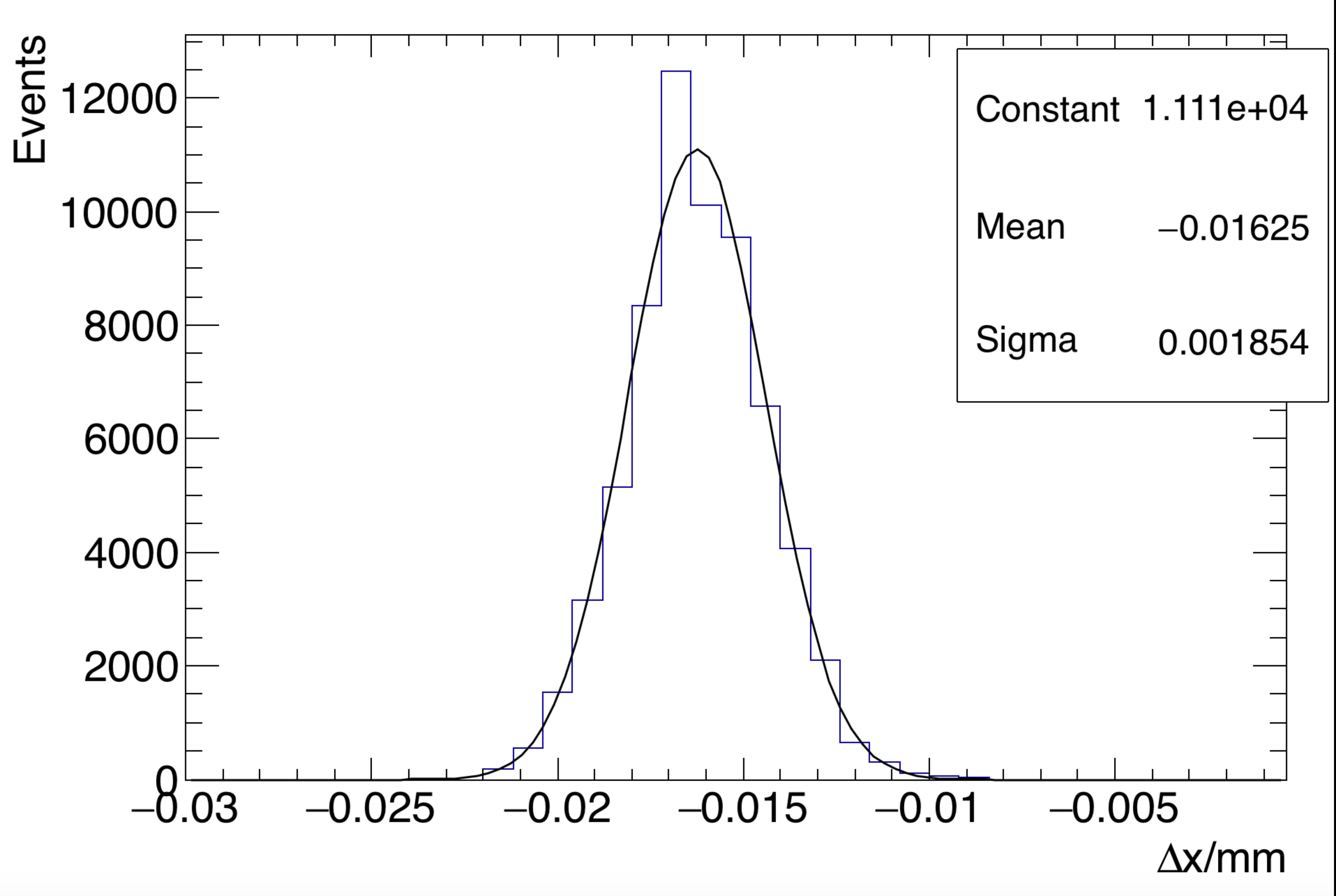
- **Test bench setup for ladder air-cooling**
- **Vibration follows Gaussian distribution**
  - **Core of Gaussian is still under control 1~2μm**



Test setup prototype for ladder cooling
Use compressed air for cooling

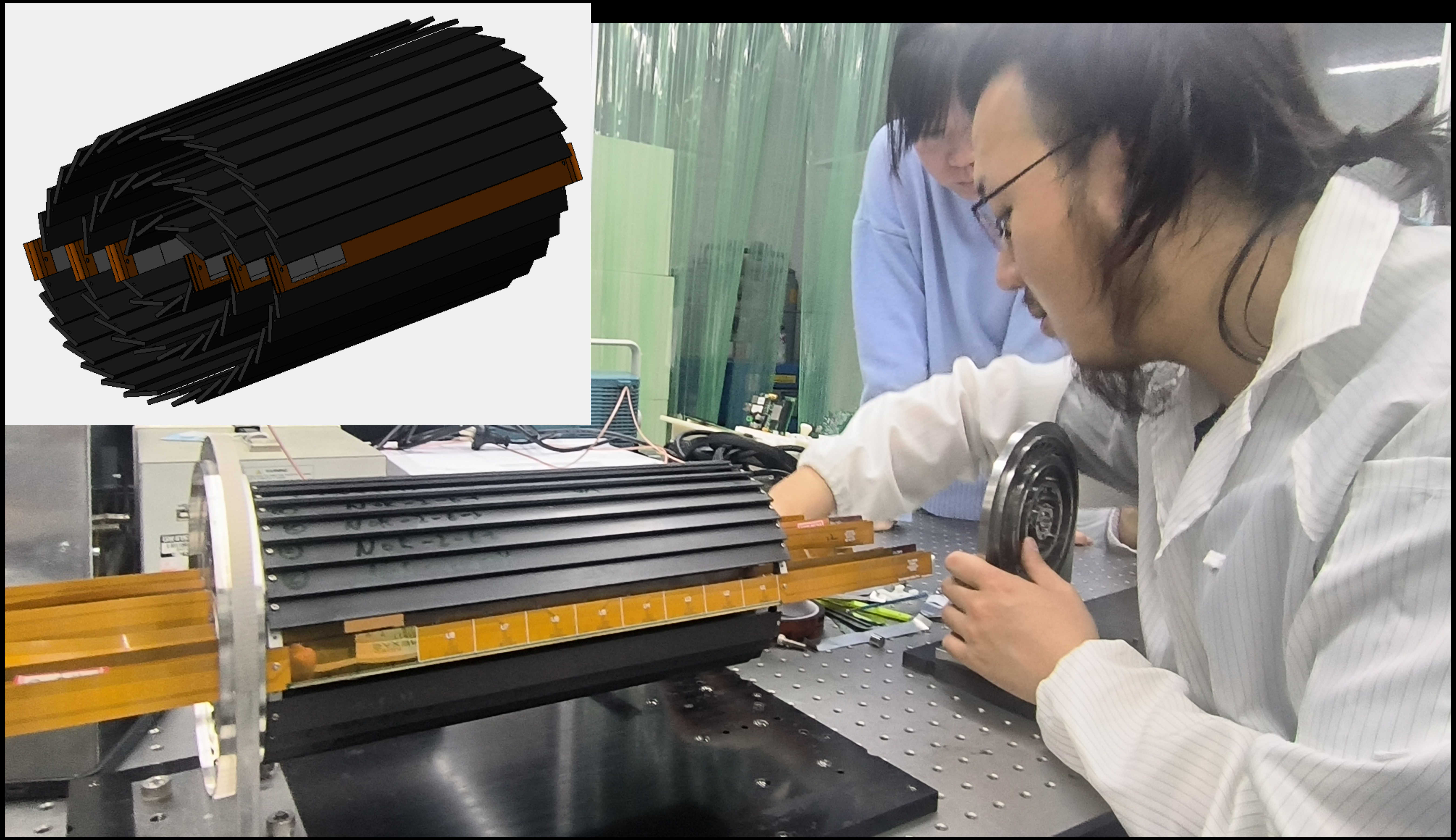


Typical Vibration displacement during air cooling



Vertex detector Prototype assembly

- Six double-side ladders installed on the vertex detector prototype
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype

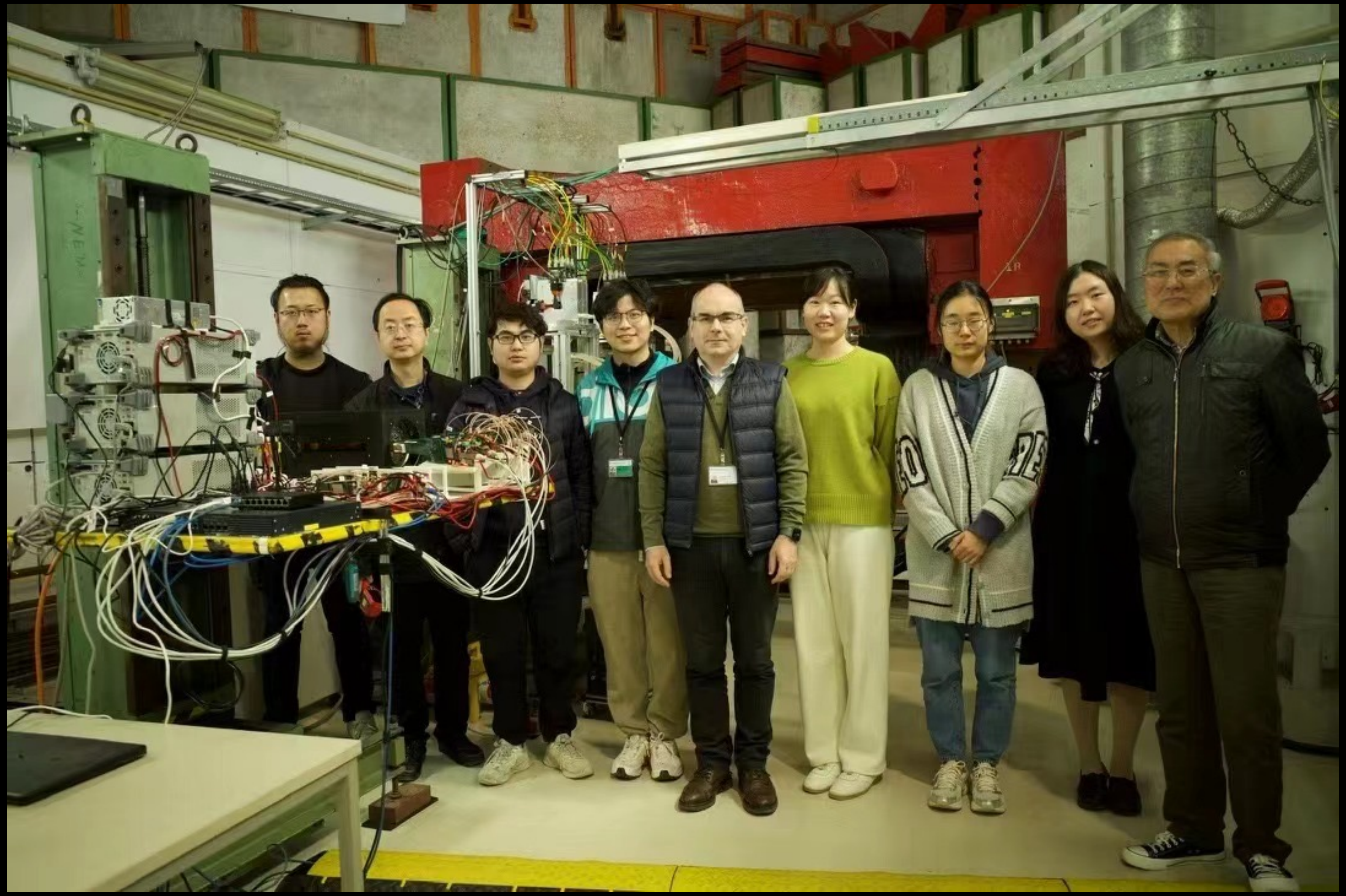


Test beam @ DESY

- 2nd testbeam: April 11-23 2023 DESY test beam in Germany (4-6GeV electron)
  - Vertex detector prototype testbeam
- 1st testbeam: Dec 12-22 2022 DESY test beam in Germany (4-6GeV electron)
  - TaichuPix Beam Telescope testbeam

2022 DESY test beam

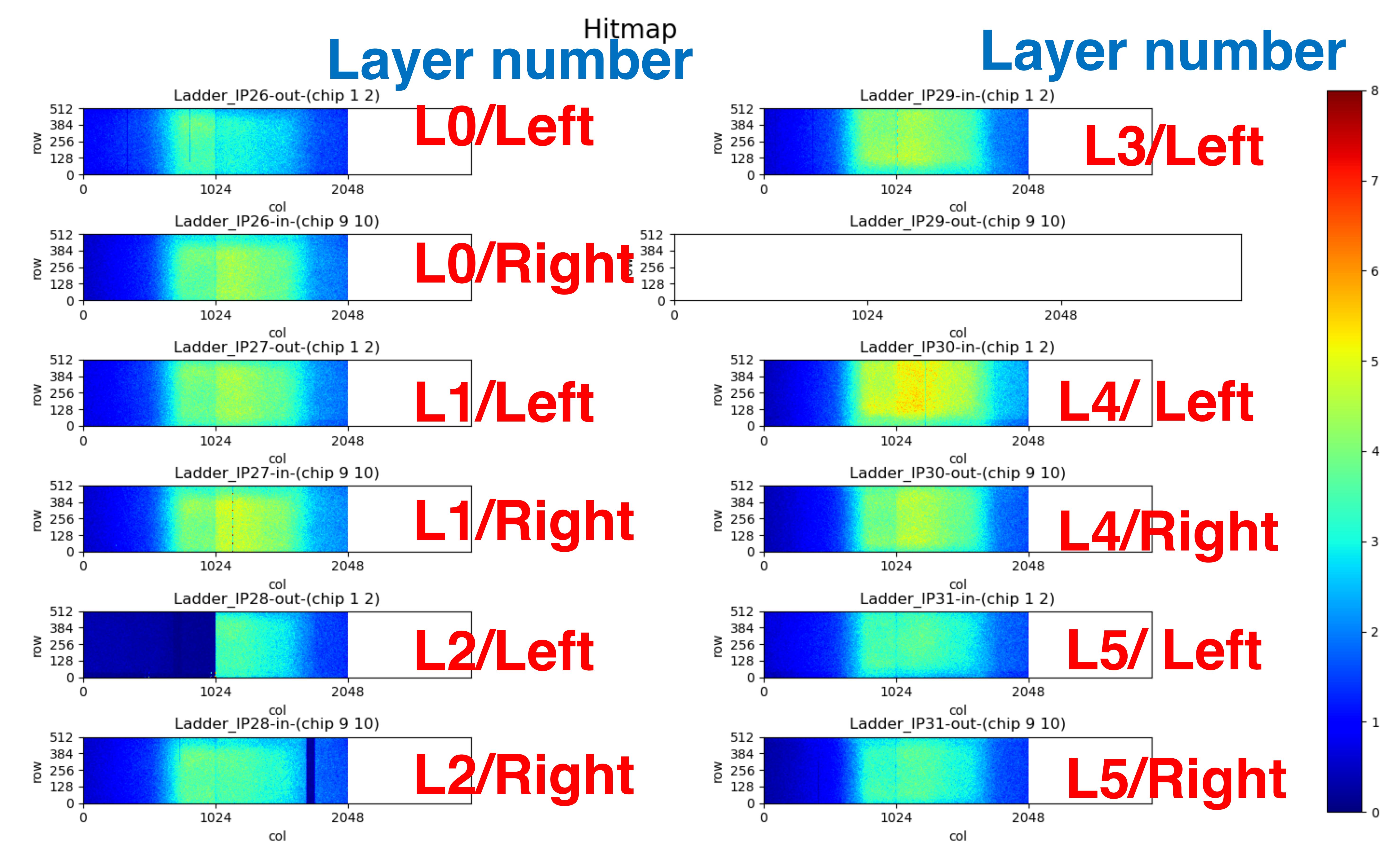
2023 DESY test beam



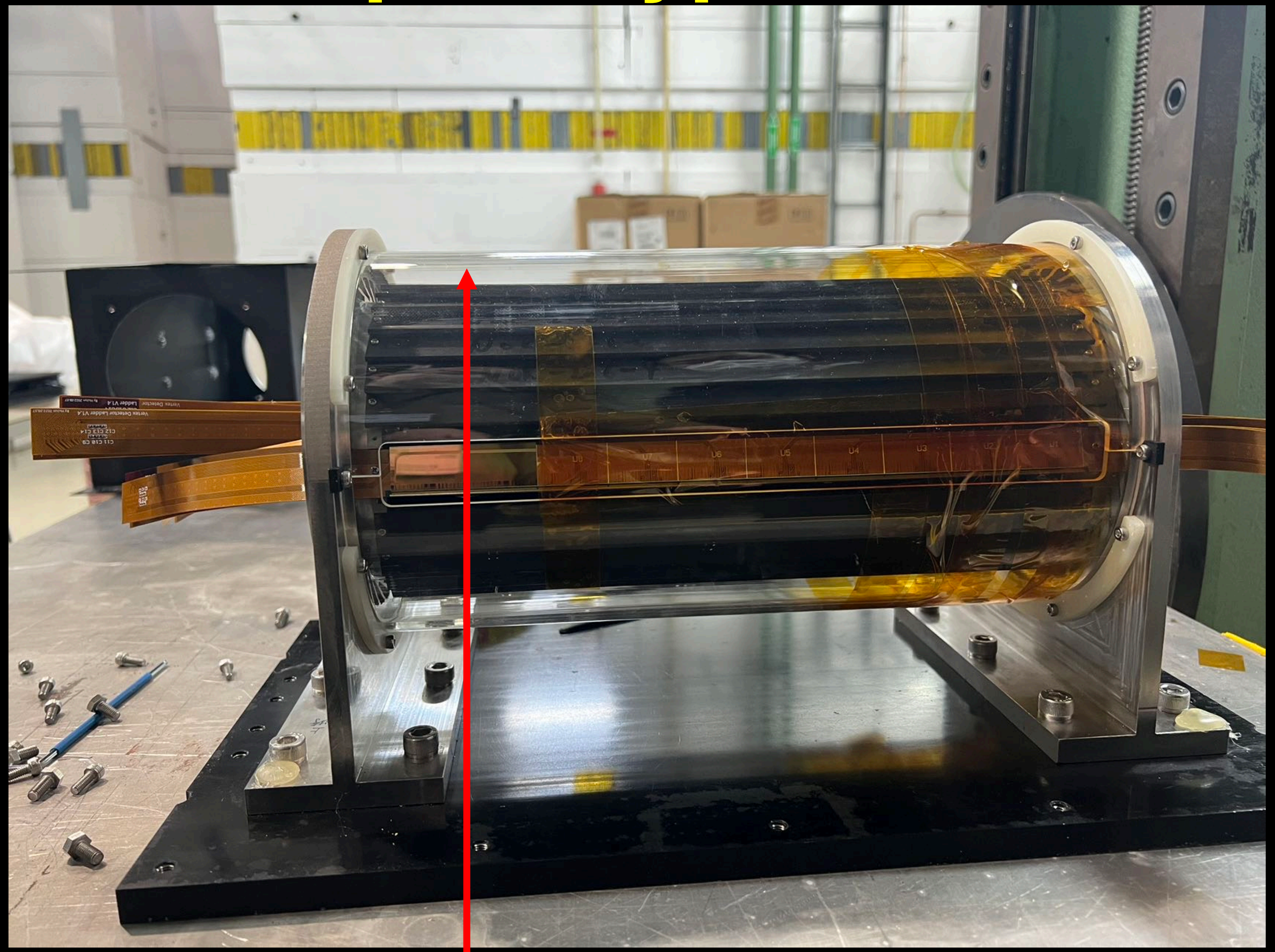
Test beam @ DESY for detector prototype

- Six double-side ladders installed on the vertex detector prototype for DESY testbeam
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype
  - Beam spot (~2×2cm) is visible on detector hit map
  - Record about one billion tracks in two weeks

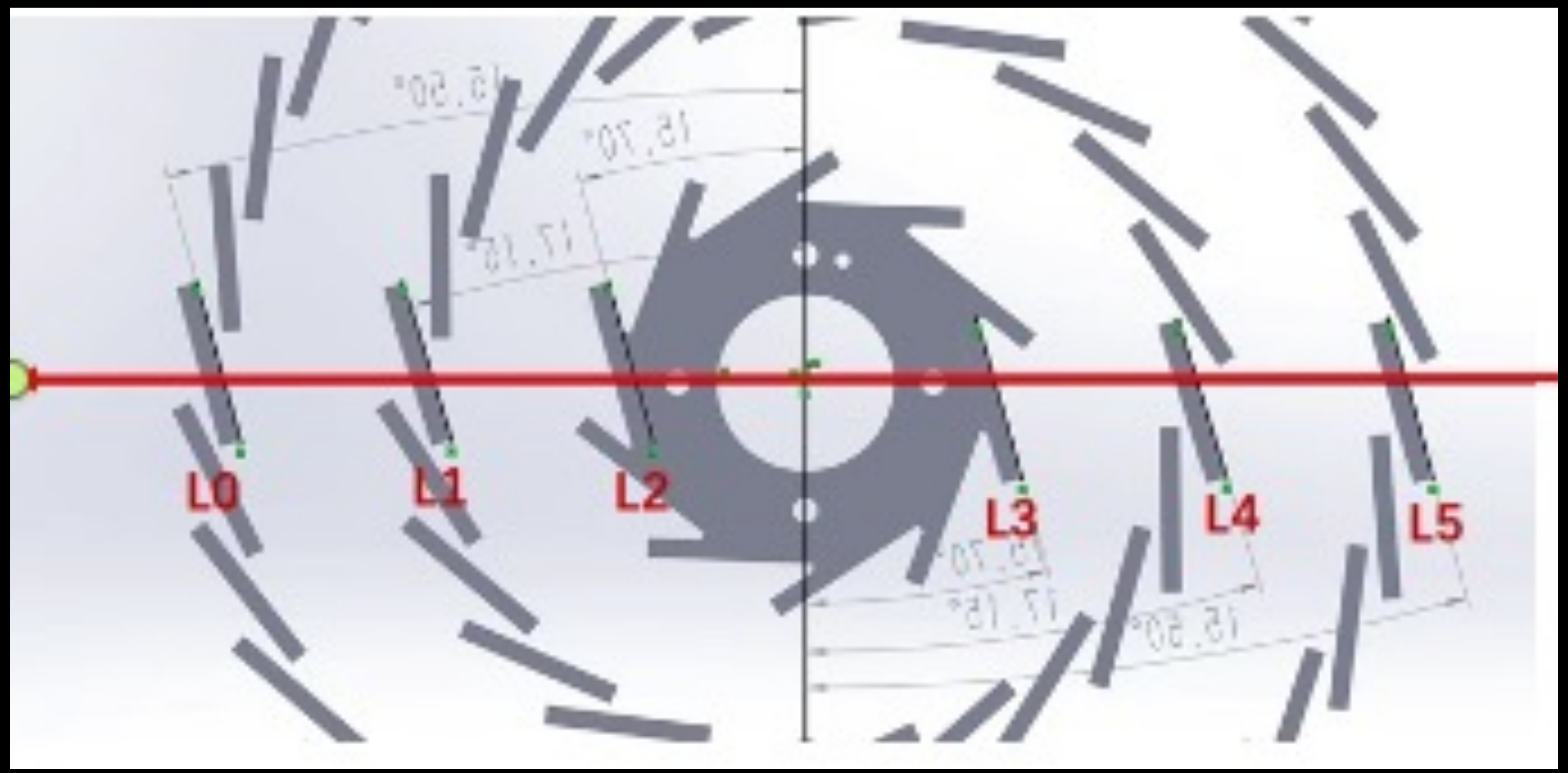
Hit maps of all layers taichupix on prototype



Detector prototype in testbeam

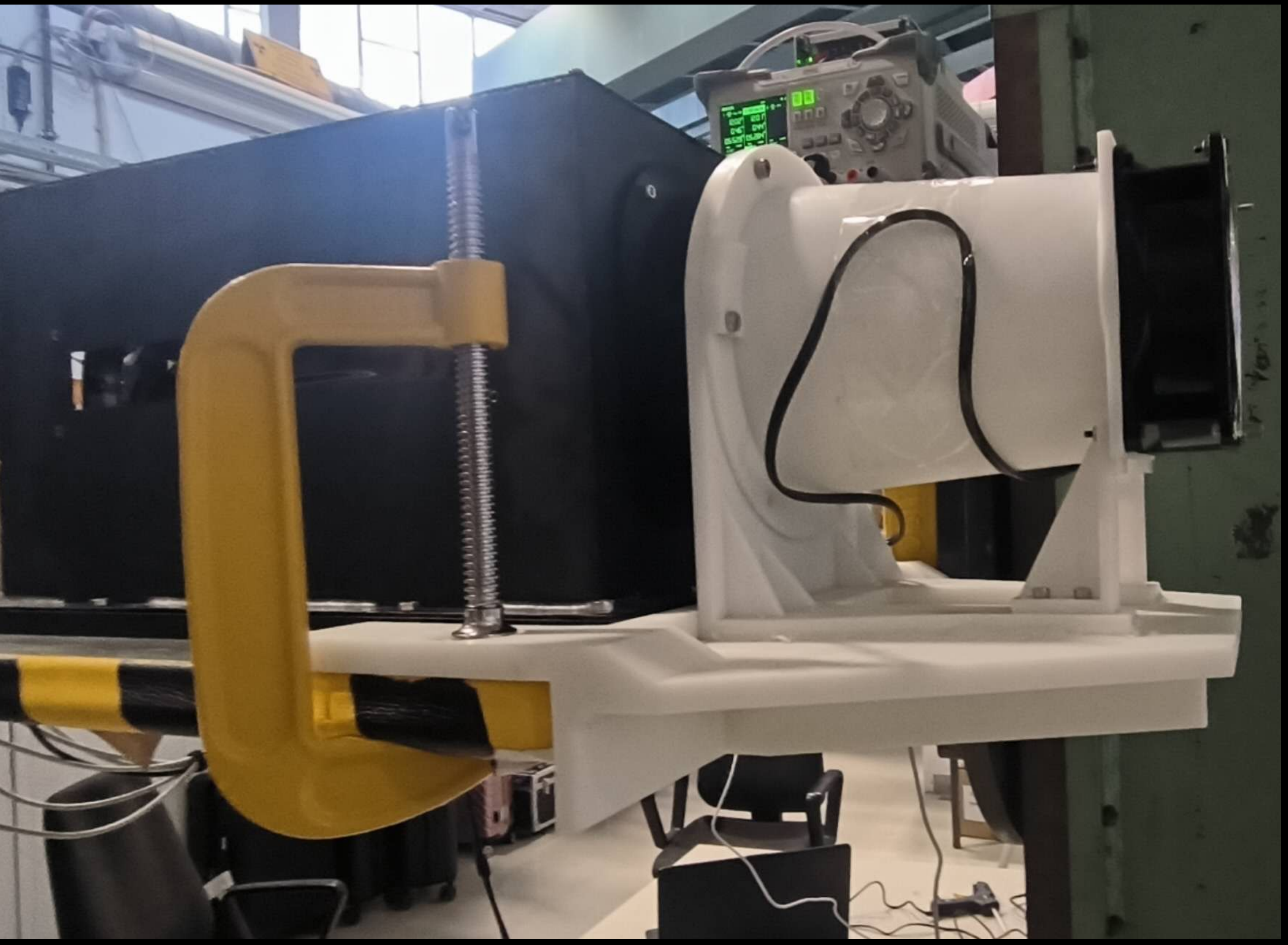


DESY Electron testbeam

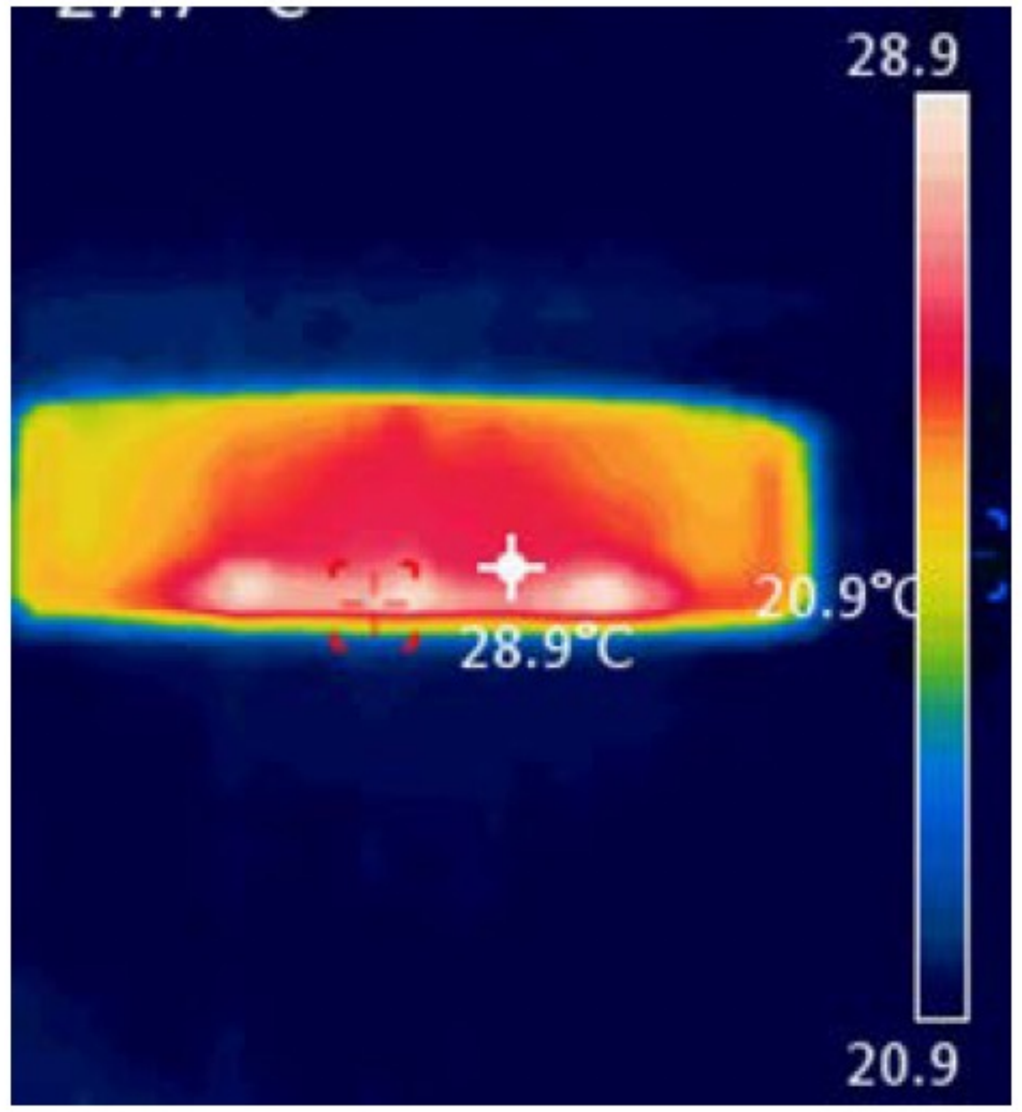


Air Cooling for vertex prototype

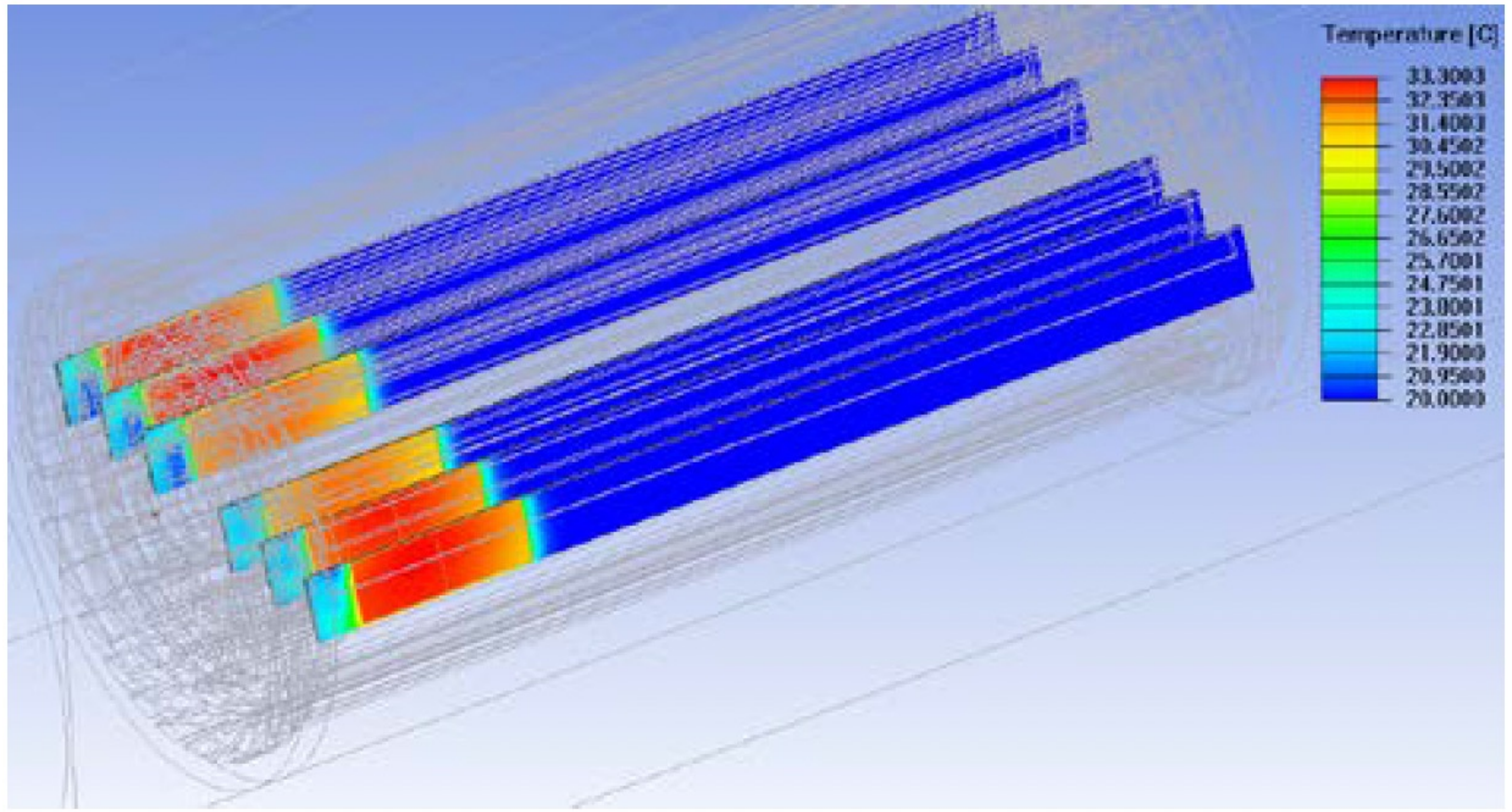
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm2 (17.5 MHz clock in testbeam)
  - Before turning on the fan, chip temperature can go above 41 °C.
  - With air cooling, chip temperature can reduced to 25 °C (in average)
    - In good agreement to our cooling simulation
  - No visible vibration effect observed in position resolution offline analysis when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃

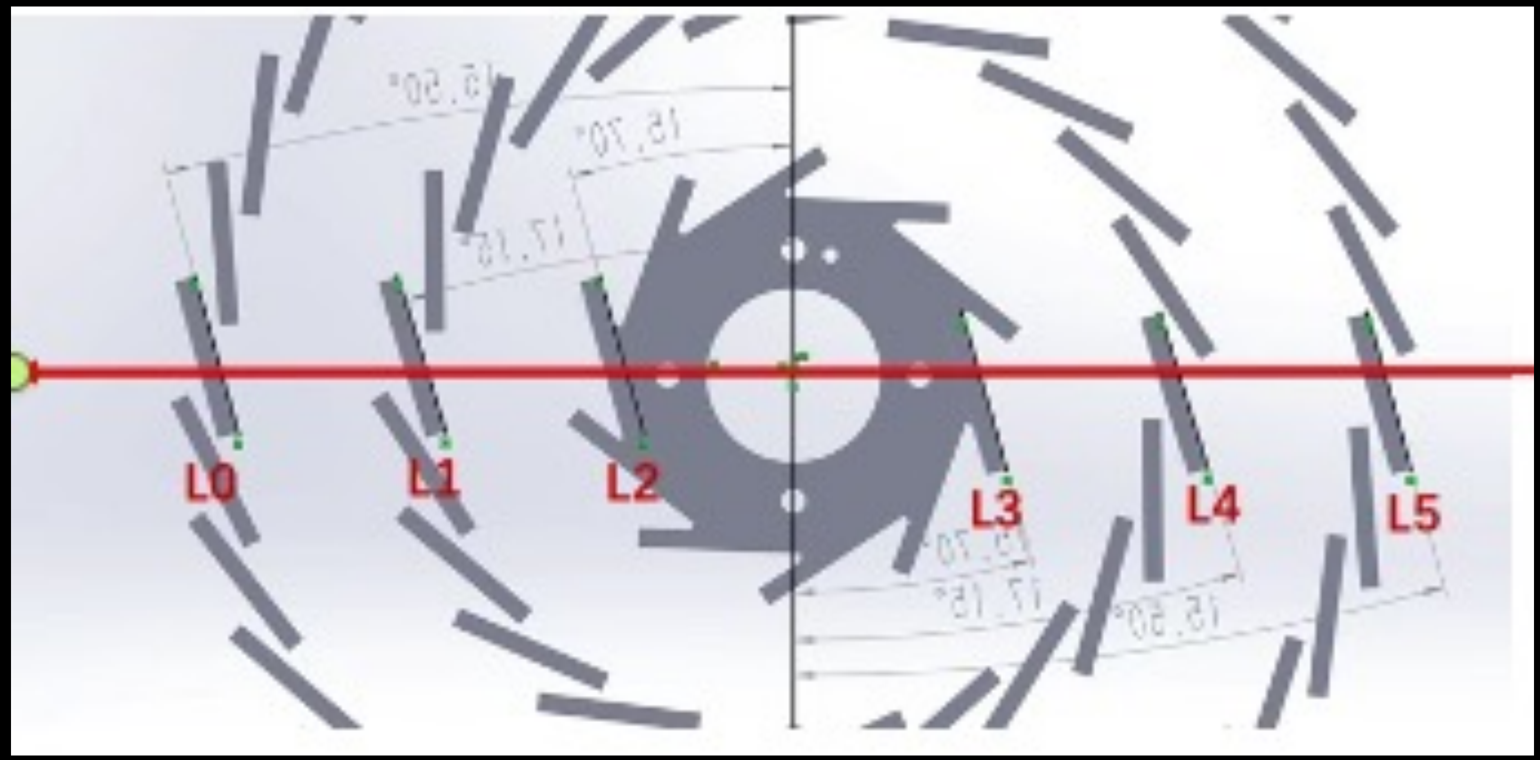


Prototype cooling simulation： Max 33.3 ℃

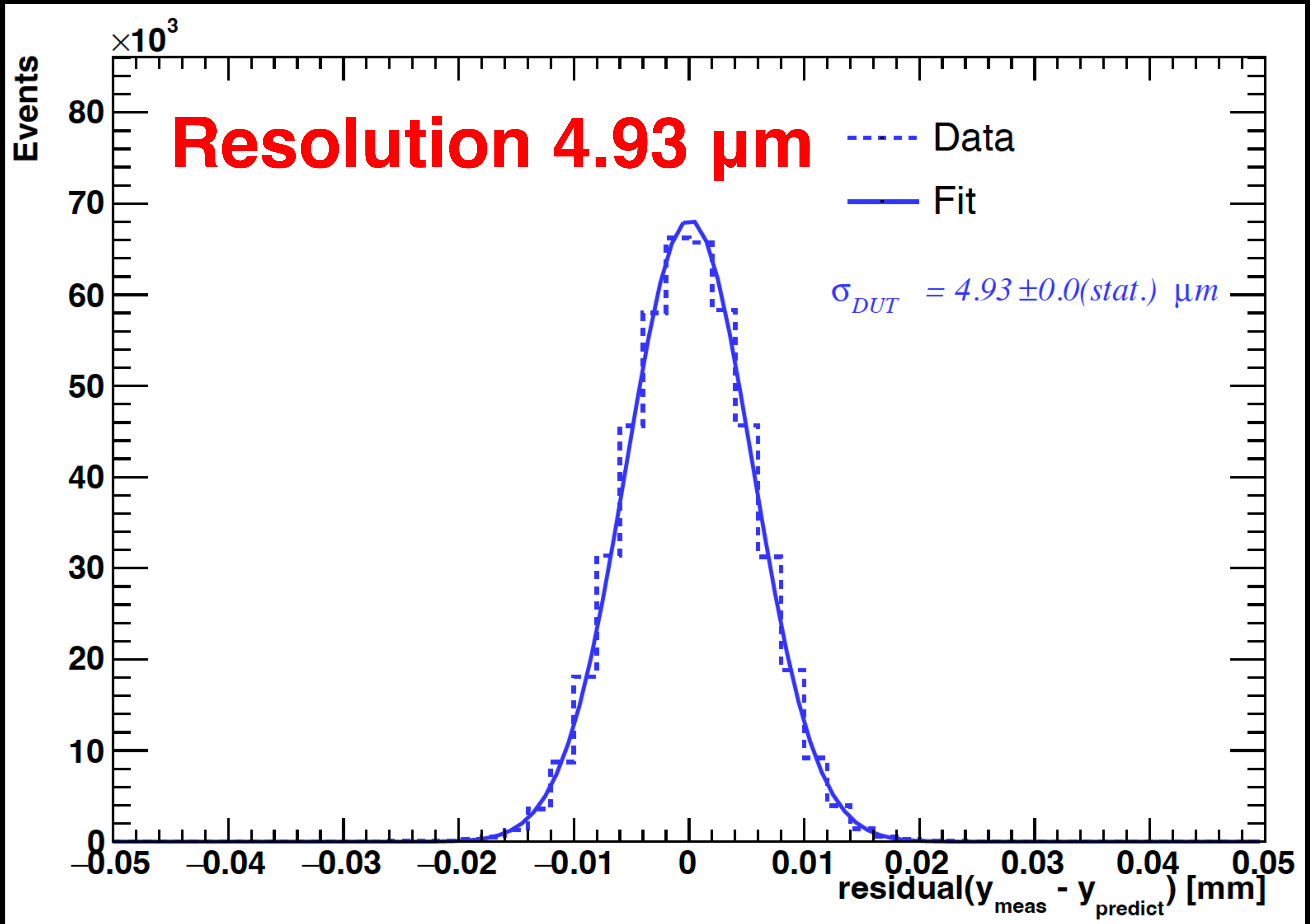


Test beam results (April 2023)

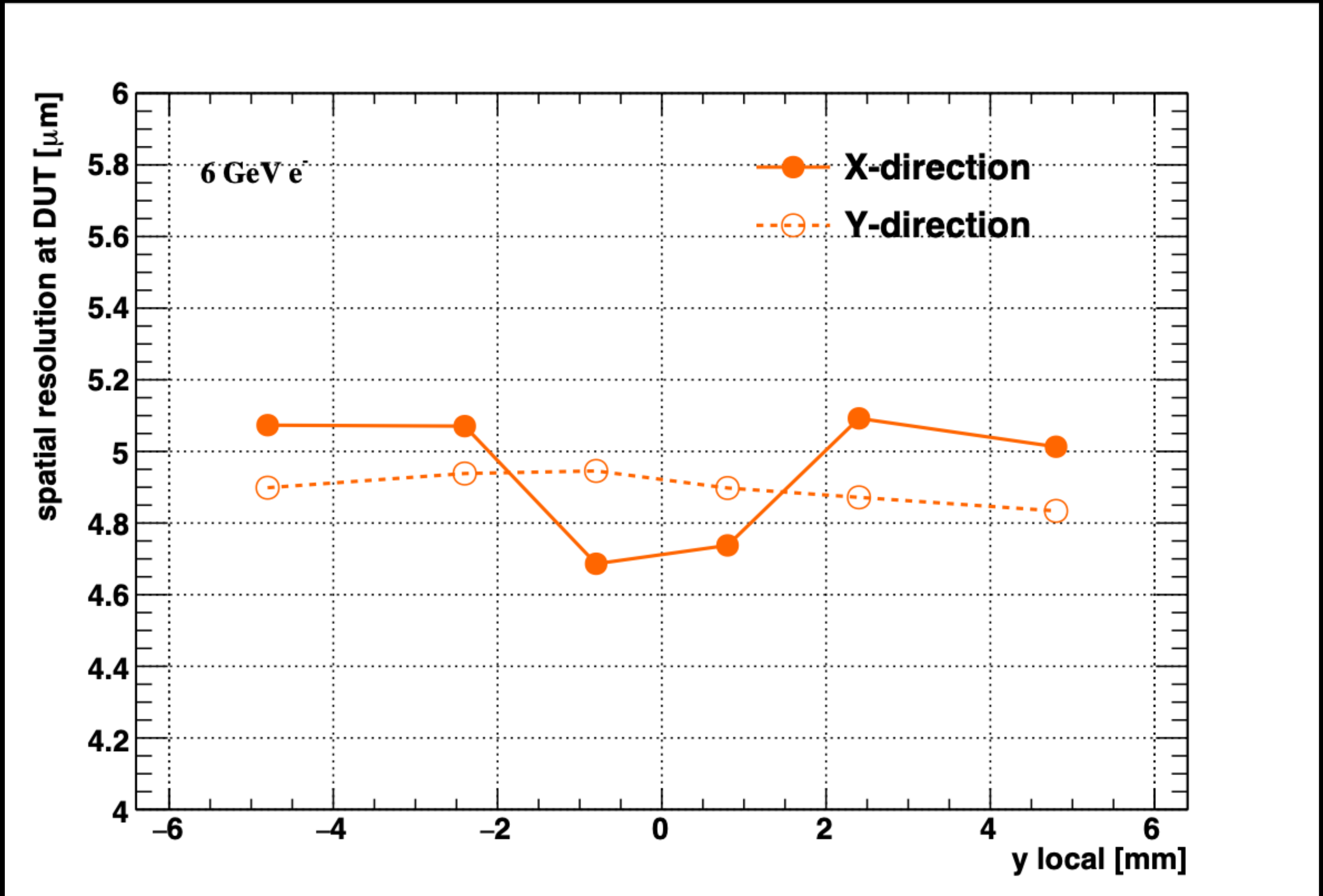
- Extract Spatial resolution from detector prototype testbeam data
  - One layer (L1) of TaichuPix used as Detector-Under-Test (DUT)
  - Other layers of vertex detector prototype used for track fitting
  - Spatial resolution reached 4.9μm (Y axis→ bending direction)
    - Spatial Resolution met the requirement (3-5μm)



Residual distribution in Y axis
DUT measured position – expected position from track



Spatial resolution vs hit positions
Y axis is bending direction

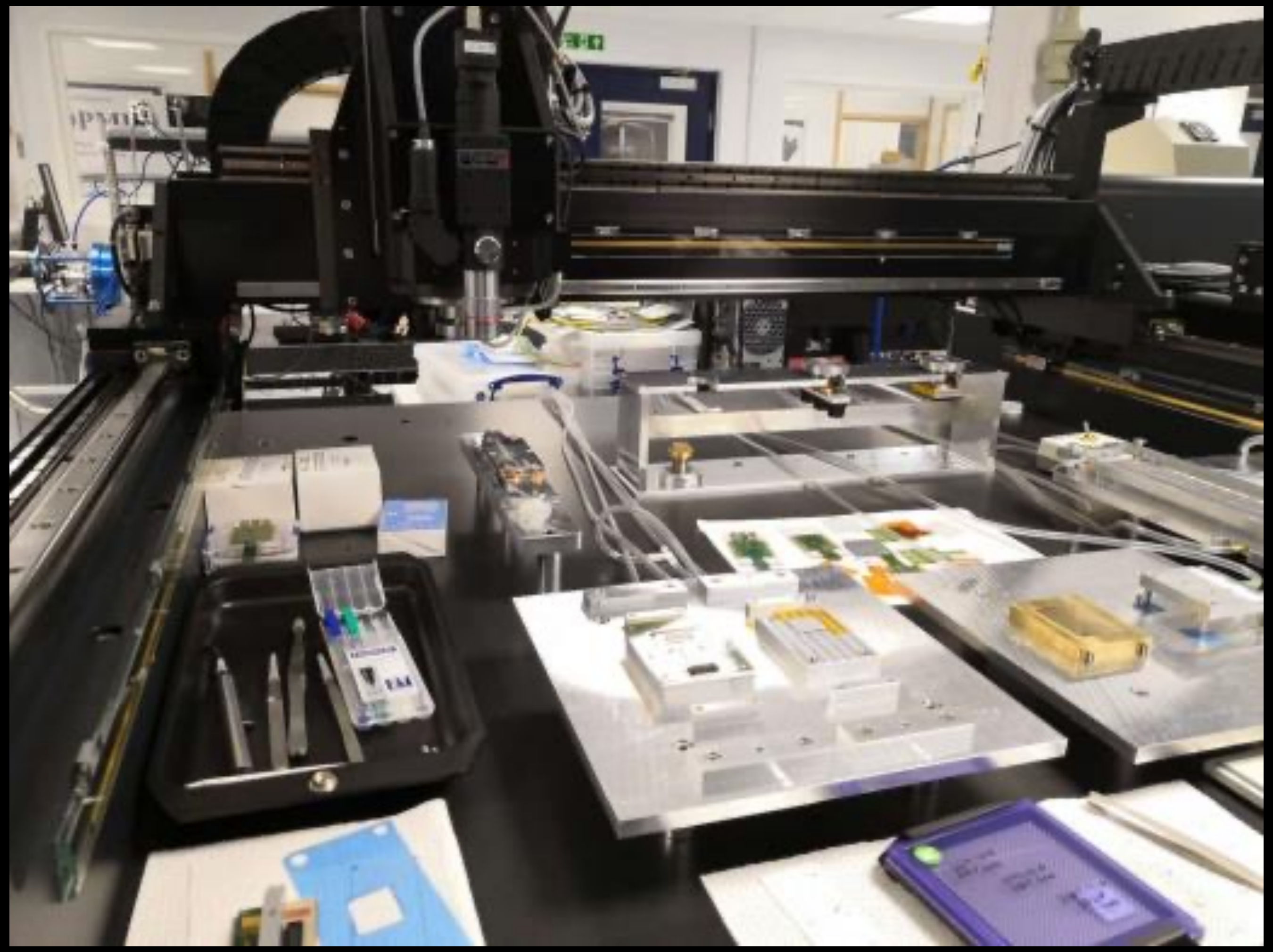


International Collaboration

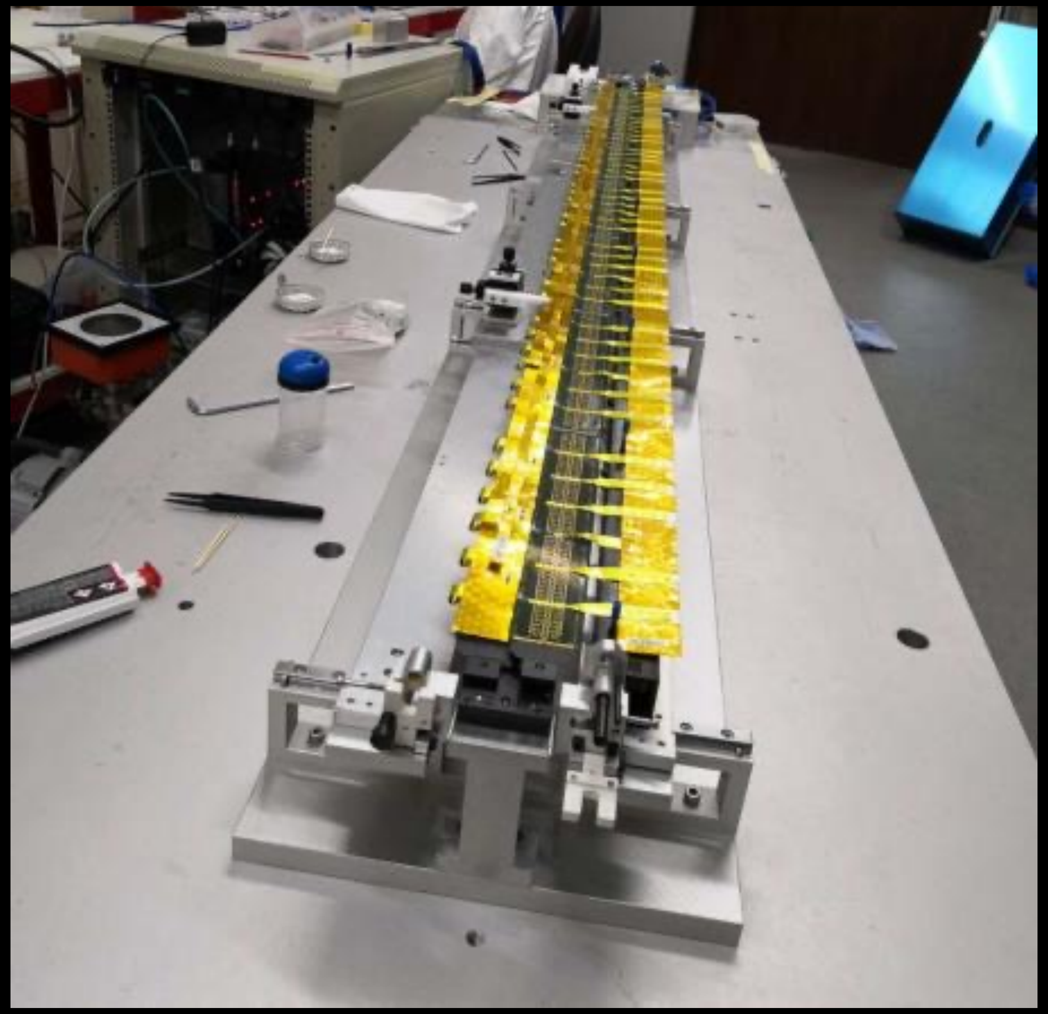
- ➢ **Active collaboration with IFAE (Spain) in sensor chip design.**
- ➢ **We have one engineer visited Oxford and Liverpool for 4 weeks in 2019**
- ➢ **Will incorporate the R & D with ECFA detector R & D (DRD3)**
- ☐ **Planning to collaborate on module and detector structure**
- ☐ **Unfortunately, Collaboration didn't continue due to CovID**

Lab visit in Oxford

Mu3e ladder, Atlas barrel strip stave prototype.



Labs visit in Liverpool

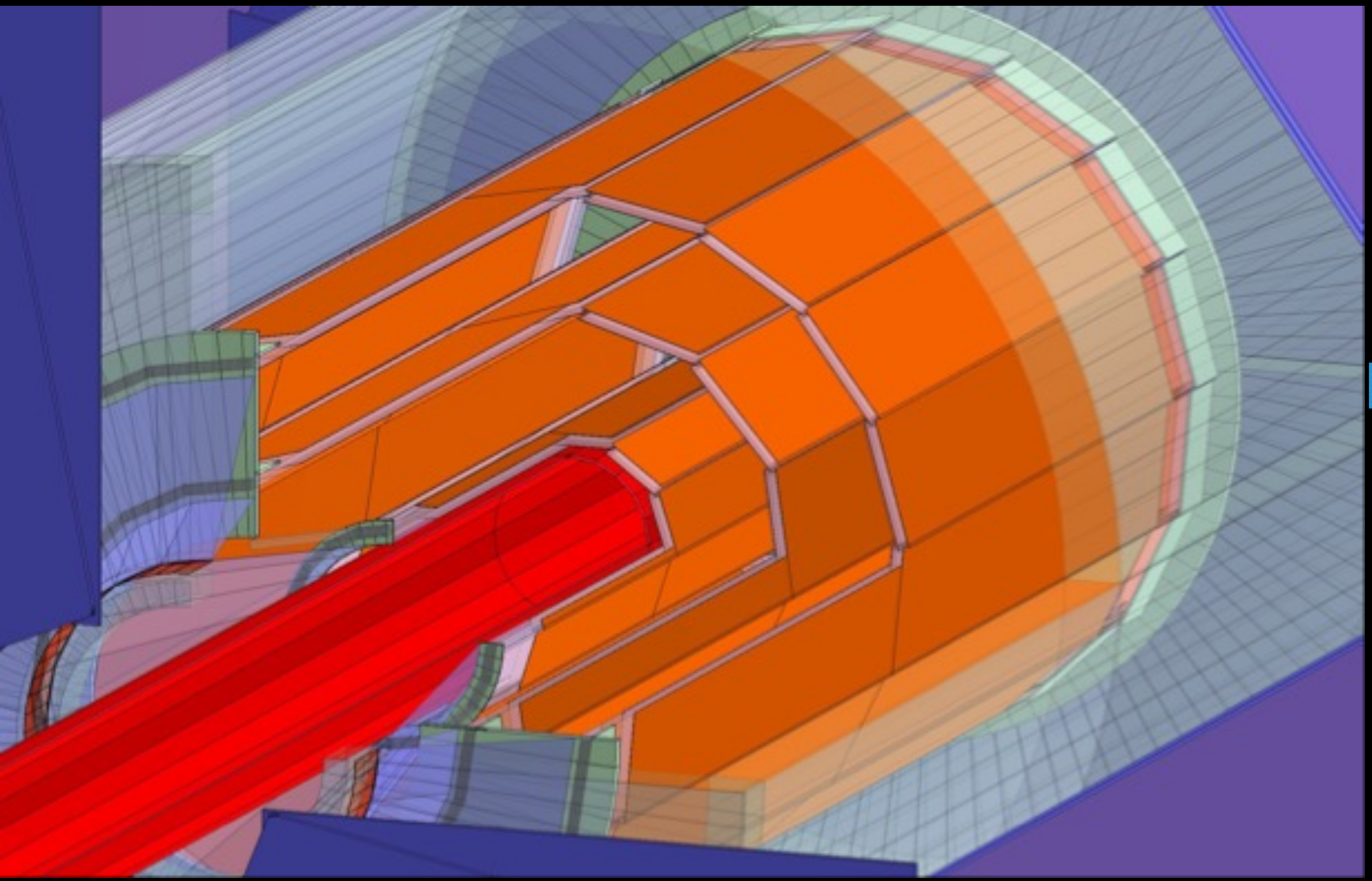


Module of Alice's OB tracker, Advance material Lab

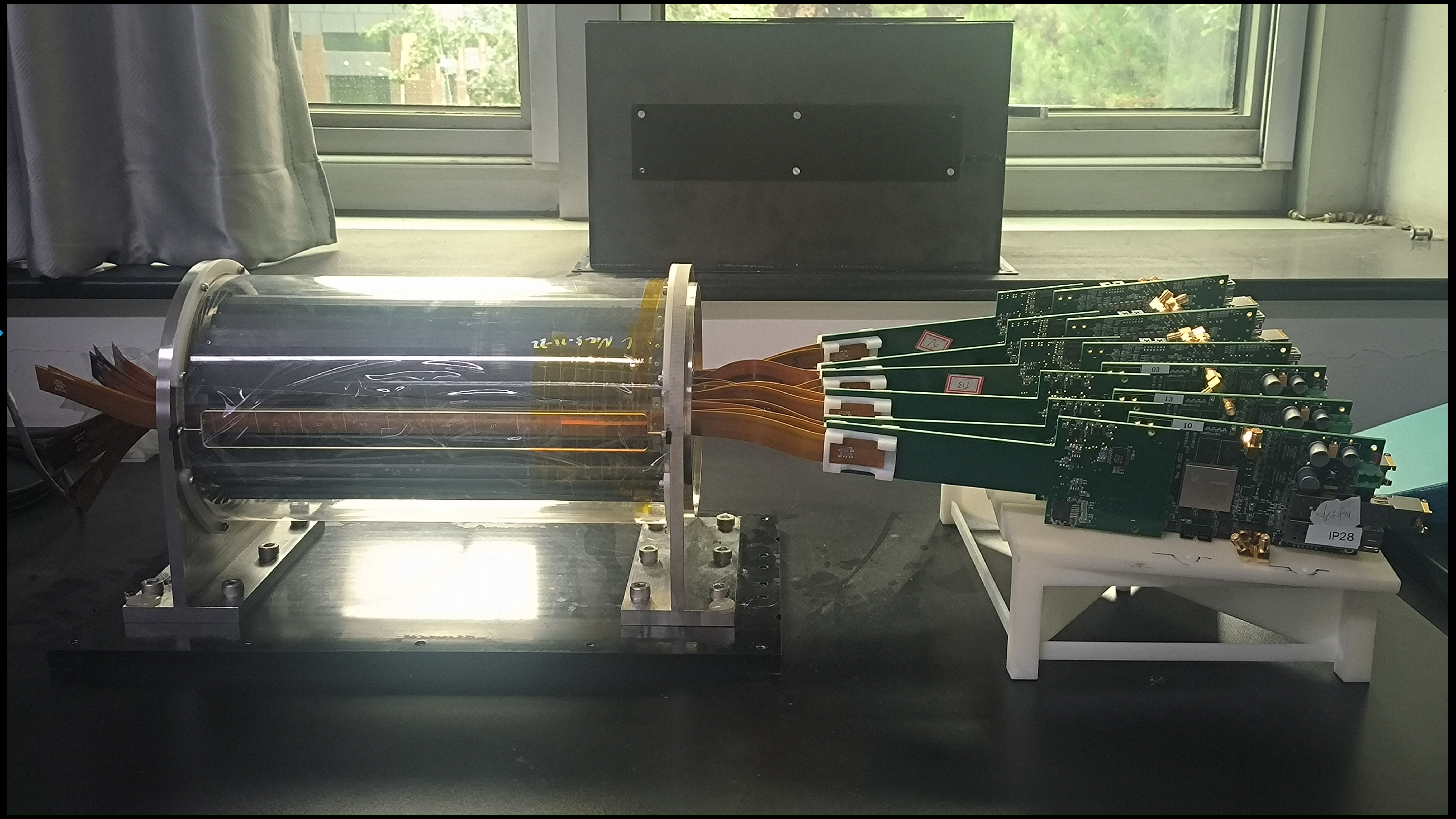
Summary of CECP vertex detector prototype

- **Developed full-size CMOS pixel sensor**
  - High spatial resolution and radiation hard
- **Developed the first vertex detector prototype in China**
  - Readout electronics and data acquisition for detector prototype was developed
- **Completed beam tests for the sensor prototype and the detector prototype at DESY**

CEPC design (2016)



Vertex detector prototype (2023)



Summary of CECP vertex detector prototype (2)

- Some remarks about future development

- Incorporate the R & D effort with ECFA detector R &D (DRD3 development)
- Cooling for vertex detector @ Z pole running is still need to explore
  - Air cooling feasibility for inner most layer is still need to be validated

- Cross talk and noise for ladder (multi-chips) are still to reduce .
  - Need to further develop In-chip LDO, reduce noise caused due to power lines.
  - Optimize the design of ladder
- Still need to reduce material budget
  - New solution of curved silicon (ALICE ITS3 like) is very attractive

backup

Air cooling for CEPC vertex detector

- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix design : $\leq$ 100 mW/cm^2. (trigger mode), $\leq$ 150 mW/cm^2 (triggerless mode),
  - Taichupix measured result: ~60 mW/cm^2(triggerless mode, 17.5MHz)
  - CEPC final goal : $\leq$ 50 mW/cm^2
- Cooling simulations of a single complete ladder with detailed FPC were done.
  - Need 2 m/s air flow to cool down the ladder

Max temperature of ladder (℃) (air temperature 5 ℃)					
Power Dissipation (mW/cm2) \ Air speed (m/s)	5	4	3	2	1
100	19.6	21.8	25.0	*30.6*	*43.4*
150	26.9	30.1	35	*43.4*	*62.6*

Summary of CECP vertex detector prototype

- **Developed full-size CMOS pixel sensor**
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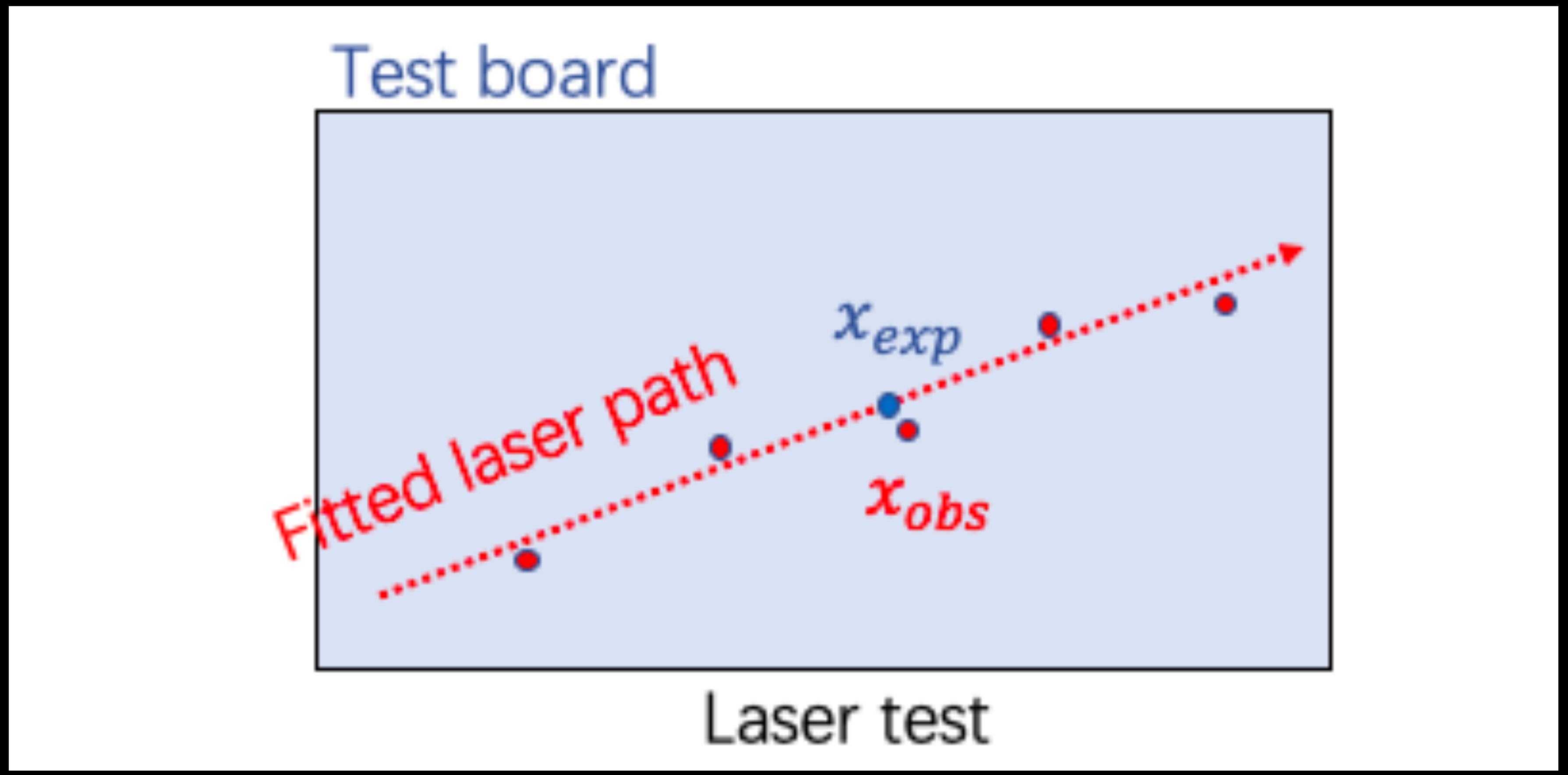
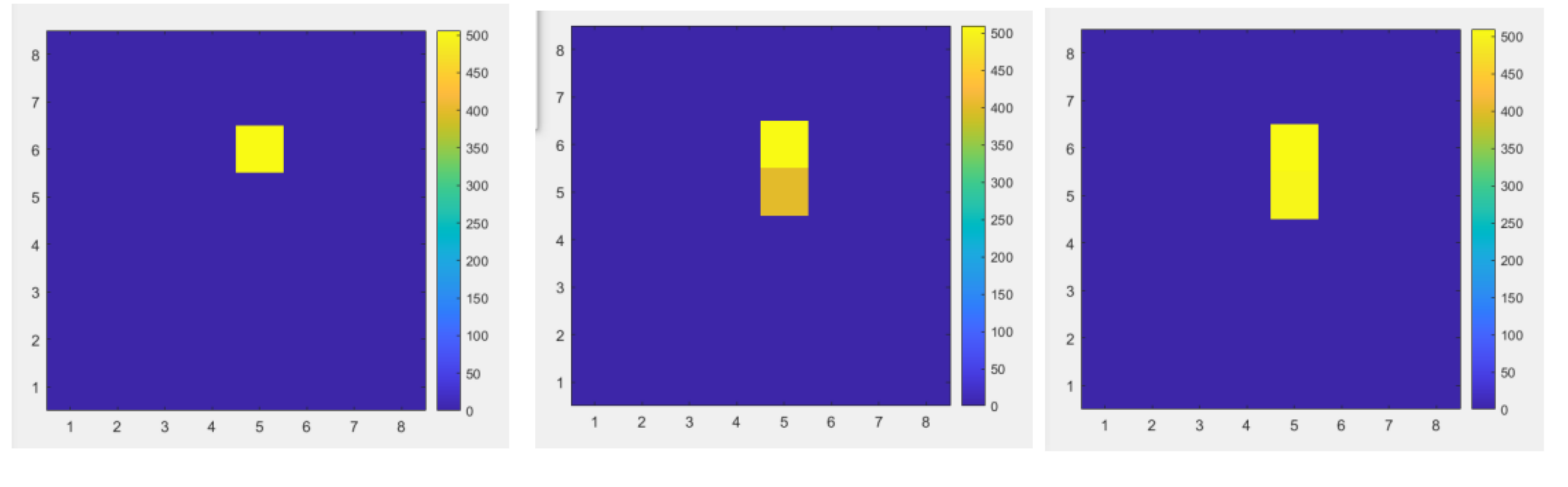
	Requirement	Result
Single point Spatial resolution	3-5 μm	Laser test: ~ 4 μm Chip-level Beam Test : 4.8 μm Prototype level Beam Test: 4.9μm

Spatial resolution measured by Laser tests

- Spatial resolution of Taichu2 can reach ~4 μm in laser tests
  - Use high precision 2D movable station in laser scan
  - Laser was scanning with a step of 1 μm



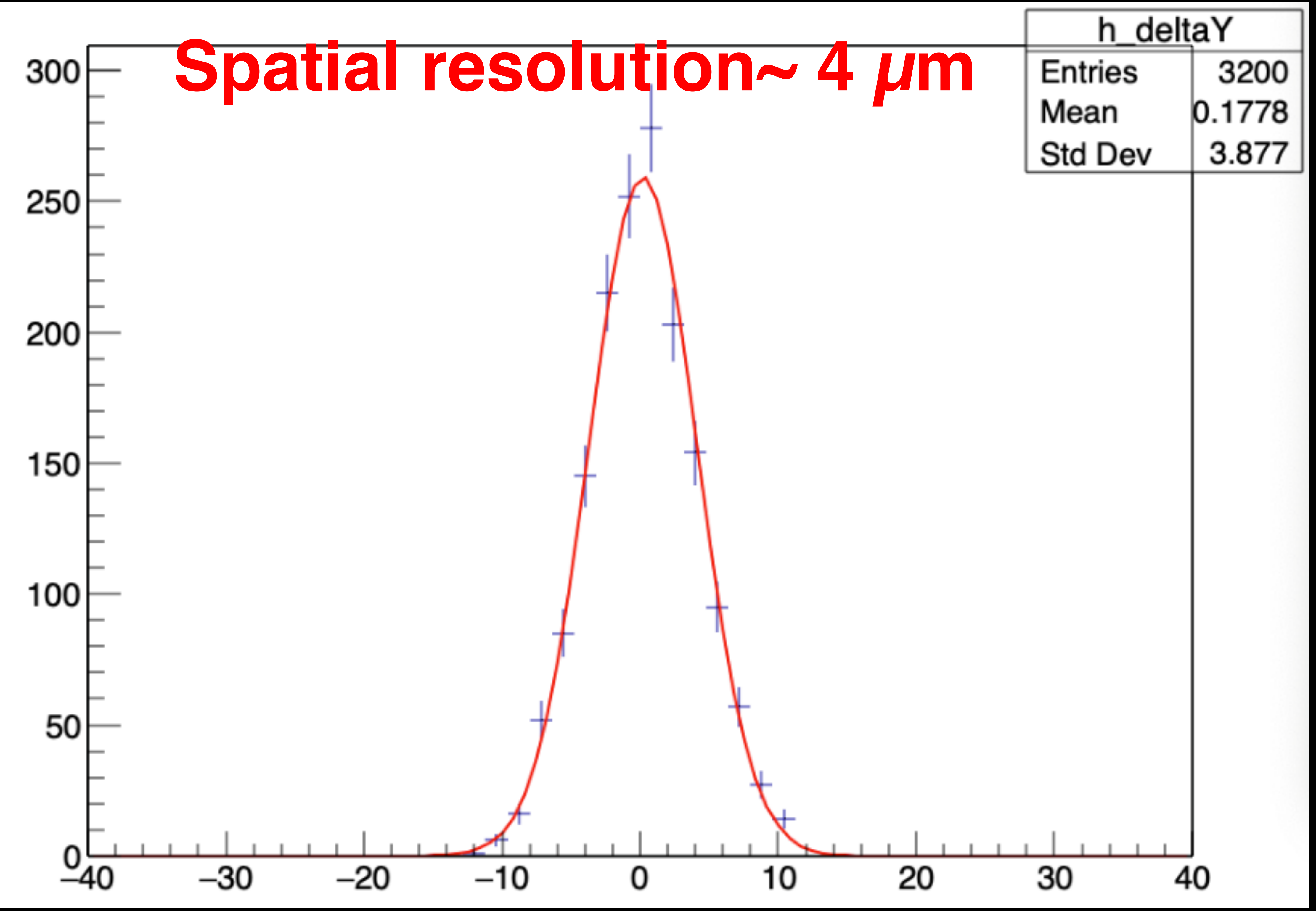
Laser beam spot during scan



Spatial Resolution in X and Y direction

	Resolution (μm)	Overall error (μm)
X	3.98	±0.23
Y	4.12	±0.25

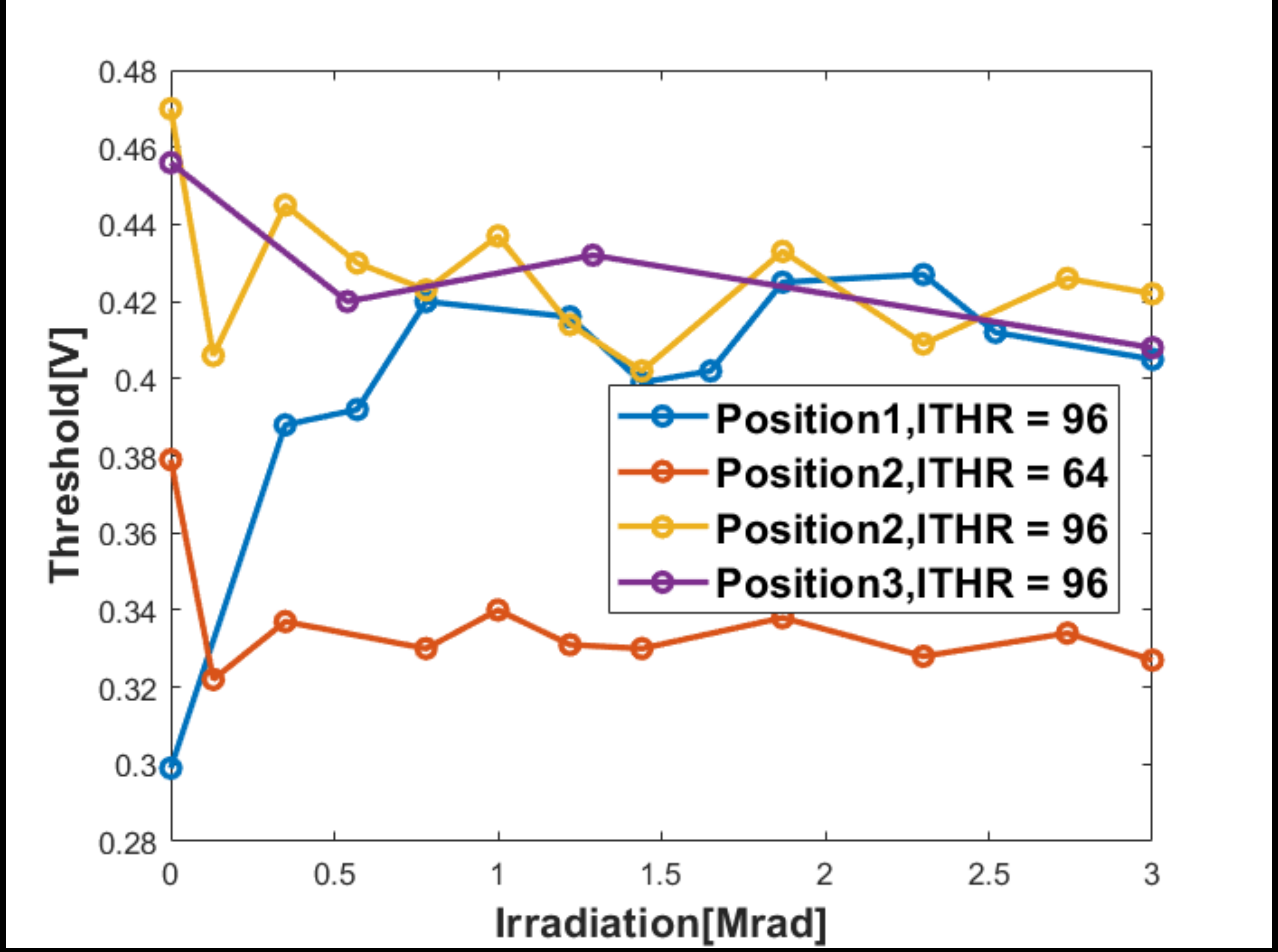
Residual distribution
(measured position – expected position from station)



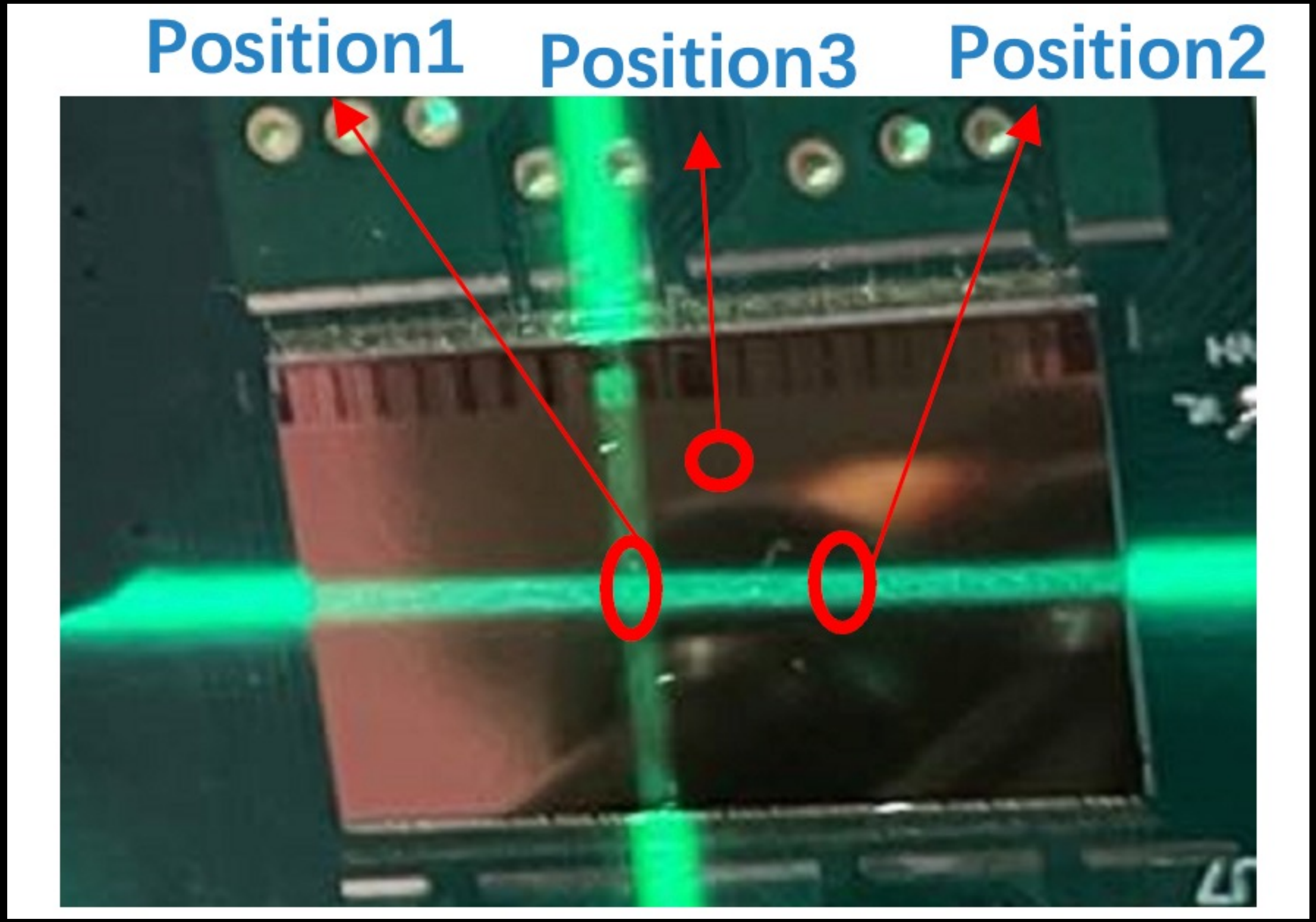
Radiation tests

- Taichupix3 was irradiated in-situ tested up to 3 Mrad
  - Normal chip functionality and reasonable noise performance
  - Reach the goal of the project: radiation hardness on total ionization does >1 Mrad

Taichupix3 irradiation test
Pixel threshold vs. TID

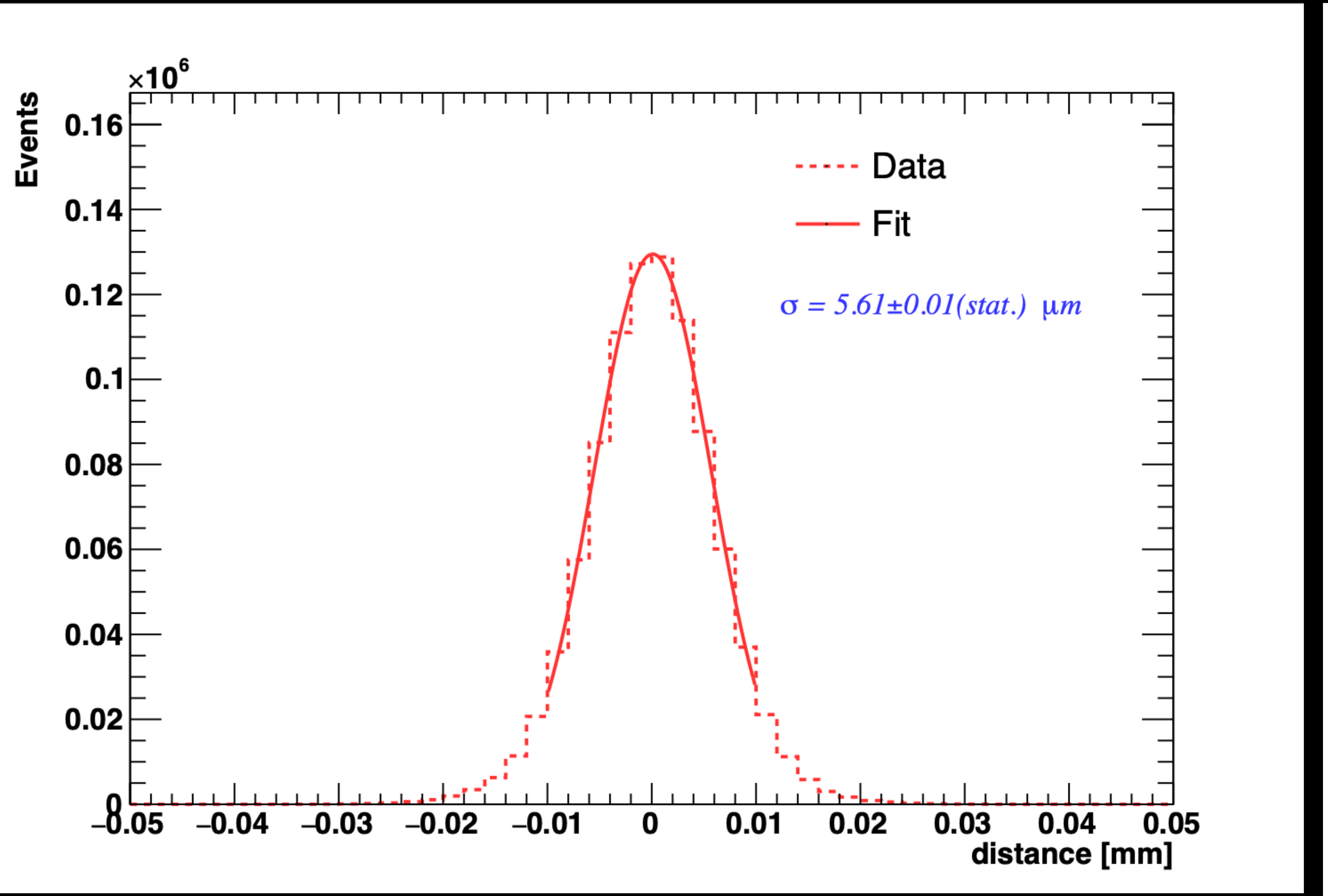


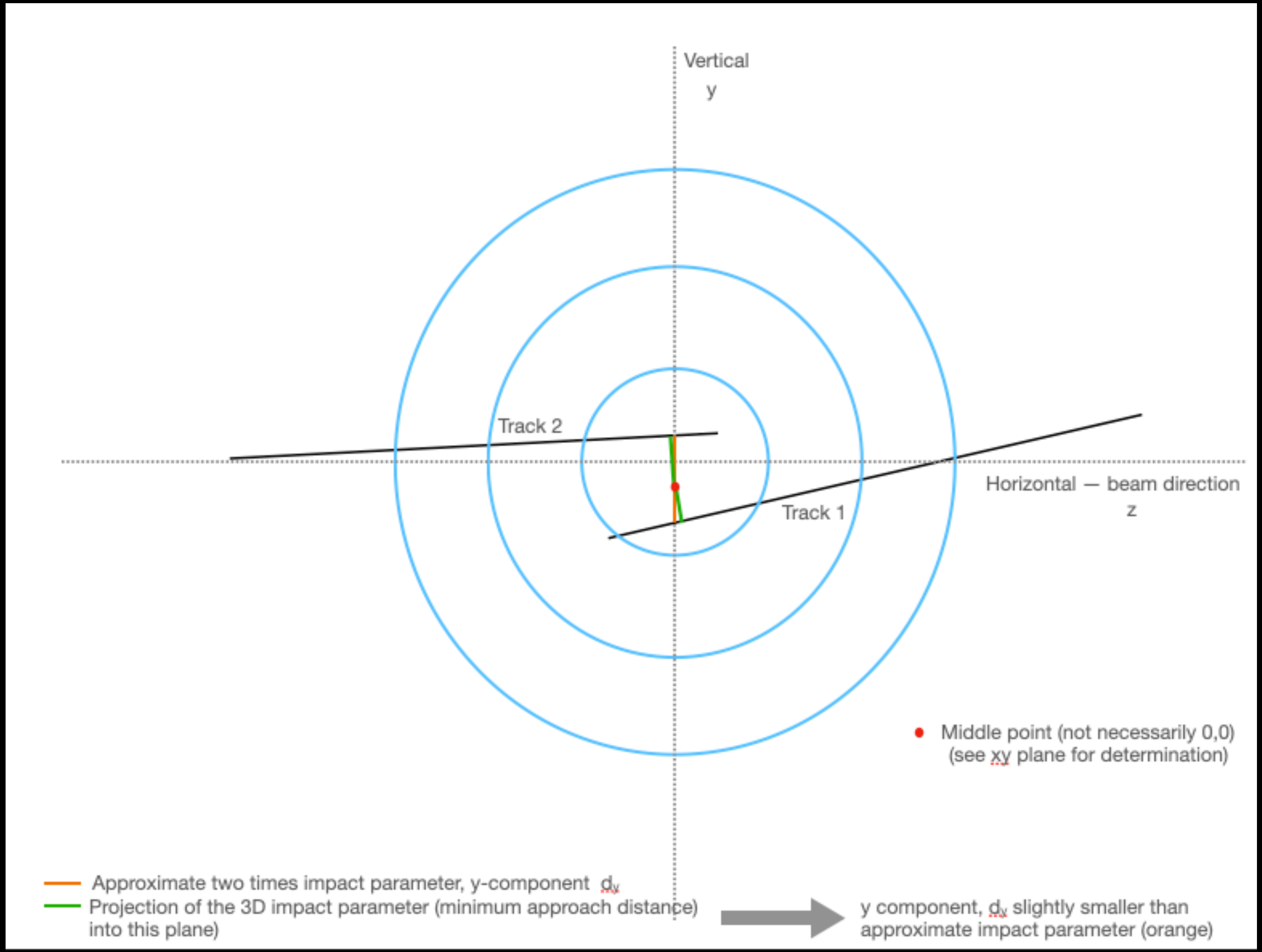
TaichuPix-3 irradiated at Synchrotron radiation beamline (12 keV X-ray)



Preliminary result of impact parameter resolution

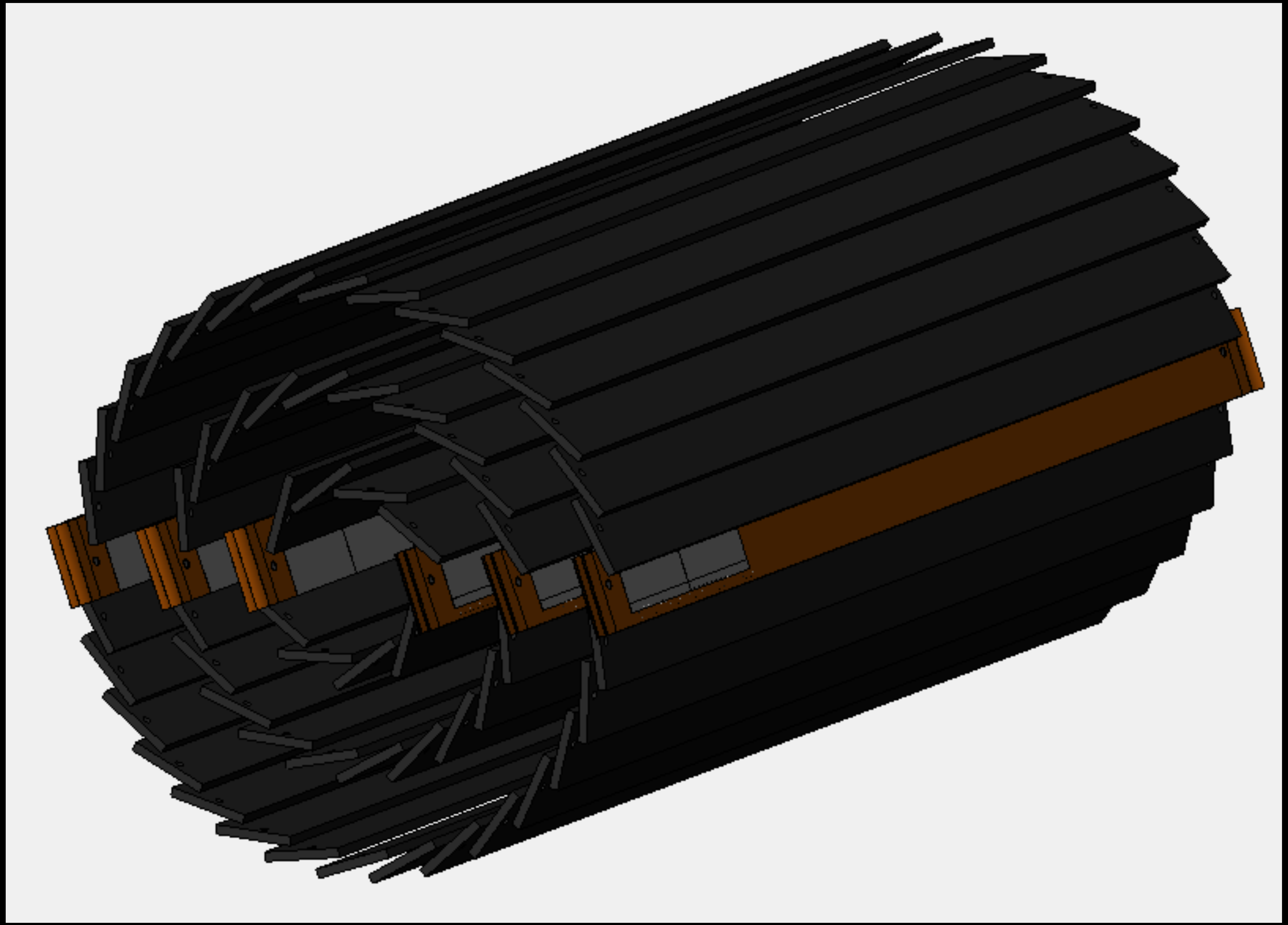
- No real interaction point or real primary vertex (PV) in testbeam setup
  - Define PV as the centre of the point in xy plane extrapolated from the up/downstream
  - Calculate the impact parameter between primary vertex and upstream/downstream tracks



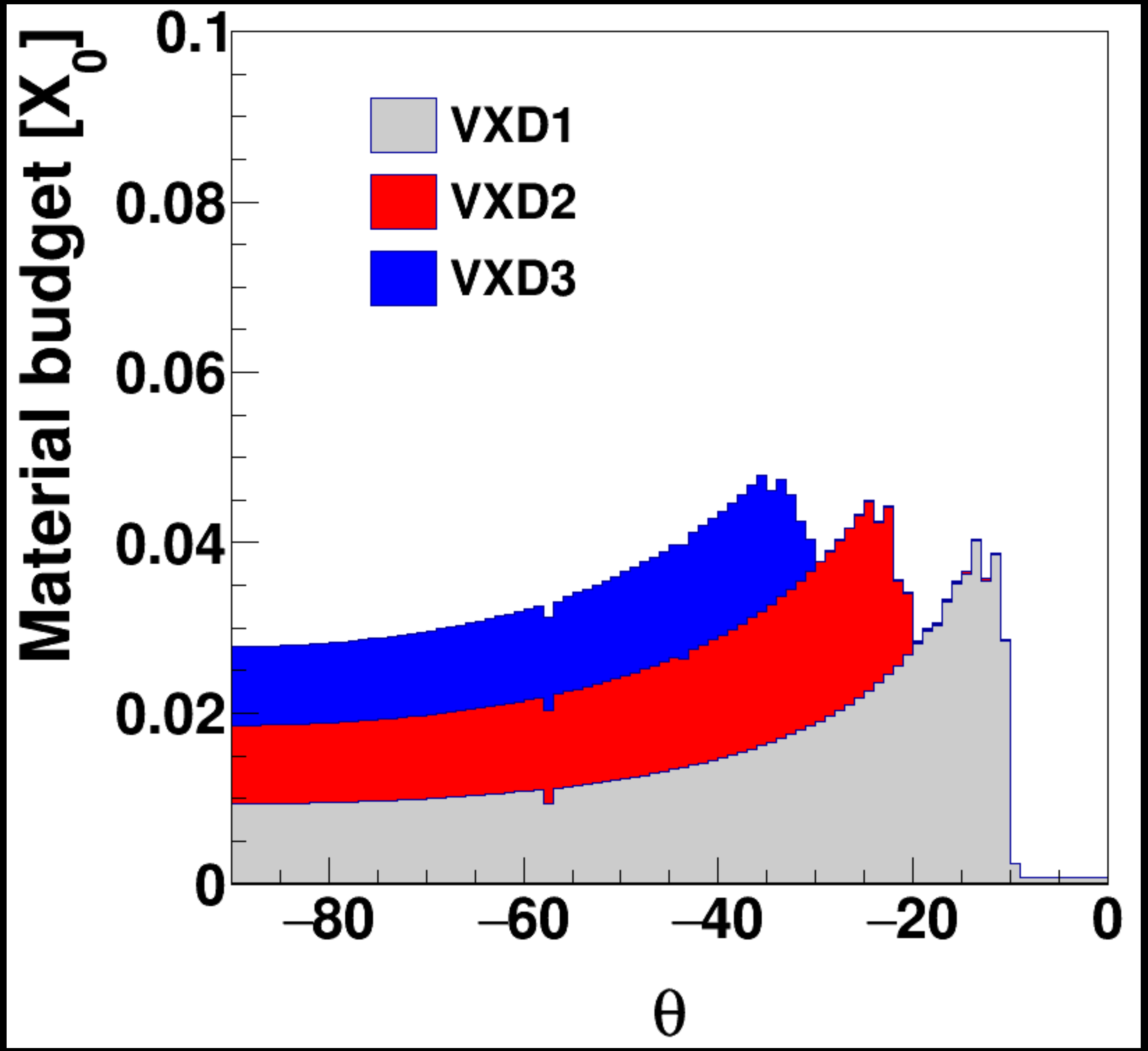


Estimated Material budget for vertex detector prototype

- Estimated material budget 0.026 X0 for three double ladders vertex detector (6 layers)
  - Target for final CEPC vertex detector is 0.009 X0 (0.015% X0 per layer)
  - Copper in flexible PCB are major contributions
  - Plan to replace copper into Aluminum in final CEPC vertex detector
  - Further thinning of silicon wafer (150um → 50um)



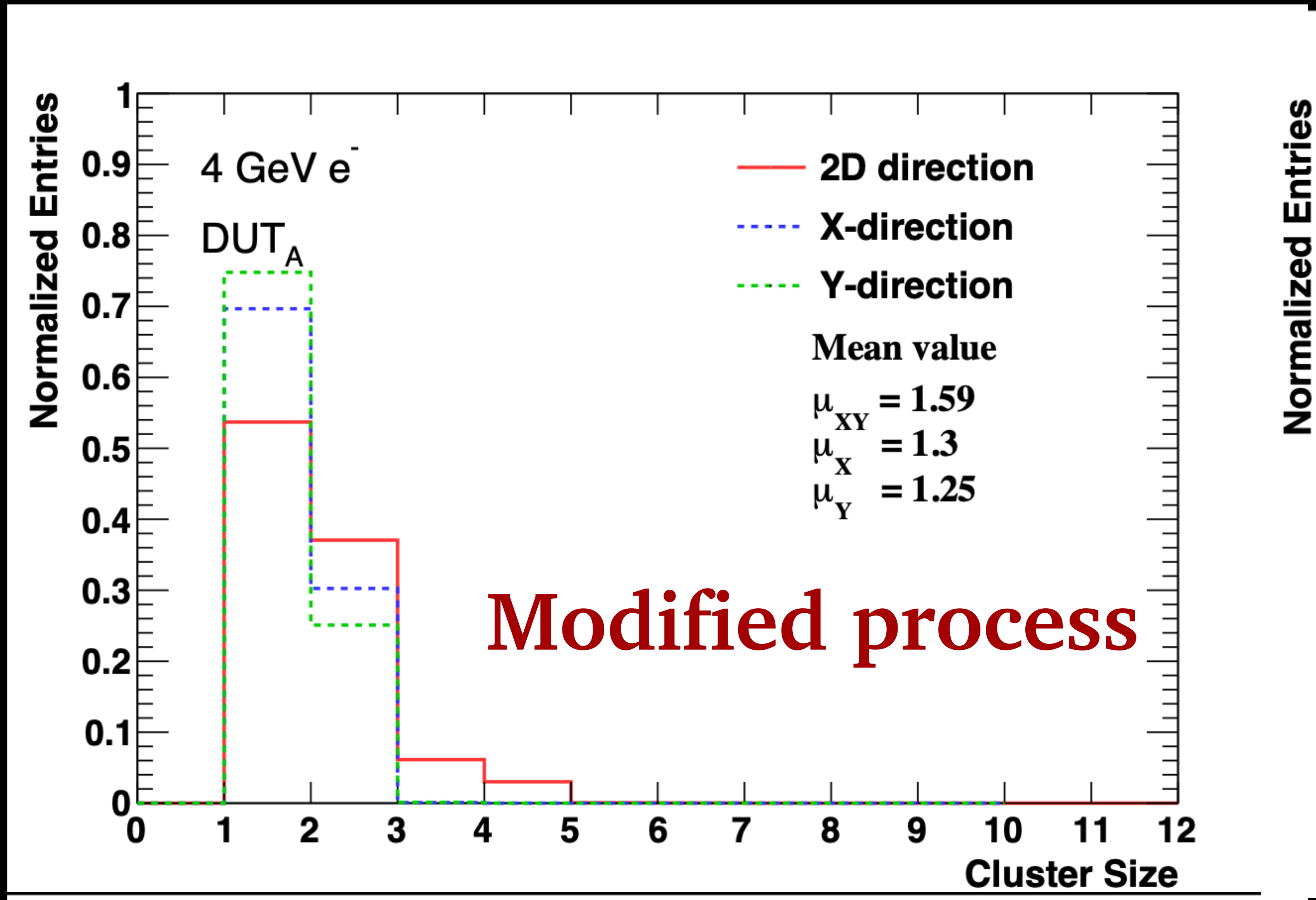
Estimated material budget for this prototype

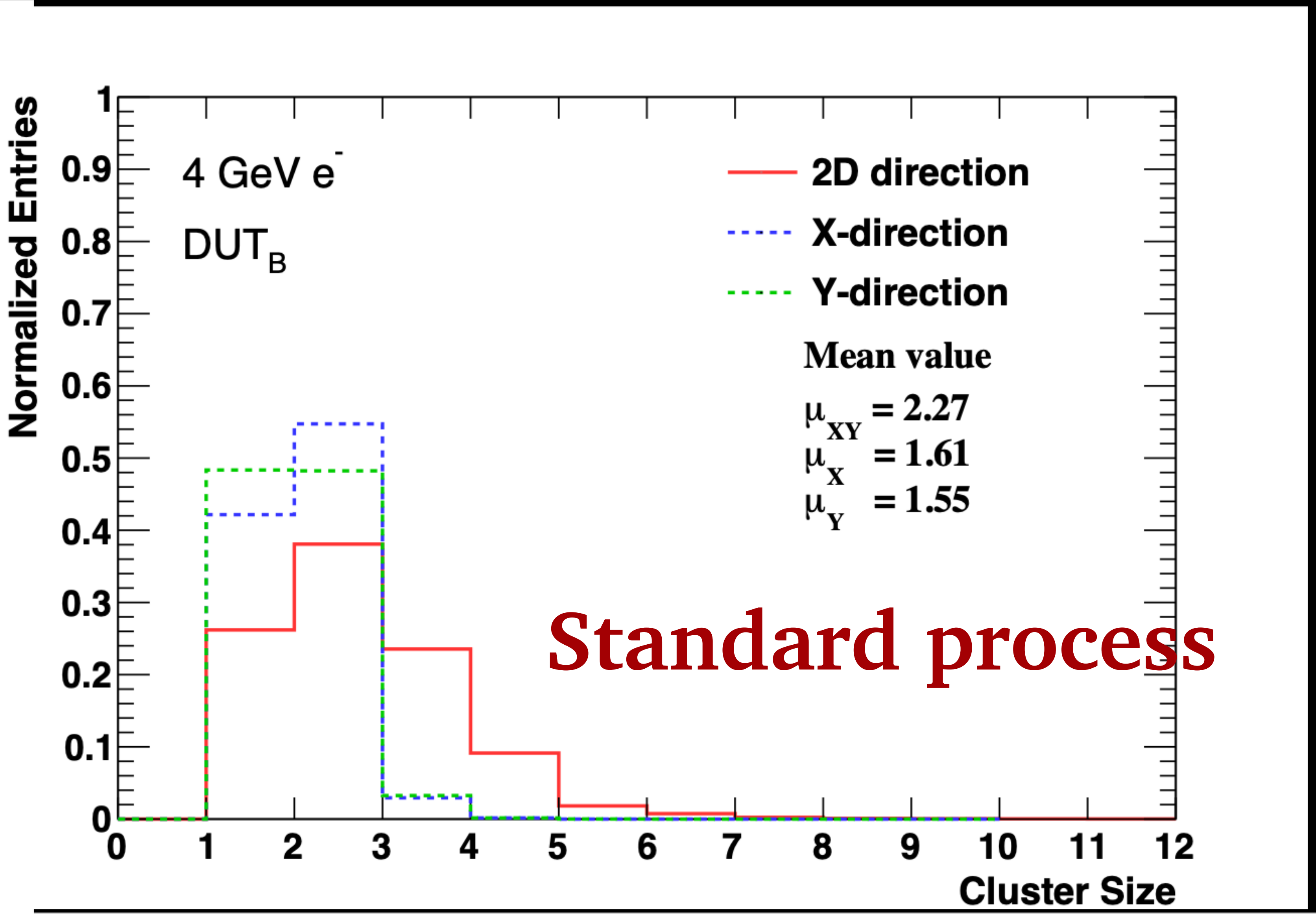


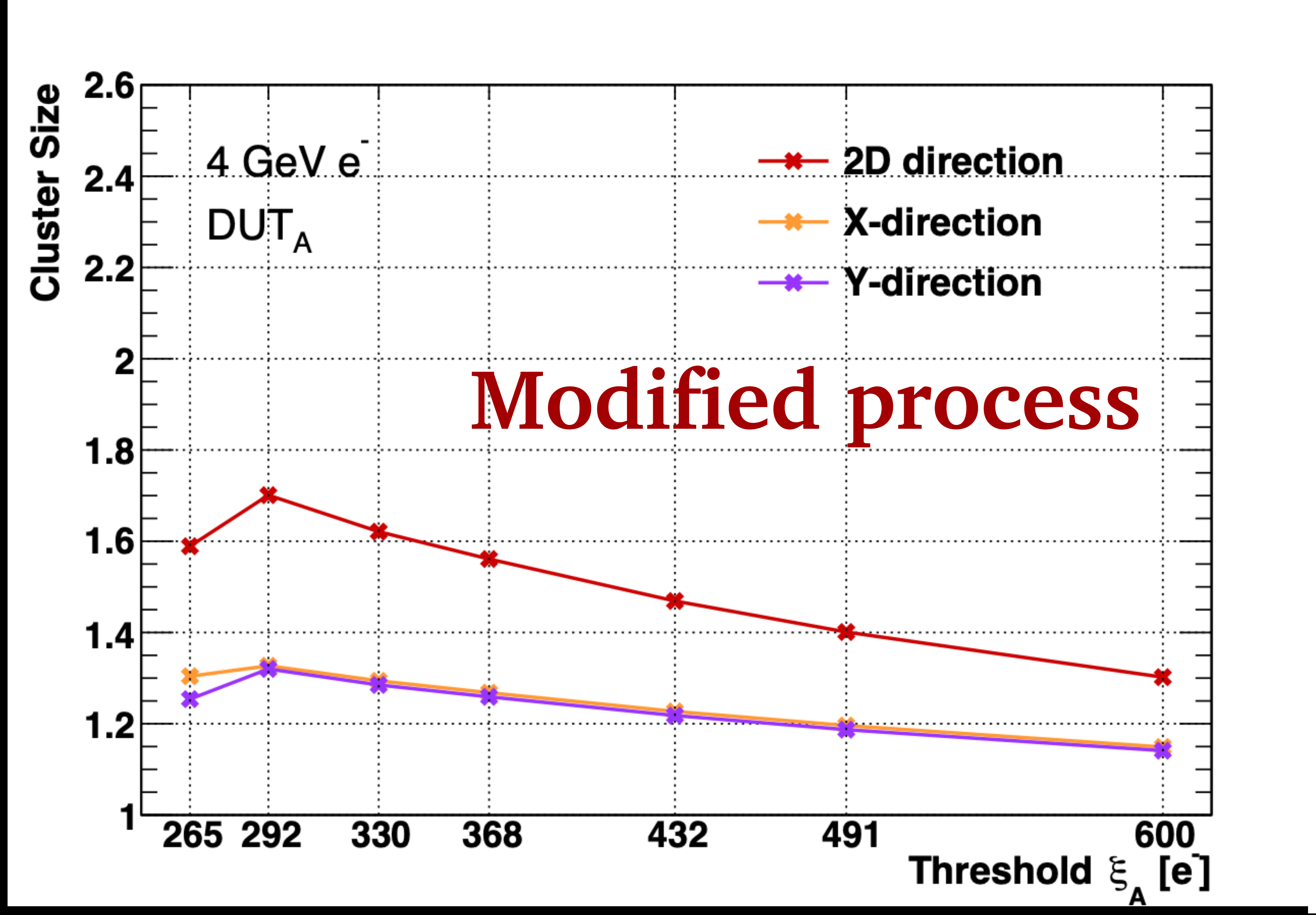
Carbon fiber Support structure of the ladder

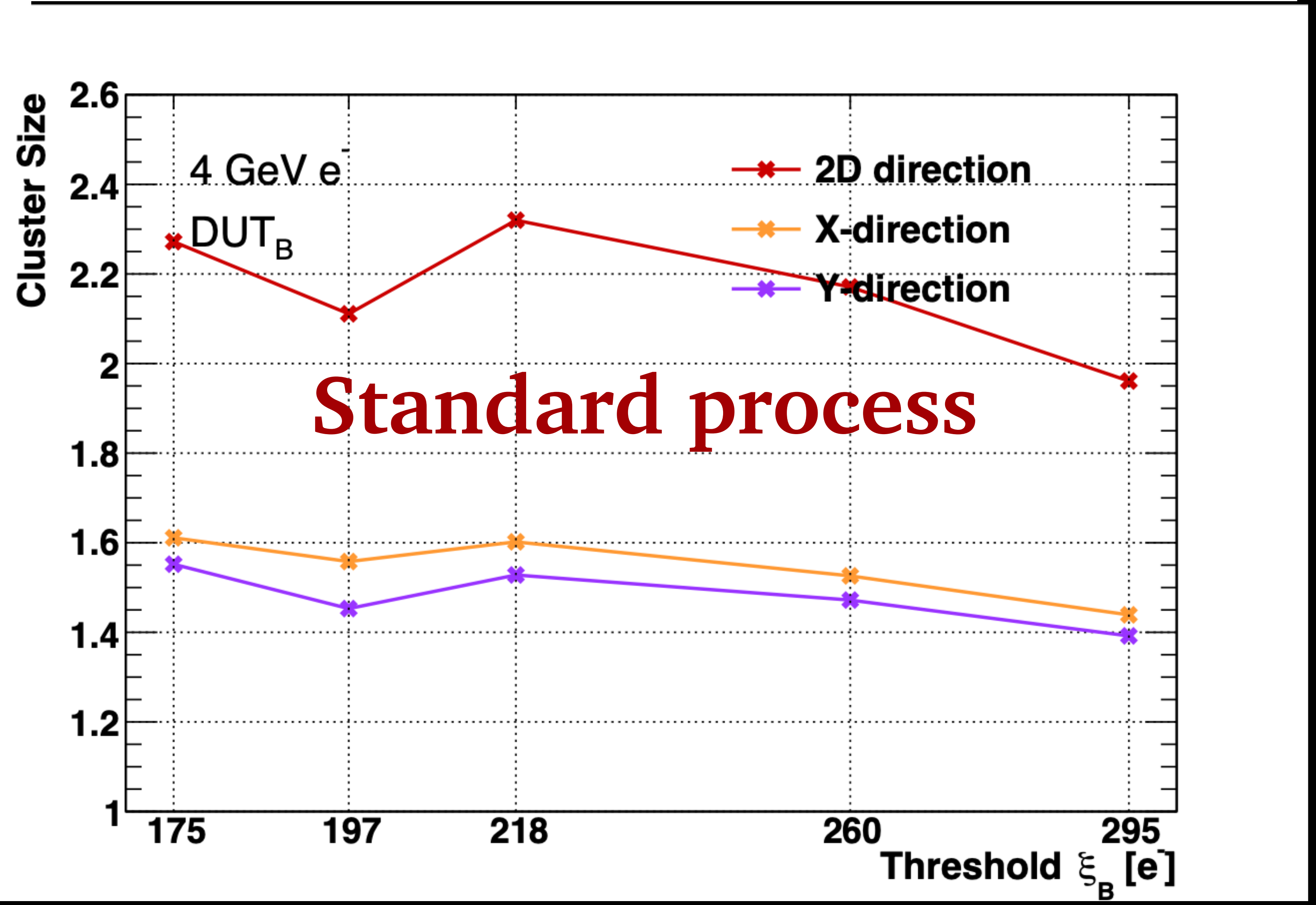
- Fabricated support structure prototype of the ladder (IHEP designed)
  - **4 layer of carbon fiber, 0.12mm thick for the whole support**
    - **Shallow design inside ladder support to reduce material**
  - **2~3 time thinner than conventional carbon fiber in China**

Offline analysis results of first test beam







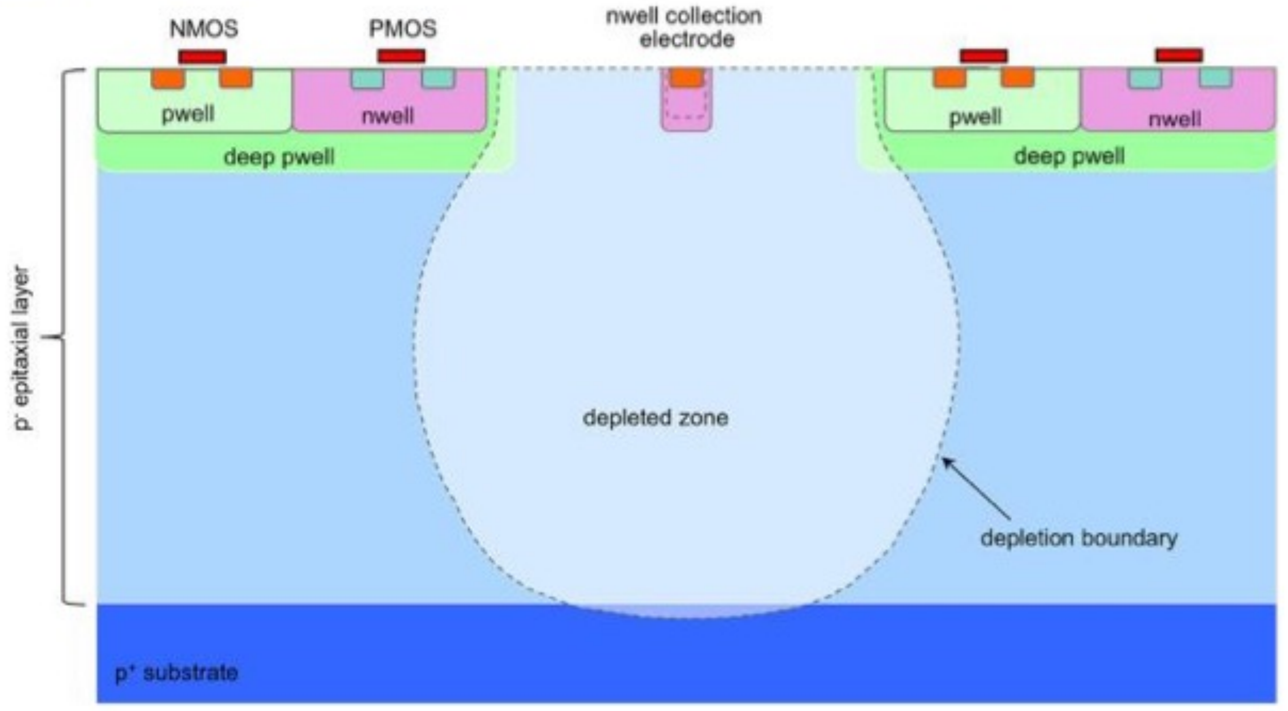


- **Less charge sharing effects in modified process with full depletion**
- **If lowering the threshold, cluster size will be dominated by noise**

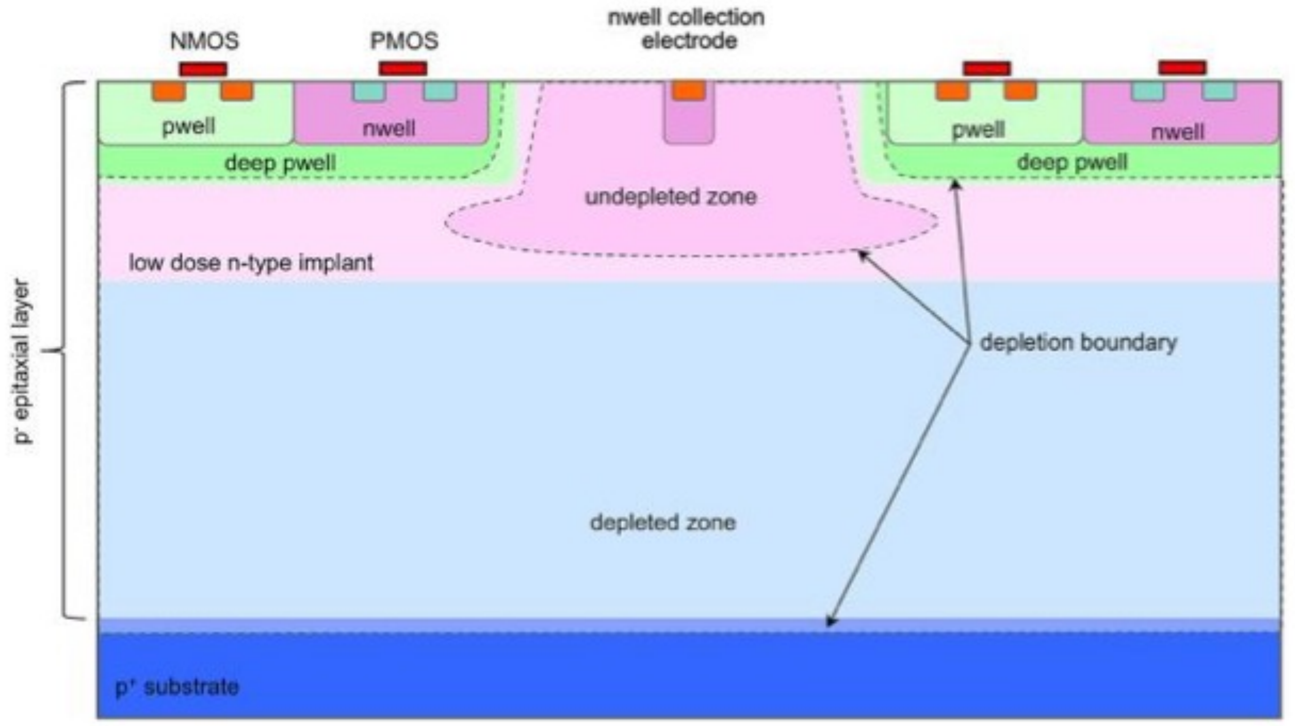
Structure and process of sensor

- **Technology: CMOS Monolithic pixel sensor**
  - N-well/P-epitaxial diodes employed collection elements
  - Readout electronics integrated on the same Si-substrate
  - ➔ Low material budget, low pixel capacitor, easy to assemble

- **Process : TowerJazz CIS 180 nm process**
  - Process splits:
    - **Standard process**
      - Baseline option, the only choice available in the MPW submissions
    - **Modified process***
      - Adding an extra low dose n-type layer based on the standard process, to achieve faster charge collection, thus a better radiation tolerance
      - Very difficult to access, the first time available to a Chinese institute



Standard process



Modified process*

*Reference: NIM, A 871 (2017) 90–96

Additional specifications on the full-scale chip

- **Additional specifications besides the main goals of project**
  - High detection efficiency → **small dead time**
  - Assembled on ladder → **large sensitivity area**
  - Low material → **low power density**
  - Bunch spacing: Higgs: 680 ns; W: 210 ns; Z: 25 ns

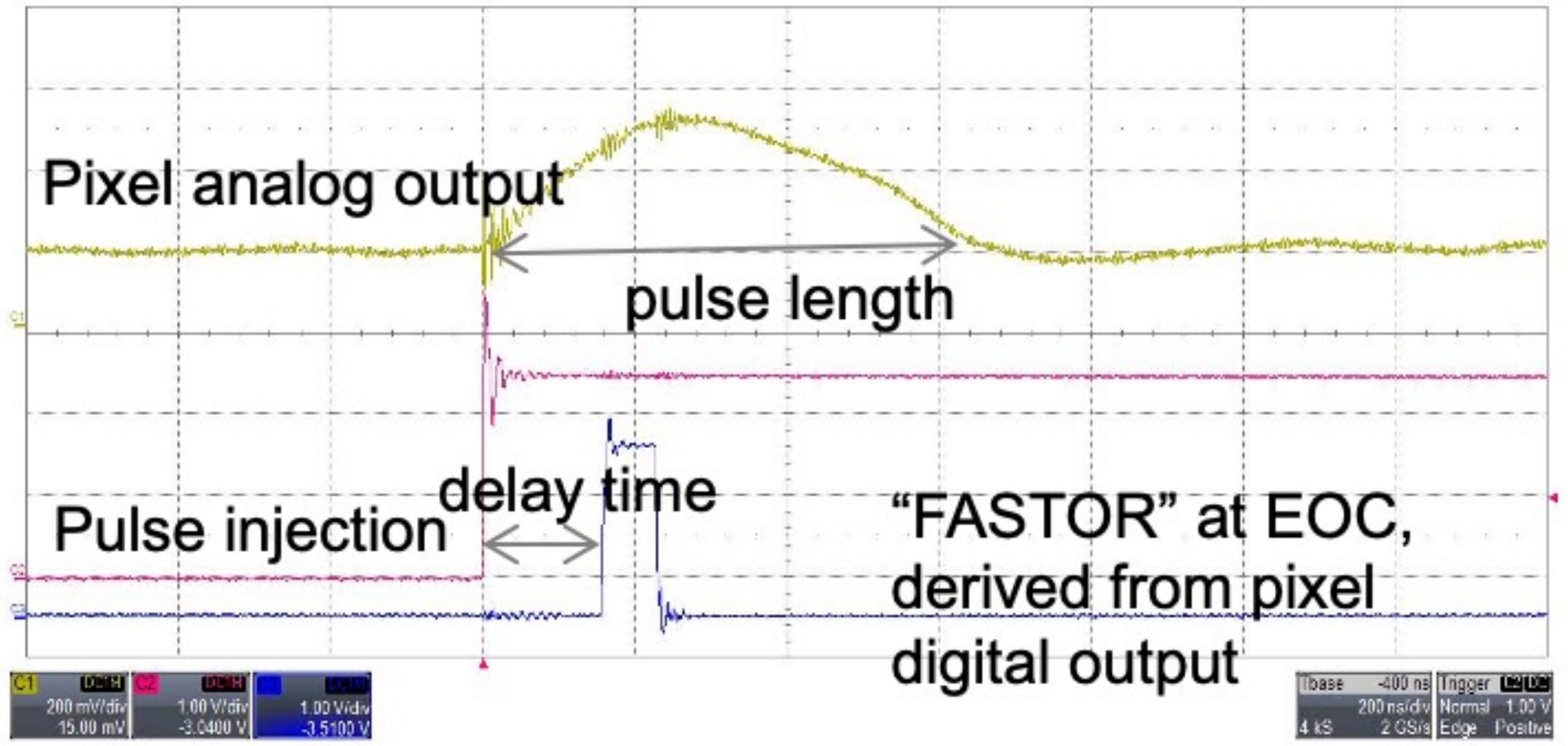
    Hit density: 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z → **high hit rate**

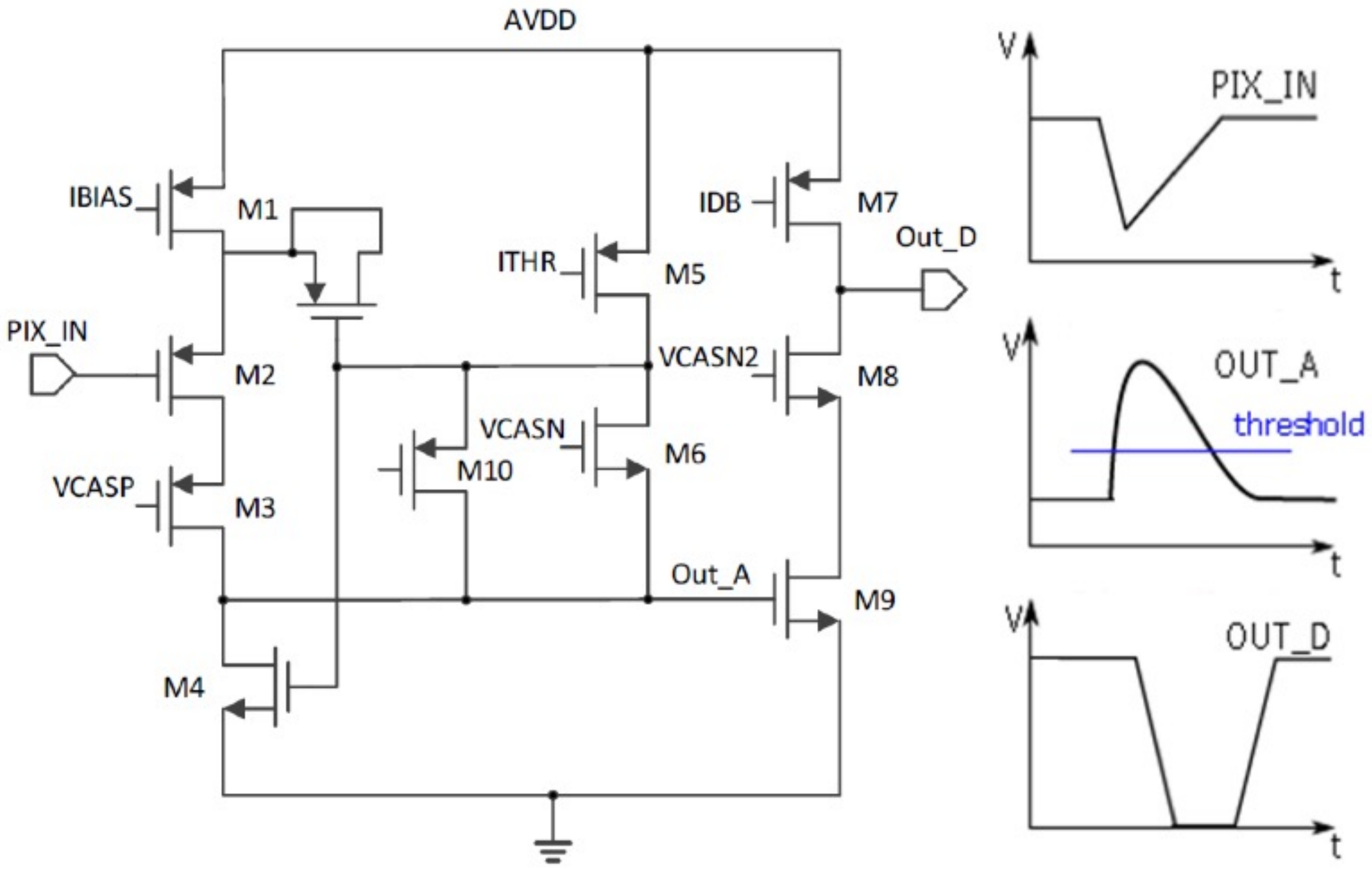
Specs	Parameter
Hit rate	120 MHz/chip
Data rate	3.84 Gbps (triggerless) ~110 Mbps (trigger)
Dead time	< 500 ns (for 98% efficiency)
Pixel array	512 row × 1024 col
Chip size	~1.4 × 2.56 cm^2
Power Density	< 200 mW/cm^2 (air cooling)

Major innovation: High data-rate processing maintaining good spatial resolution

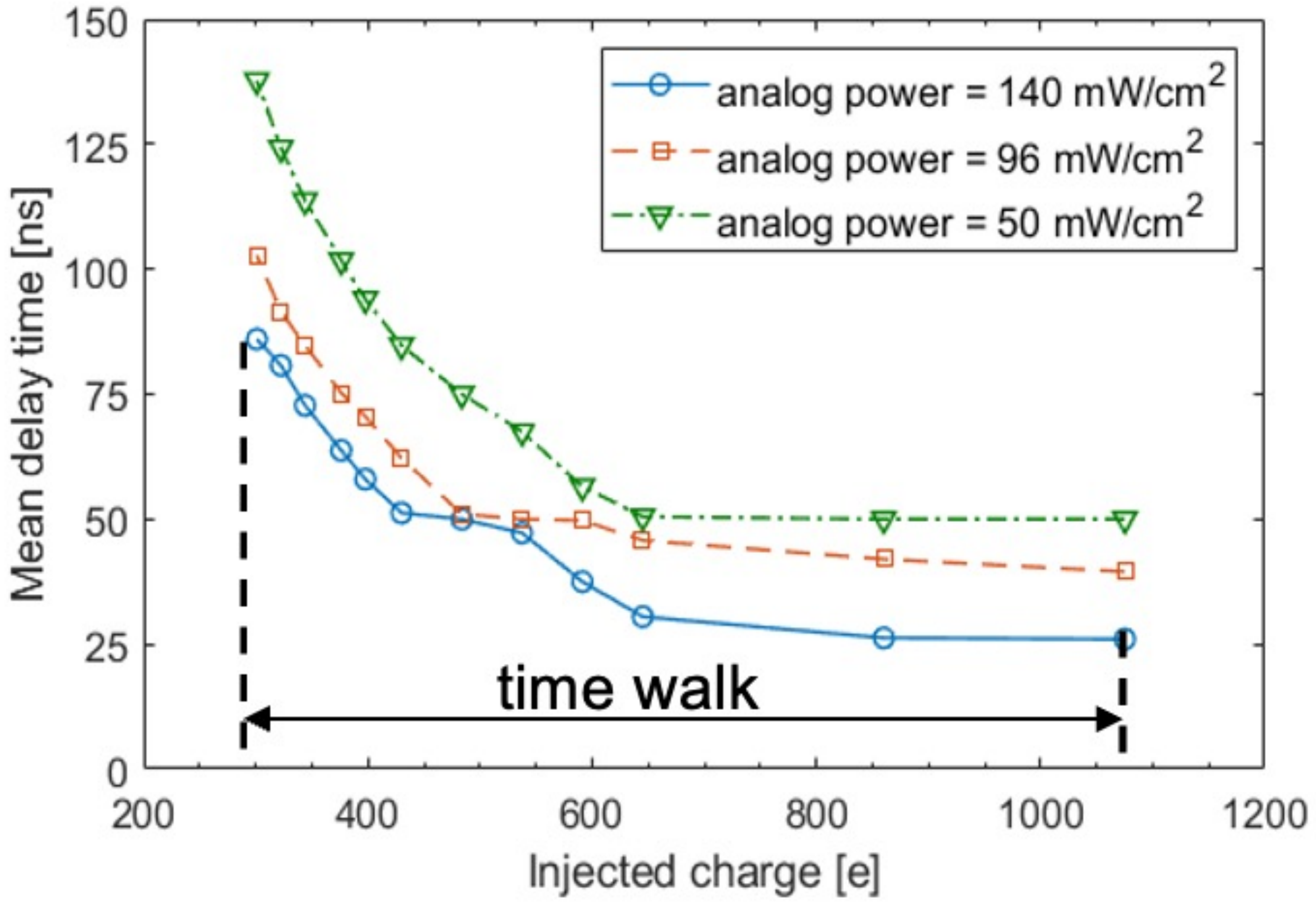
Pixel analog front-end

- **Based on ALPIDE* front-end scheme**
  - modified for faster response
  - ‘FASTOR’ signal delivered to the EOC (end of column) when a pixel fired, timestamps of hit recorded at pos. edge of ‘FASTOR’





Schematic of pixel front-end



Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

*Ref: D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

CEPC vertex detector R & D

- Three on-going R & D programs on vertex detector
  - Previous update in CEPC day (June 15th)   https://indico.ihep.ac.cn/event/11875/
- This talk focuses on MOST2 project
  - MOST2 aims to build full-size vertex detector prototype

Funding agency	Process	International collaborators	Objectives of the project	schedule
CEPC MOST1	CMOS	Strasburg IPHC	Small pixel size design with in-pixel digitization and low power frontend	2016.6-2021.5
MOST2	CMOS	IFAE/Oxford/ Livepool …	vertex detector prototyping （Full-size sensor support structure, module …)	2018.5-2023.4
NSFC	SOI	KEK/SOIPIX collaboration	Verification of SOI process with small pixel size and low noise design	2016-