Valerio Sarritzu* on behalf of the ALICE collaboration
*CERN, UniCA, INFN

The ALICE Inner Tracking System Upgrade

CEPC 2023, Nanjing, 23 Oct 2023

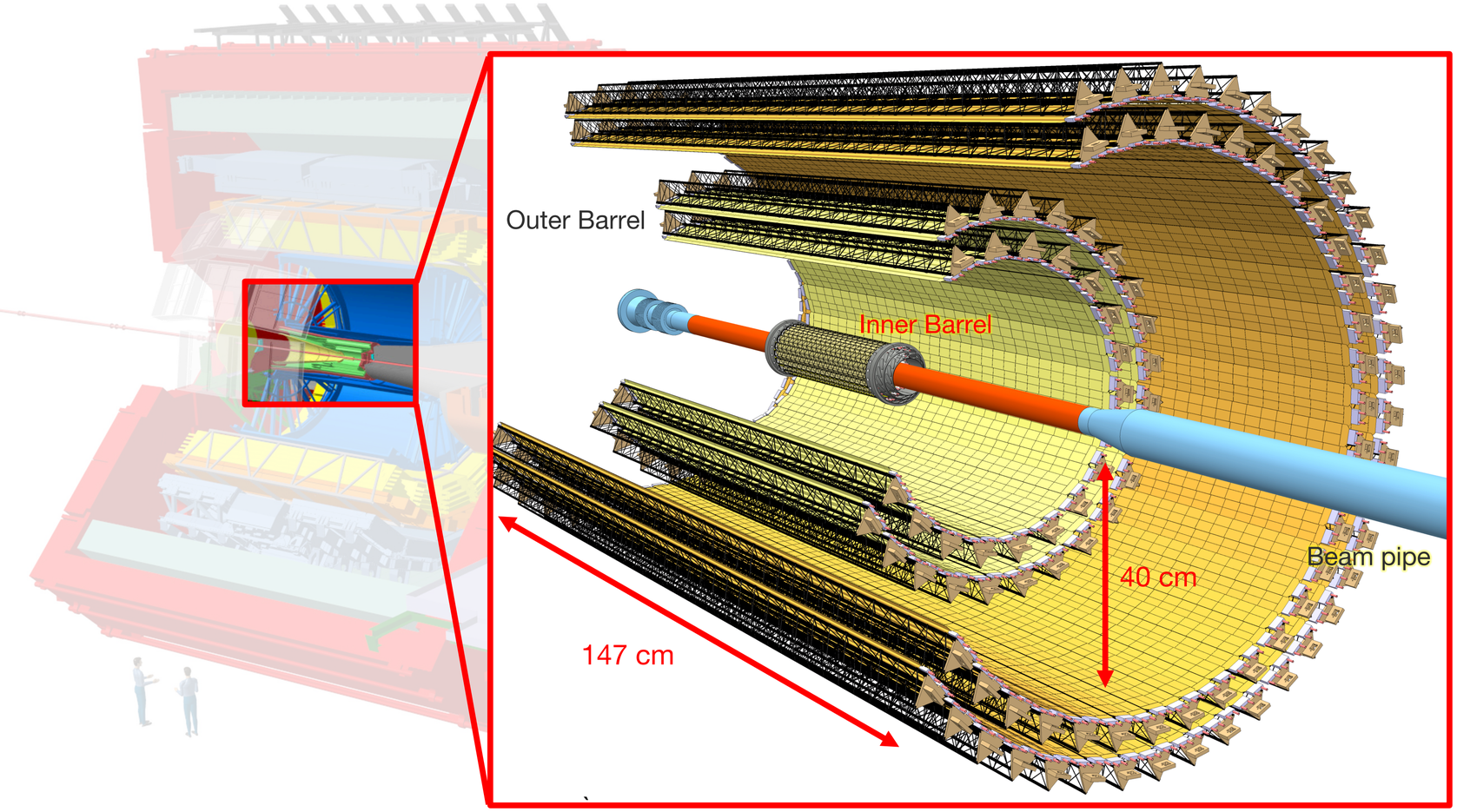
The ALICE ITS Upgrade

Outline

- **Overview**
  - Motivation
  - Concept
- **Sensor R&D**
  - Wafer-scale stitched sensors
  - Milestones
- **Monolithic Stitched Sensor (MOSS) prototype**
  - Design and features
  - Testing

Overview

The ALICE Inner Tracking System

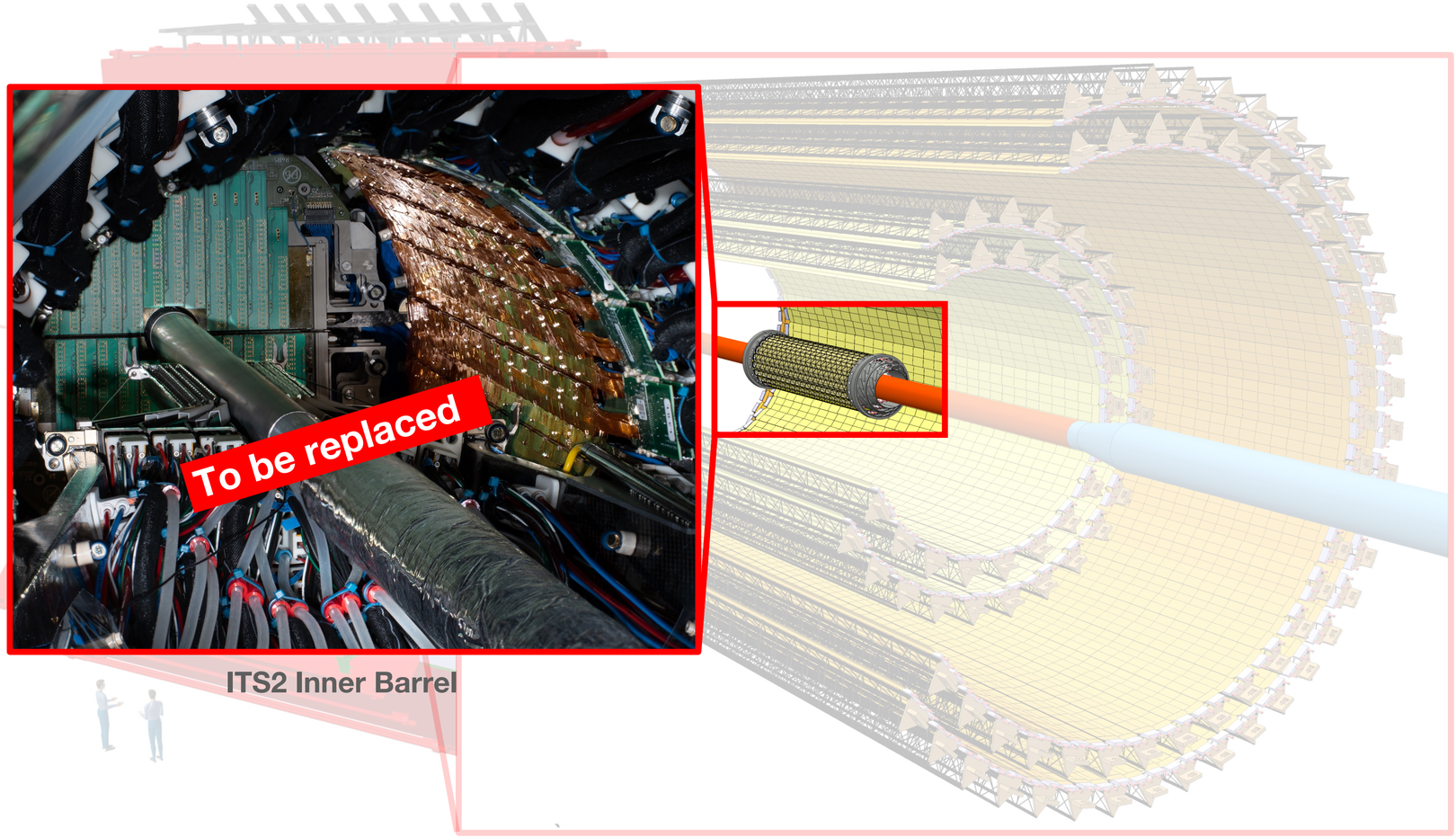


ITS2

- Largest MAPS detector ever built
  - 7 layers
  - **10 m²**
  - **12.5 Gpixel**
- Installed in **2021**

Overview

The ALICE Inner Tracking System

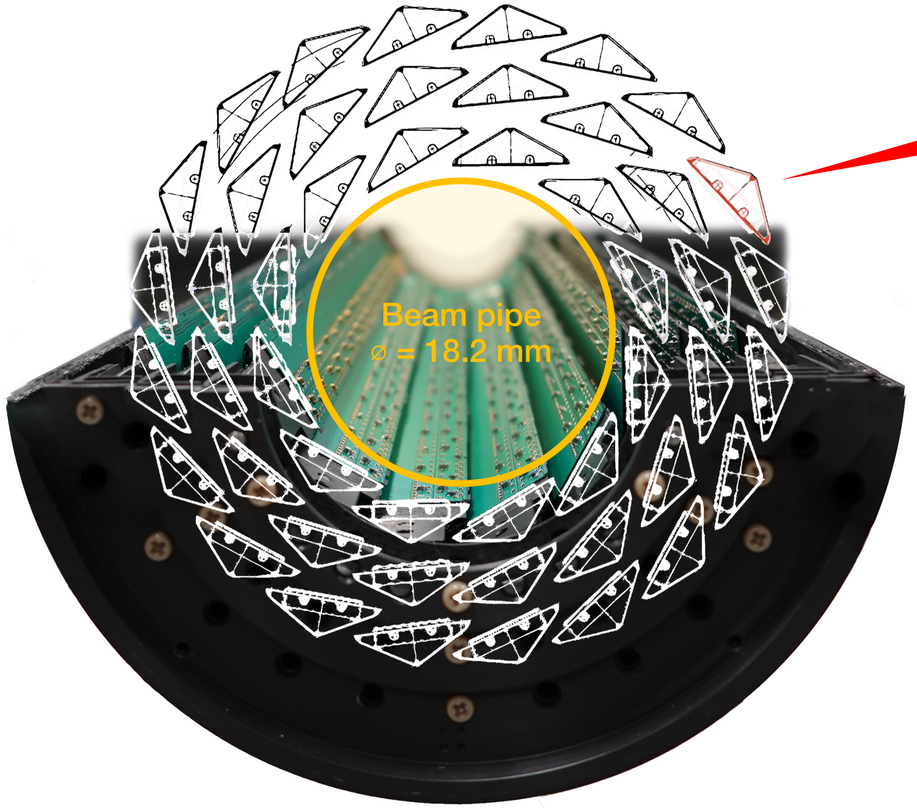


ITS3

- **Goal: improve tracking performance** by replacing Inner Barrel
- To be installed during LHC LS3 (**2025-27**)

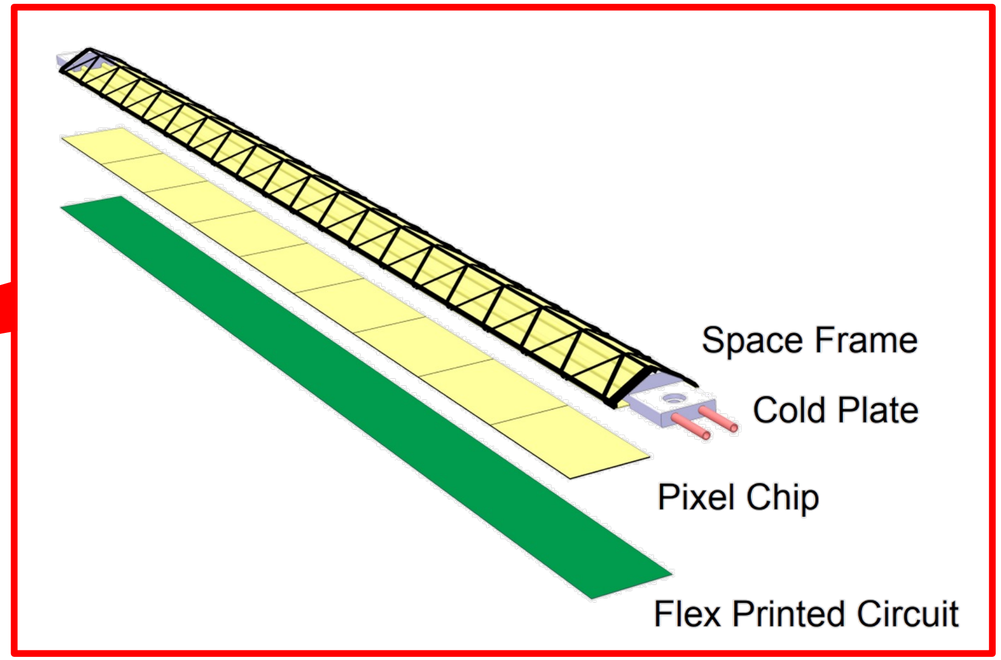
Overview

Motivation



ITS2 half inner barrel

ITS2 inner barrel stave



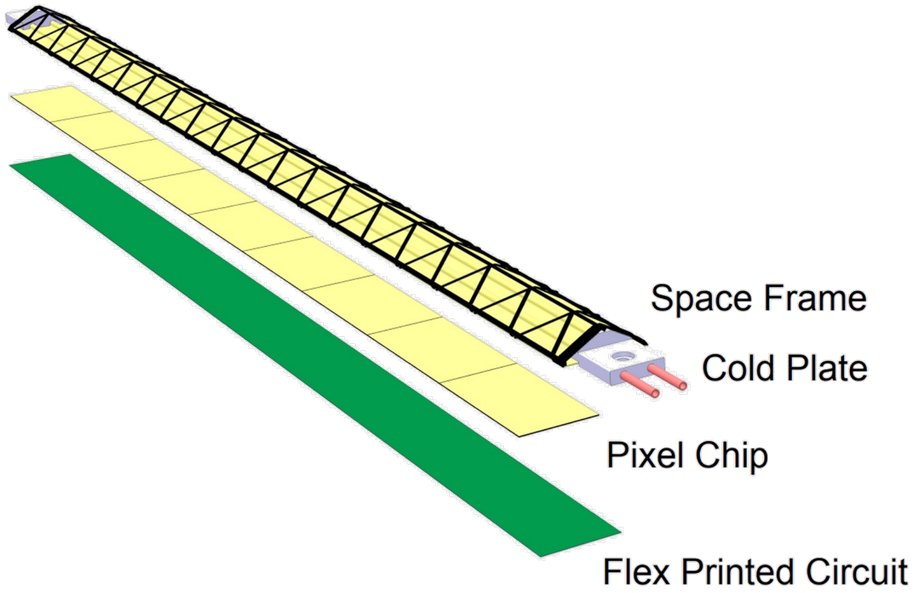
Three layers of staves. State-of-the-art, but:

1. **Can the material be further reduced?**
2. **Can we get closer to the interaction point?**

Overview

Motivation

1. **Can the material be further reduced?**



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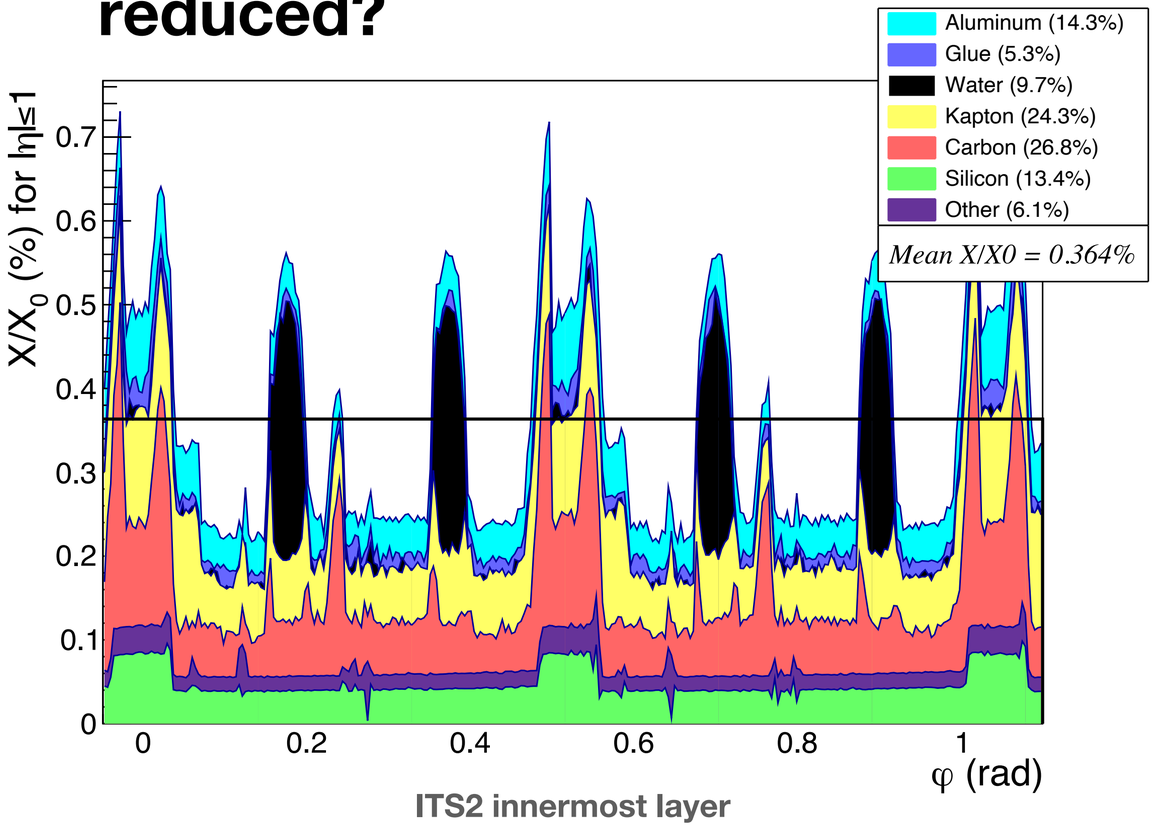
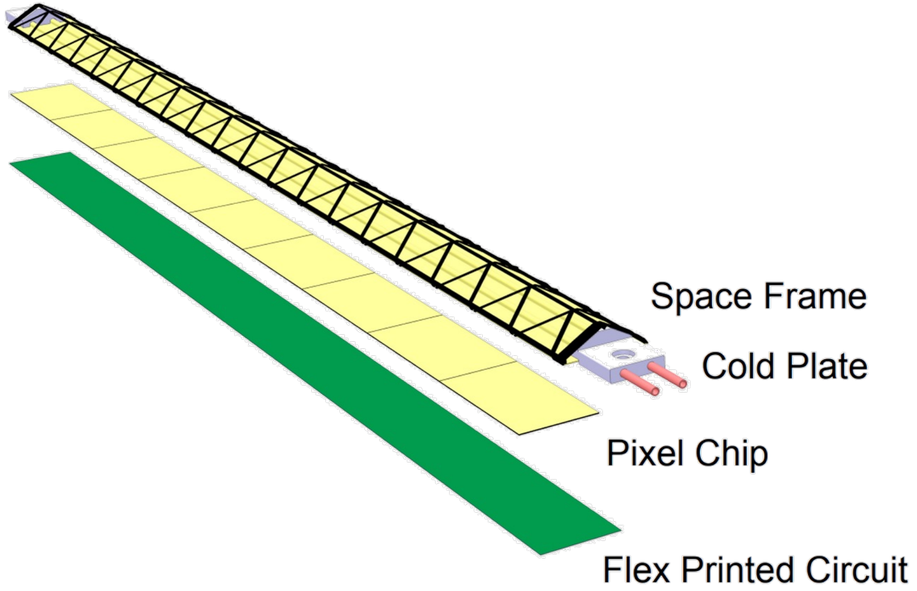


ITS2 innermost layer



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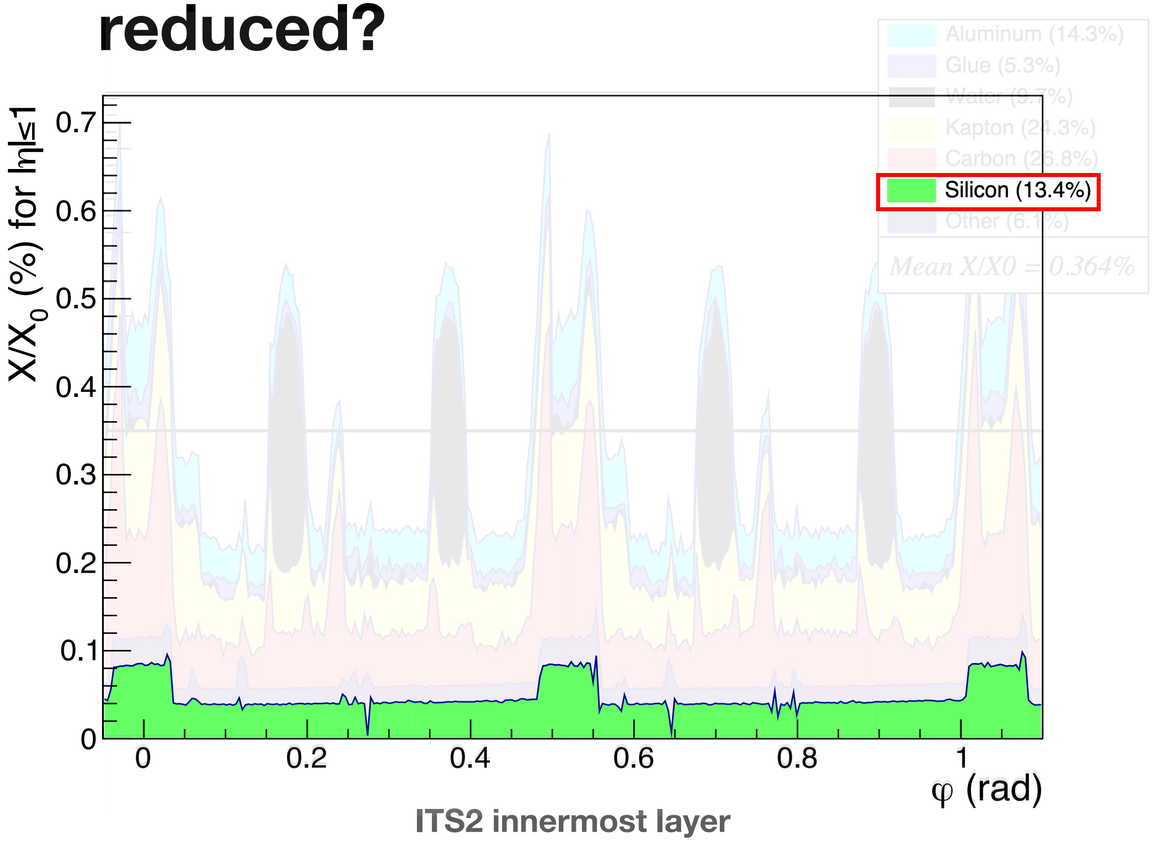

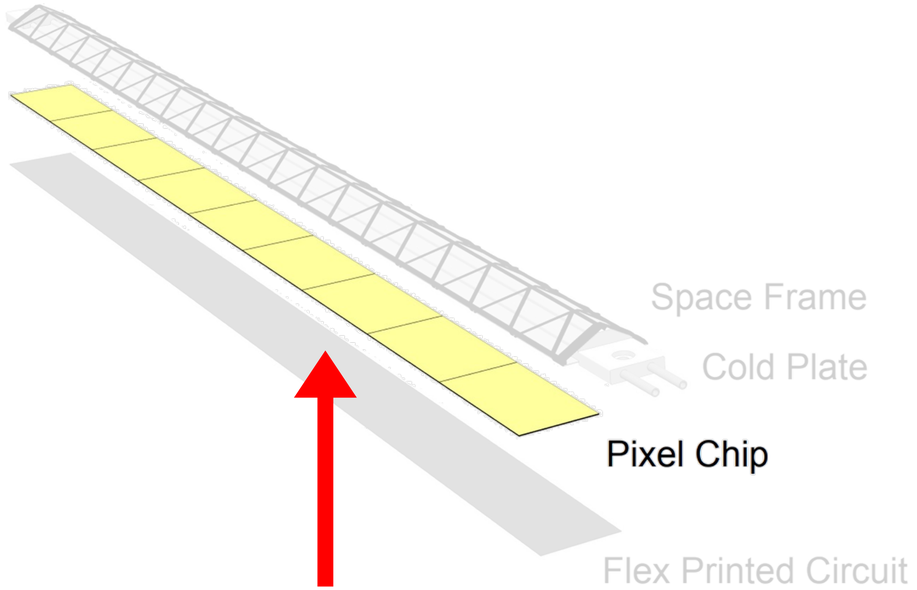

- **Si** (■) is **only 1/7th** of total material

Overview

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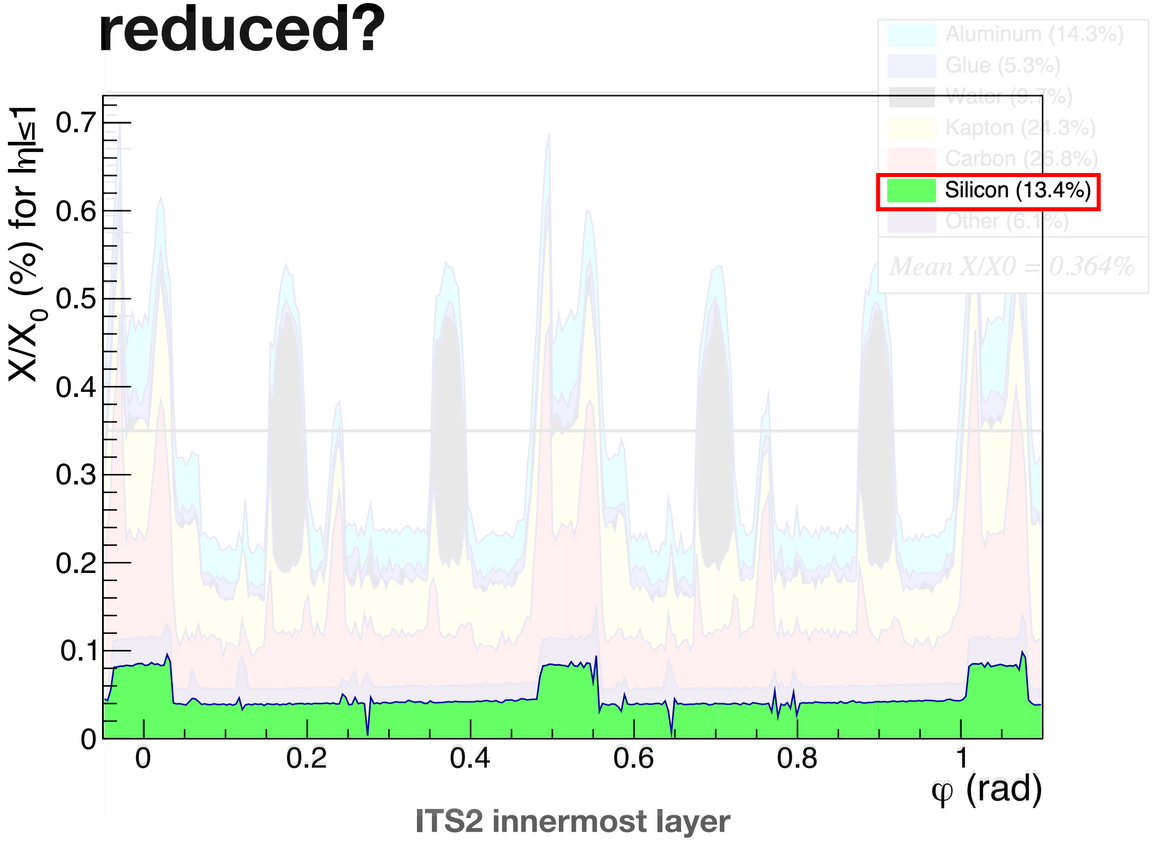

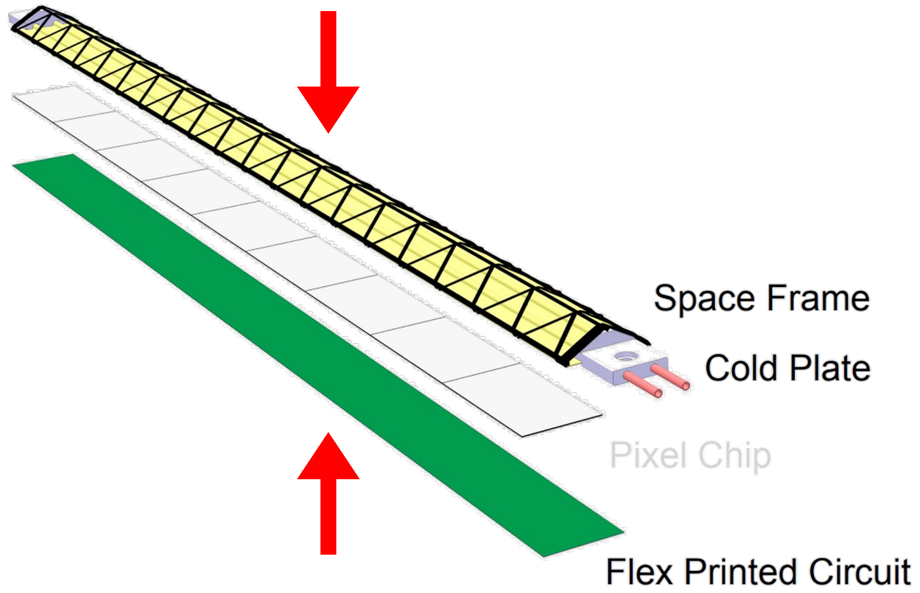

- **Si** (■) is **only 1/7th** of total material
- Irregularities due to support/cooling and staves overlapping

Overview

Motivation

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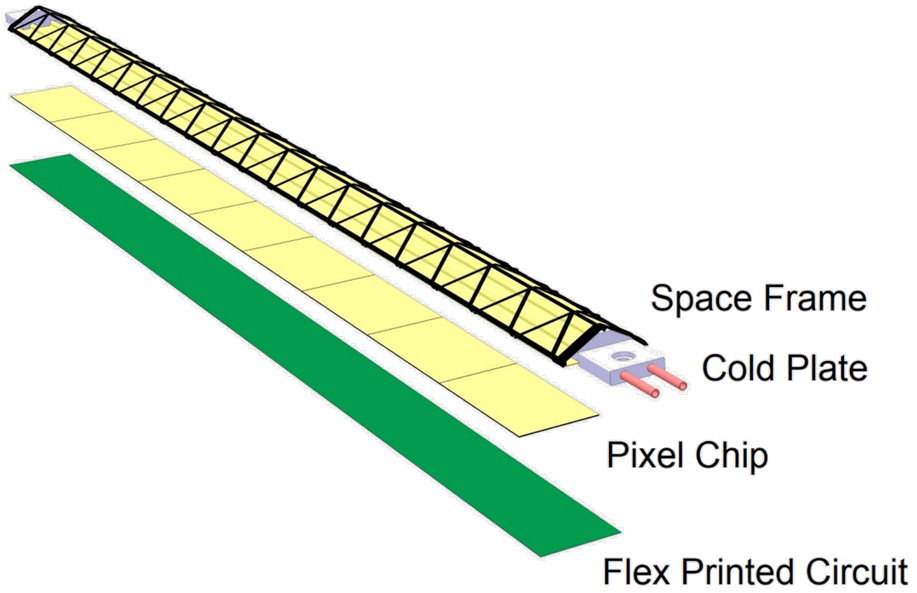
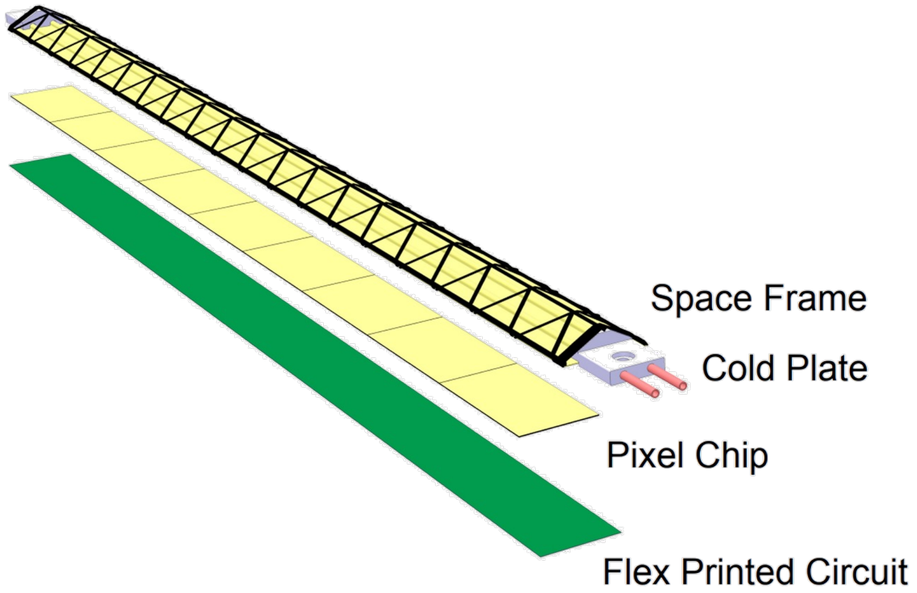


Overview

Motivation

1. **Can the material be further reduced?**

Wishlist:



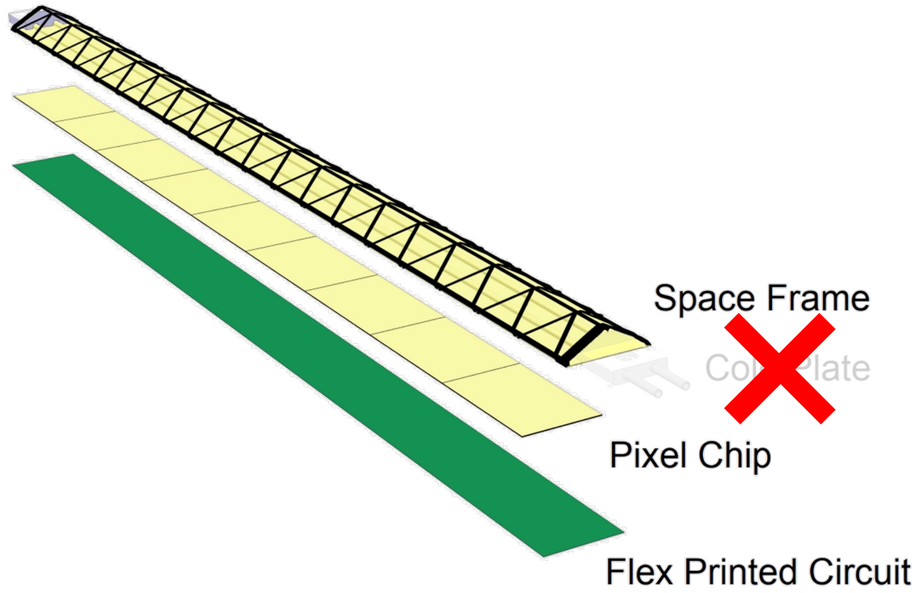
Overview

Motivation

1. **Can the material be further reduced?**

Wishlist:

- **Removal of water cooling**
  - Needs drastic reduction in power consumption



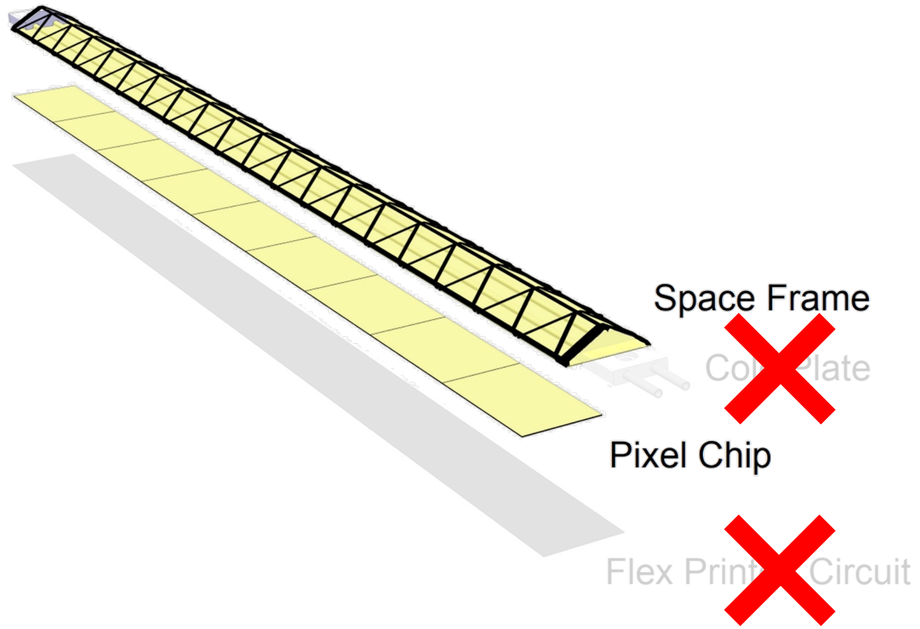
Overview

Motivation

1. **Can the material be further reduced?**

Wishlist:

- Removal of water cooling
  - Needs drastic reduction in power consumption
- **Removal of the circuit board**
  - Needs power+data integrated on chip



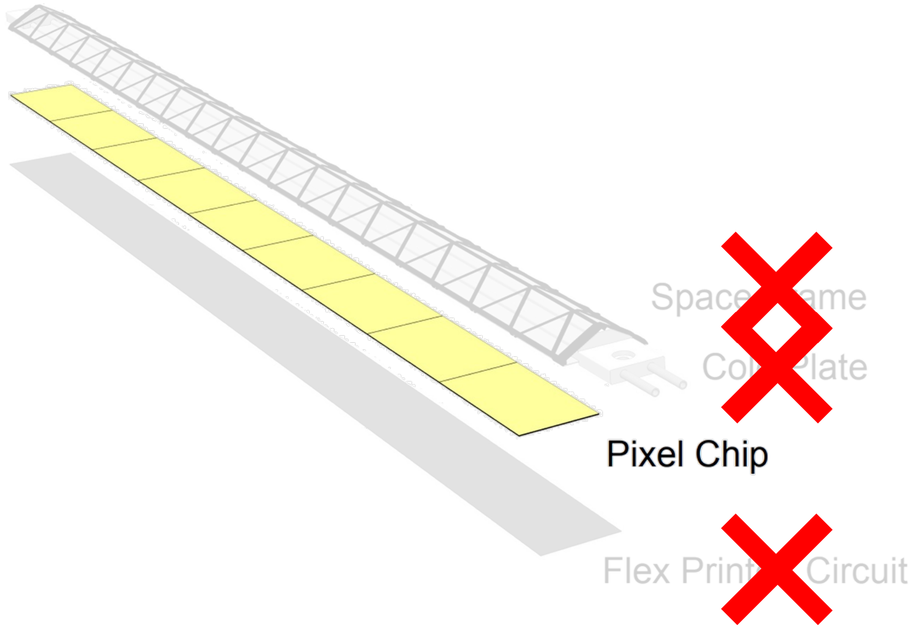
Overview

Motivation

1. **Can the material be further reduced?**

Wishlist:

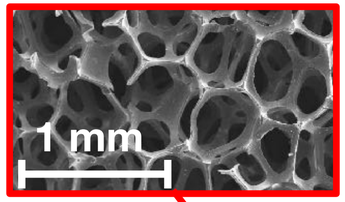
- Removal of water cooling
  - Needs drastic reduction in power consumption
- Removal of the circuit board
  - Needs power+data integrated on chip
- **Removal of mechanical support**
  - Needs self-supporting arched Si wafers



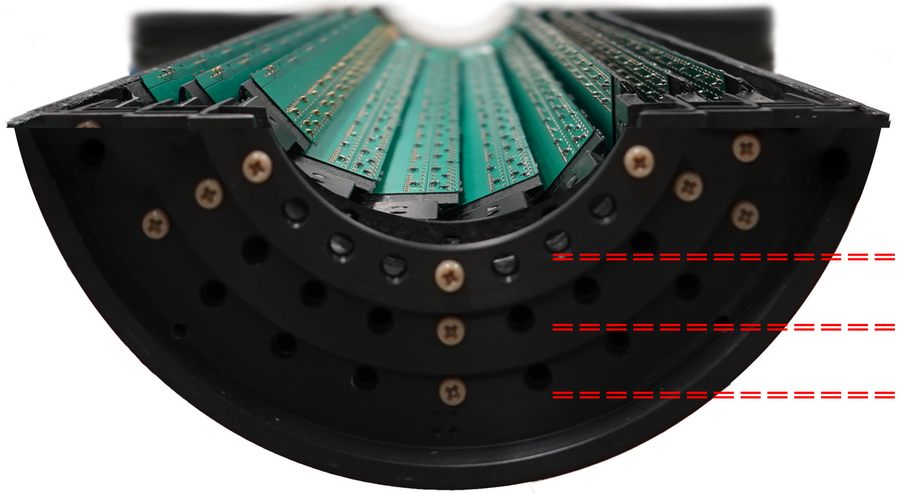
Overview

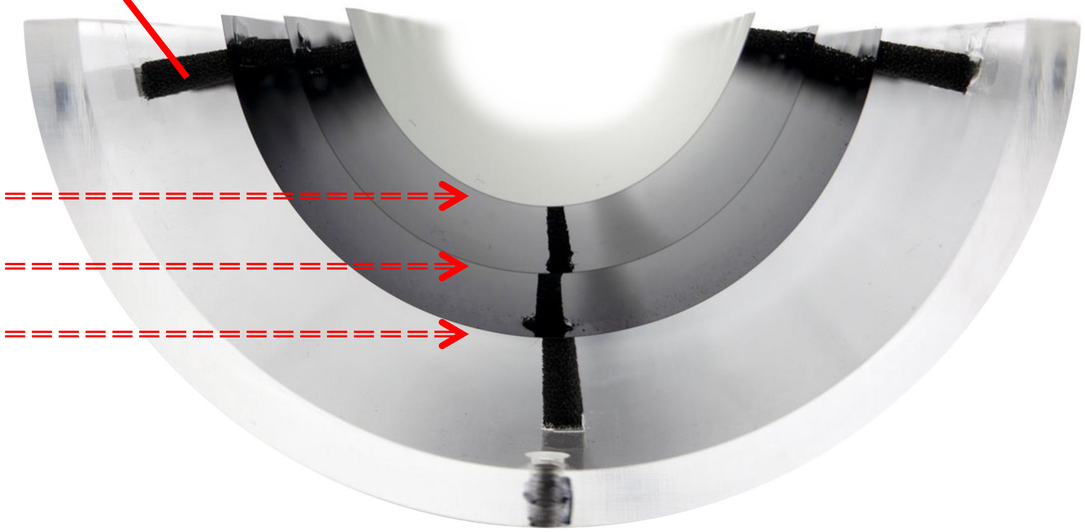
Concept

Carbon foam



Getting closer to the ideal detector: real half-cylinders of bent, thin silicon





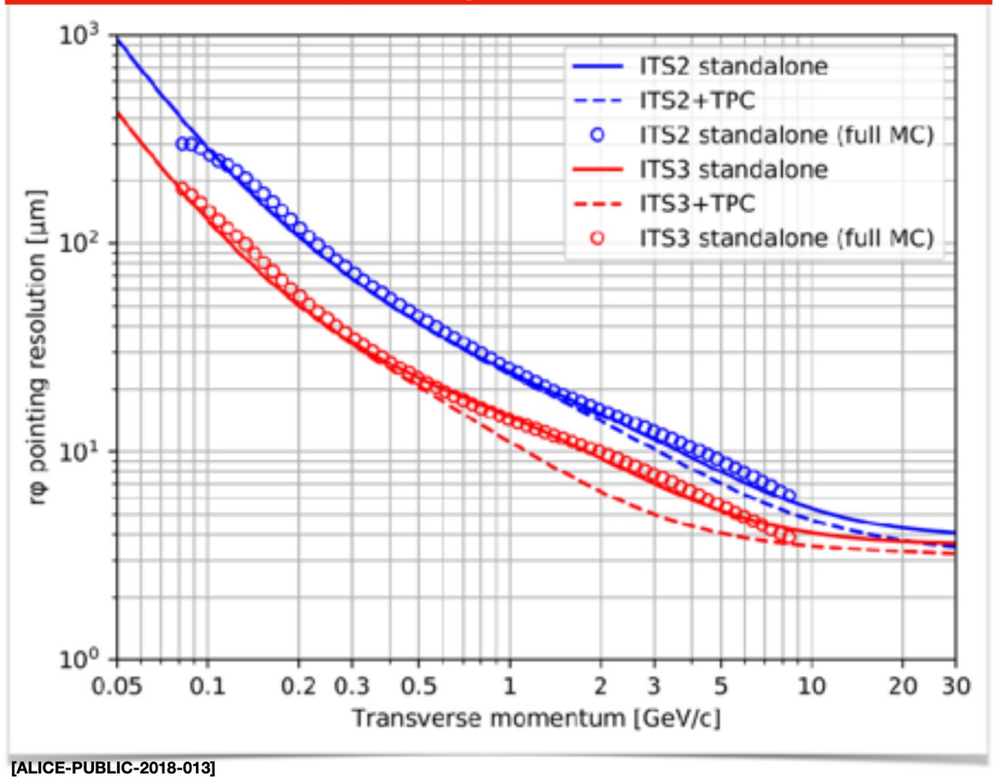
ITS2 half Inner Barrel

ITS3 Engineering Model 1

Overview

Concept

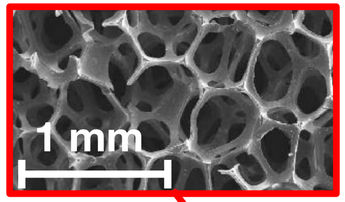
pointing resolution



improvement of factor 2 over all momenta

e.g. Λc S/B improves by factor 10, significations by factor 4

Carbon foam



Getting closer to the ideal detector: real half-cylinders of bent, thin silicon

ITS3 Engineering Model 1

Overview

Concept

1. **Can the material be further reduced?**
   - Real half-cylinders of bent, thin silicon

Overview

Concept

1. Can the material be further reduced?
   - Real half-cylinders of bent, thin silicon

2. **Can we get closer to the interaction point?**

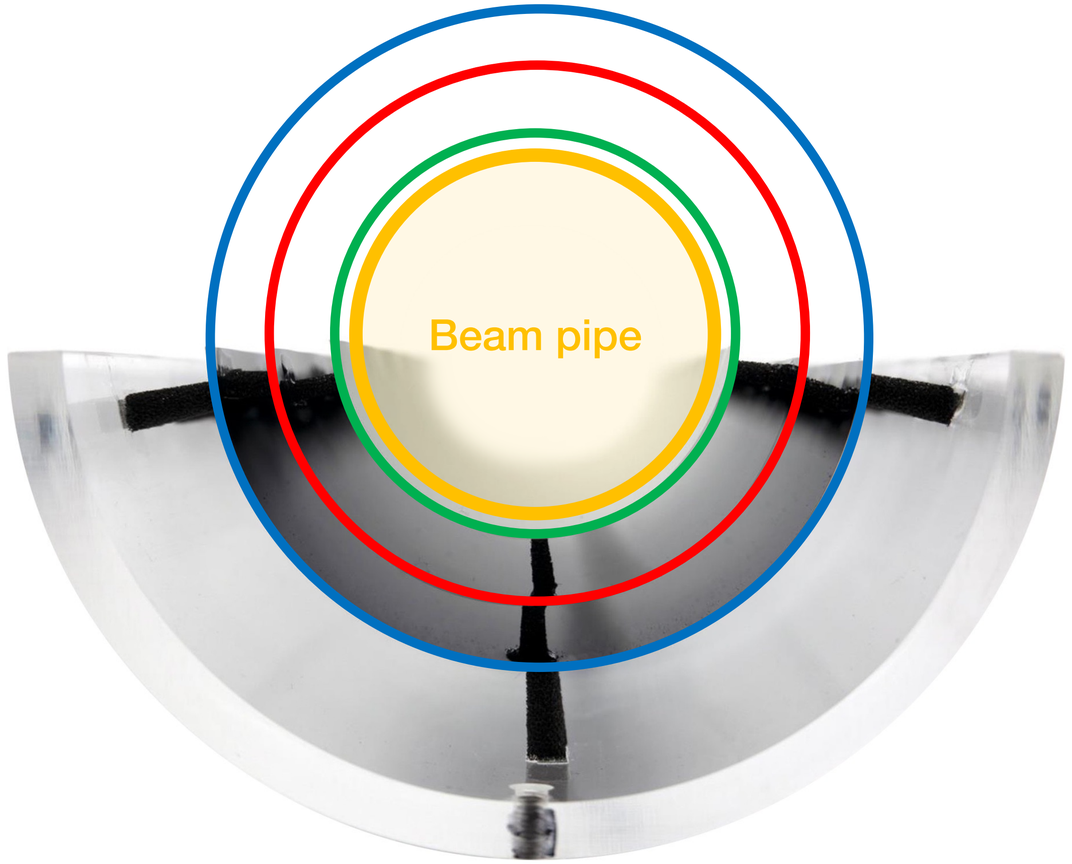
Overview

Concept

1. Can the material be further reduced?
   - Real half-cylinders of bent, thin silicon

2. **Can we get closer to the interaction point?**
   - **Thinner beam pipe** (radius: **18.2** → **16.0** mm)
   - **Layer 0 closer to IP** (22.4–**26.7** → **18.0** mm)

	Radius (mm)	Sensor size (mm^2)
Layer 0	18	266 x 55
Layer 1	24	266 x 74
Layer 2	30	266 x 93



Overview

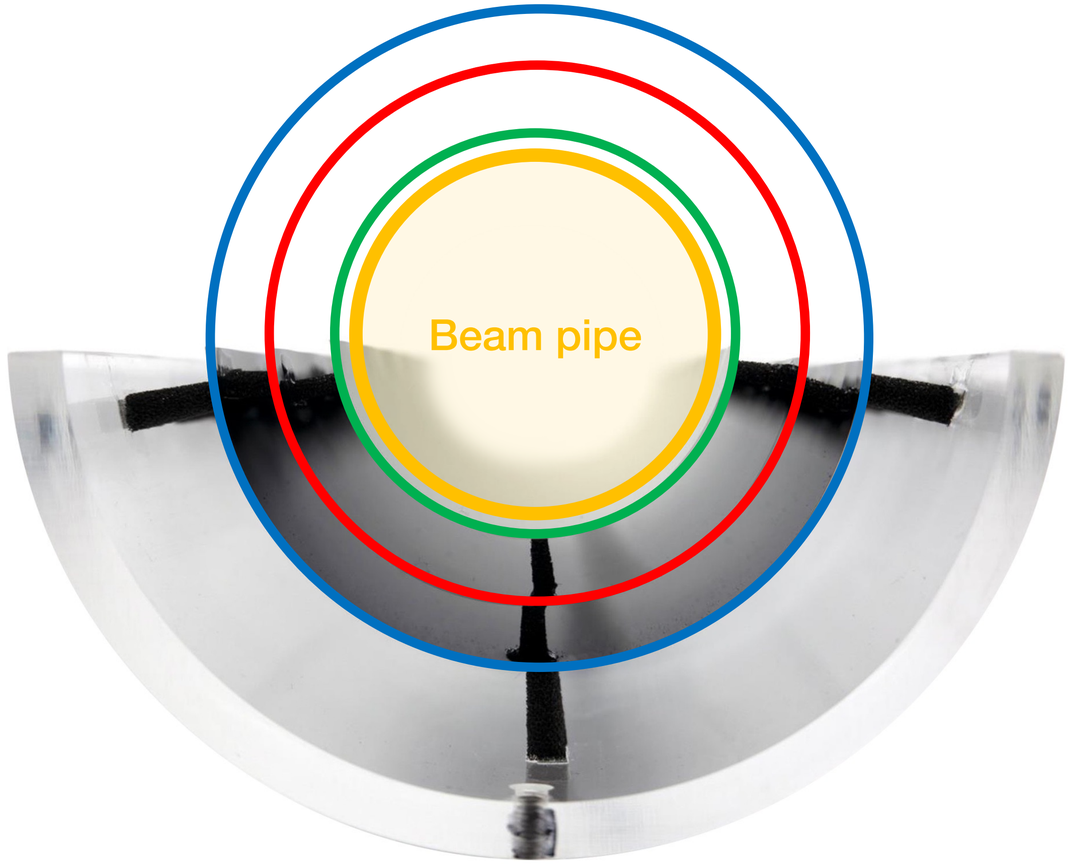
Concept

How do we get there?

- **Sensor R&D**
  - 5 μm resolution (pixel size O(20x20 μm^2))
  - 1×10^{13} 1 MeV n_{eq} cm^{-2} (NIEL)

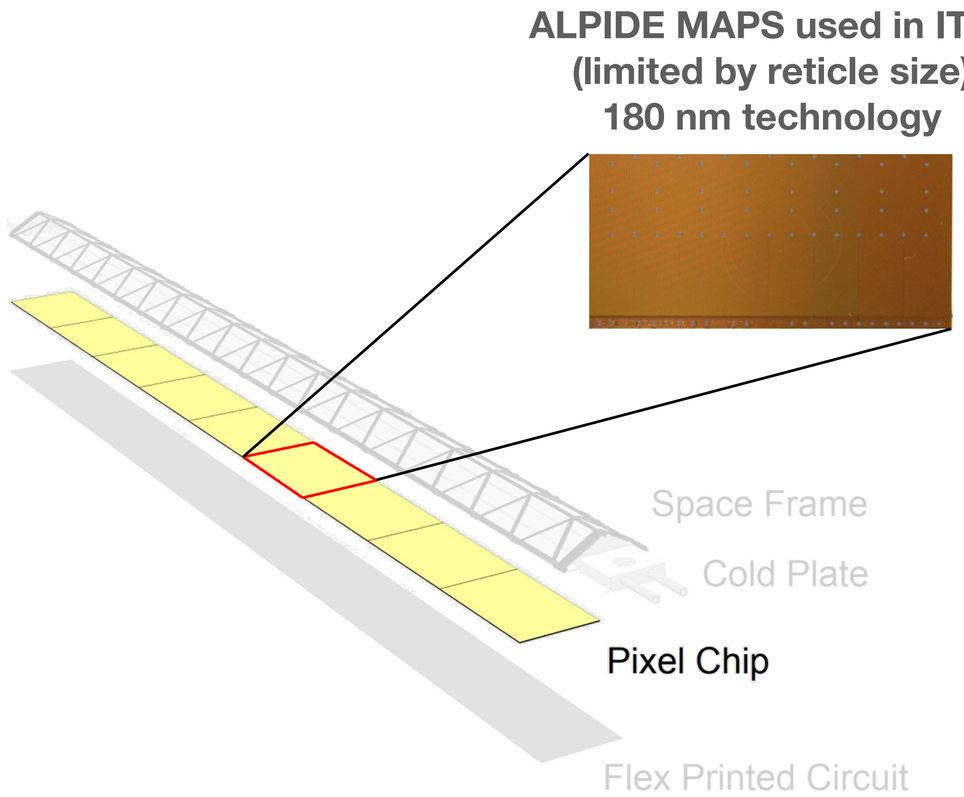
- **Electro-mechanical integration**
  - Silicon bending
  - Carbon foam properties
  - Sensor cooling
  - Interconnection

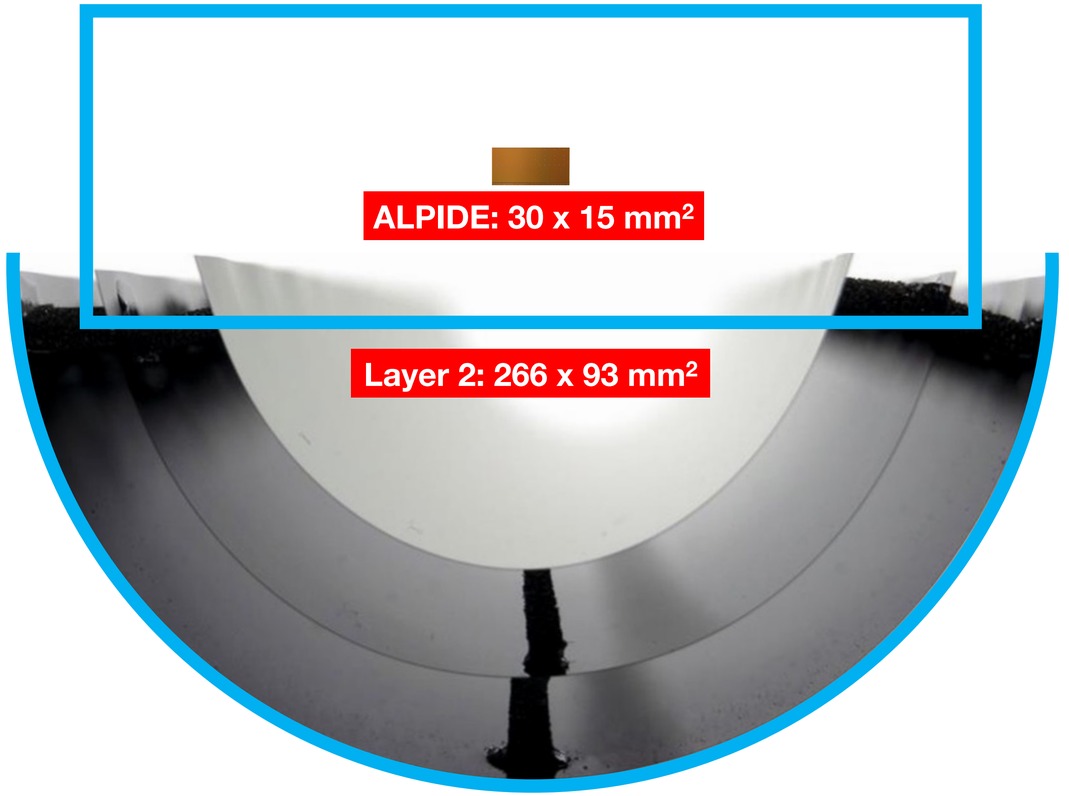
More in backup slides!



Sensor R&D

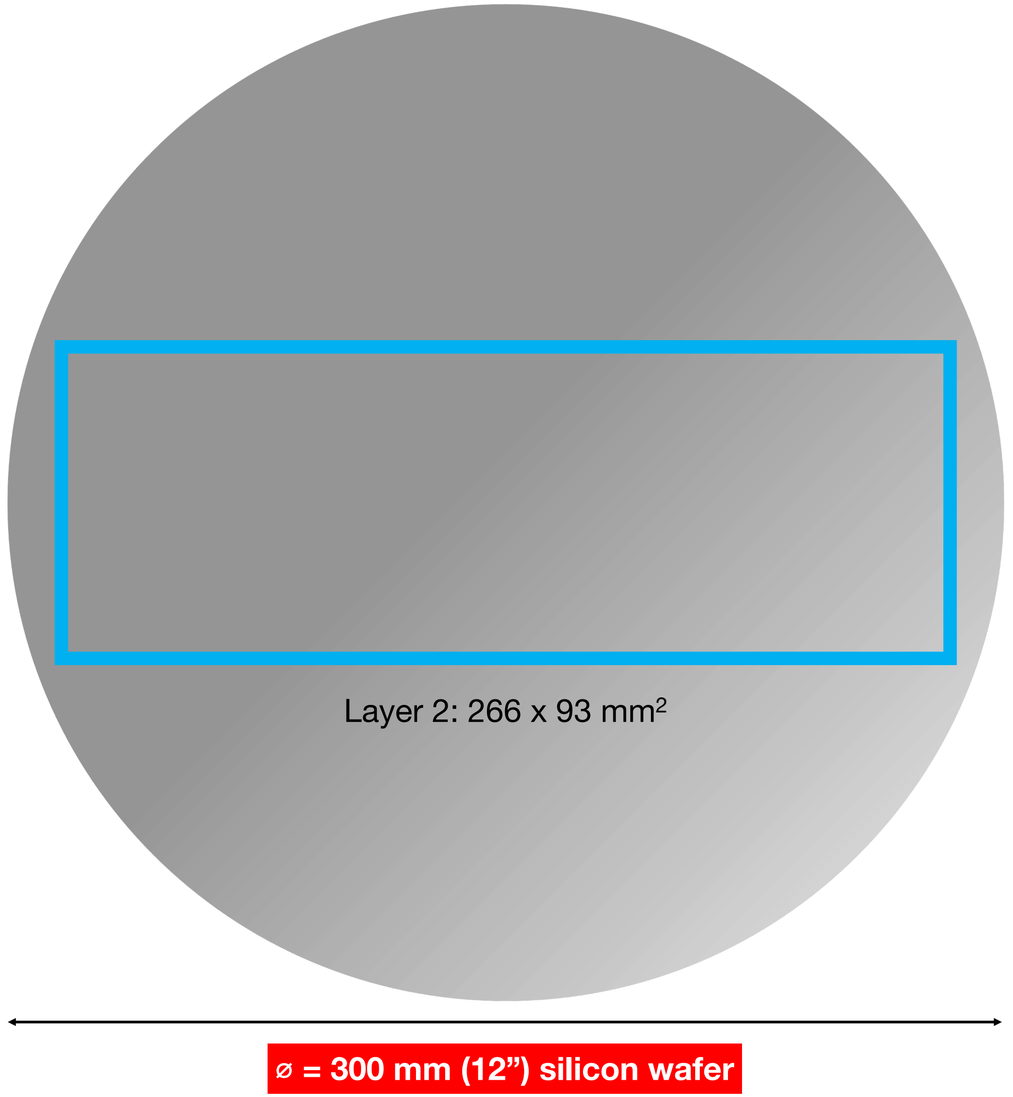
Wafer-scale stitched sensors





Sensor R&D

Wafer-scale stitched sensors

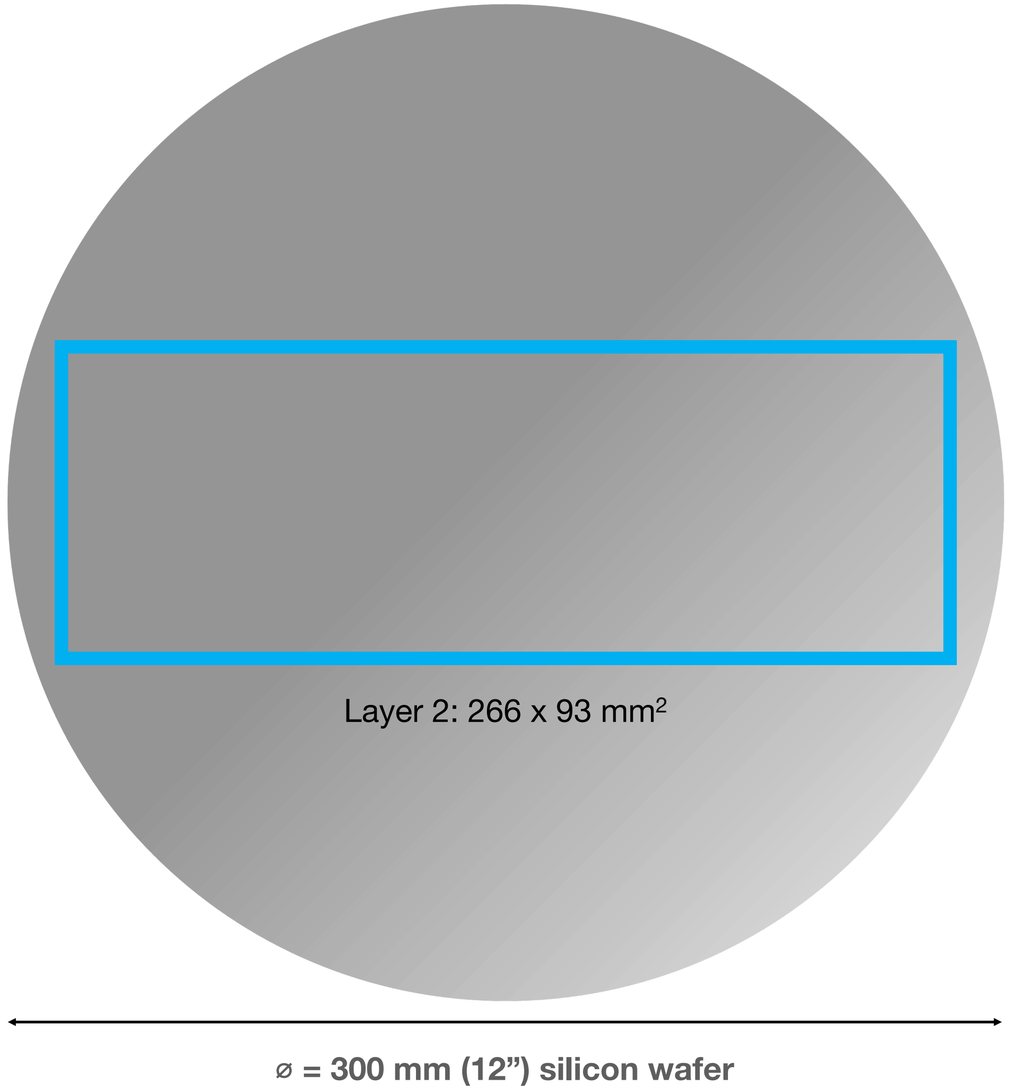


Sensor R&D

Wafer-scale stitched sensors

Three main ingredients:

1. **65 nm** technology by TPSCo*
   - ➛ Lower power, tighter integration
   - ➛ **300 mm wafers**



* Tower Partners Semiconductor Co.

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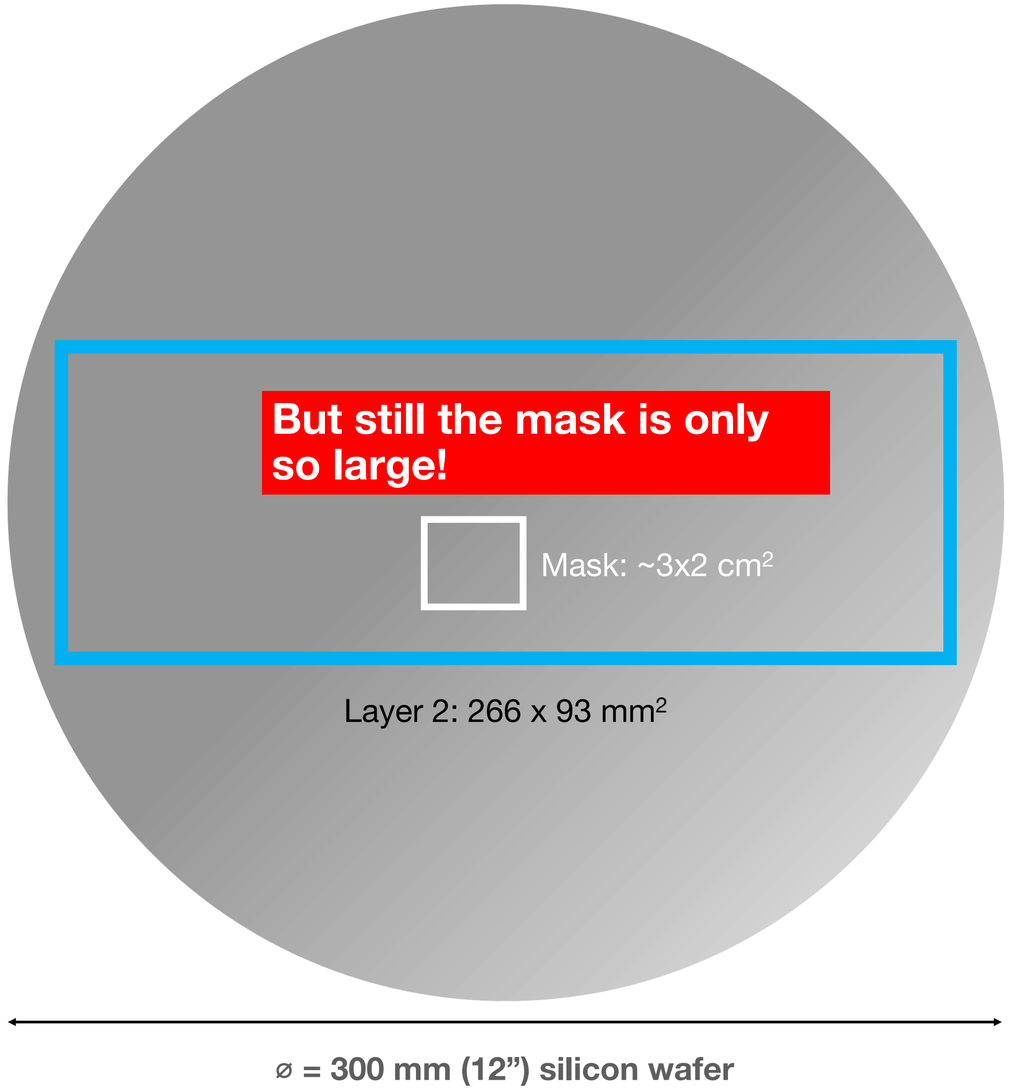

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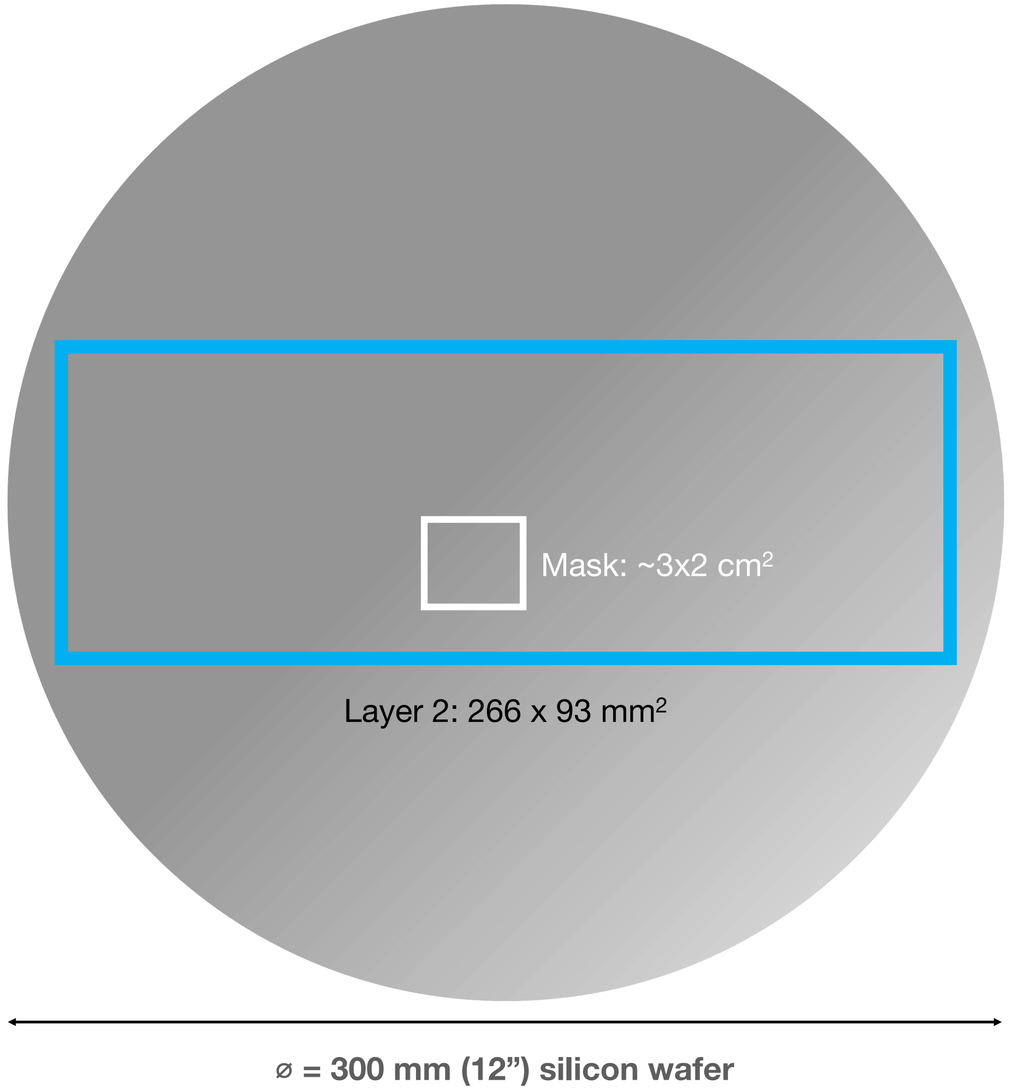

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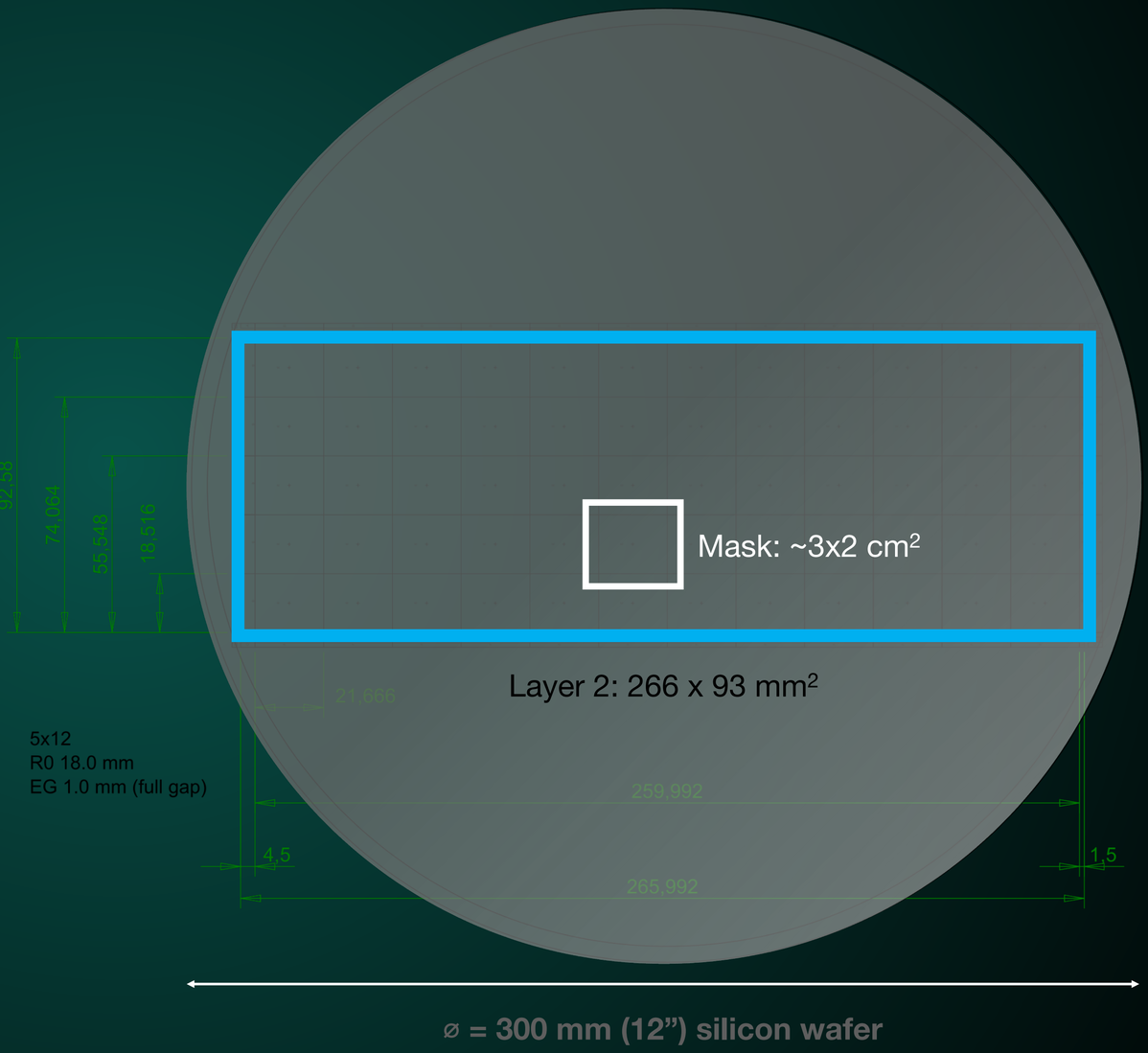
Sensor R&D

Interlude: stitching

Two main steps:

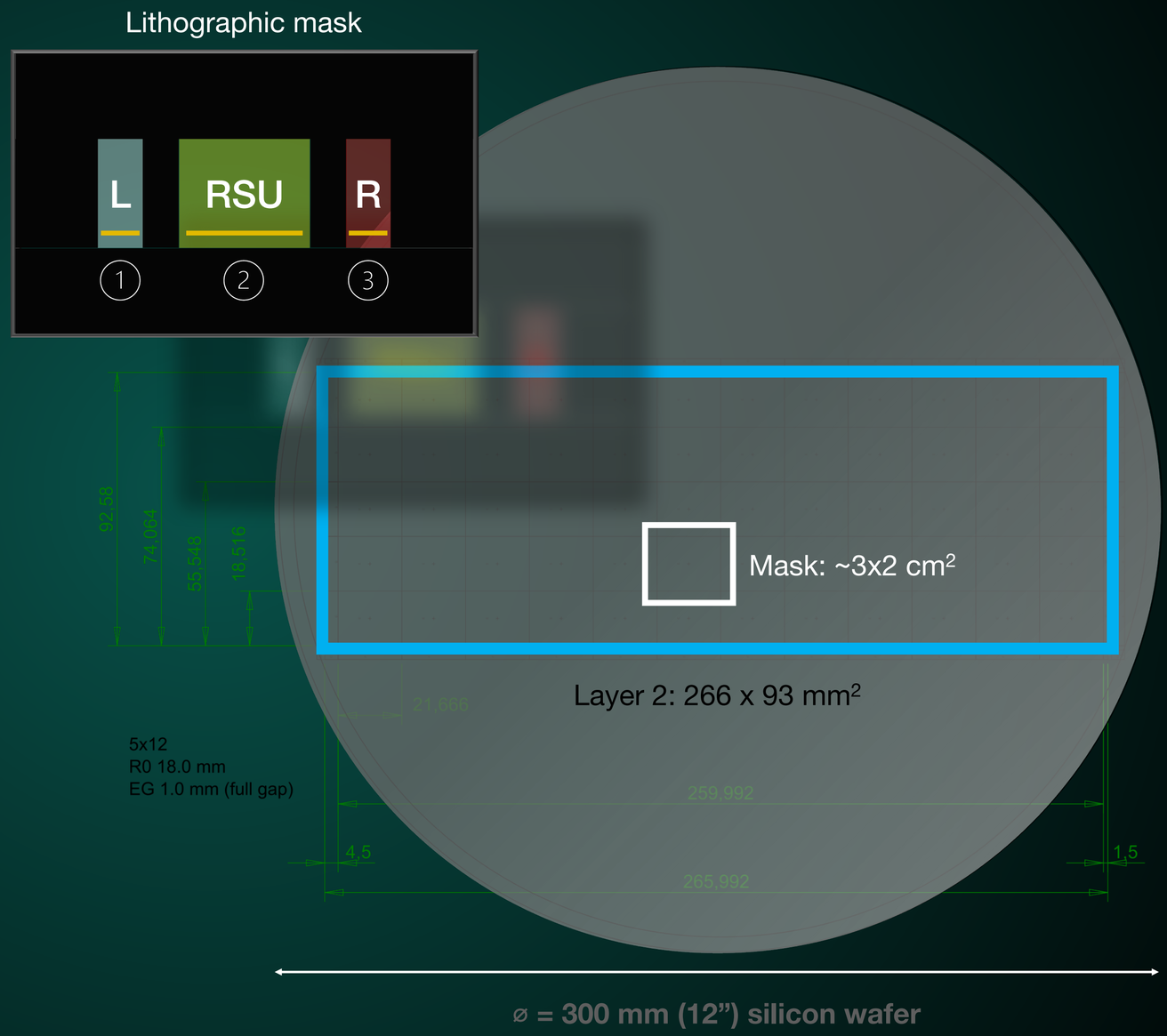


Sensor R&D

Interlude: stitching

Two main steps:

1. **Lithography**

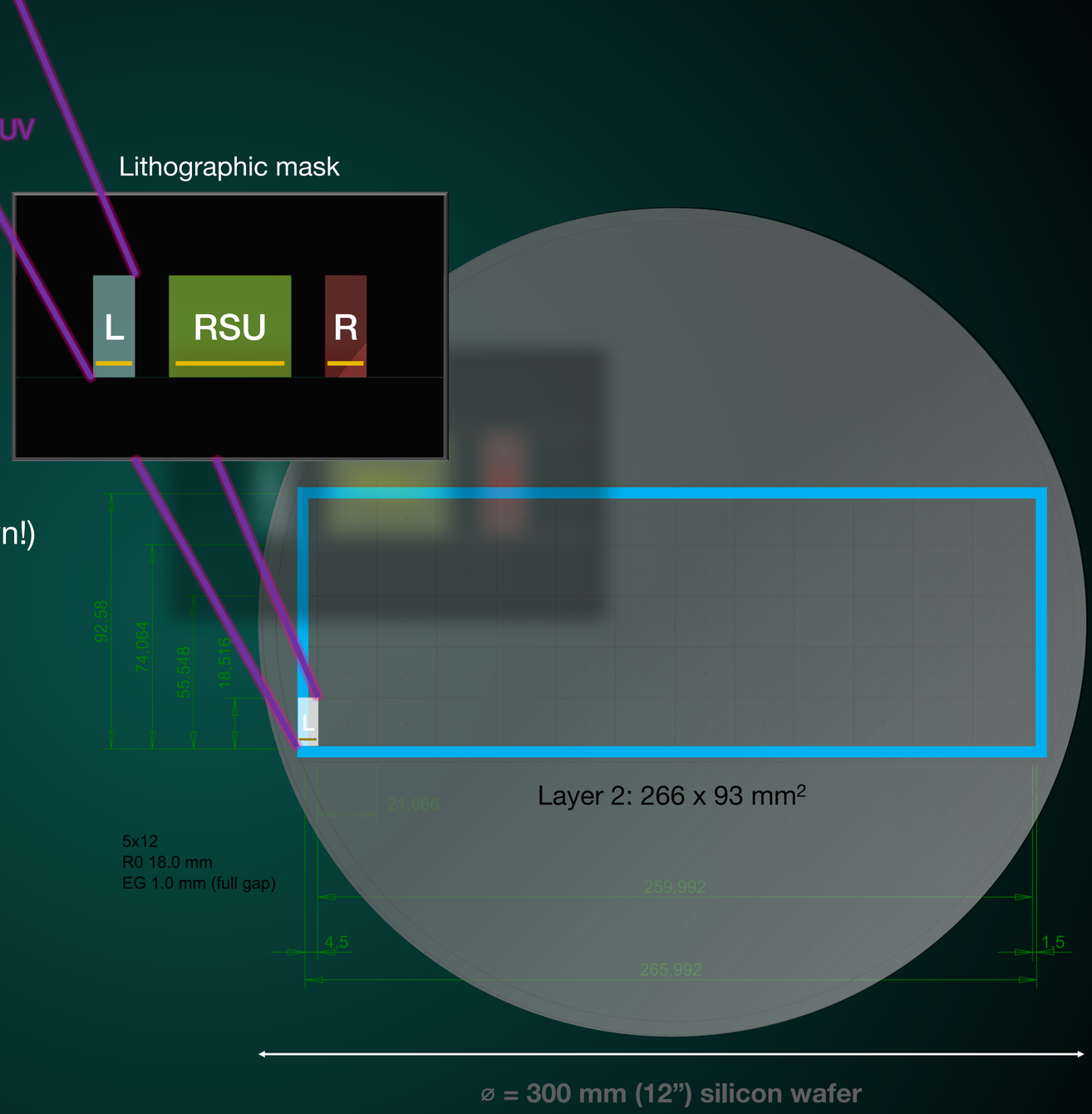


Sensor R&D

Interlude: stitching

Two main steps:

1. **Lithography**
    1. Left **endcap** (a challenging design on its own!)



Sensor R&D

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Two main steps:

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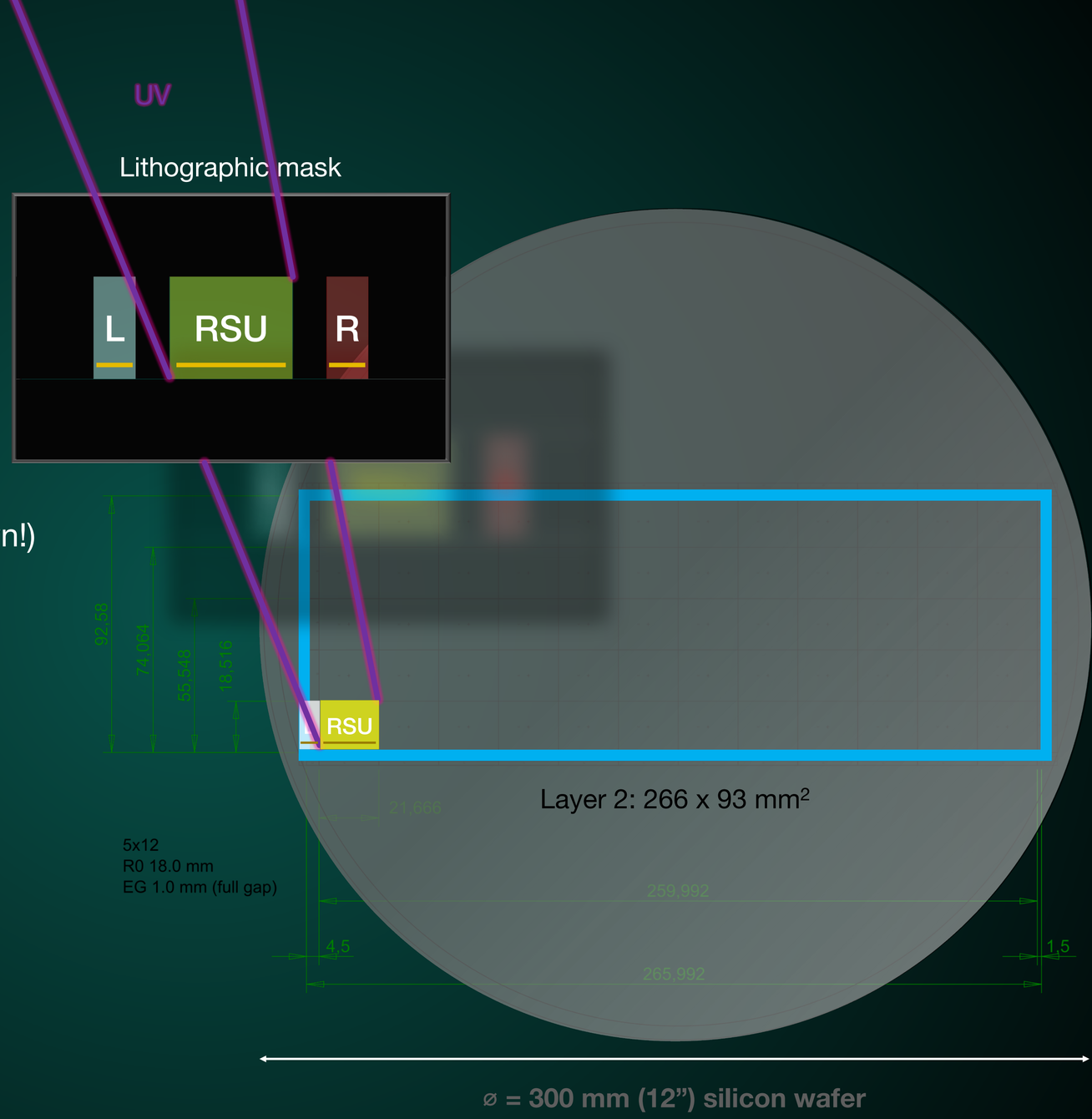

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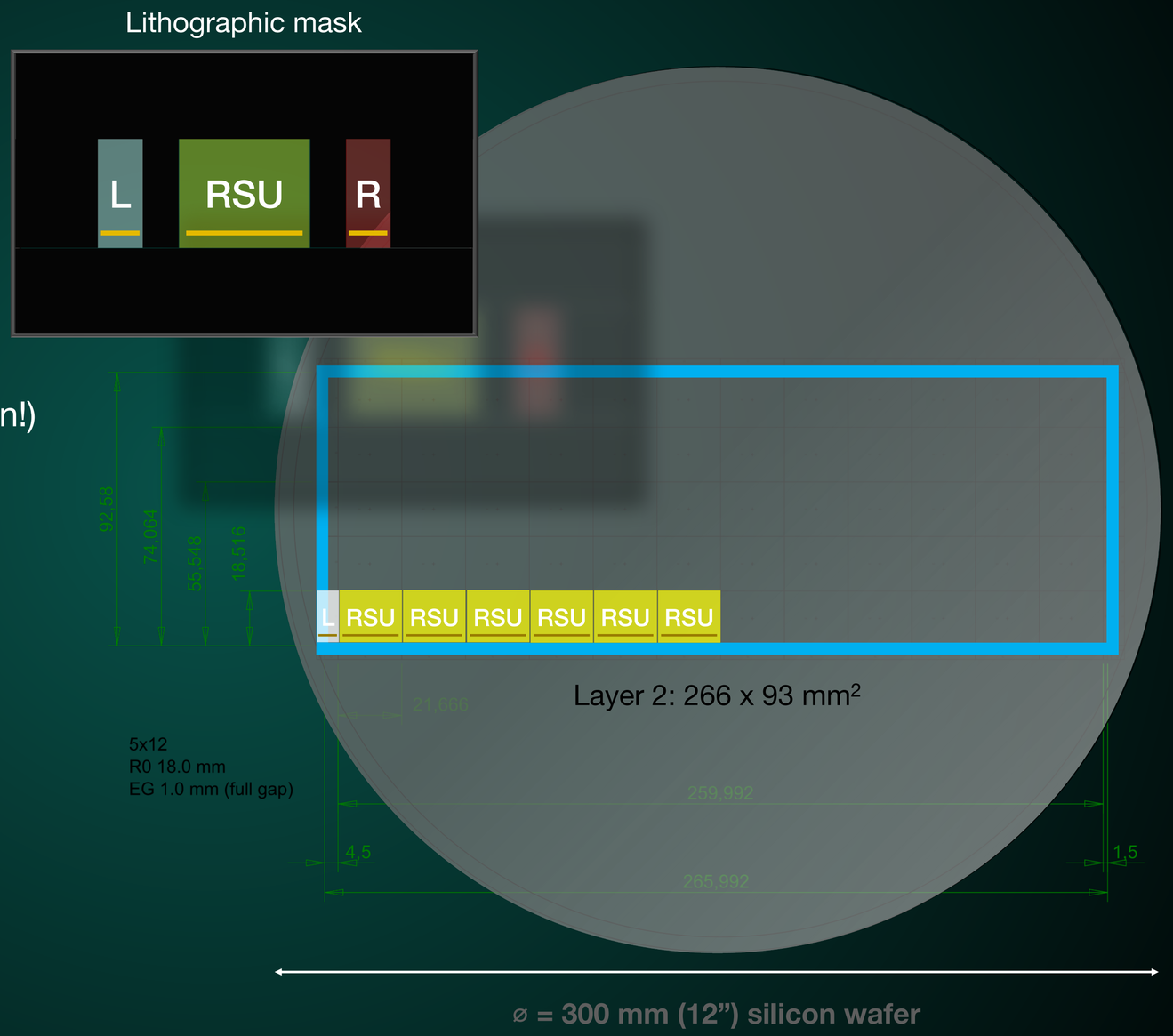

Sensor R&D

Interlude: stitching

Two main steps:

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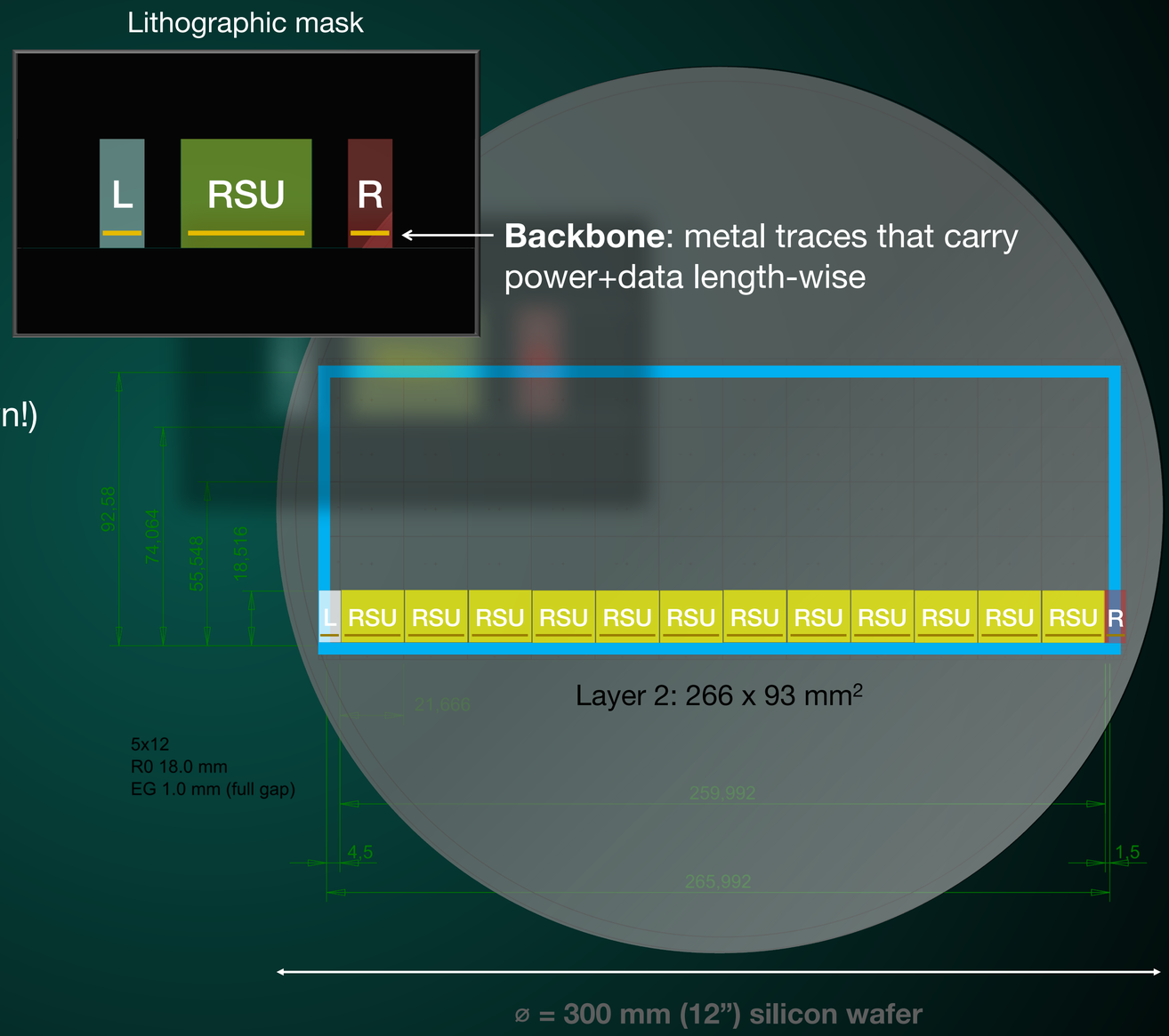

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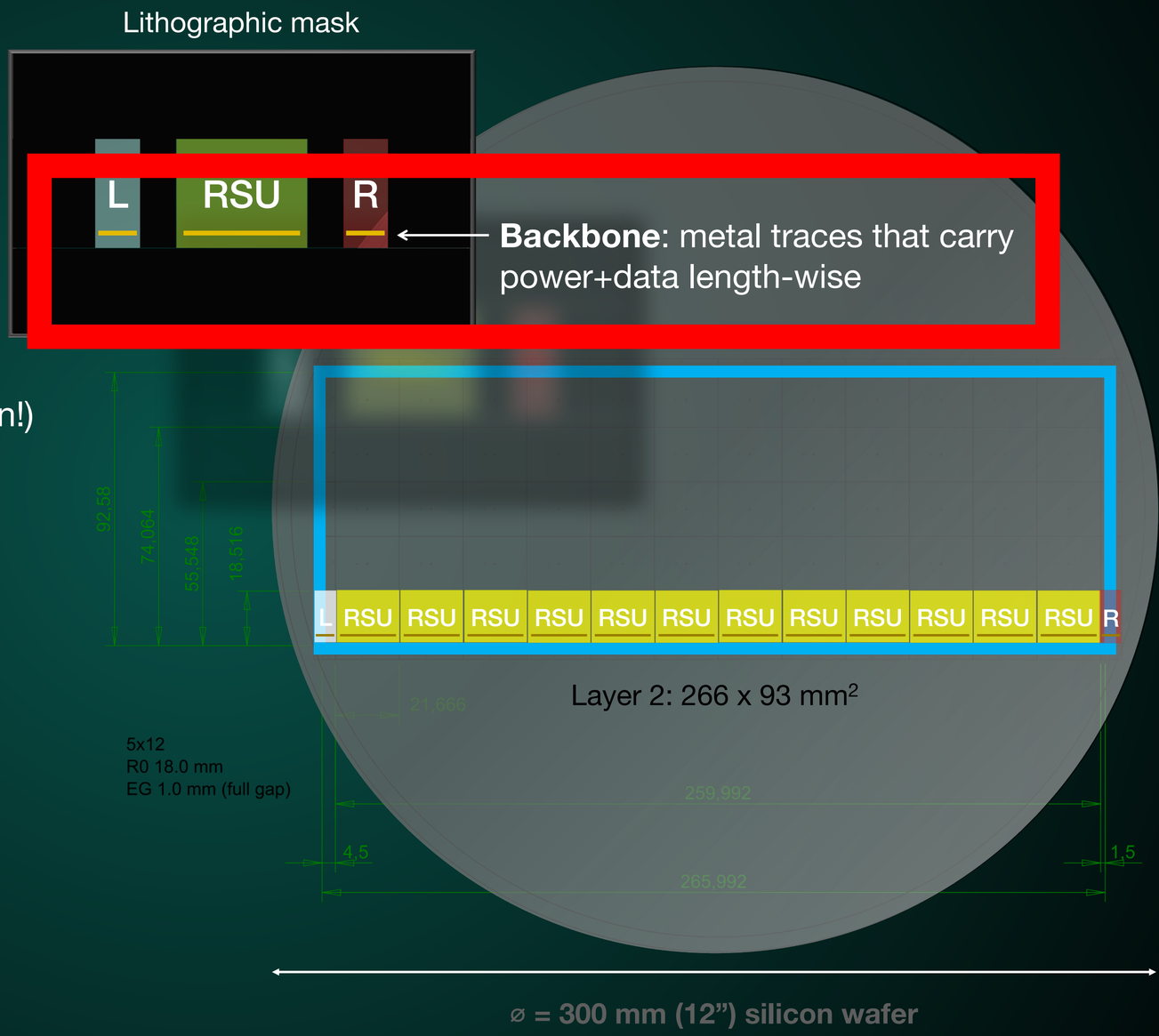

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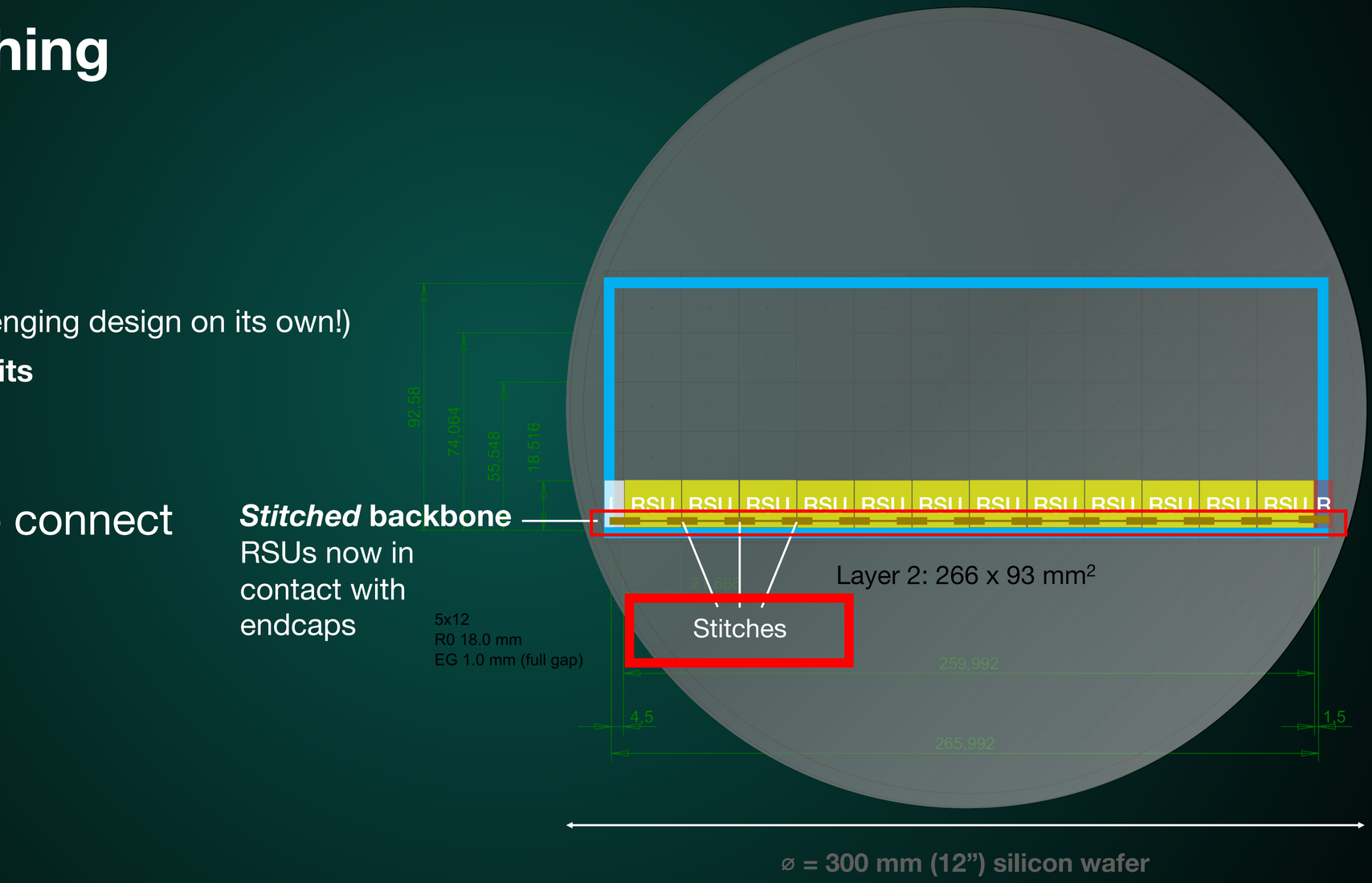
2. **Stitching** used to connect metal traces



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Interlude: stitching

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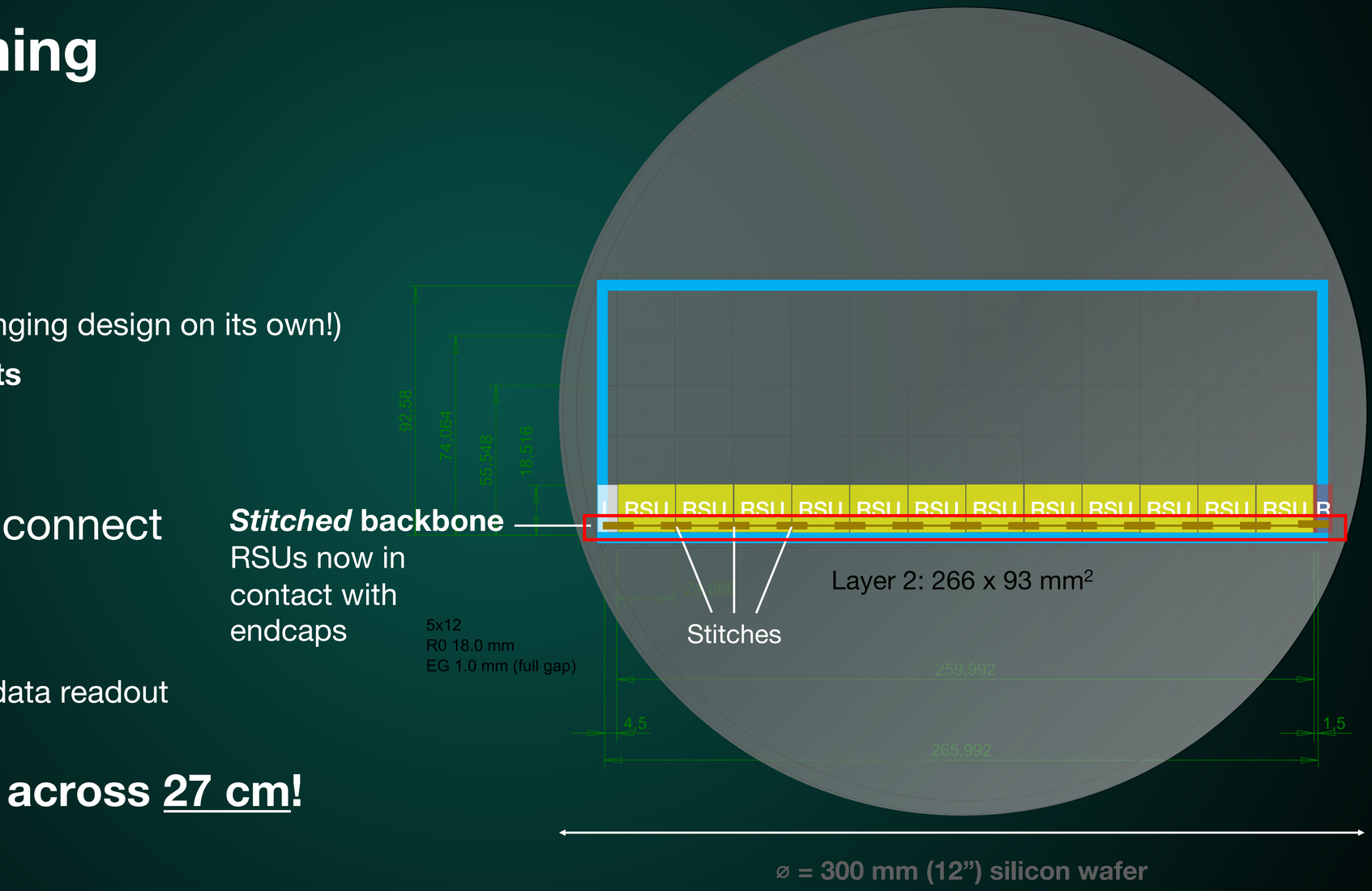
2. **Stitching** used to connect metal traces
    - power distribution
    - buses for control and data readout

Power+data carried across <u>27 cm</u>!



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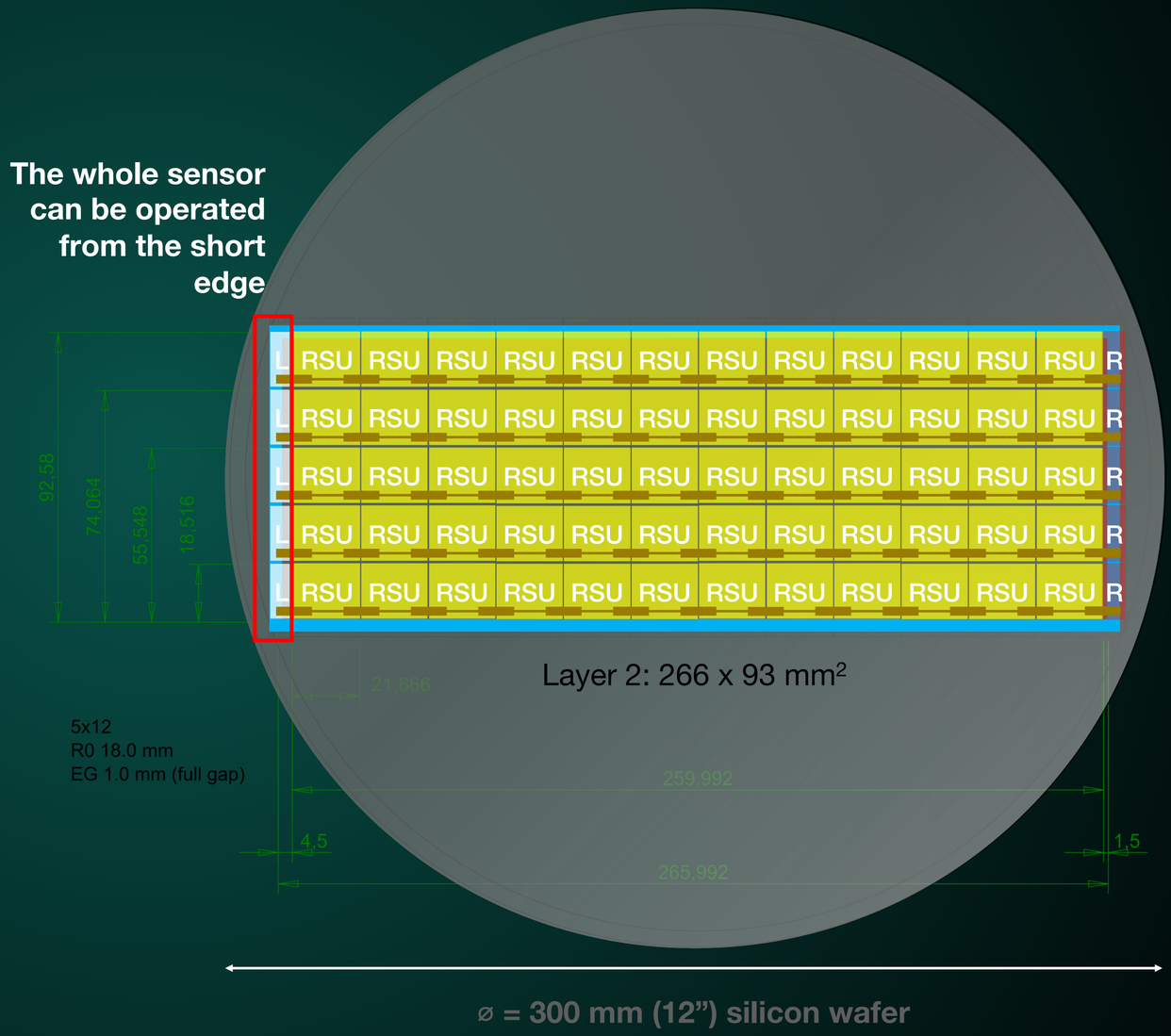

Sensor R&D

Wafer-scale stitched sensors

Three main ingredients:

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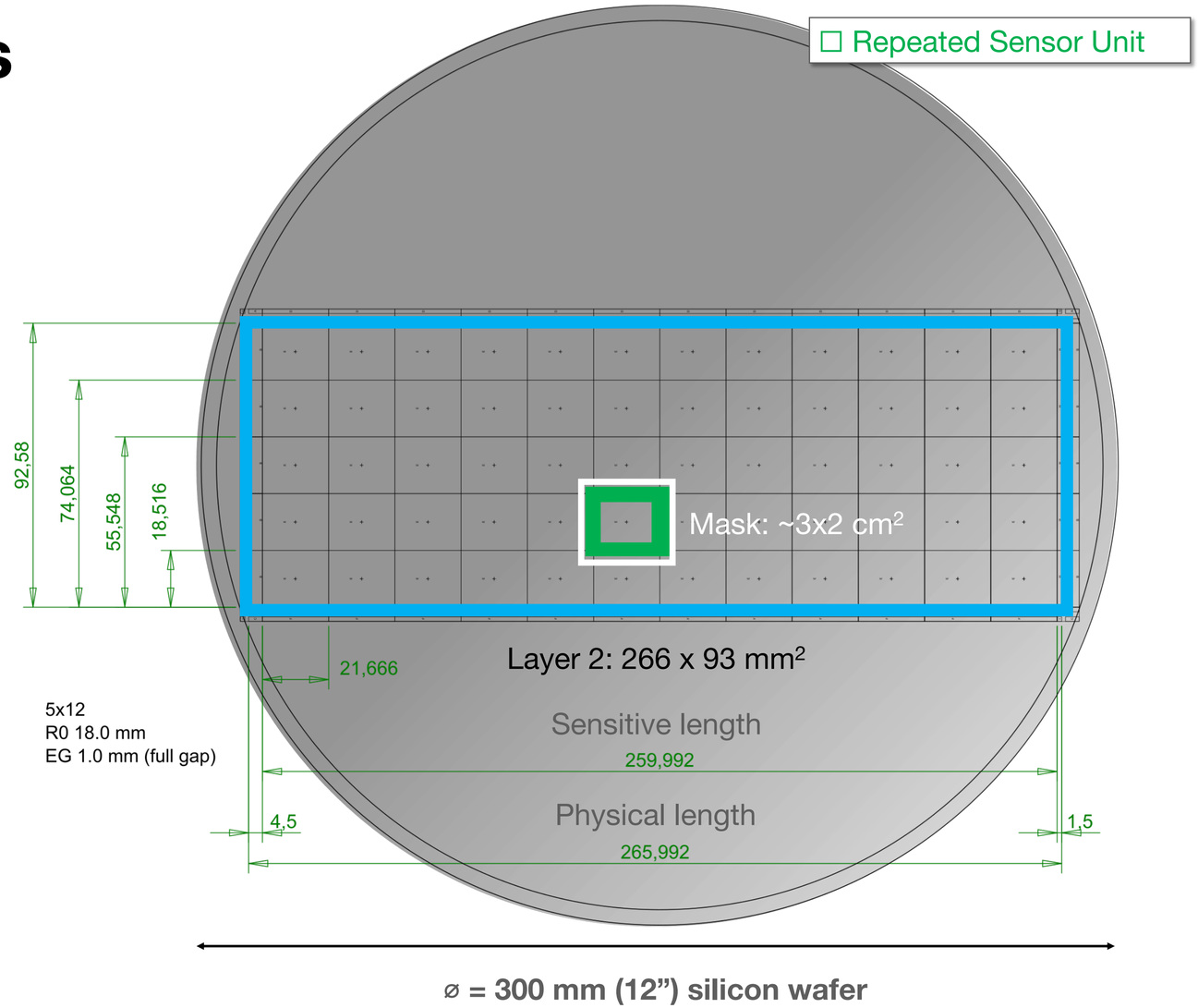

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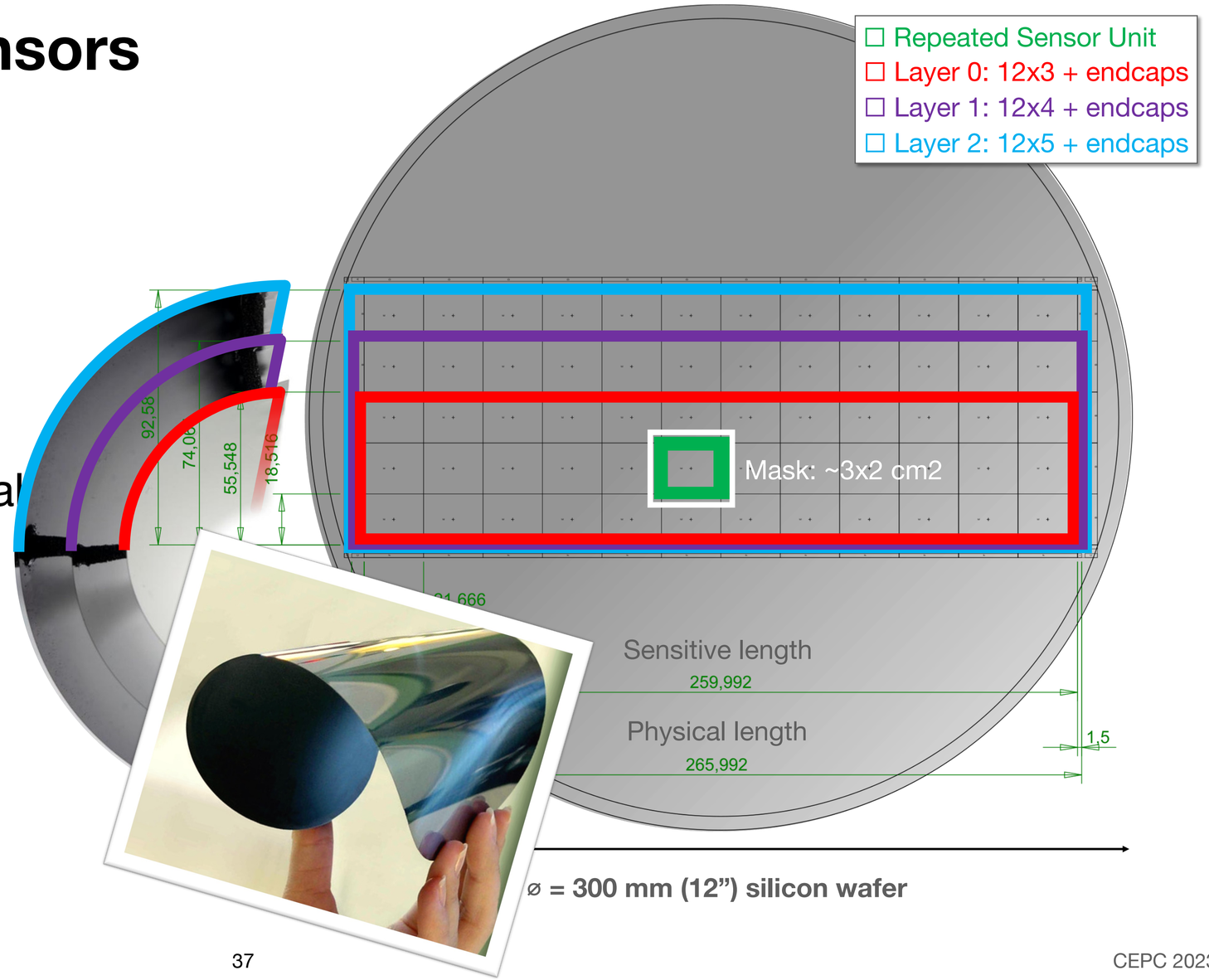
   - buses for control and data readout

3. **Bending** (Si thinned <50 μm)



* Tower Partners Semiconductor Co.

Sensor R&D

Wafer-scale stitched sensors

Three main ingredients:

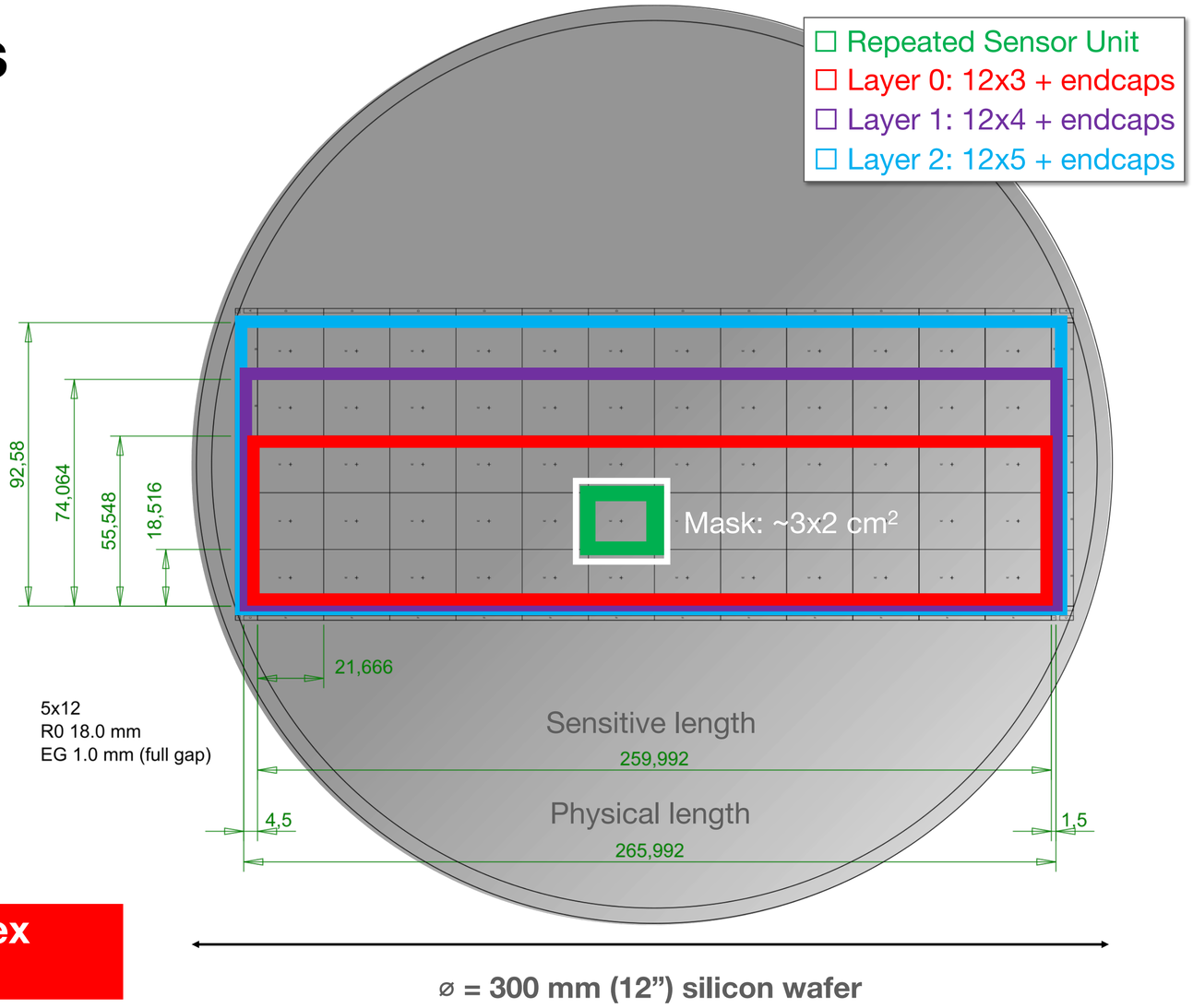
1. **65 nm** te[1st in HEP!] [TPSCo]*
   - ➛ Lower pow[er], tighter integration
   - ➛ **<u>300 mm wafers</u>**

2. **Stitching** [1st in HEP!] nnect metal traces
   - power distribution
   - buses for control and data readout

3. **Bending** [1st in HEP!] <50 µm)

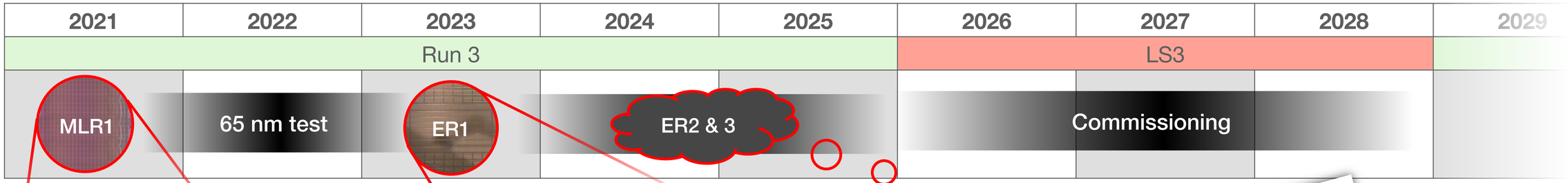
* Tower Partners Semiconductor Co.

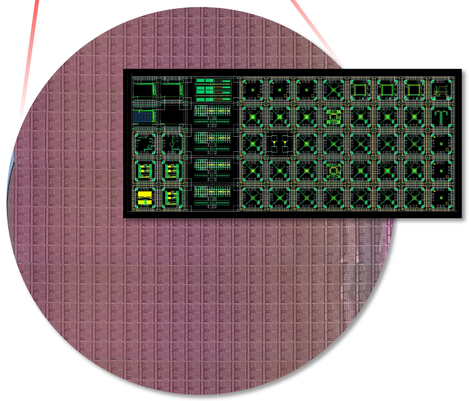
A breakthrough vertex detector!

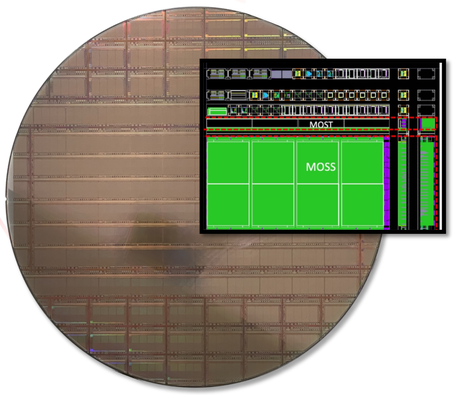


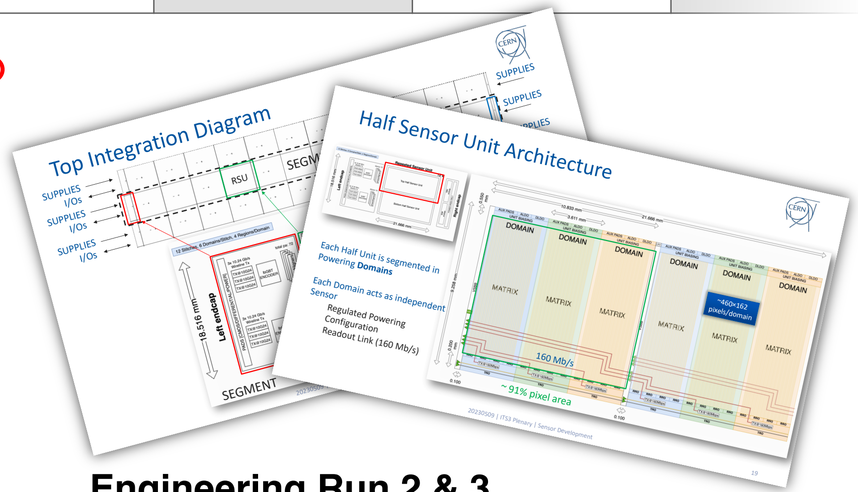
Sensor R&D

Milestones









Multi-Layer Reticle 1

First submission in TPSCo 65 nm:

- Lots of prototypes: 55 chips
- **Goal**: qualify the technology (**achieved**)

Engineering Run 1

First wafer-scale stitched sensors:

- Two large stitched prototypes
- **Goal**: assess yield (**ongoing**)

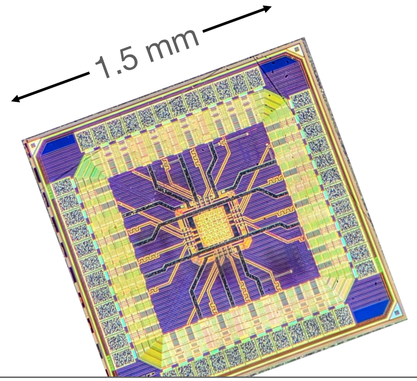
Engineering Run 2 & 3

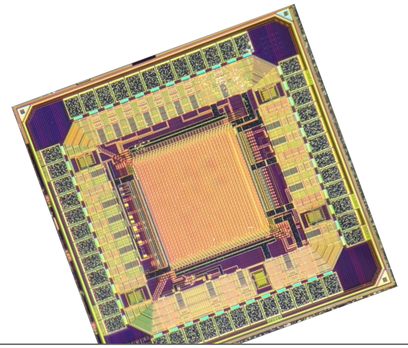
Final sensor

- ER2: final sensor prototype (design **ongoing**)
- ER3: final sensor production

Sensor R&D

Multi-Layer Reticle 1: first 65 nm prototypes





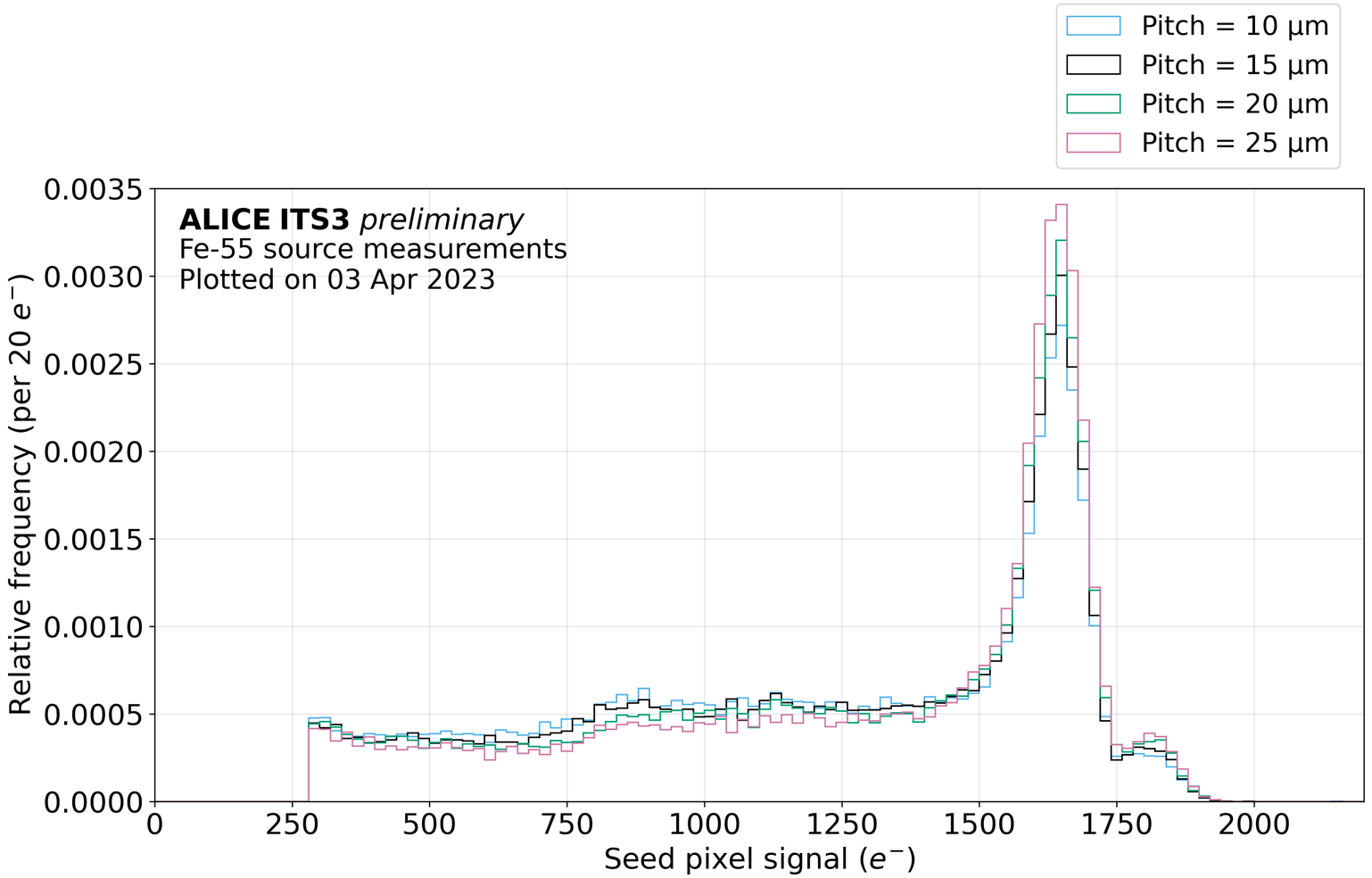
	APTS	DPTS
	Analog Pixel Test Structure	*Digital Pixel Test Structure*
Matrix	6x6	32x32
Readout	direct analog readout of central 4x4	async. digital with ToT
Pitch	10, 15, 20, 25 µm	15 µm
Number of dies	34	4

Lots of (small) prototypes to explore the technology for particle detection

Sensor R&D

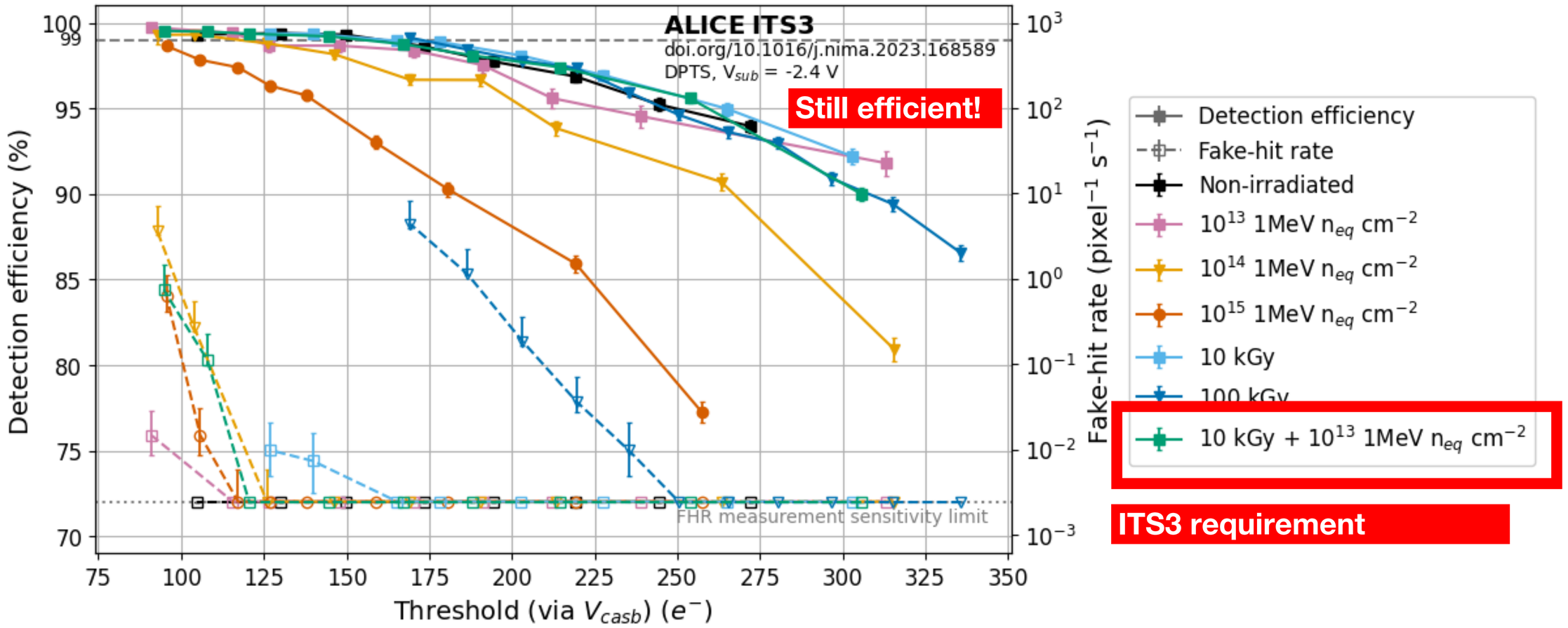
Multi-Layer Reticle 1: APTS

- **Pixels of pitches of 10–25 µm show similar results**
  - charge collection is very efficient
- We can ***choose*** the optimal pitch for the final sensor



Sensor R&D

Multi-Layer Reticle 1: DPTS

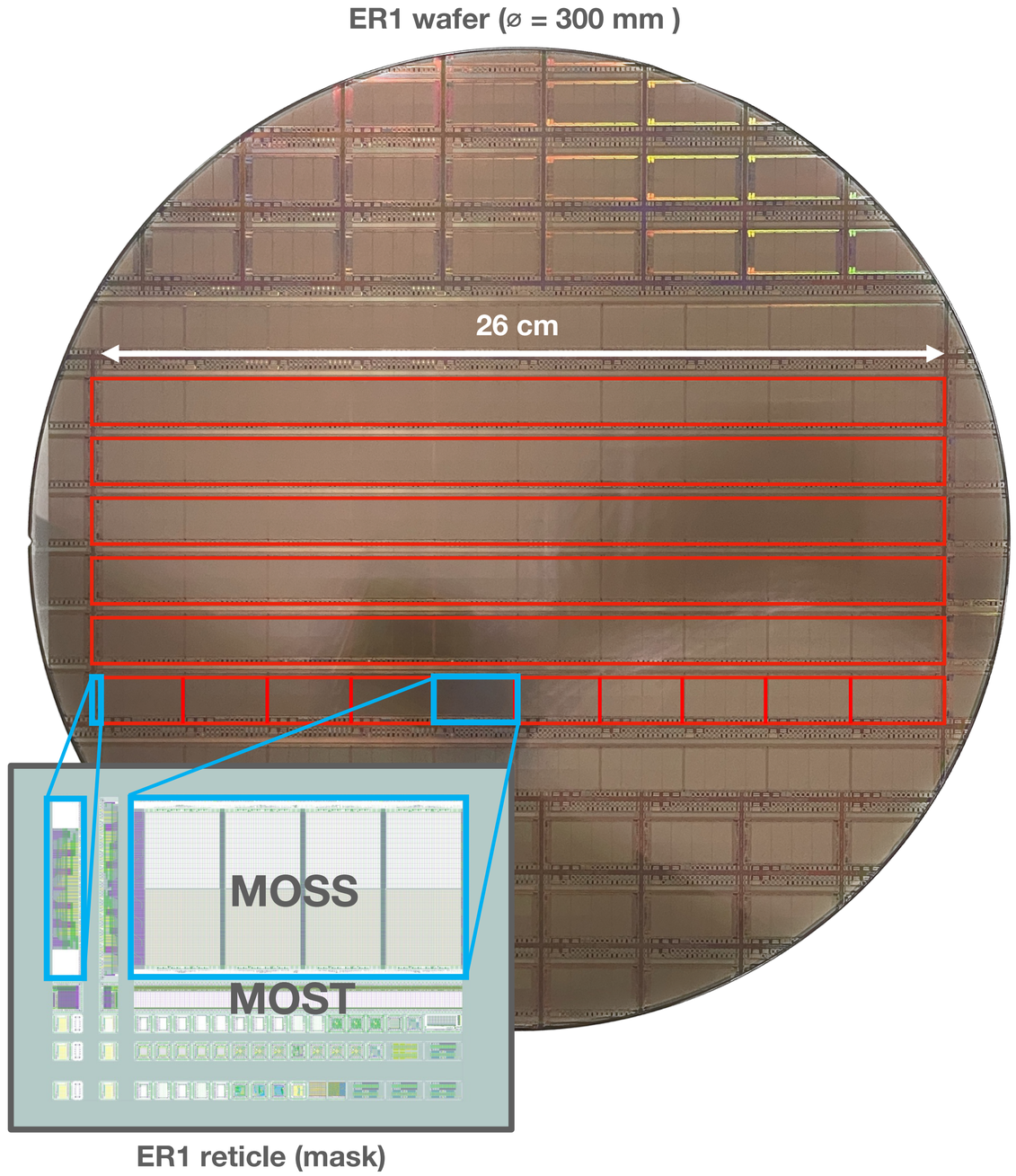


Sensor R&D

Engineering Run 1

Designing **the first wafer-scale MAPS detector for high-energy physics**

- Two large stitched sensors:
  - **MOSS** (14 x 259 mm^2)
  - **MOST** (2.5 x 259 mm^2)
- Both with digital readout, but different approaches



Sensor R&D

Engineering Run 1

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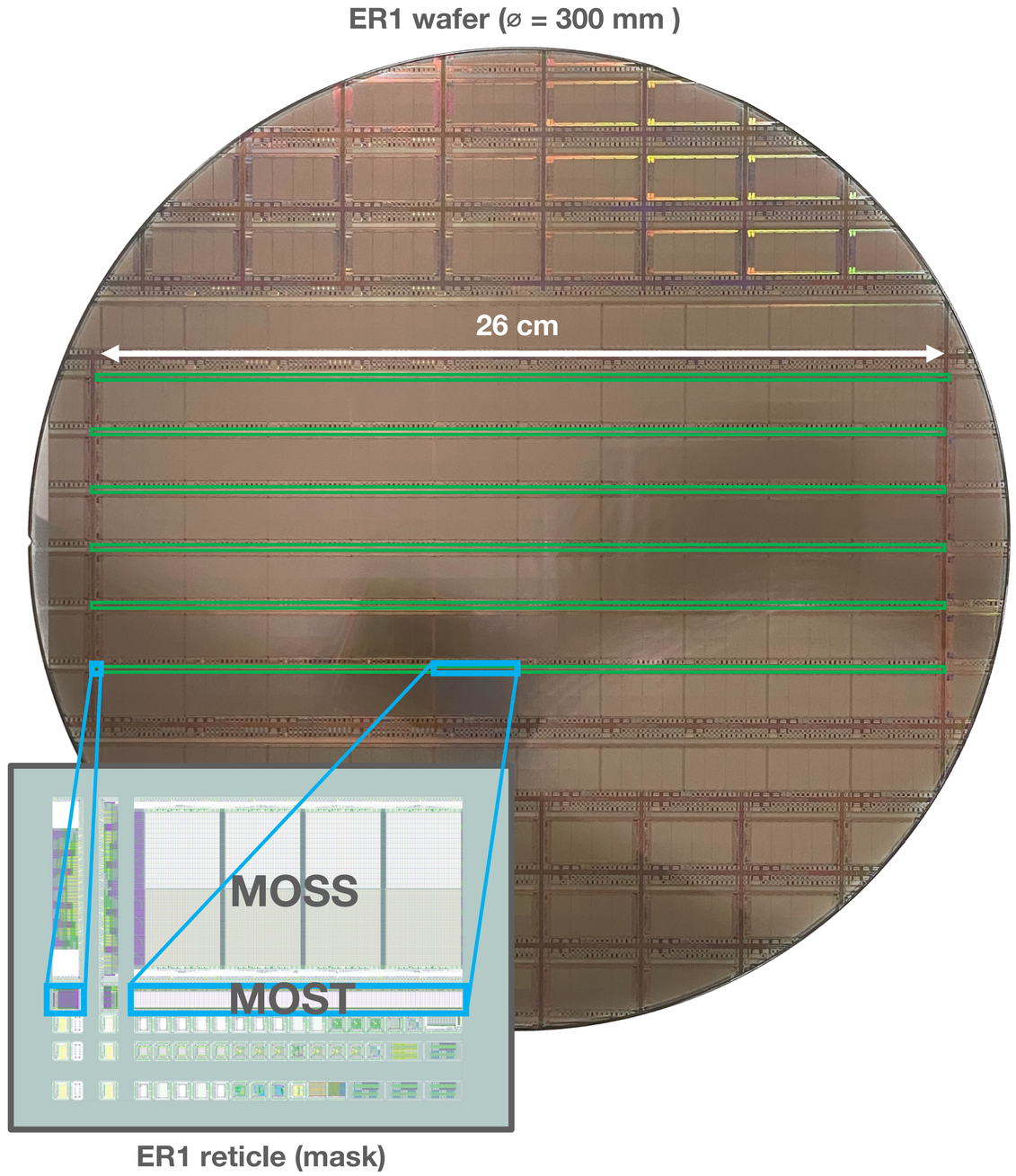
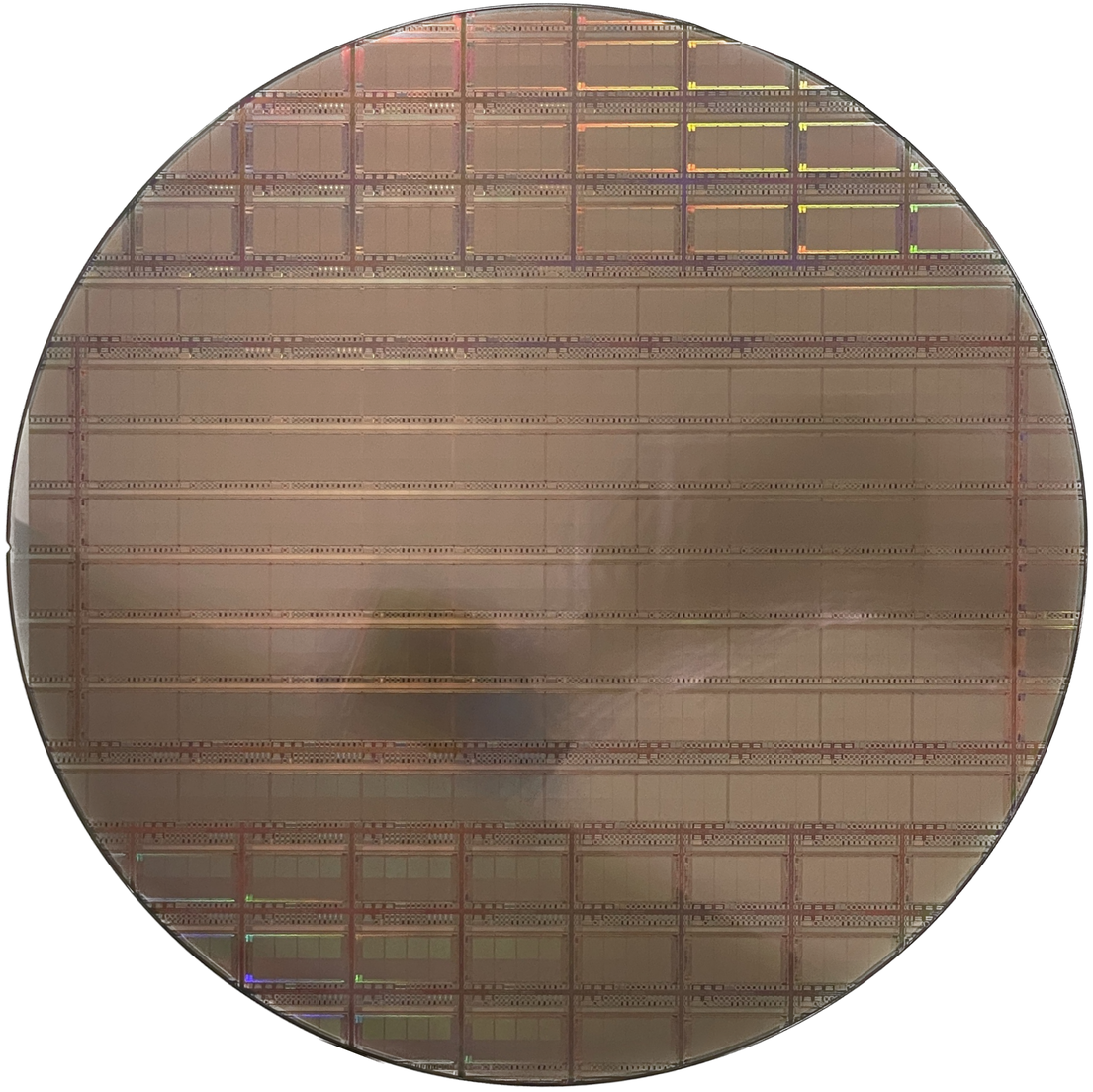


Sensor R&D

Engineering Run 1

Designing **the first wafer-scale MAPS detector for high-energy physics***

- Dedicated design effort:
  - Understanding of “**stitching**” rules
  - Incorporation of **redundancy**, **fault tolerance**
- Crucial exercise to understand:
  - **Yield:** input for granularity of power segmentation
  - **Uniformity**
  - **Power distribution and consumption**
  - **Readout over long distances** (26 cm!)
  - **Pixel architecture**
    (targets: ~5 μm resolution, 10^{13} 1 MeV n_{eq} cm^{-2} (NIEL)

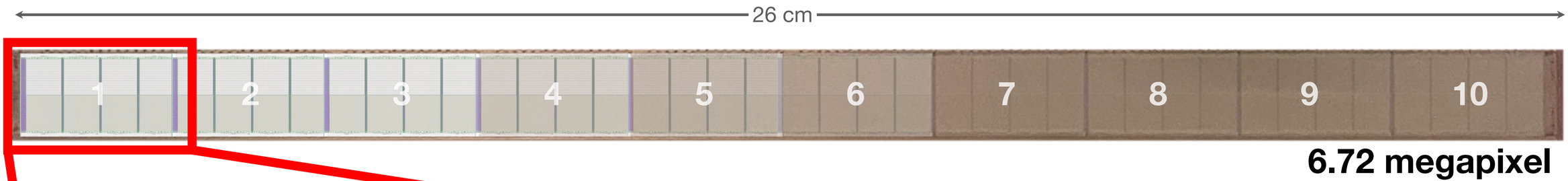


ER1 wafer (⌀ = 300 mm)

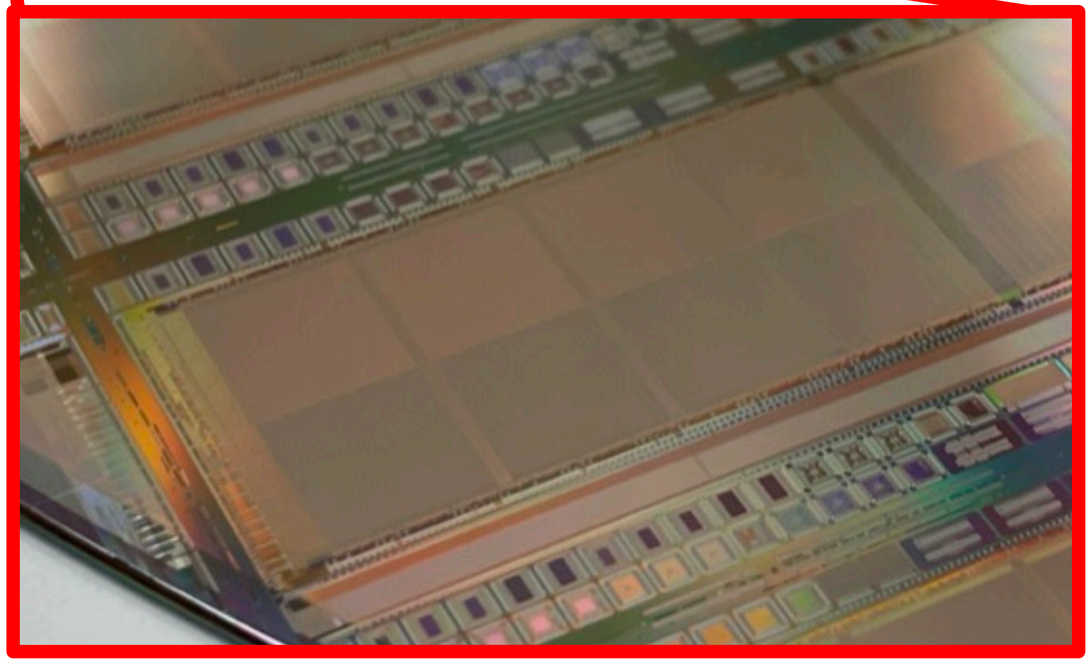
* But not yet the sensor for ITS3

MOSS

MOnolithic Stitched Sensor



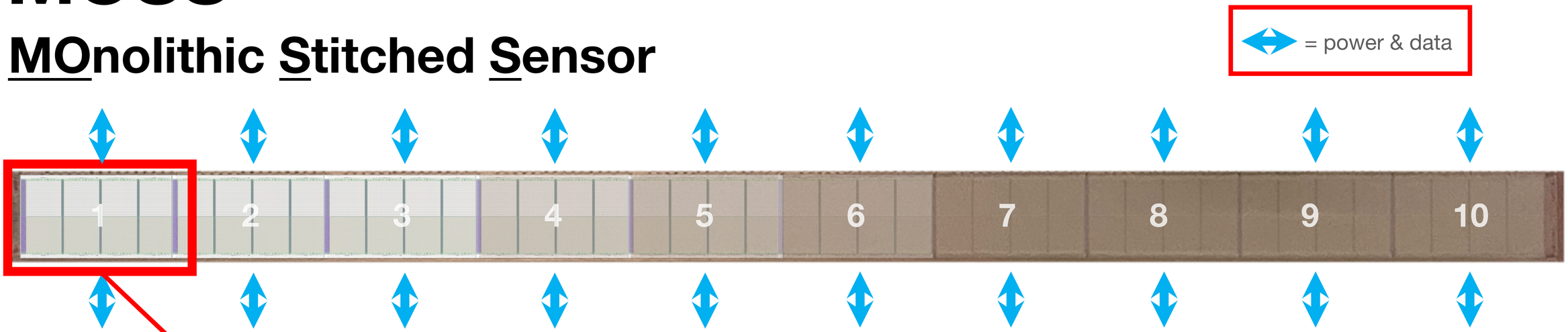
6.72 megapixel

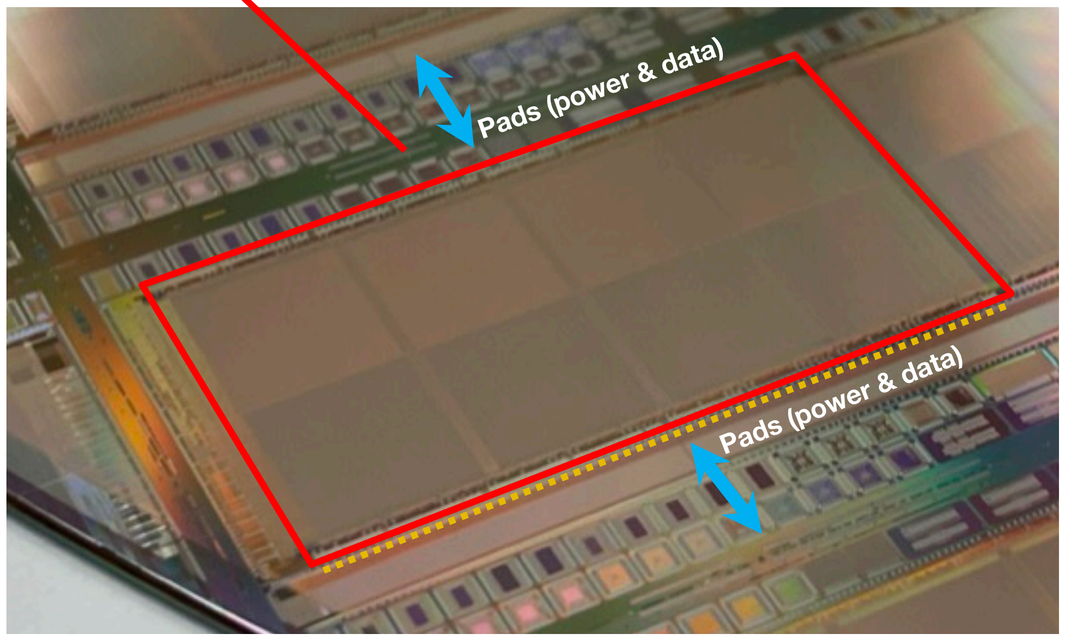


- **10 Repeated Sensor Units** (**RSUs**) per sensor

MOSS

MOnolithic Stitched Sensor

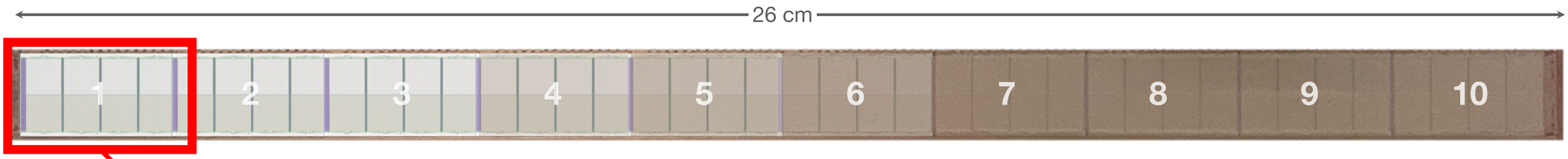


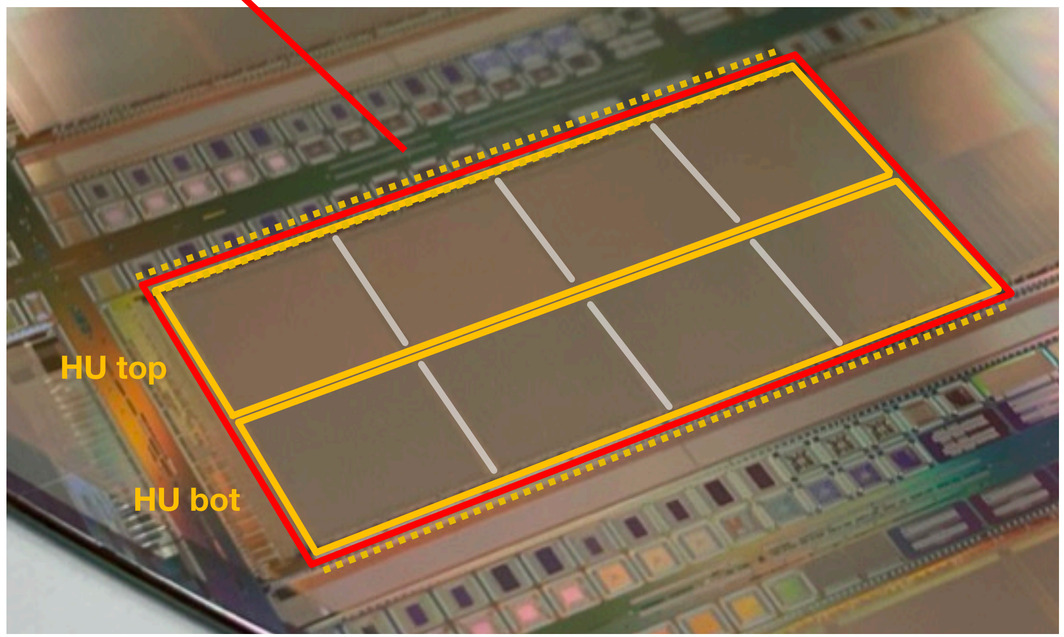


- **10 Repeated Sensor Units** (**RSUs**) per sensor
  - Independent power supply, control & readout

MOSS

MOnolithic Stitched Sensor

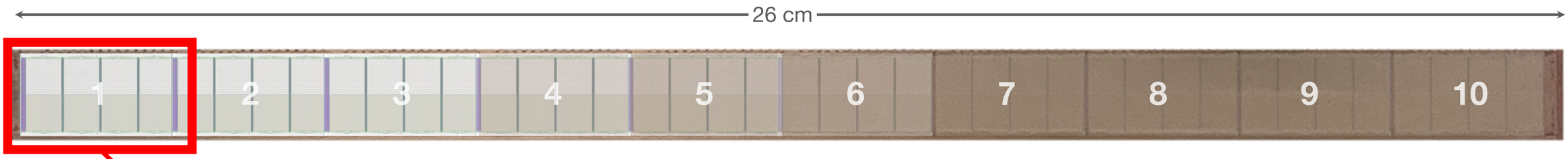


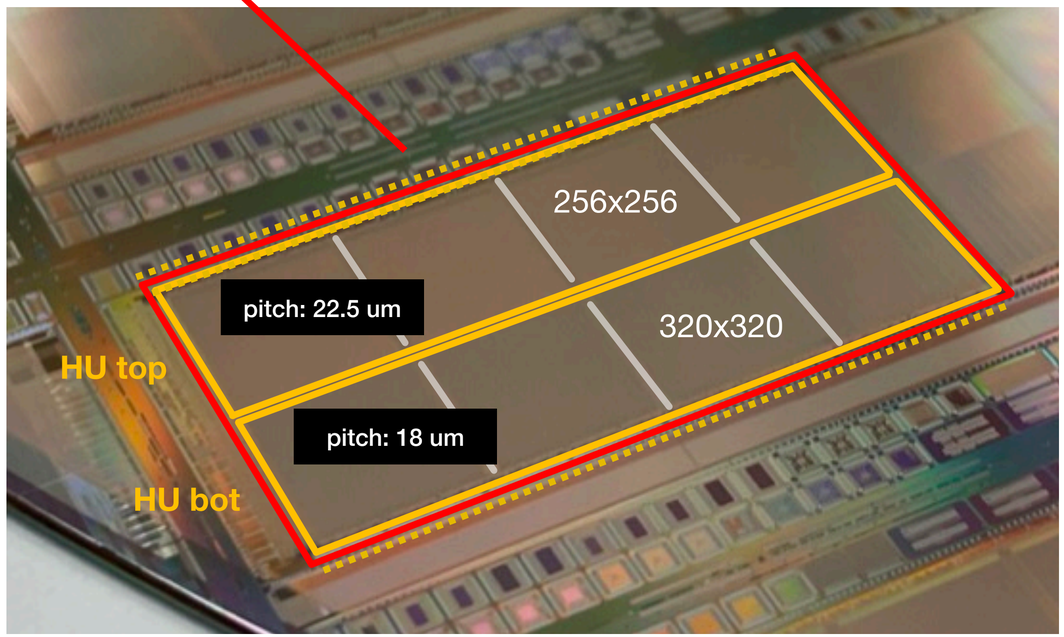


- **10 Repeated Sensor Units** (**RSUs**) per sensor
  - Independent power supply, control & readout
  - **2 half-units** (**HUs**) per RSU

MOSS

MOnolithic Stitched Sensor

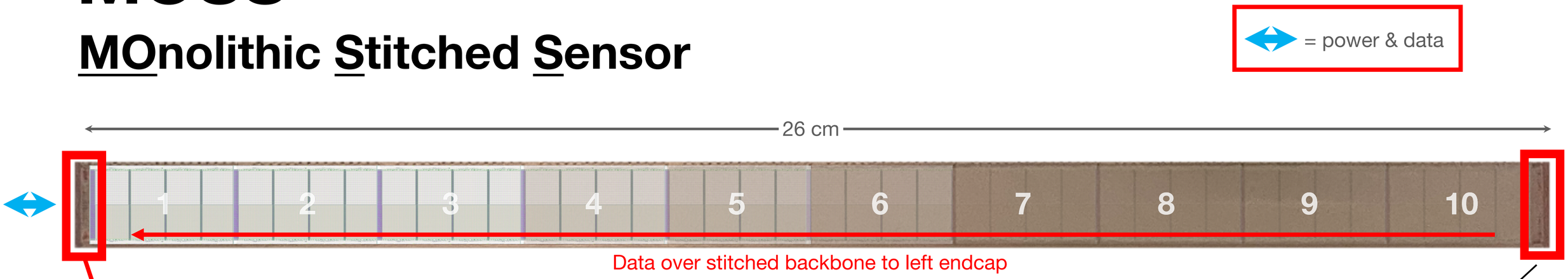


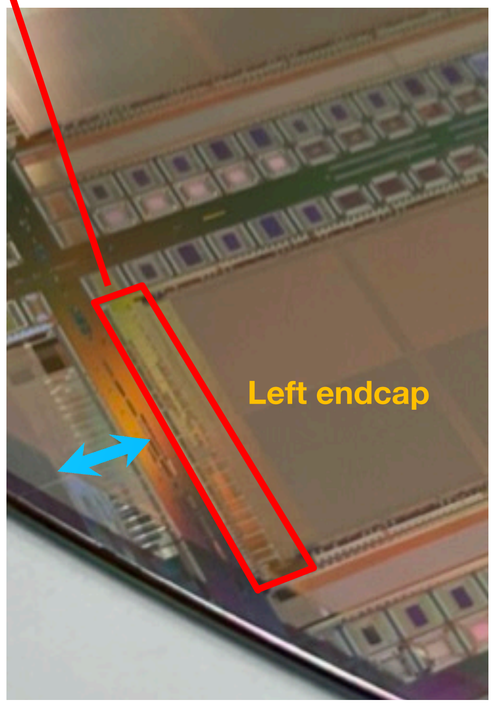


- **10 Repeated Sensor Units** (**RSUs**) per sensor
  - Independent power supply, control & readout
  - **2 half-units** (**HUs**) per RSU
    - Power segmentation domains
    - **Top:**
      - **22.5 um pitch** ← Conservative approach
      - 7 mW/cm^2 (analog FE)
    - **Bottom:**
      - **18 um pitch** ← Compact design
      - 11 mW/cm^2 (analog FE)
    - **4 regions** in each half-unit
    - 8 DACs to bias the analog frontend

MOSS

MOnolithic Stitched Sensor





- **Stitched backbone**
  - CMOS signalling with regeneration **across 26 cm**
  - Capable of **addressing the 10 sensors simultaneously from left endcap**
- **Endcaps**
  - Challenging design on their own!
  - **Left endcap**:
    - Up to 160 Mbps reading one sensor at a time (4-bit bus)
    - Up to 40 Mbps / sensor reading all sensors at once (10x 1-bit buses)
    - Intermediate design: target is 5-10 Gb/s for the final sensor
  - **Right endcap**: power supply only
  - Not for free: **to be accounted for in power budget**

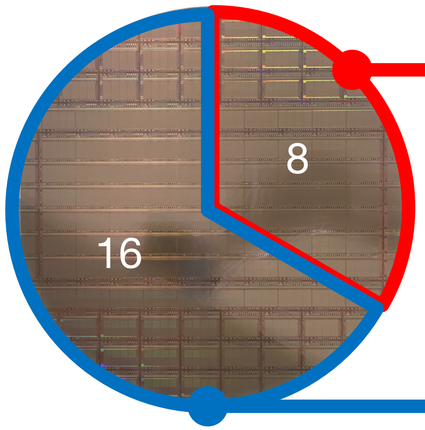
MOSS

Test system requirements & challenges

- **Main goals:**
  - Test all features of the chip
  - Assess manufacturing yield
  - Assess functional yield at half unit, region, column/row/pixel level granularity
- **Main challenge: huge chip!**
  - 259x14 mm^2
  - 6.72 megapixels
  - **2800 pads**
  - 9 power nets per HU
  - **67 power domains**
  - Delicate, needs **mechanical support** in many use cases

MOSS

From wafer to carrier



ER1 production: 24 wafers

Probing

Thinning & dicing

Probing

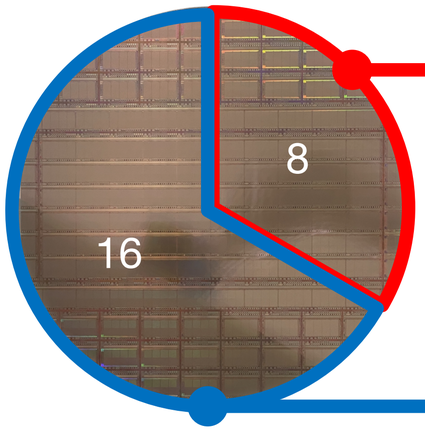
Picking

Glueing

Bonding

MOSS

From wafer to carrier



ER1 production: 24 wafers

Probing

Thinning & dicing

Probing

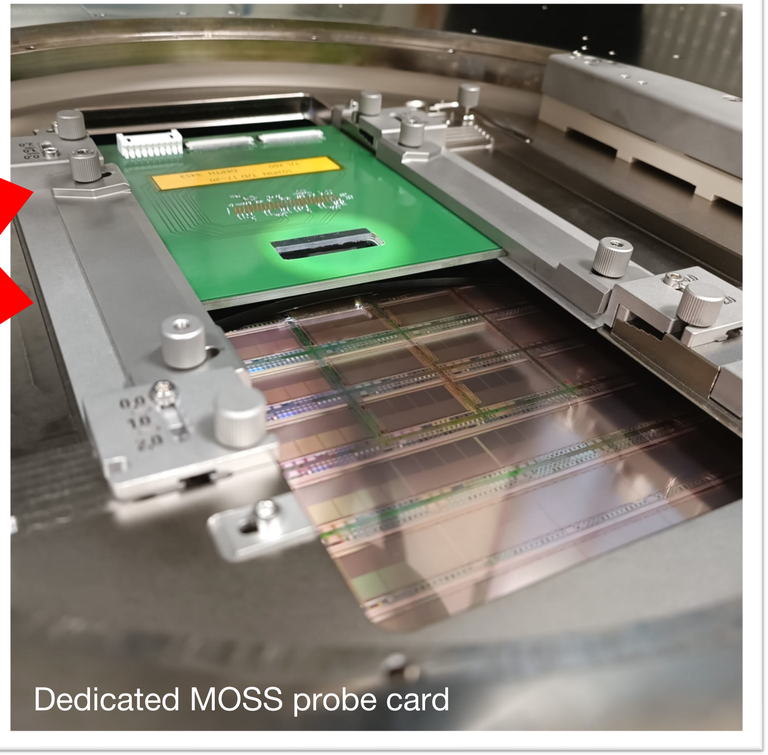
Picking

Glueing

Bonding

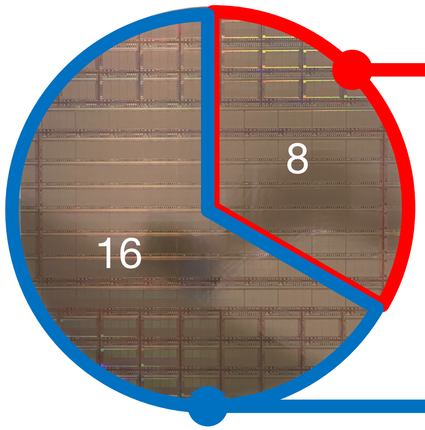
May 11th
First register readback

May 19th
First data readout


Dedicated MOSS probe card

MOSS

From wafer to carrier



ER1 production: 24 wafers

Probing

Thinning & dicing

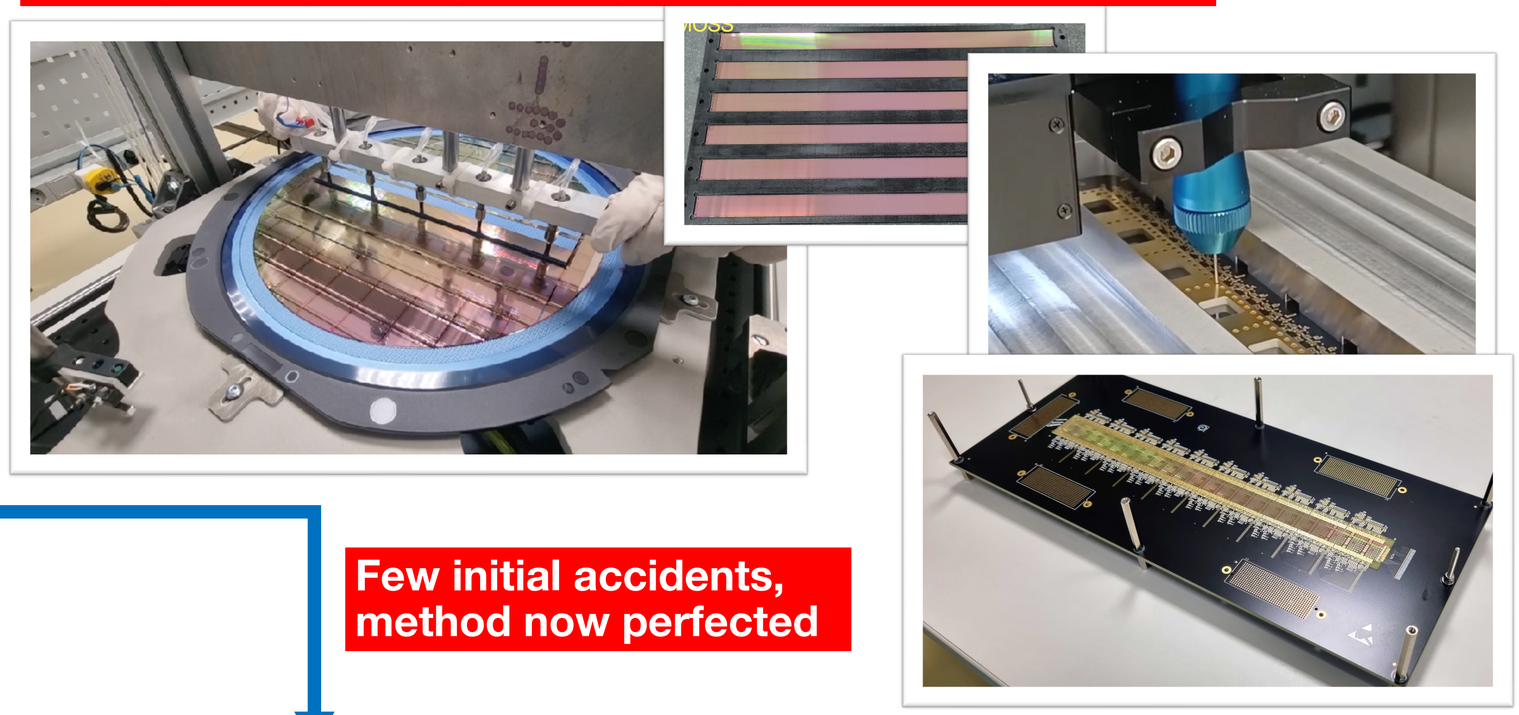
Probing

Picking

Glueing

Bonding

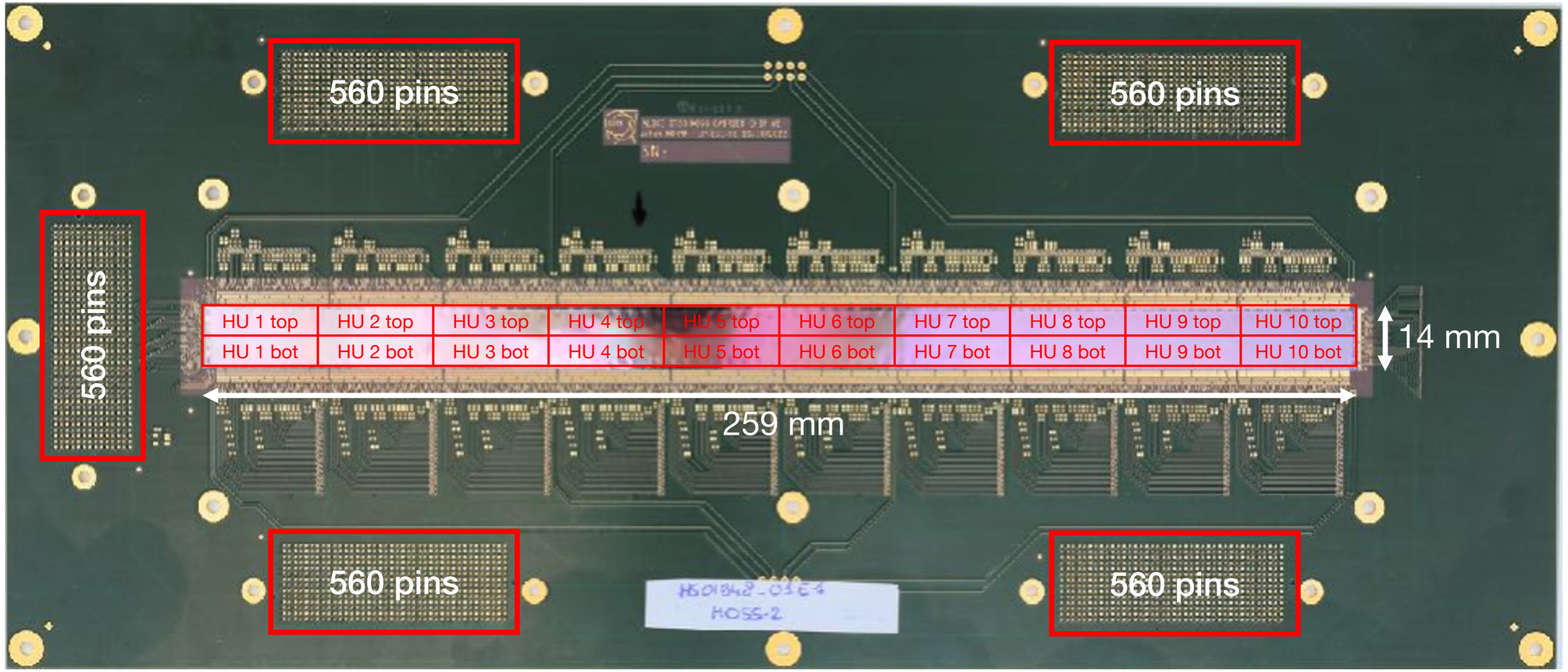
Tools (and expertise!) developed by the ITS collaboration



Few initial accidents, method now perfected

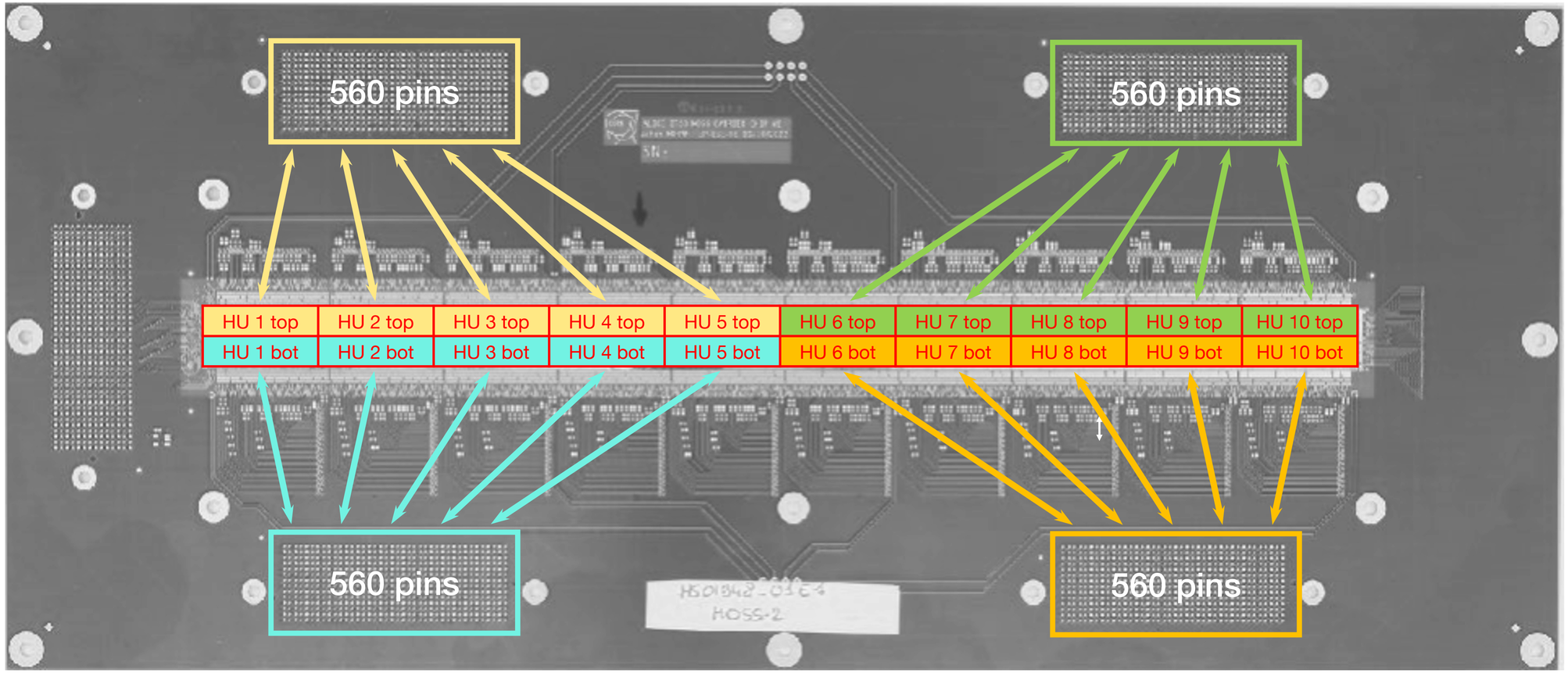
MOSS

Carrier card



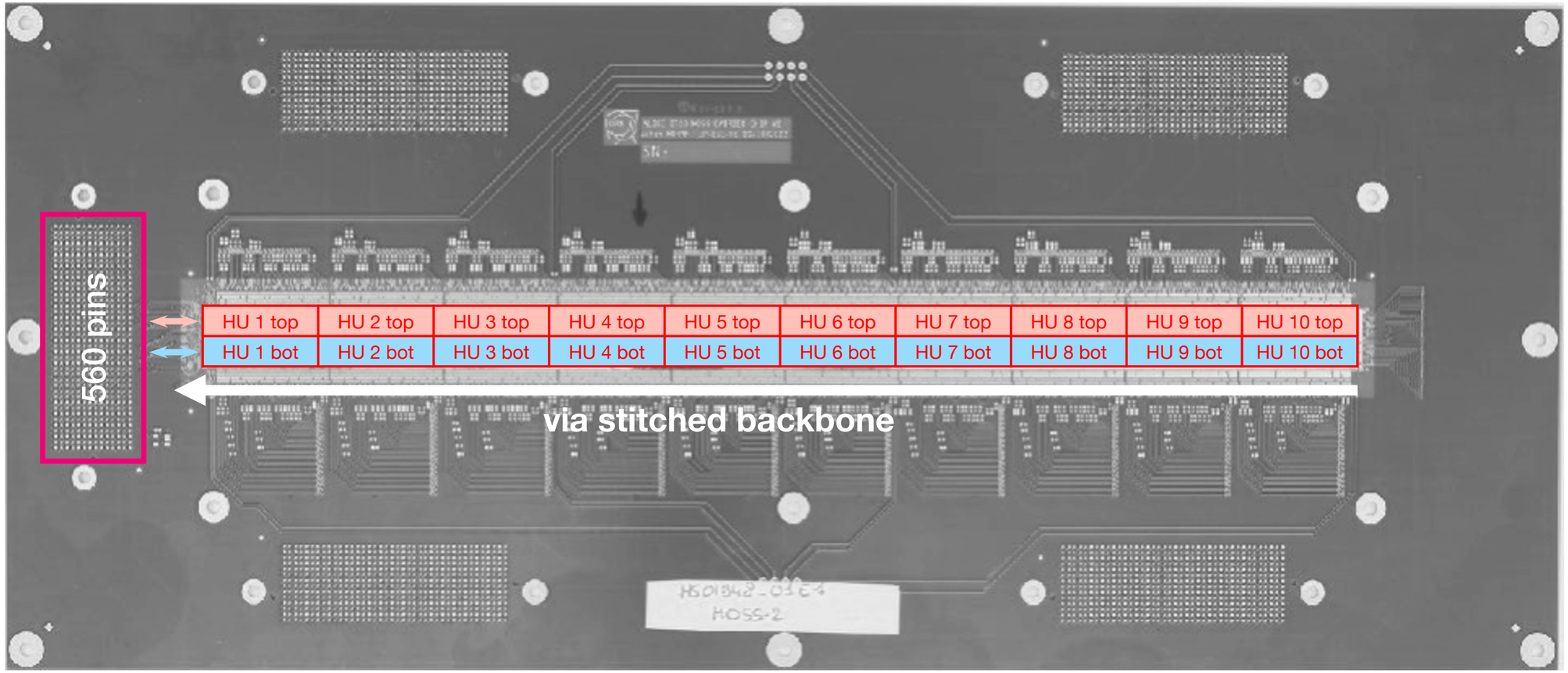
MOSS

Carrier card ↔ sensor long edge



MOSS

Carrier card ↔ sensor short edge

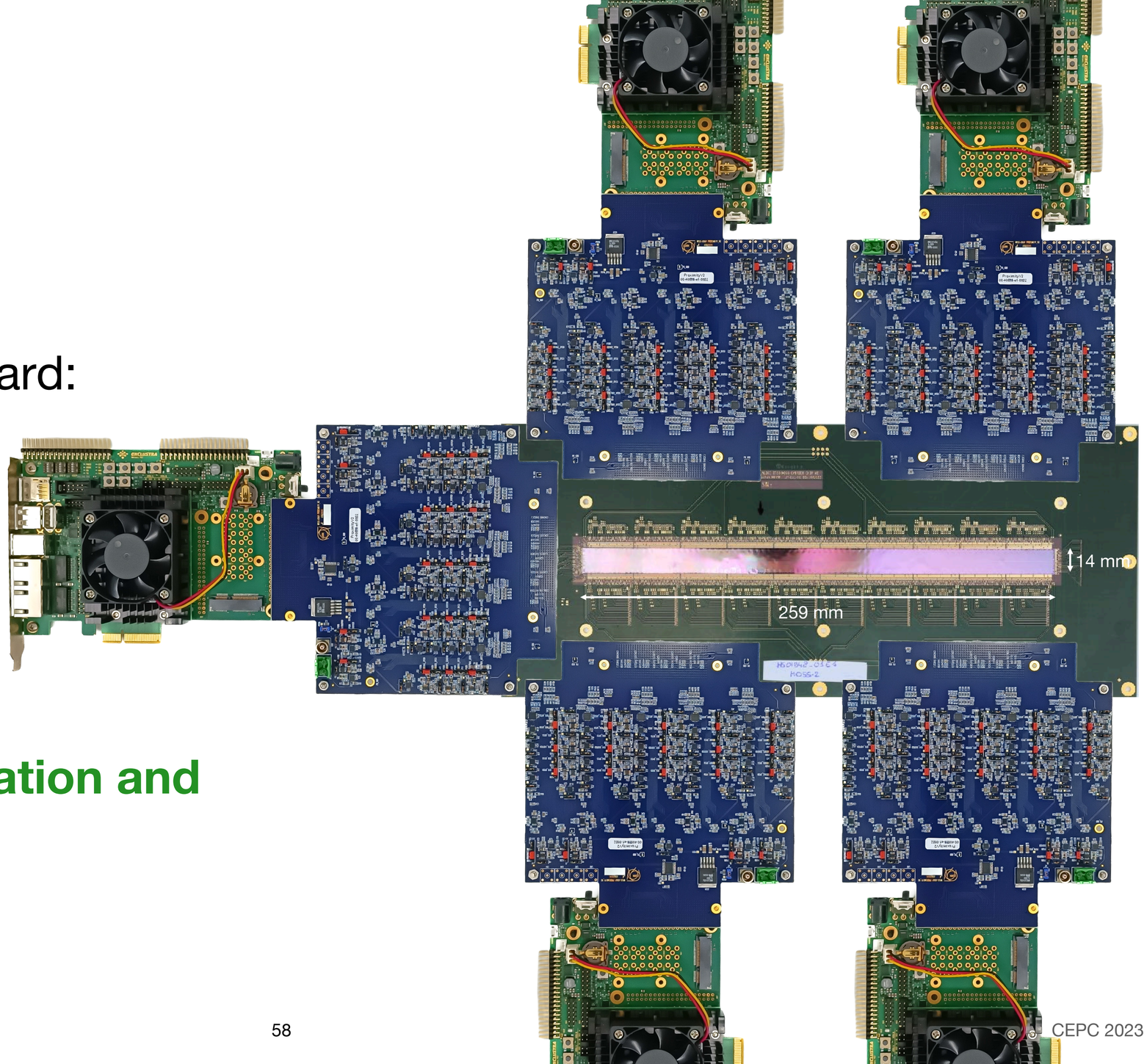


MOSS

Test system

Three different types of board:

- **Carrier card**
- **5x proximity cards**
  - 1 card x 4 quadrants
  - 1 top/bottom halves
- **5x FPGA-based automation and readout modules**



MOSS

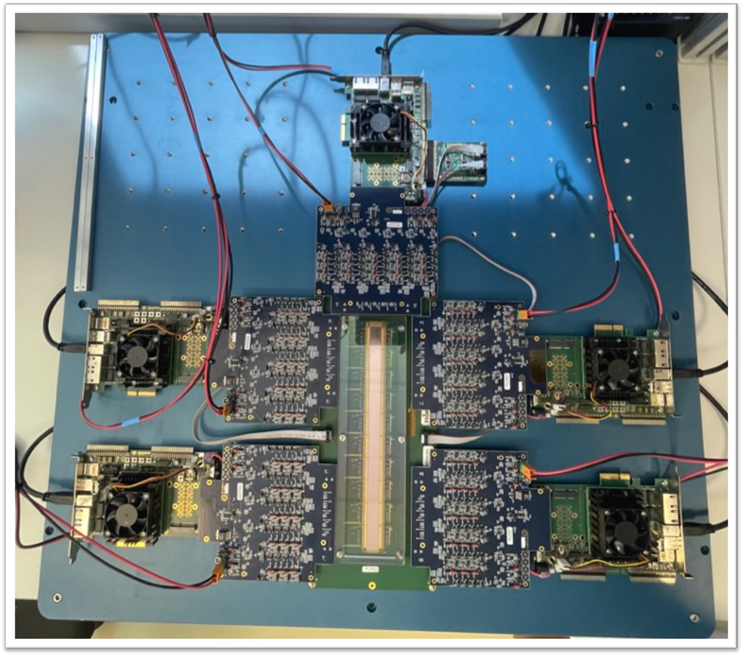
Testing campaign

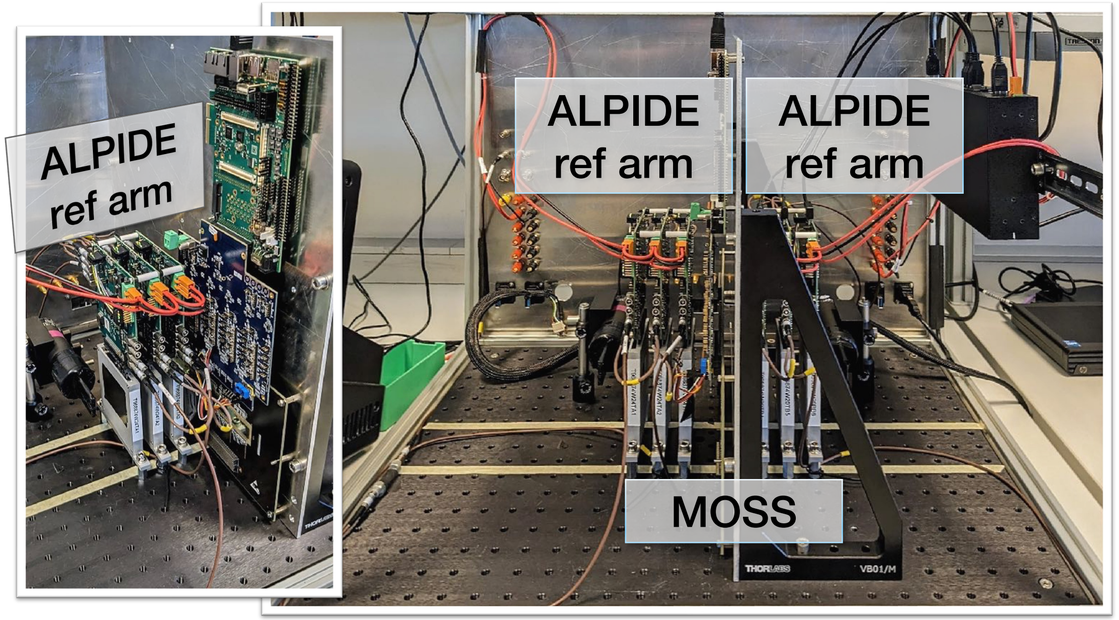
Extensive testing program **ongoing**:

- **Impedance between power nets**: shorts?
- **Power ramps**: how do we power the sensor?
- **Register scan**: reset value check, read/write
- **DAC scan**: linearity
- **Pulsing** (digital, analog)
- **Fe55**
- **Beam test**

24x6 sensors to test: stay tuned!

MOSS test system





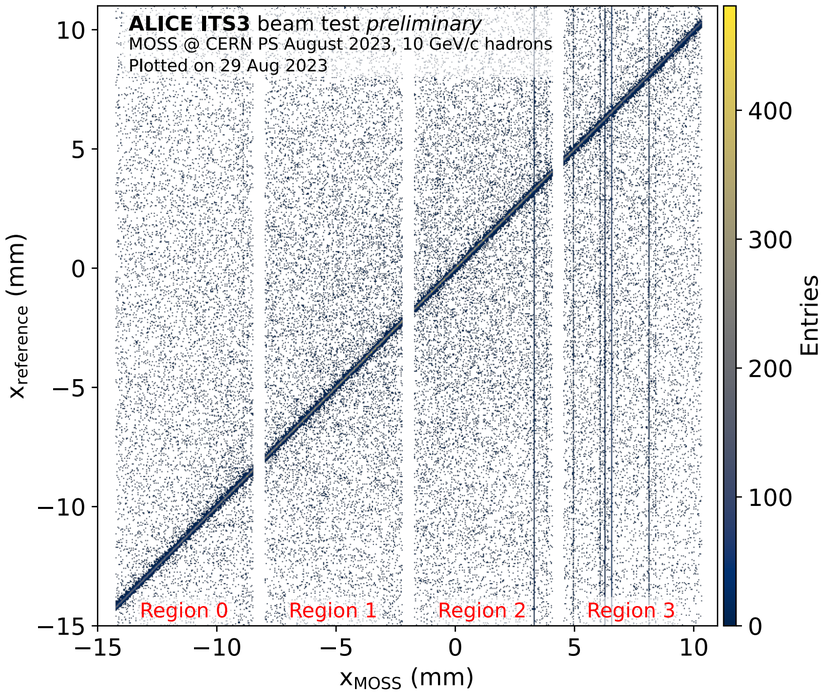
ALPIDE+MOSS telescope

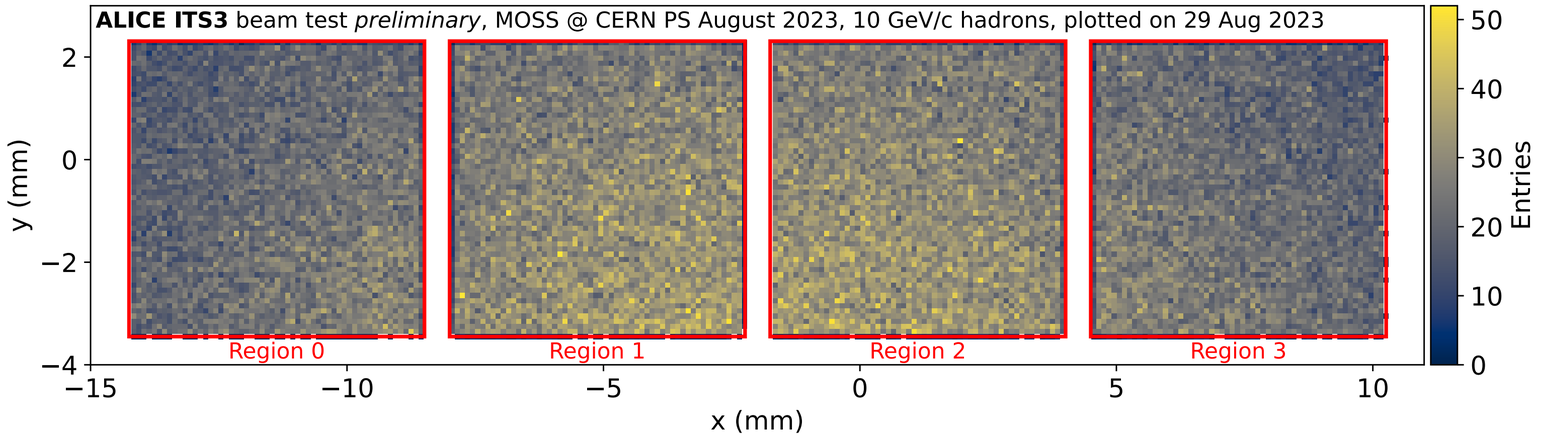
MOSS

Preliminary results

- **16** MOSS successfully **wire-bonded**
- **No failures so far**
  - 40 HUs tested from long edge up to register/DAC scan and fully functional
- **First correlations** from beam test in Jul/Aug/Sep!

Correlations with reference planes





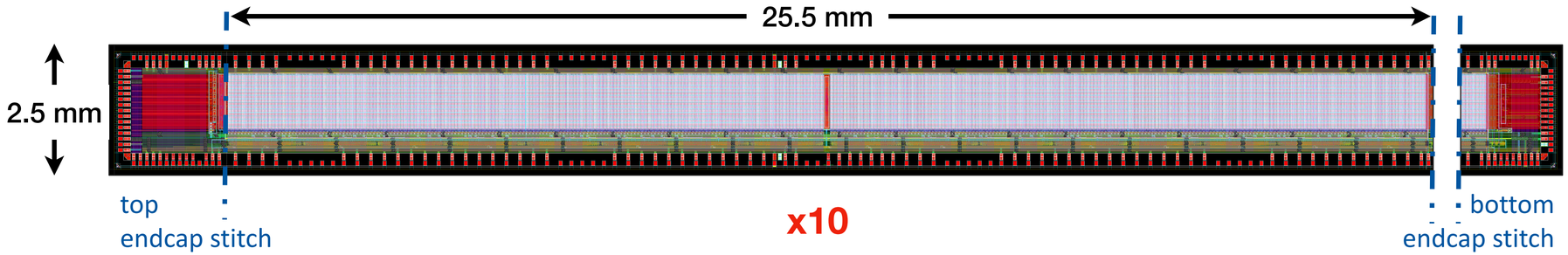
Summary & Outlook
(and thanks for your attention)

- ITS3 upgrade: a **breakthrough cylindrical inner tracker**
- **Three key innovations**
  - **65 nm**: low power & 300 mm wafers (**validated**)
  - **Stitching**: first wafer-scale MAPS sensors for HEP
  - Thinning and **bending**
- **ER1** (**now testing!**): first stitched sensors
  - **Goal: asses the yield** of wafer-scale stitched sensors
  - Testing started with **promising results**
- **Next steps**
  - Full characterisation of MOSS & MOST (yield, pixel performance...)
  - **ER2** (prototype of the final sensor, 2024) and **ER3** (final ASIC, 2025)

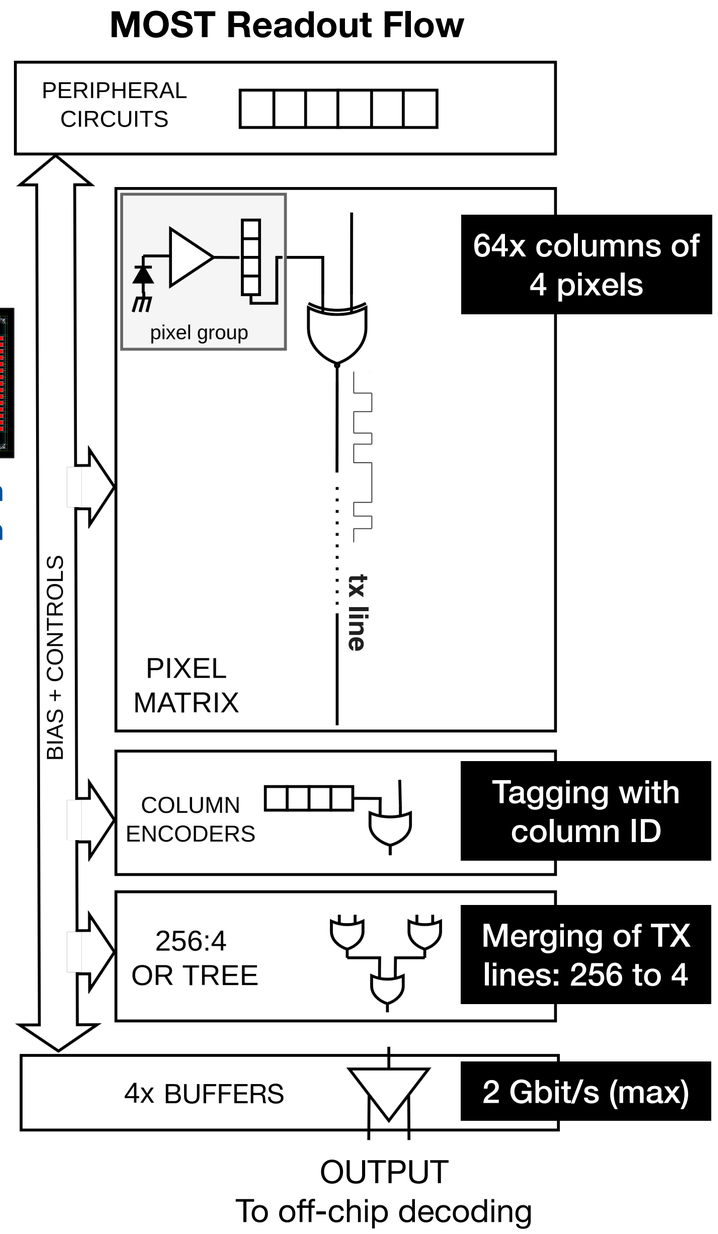
Backup

MOST

MOnolithic Stitched sensor with Timing

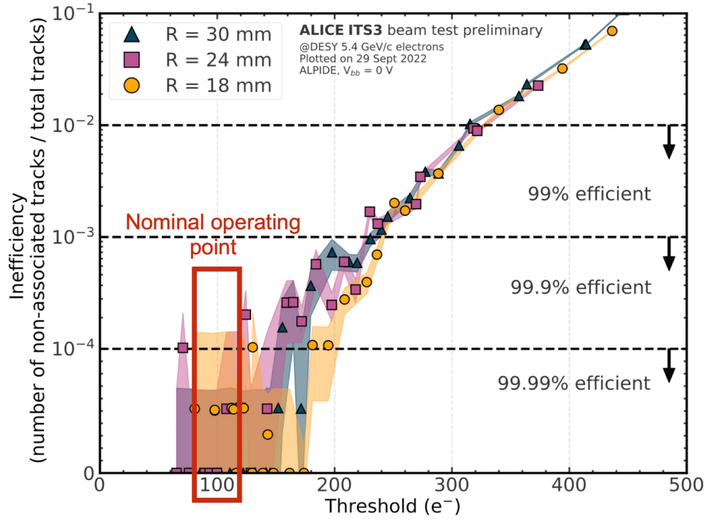


- **Event-driven, asynchronous readout (data time stamp → ToA and ToT)**
- **Global power net with finer power segmentation**
- **Pros:**
  - reduced dead-area (readout is distributed in active matrix area)
  - no strobing, no clock distribution: more power-efficient for low hit-rates
- **Cons:**
  - Asynchronous decoding off-chip @ up to 2 Gbit/s (more development)
  - Asynch sharing of tx lines -> hit data packets might collide @ high hit rates (data loss)



ITS3 R&D - Silicon bending

» Laboratory and test beam measurements (Jun 2020) allow to conclude that **chip (180 nm CMOS) performance doesn't change after bending**
- Pixel matrix threshold distribution does not change when sensor is bent
- Efficiency above 99.9% at a threshold of 100 e^-



Credits:

ITS3 R&D - Carbon foam properties

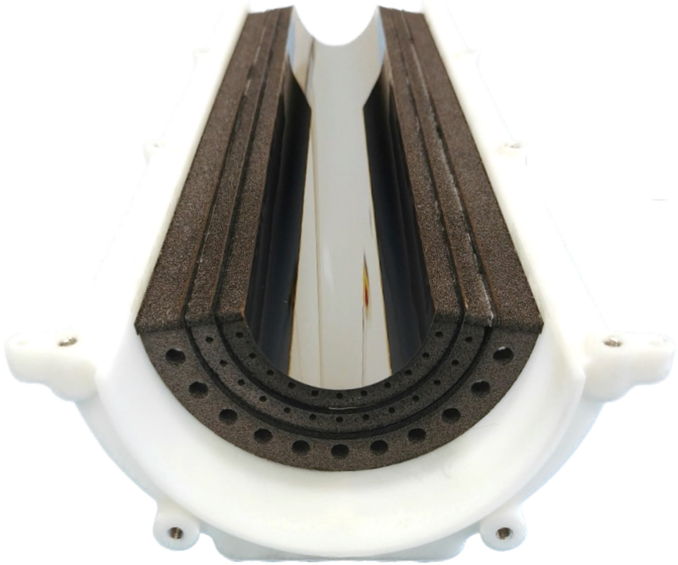
» Silicon sensor kept in position by:

Longerons
Support structures

ERG Duocel (RVC)

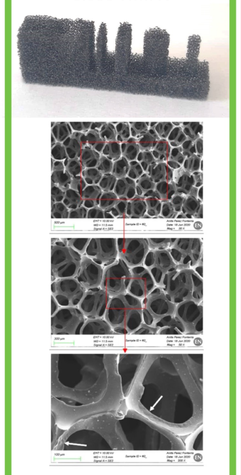
Half-rings
Support structures and cooling radiator

ALLCOMP LD (K9)

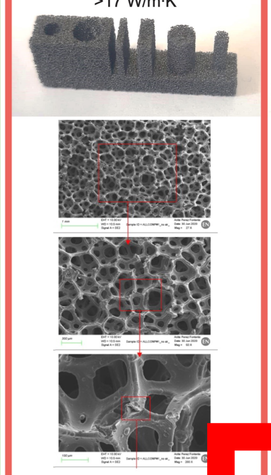


» Carbon foams characterised for machinability and thermal properties

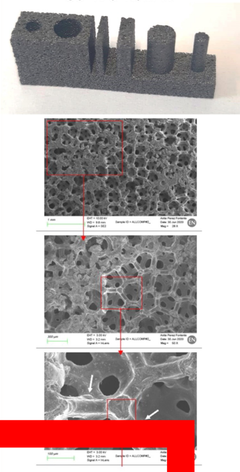
ERG DUOCEL (RVC)
0.06 kg/dm³
0.033 W/m·K



ALLCOMP LD (K9)
0.2-0.26 kg/dm³
>17 W/m·K



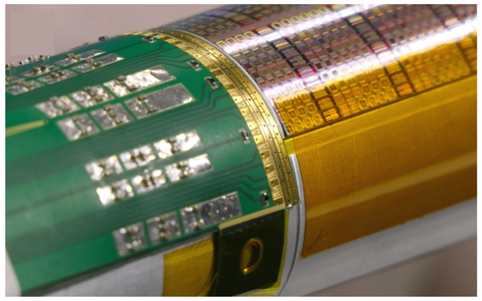
ALLCOMP HD
0.45-0.68 kg/dm³
85-170 W/m·K

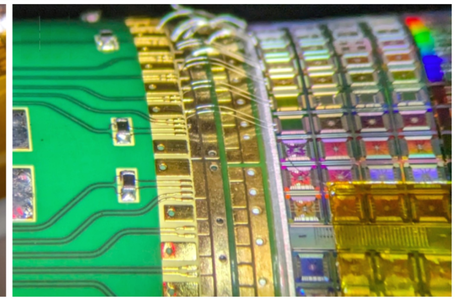


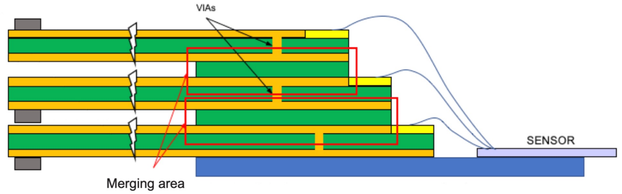
Credits:

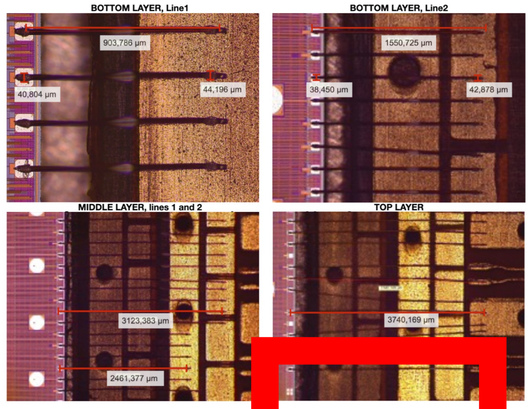
ITS3 R&D - Interconnection

» Flexible printed circuits for communication and powering
- placed outside the sensible area
- three double copper layers flex, multi-strip shaped (15-30 cm long), connected in a merging area
- **interconnected via wire-bonding** at the edge of the sensor **verified**
  - wire-bonds loops optimisation based on pull-force measurements
  - present setup (not final grade material): 6.6±0.3 g at ~900 µm pad-to-pad distance





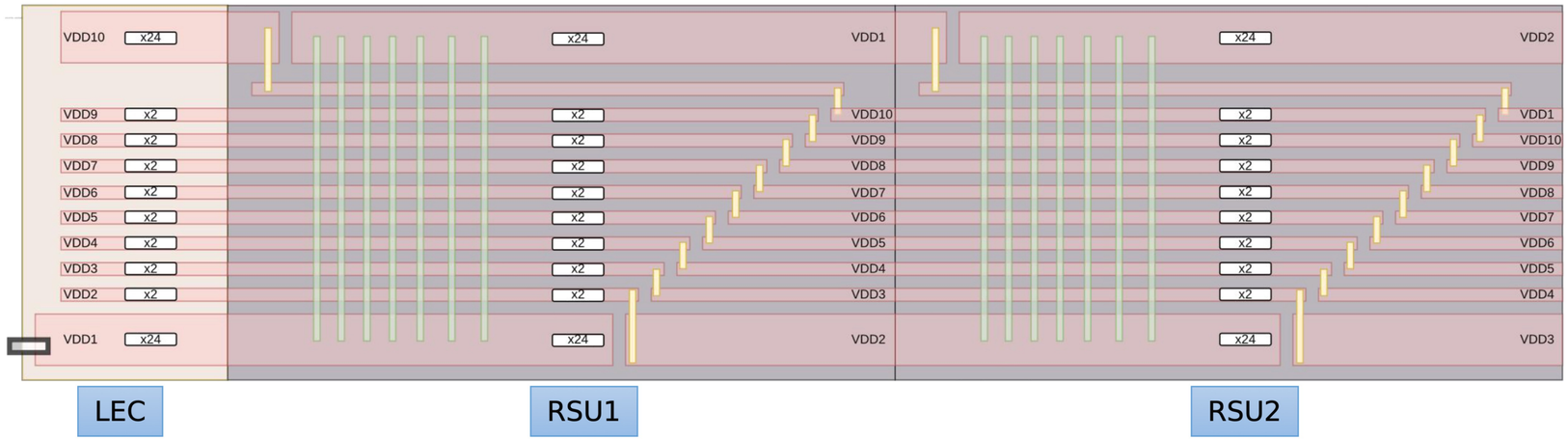




Credits:

MOSS Power distribution

Powering & monitoring from the short-edge (example for VDD)



With the same physical RSU, it is necessary to forward power from the short edges to the most far RSUs

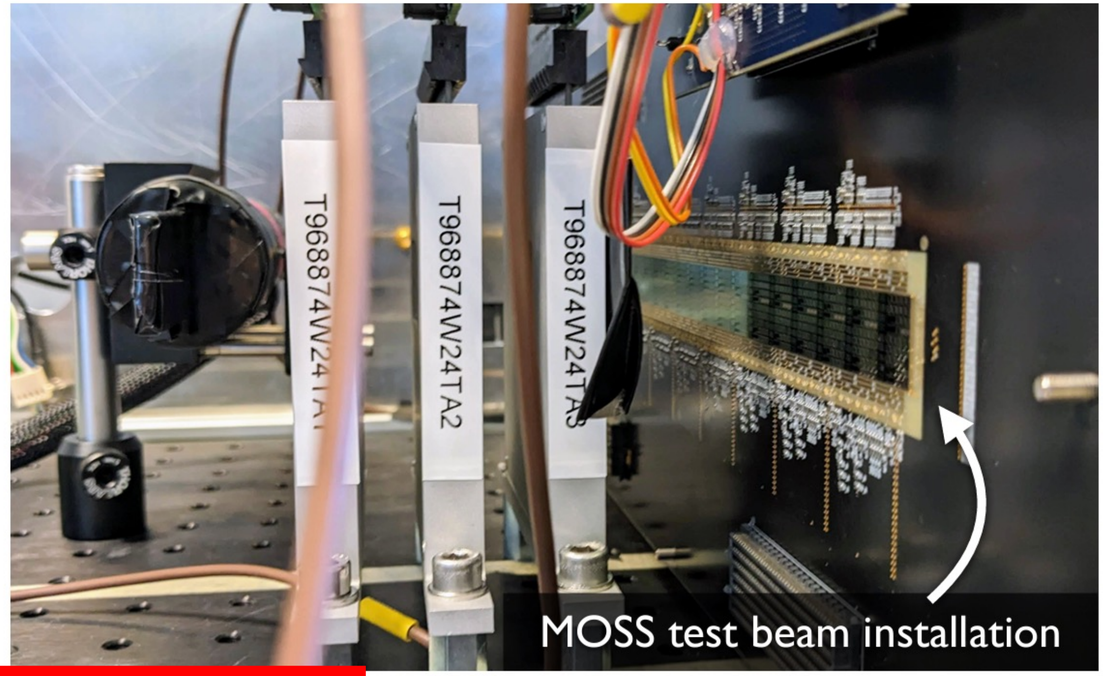
We achieve this by performing *line-hopping*

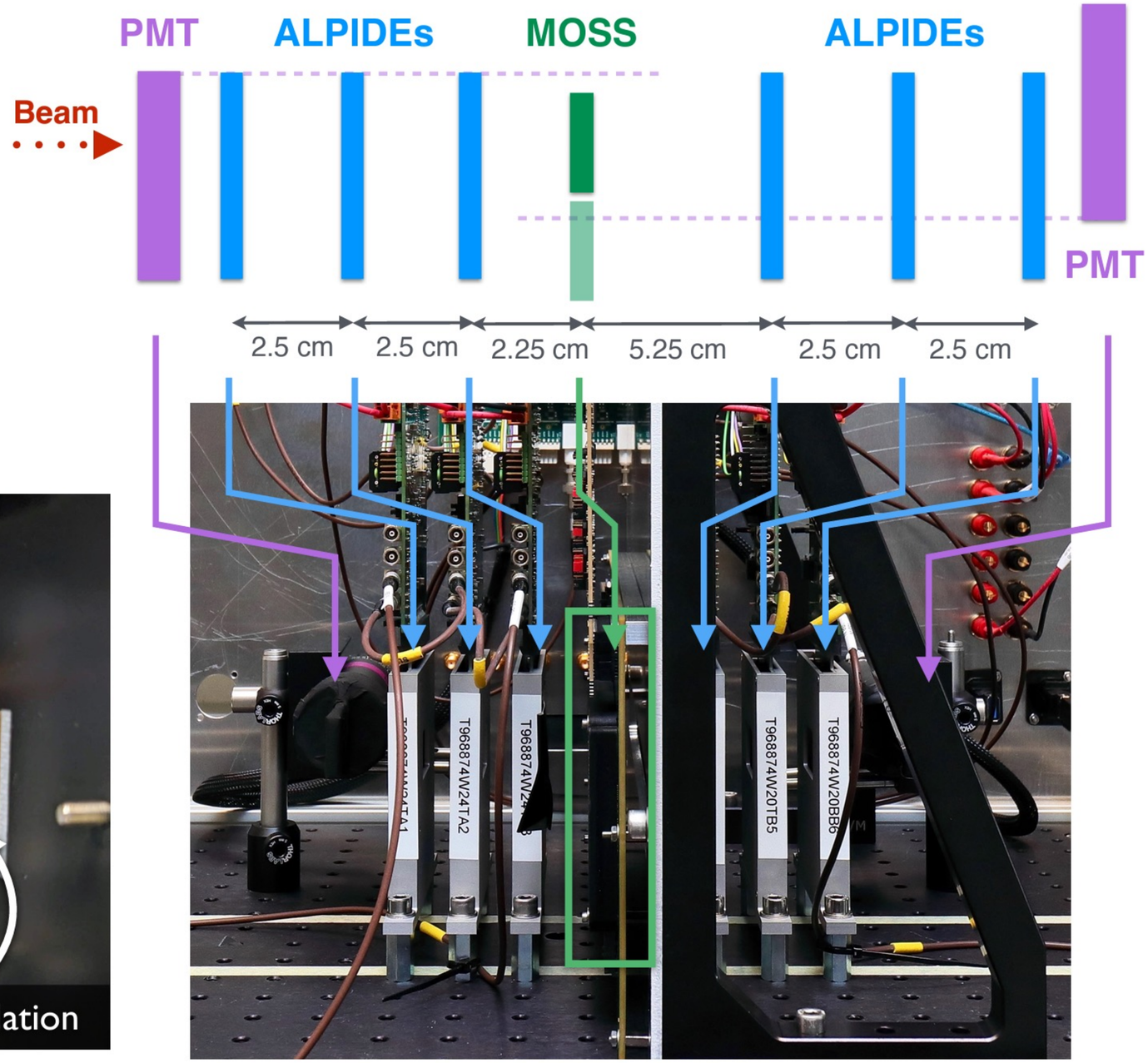
For the MOSS prototype, the current metal stack only allows to power the most left (RSU1) or most right RSU (RSU10). All the other power pads are only used for *monitoring* in order to verify the stitching. More on the backup slides.

Credits:

Test Beam Setup – MOSS

- T10@PS: 10 GeV negative hadrons
- Examined 1x MOSS HU in beam
- 6x ALPIDE reference planes
- Trigger: 2 PMTs in coincidence





Slide credits: Jordan Lang
Valerio Sarritzu

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