Silicon Detector Technologies for the IDEA Tracker

2023 international Workshop on the high energy Circular Electron Positron Collider (CEPC)

23-27 October 2023

Riccardo Zanzottera - Università di Milano and INFN

For the RD_FCC Silicon Tracker community

(COMO, GENOVA, MILANO, PADOVA, PERUGIA, PISA, TORINO)

UNIVERSITÀ DEGLI STUDI DI MILANO
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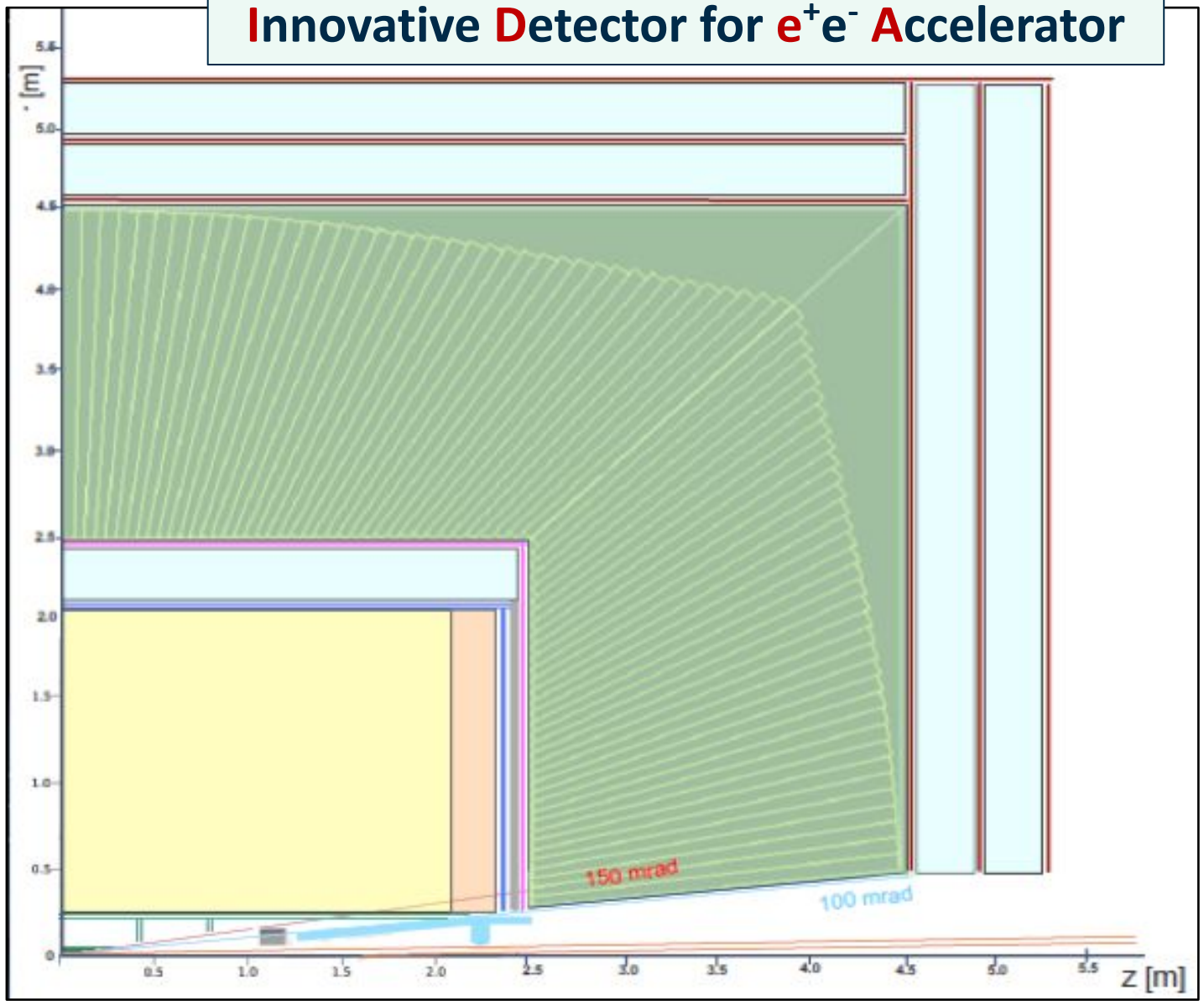
The IDEA Concept

Innovative Detector for e^+e^- Accelerator

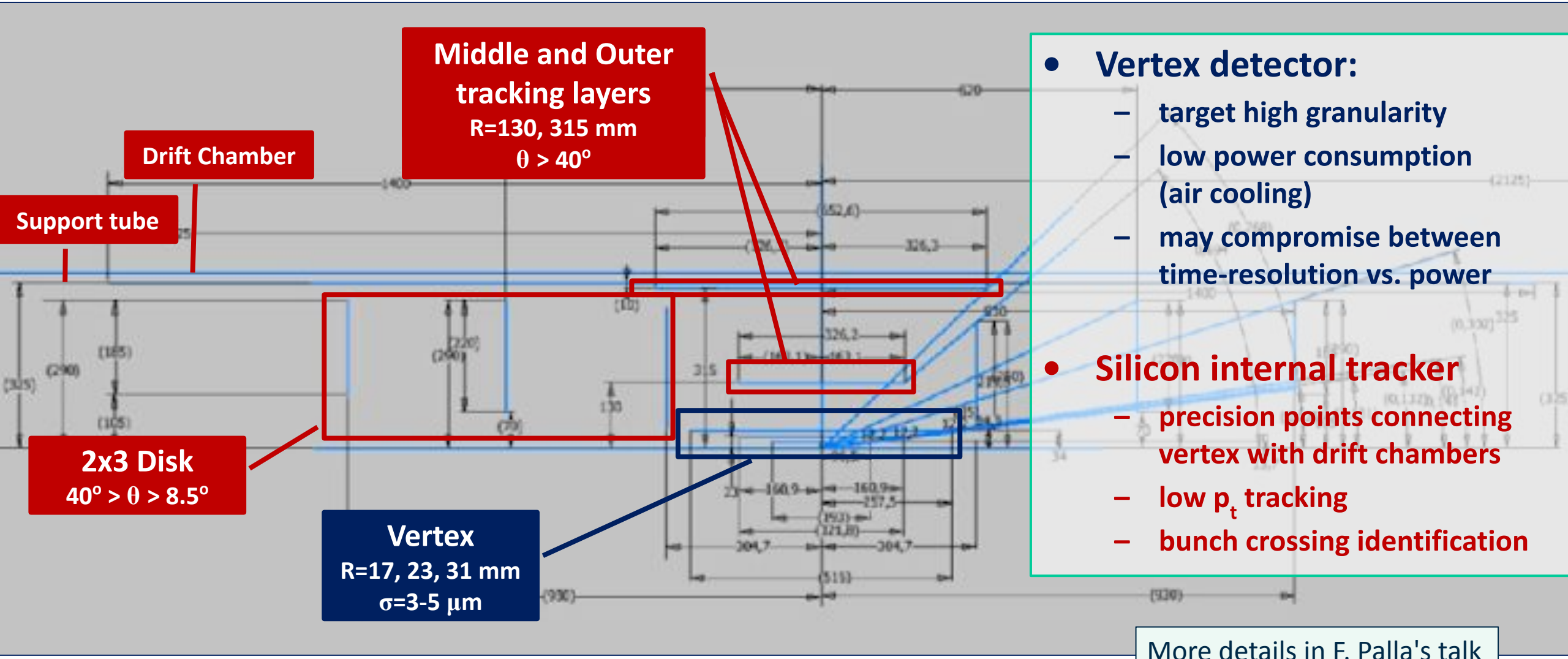


- Central tracking device:
  - light Drift Chamber

    N. De Filippi's talk
- **Silicon detectors for precision measurements**
  - **vertex detector**
  - **silicon internal tracker**
  - **silicon wrapper/TOF**
- Thin solenoid with 2T field (according to MDI limits)
- Dual readout calorimeter
  - supplemented by a pre-shower detector

    R. Ferrari's talk
- Muon chambers in the solenoid return yoke

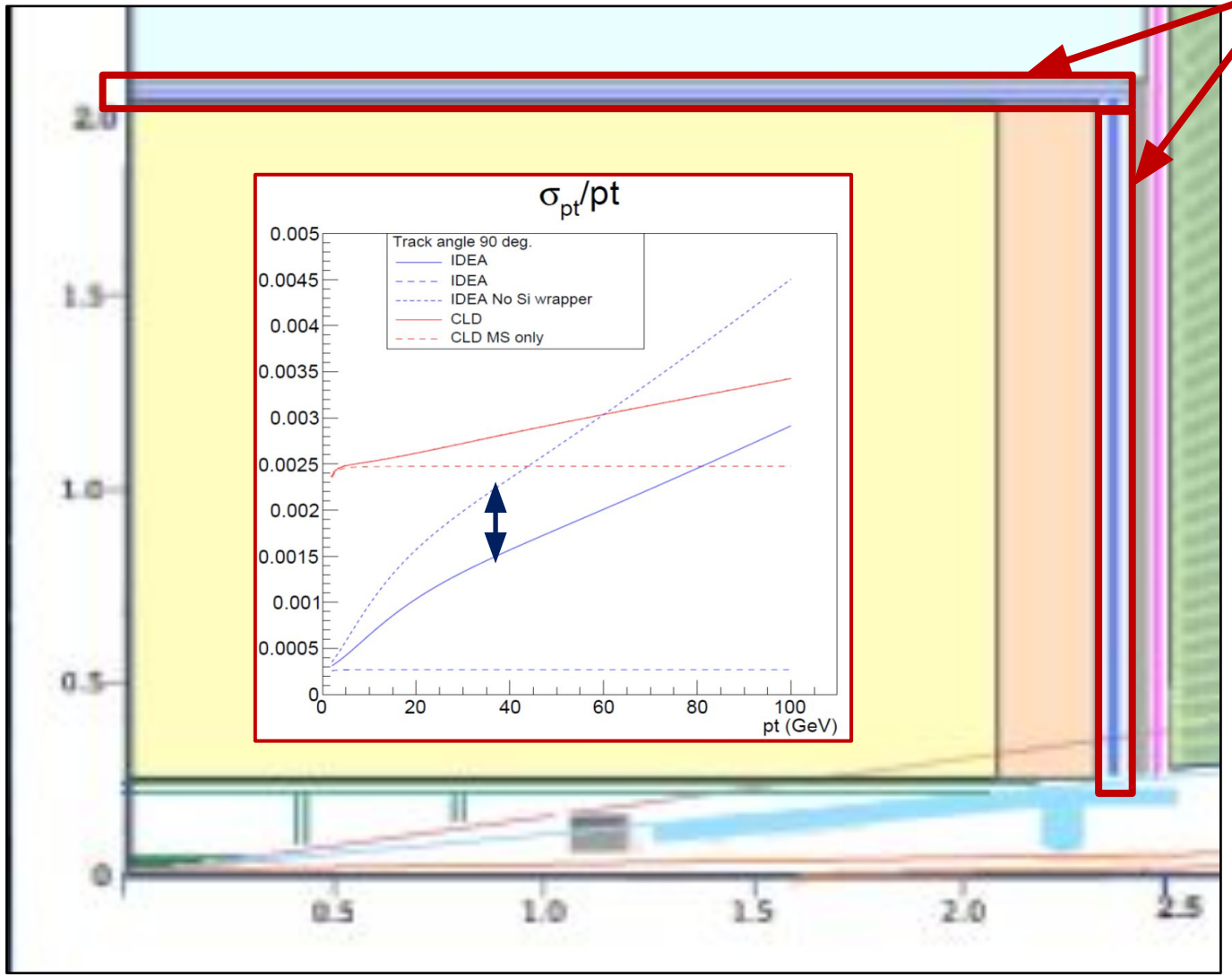
The IDEA Concept: inner tracking



- **Vertex detector:**
  - target high granularity
  - low power consumption (air cooling)
  - may compromise between time-resolution vs. power
- **Silicon internal tracker**
  - precision points connecting vertex with drift chambers
  - low p_t tracking
  - bunch crossing identification

More details in F. Palla's talk

The IDEA Concept: Si Wrapper



- **Precision silicon layer around the central tracker**
  - **improve momentum resolution**
  - **extend tracking coverage in the forward/backward region**
    by providing an additional point to particles with few measurements in the drift chamber
  - precise and stable ruler for acceptance definition
  - *it may provide TOF measurement*

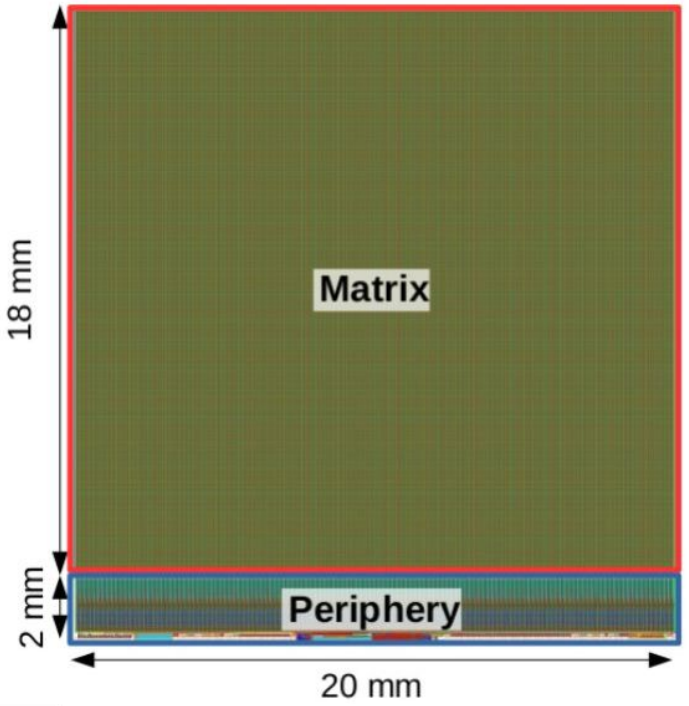
- Covered area ~90 m^2
  - important impact on services
  - technology suitable for large size production

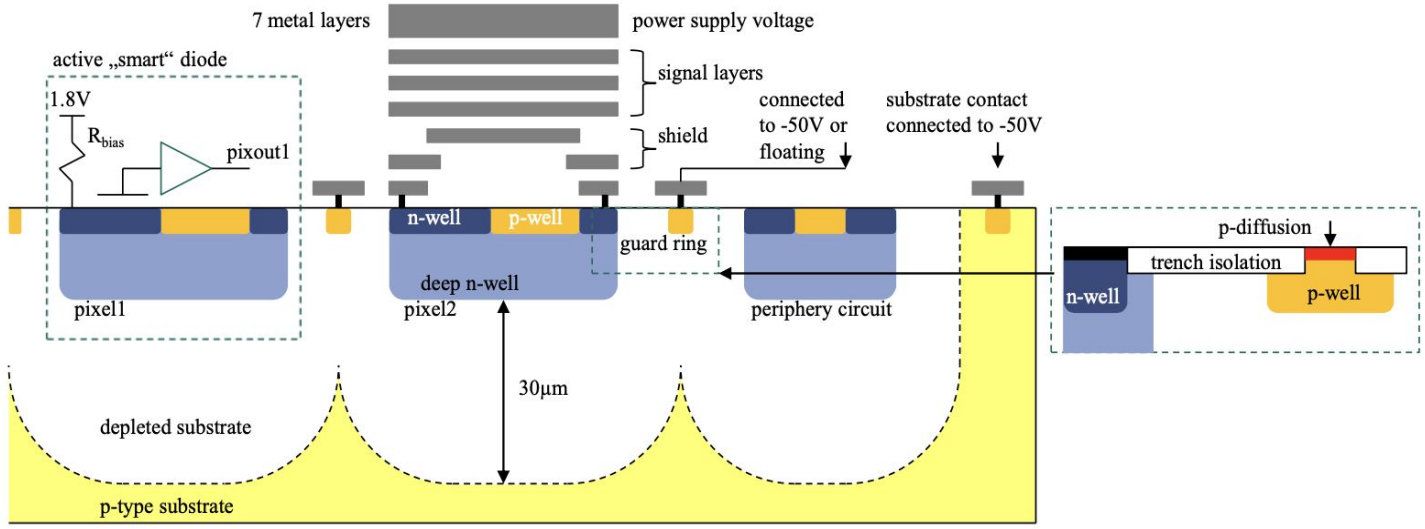
Si Detector Technologies

- Focus on **depleted monolithic CMOS detectors**
  - High-Voltage/High-Resistivity CMOS processes commercially available
  - CMOS Foundries are able to produce large volume of detectors at a convenient price
  - Depleted region provide fast rising and "high-amplitude" signals
  - No need of the complex and costly interconnection technique used in hybrid detectors
- Two technologies presented in this talk:
  - **ATLASPIX3** – KIT, China, INFN, UK collaboration
    - full reticle size detector, implementing most features needed for deployment in the **Internal Tracker and Si Wrapper**
  - **ARCADIA** – INFN/LFoundry driven development, collaborations with PSI
    - fully depleted sensors, with high granularity and low power consumption for the **Vertex Detector**
    - more detail in D.Falchieri's talk
- **Resistive Silicon Detectors**, with **tens of ps time resolution** are considered as an opportunity for the Silicon Wrapper
  (showing results from Torino, Trento, Perugia and FBK collaboration)

ATLASPIX3 Detector

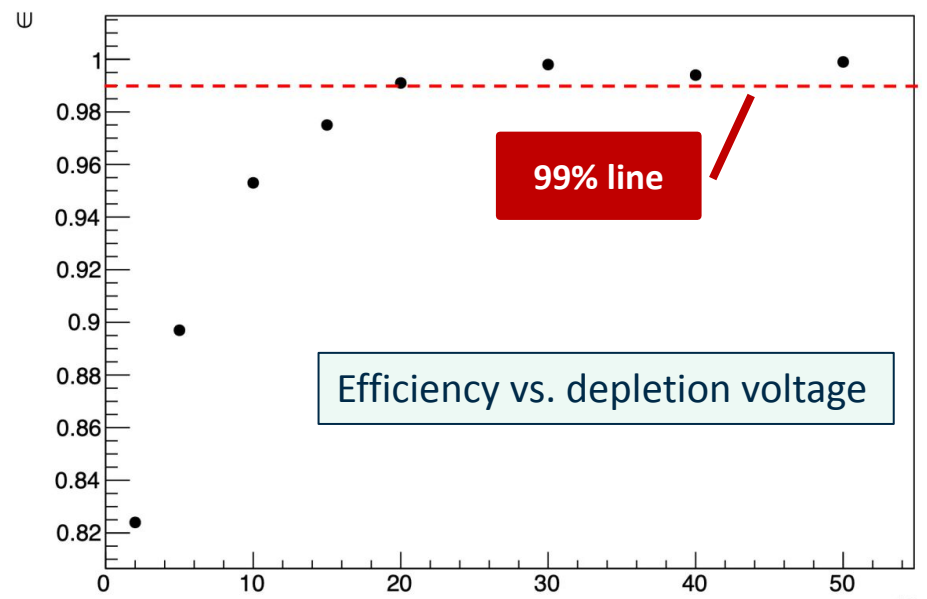
- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ∼-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout

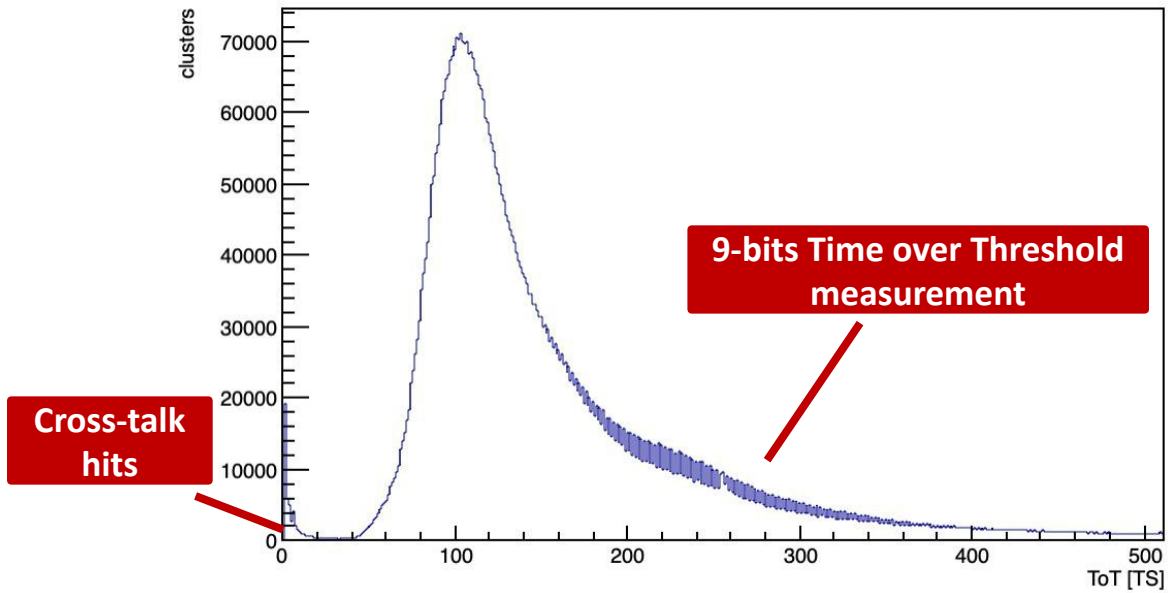


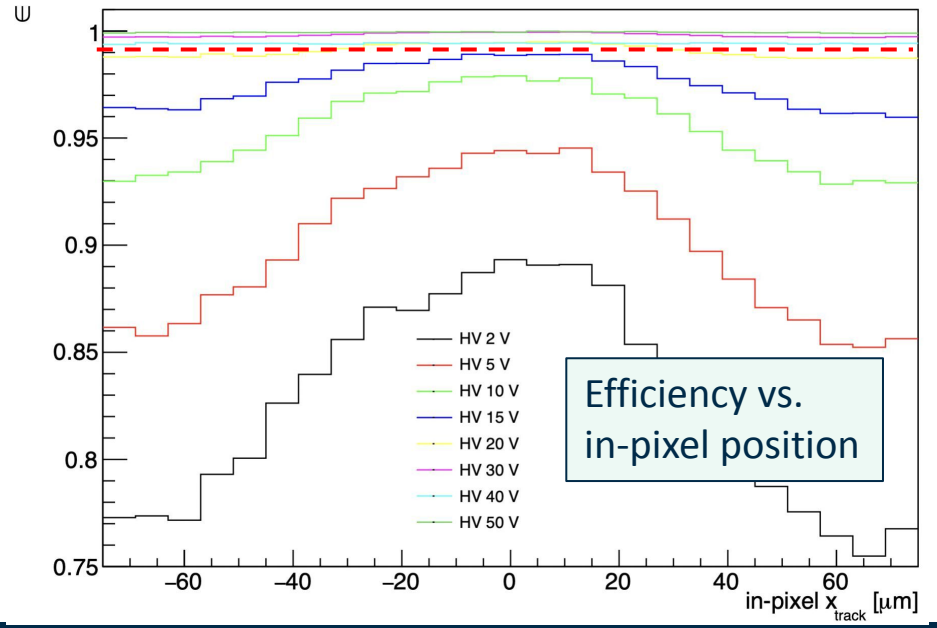


ATLASPIX3: Testbeam performance

- Telescope of 4 ATLASPIX3 single chips in DESY electron beam
- **Cross-talk** between pixels due to the capacitive coupling of the transmission lines between the matrix and the end-of-column logic is limited to **~1% of total hits**
- **Efficiency > 99%** and **uniform in the detector** for depletion voltages >20 V
- **Position resolution** in the **10-11 µm** range

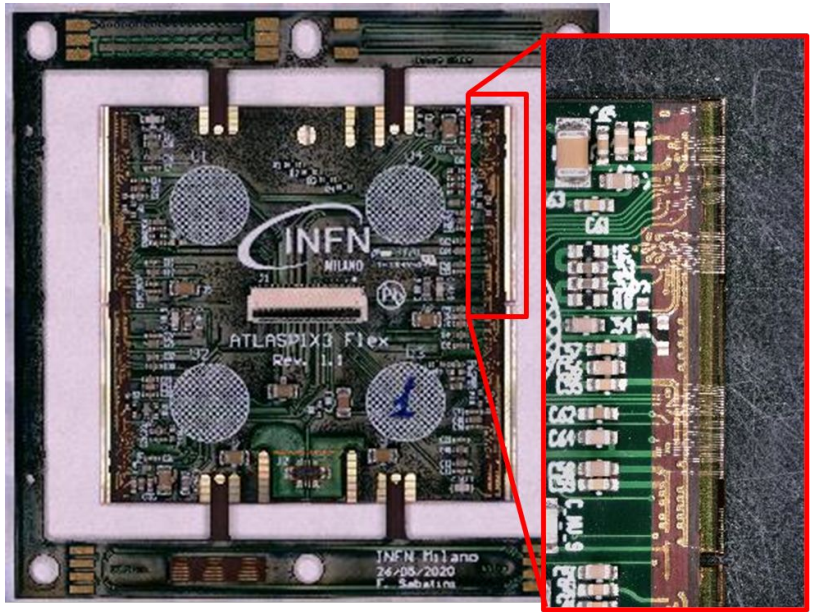


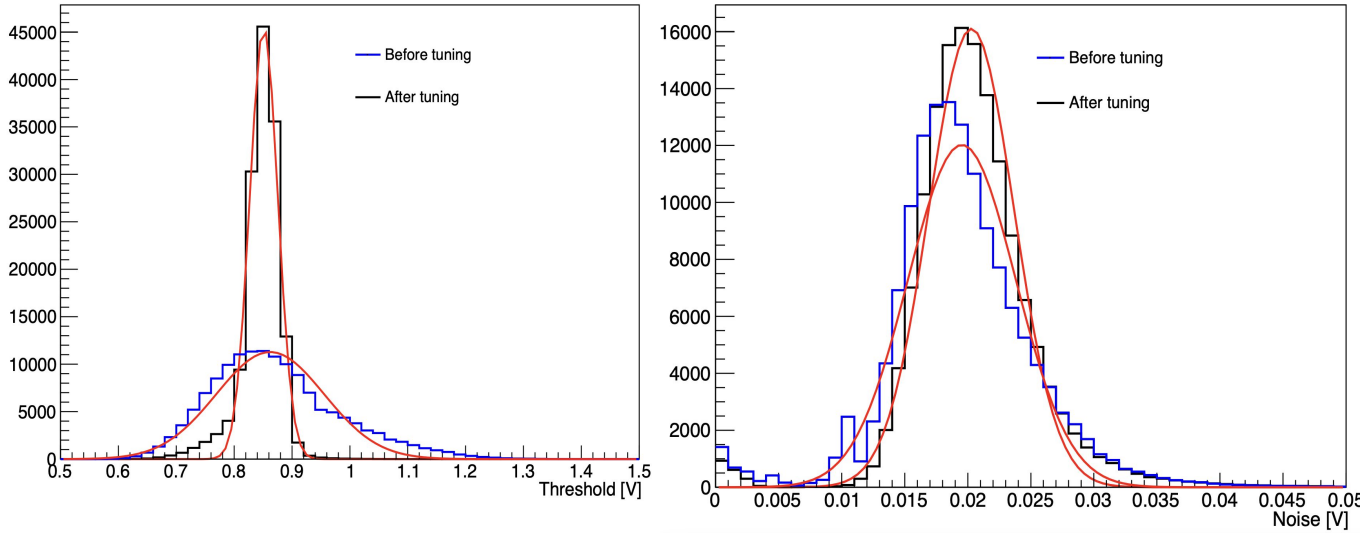


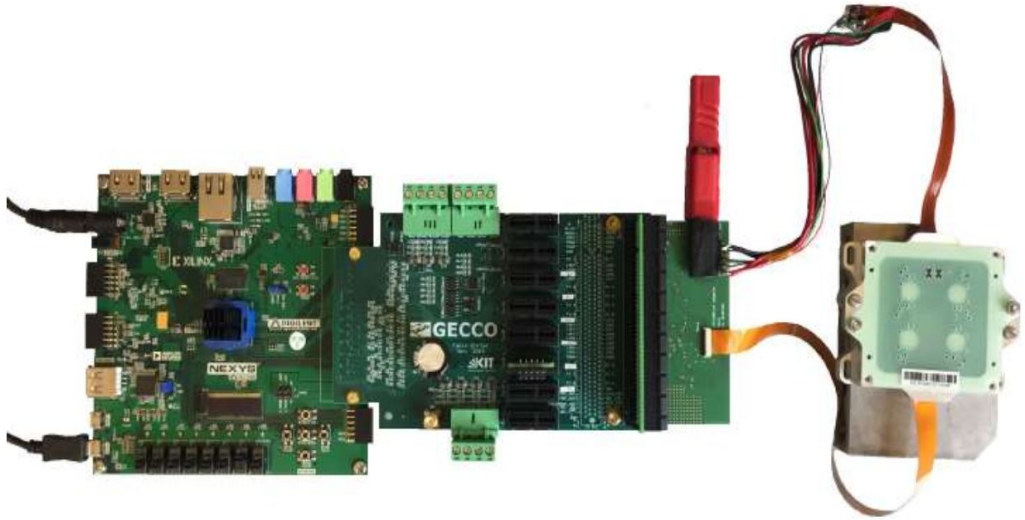


ATLASPIX3: Multi-chip module

- **Multi-chip** module **assembly**
  - aggregates electrical services and connection for multiple sensors
  - **quad module**, inspired by ITk pixels
  - building block for staves and disks
- No interference observed in the simultaneous operation of multiple chips
  - threshold tuning and noise performance same as individual chip characterization
  - testbeam and X-ray tube data

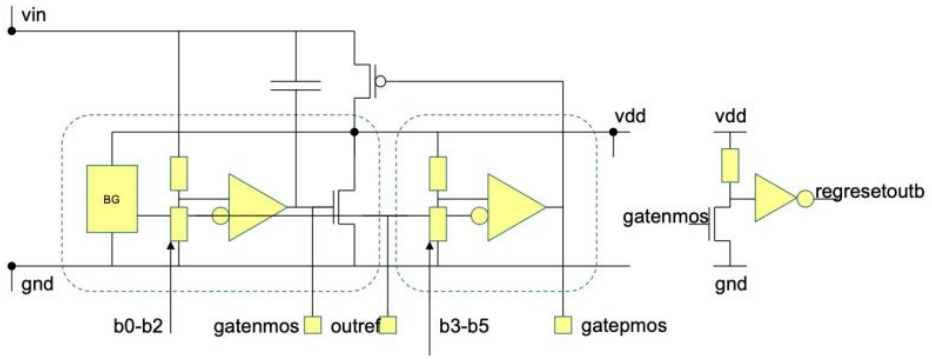


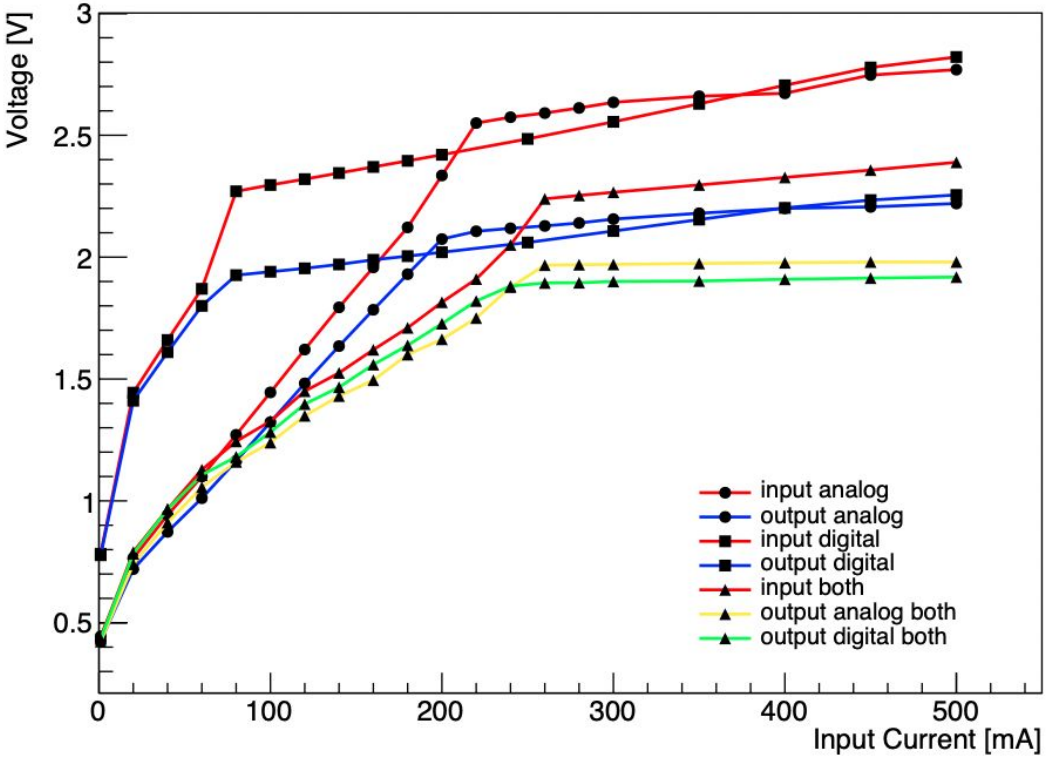




ATLASPIX3: Serial powering

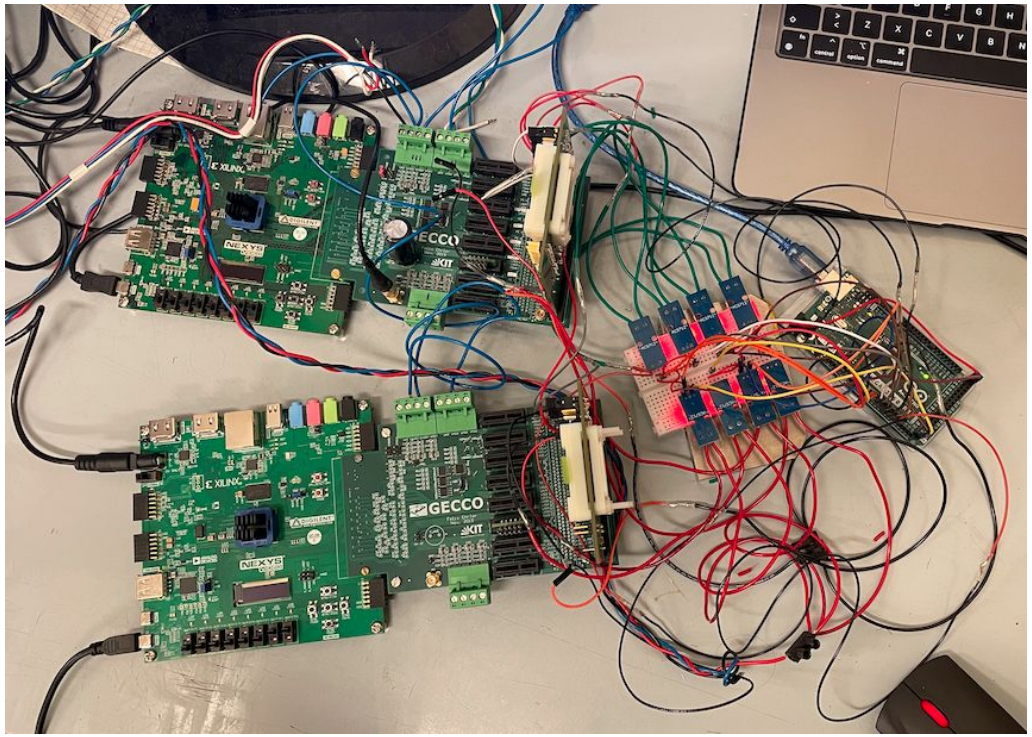
- Version ATLASPIX3.1 can be biased by **serial powering** through two **shunt/low dropout regulators**
  - digital and analog (VDDD/A)
  - 3 bits to tune threshold of shunt regulator
  - 3 bits to tune VDD
- Measured regulator performance
  - threshold and noise performance are the similar using SLDO or direct VDDD/A powering
  - DAC dinamic range of few tens of mV
  - Full chip turn-on at I=300 mA
  - Input voltage 2.3 V
  - Power consumption: ∼700 mW/chip or ∼175 mW/cm^2
- **Integration model is to join modules by a bus implementing a serial powering chain**
  - examples in F. Palla's talk
  - metal in the module hybrid and the power bus dominates the thickness of a detector layer (~0.44% X_0)
  - considering to move Al as conductor for PCBs

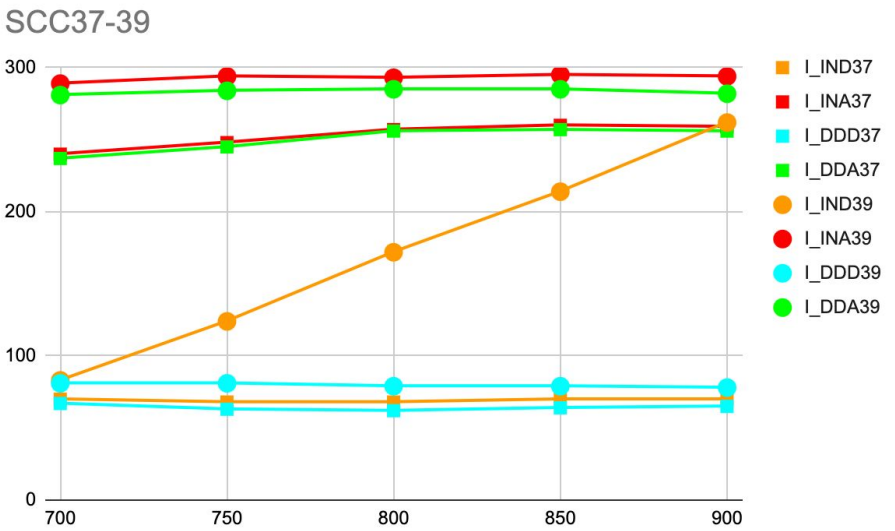


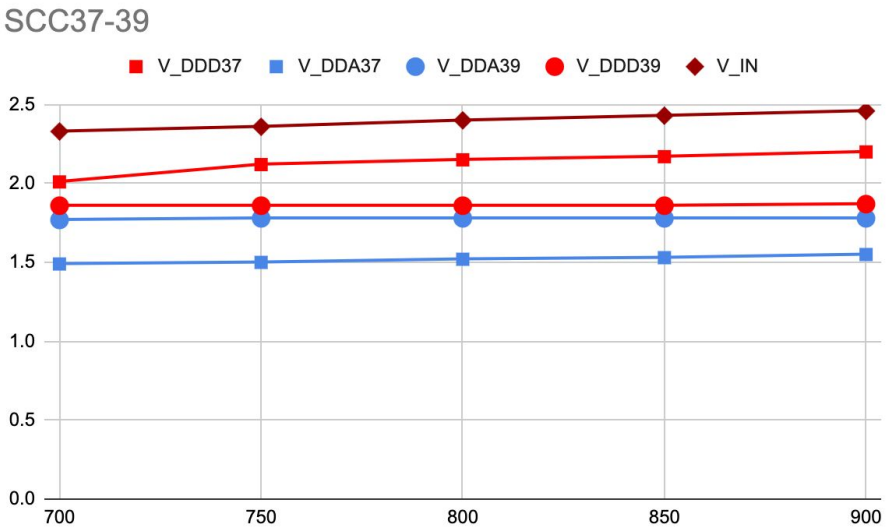


ATLASPIX3: Serial powering

- **Serial powering of two SCCs with regulators connected in parallel**
  - measurements of the current distribution between digital and analog part of the two chips and the resulting operation voltages
- **New design of quad modules implementing Serial Powering**
  - chips regulators connected in parallel
  - need to study how regulator to regulator differences influence operation of the chips
  - design of the **PCB almost ready** for production







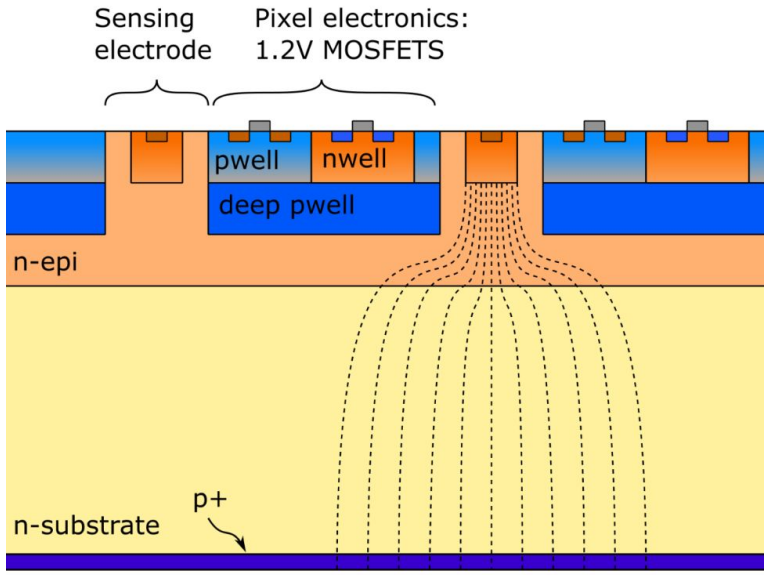
ATLASPIX3: Serial powering

- Comparison of **performances** of the two chips for **Direct Voltage powering and for Serial powering** when **singularly powered** and when **connected** as shown before
  - **degradation of performance for one the chips** due to non-optimal values of operating voltages
  - results resumed in table

	DV single (tuning)		DC single (tuning)		DC connected (scan)	
	Threshold [V]	Noise [V]	Threshold [V]	Noise [V]	Threshold [V]	Noise [V]
SCC37	0.644±0.015	0.019±0.003	0.654±0.015	0.023±0.003	0.884±0.074	0.032±0.003
SCC39	0.715±0.028	0.021±0.003	0.718±0.019	0.023±0.003	0.788±0.069	0.020±0.002

ARCADIA

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays



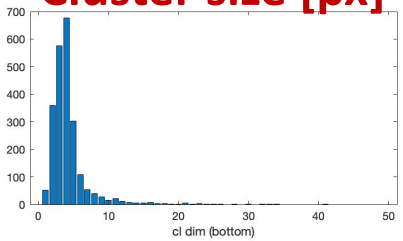
- Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:
  - Active sensor thickness in the range 50 µm to 500 µm;
  - Operation in **full depletion** with fast charge collection by drift
  - **Small collecting electrode** for optimal signal-to-noise ratio;
  - Scalable readout architecture with ultra-low power capability O(**10 mW/cm^2**);
  - Compatibility with standard CMOS fabrication processes
  - LF 110nm technology
- **MD3 demonstrator**
  - sensitive area 12.8cmx12.8cm
  - 512x512 pixels, Double Column arrangement
  - 25x25 µm^2 pixels
  - Clockless

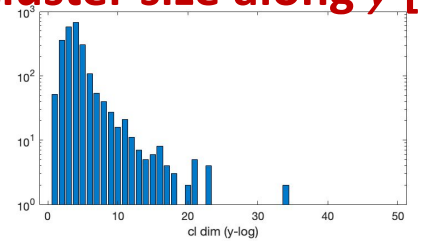
All details in D.Falchieri's talk tomorrow moring!

ARCADIA: MD3 Results with cosmics

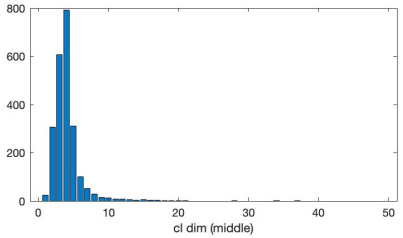
Cluster size [px] **Cluster size along *y* [px]**

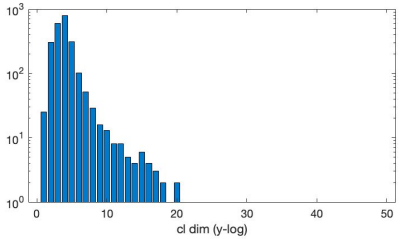
Bottom layer



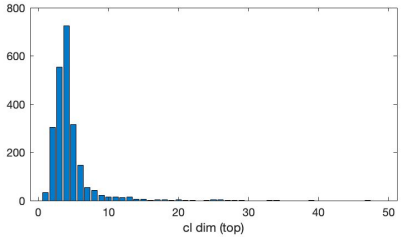


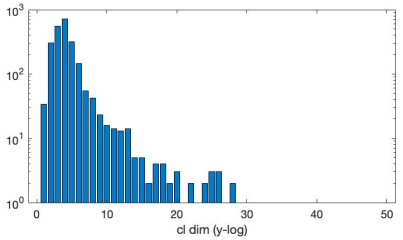
Middle layer

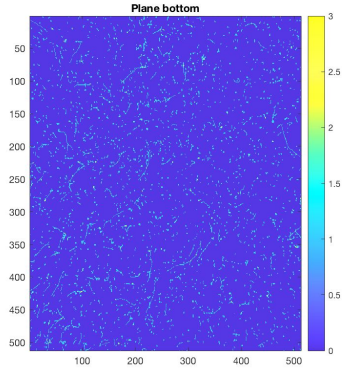


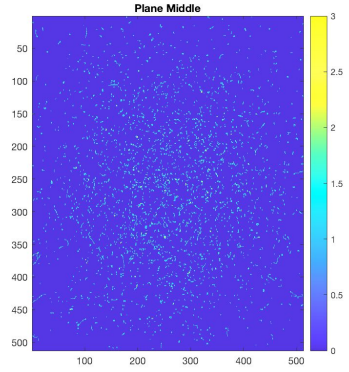


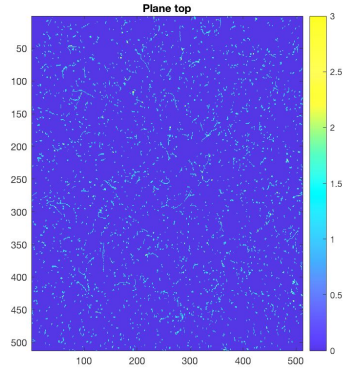
Top layer



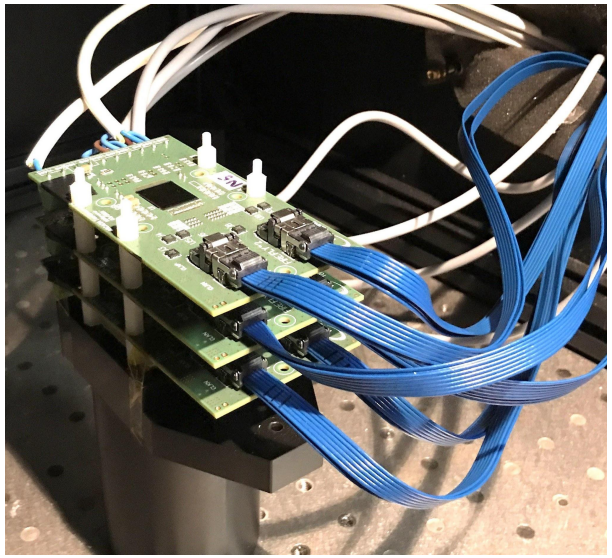








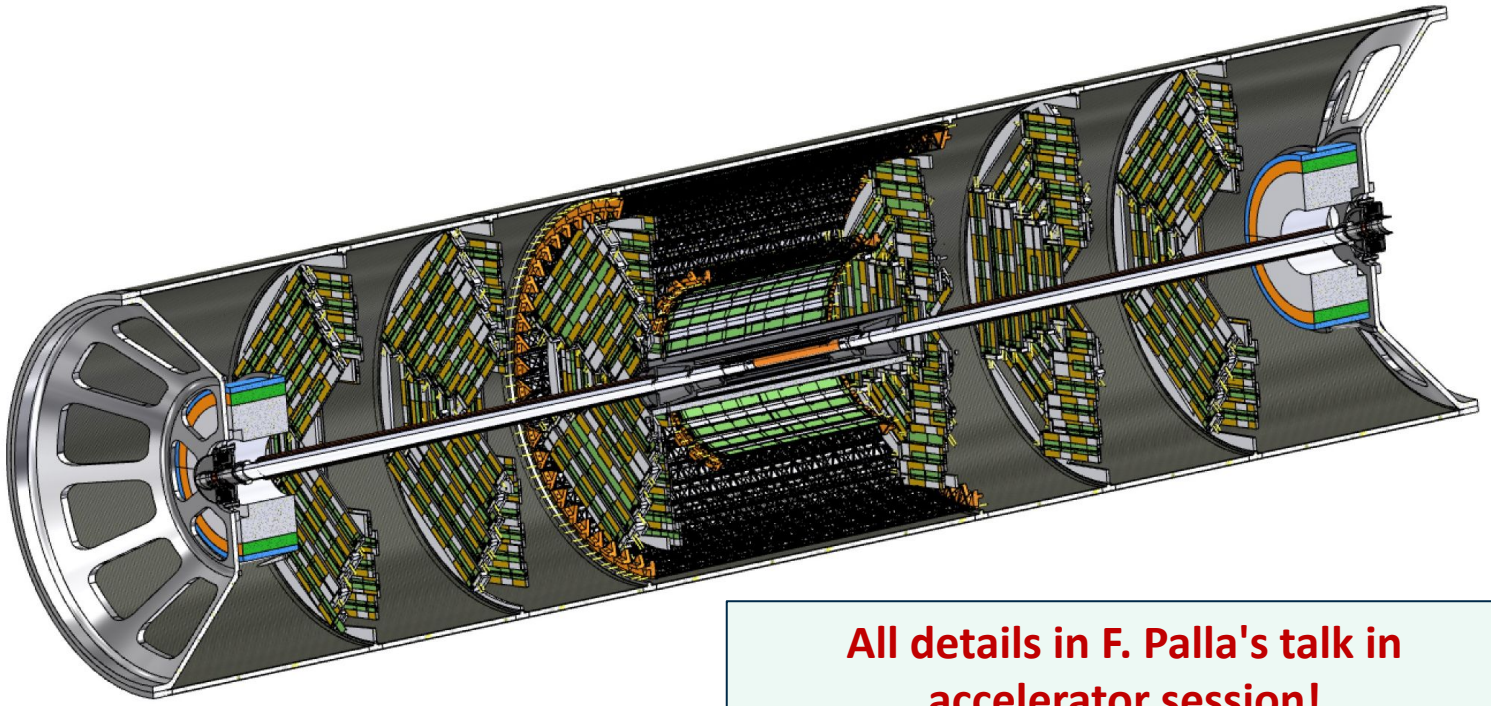
- Cosmic ray data taking: 1 week
- 3-plane MD3 installed on a black box
- Threshold 290 e-, MPV = 4 pixels
- More than 90% of clusters with less than 6 fired pixels
- Preliminary results on residuals show a standard deviation of 12-14 μm (multiple scattering...)



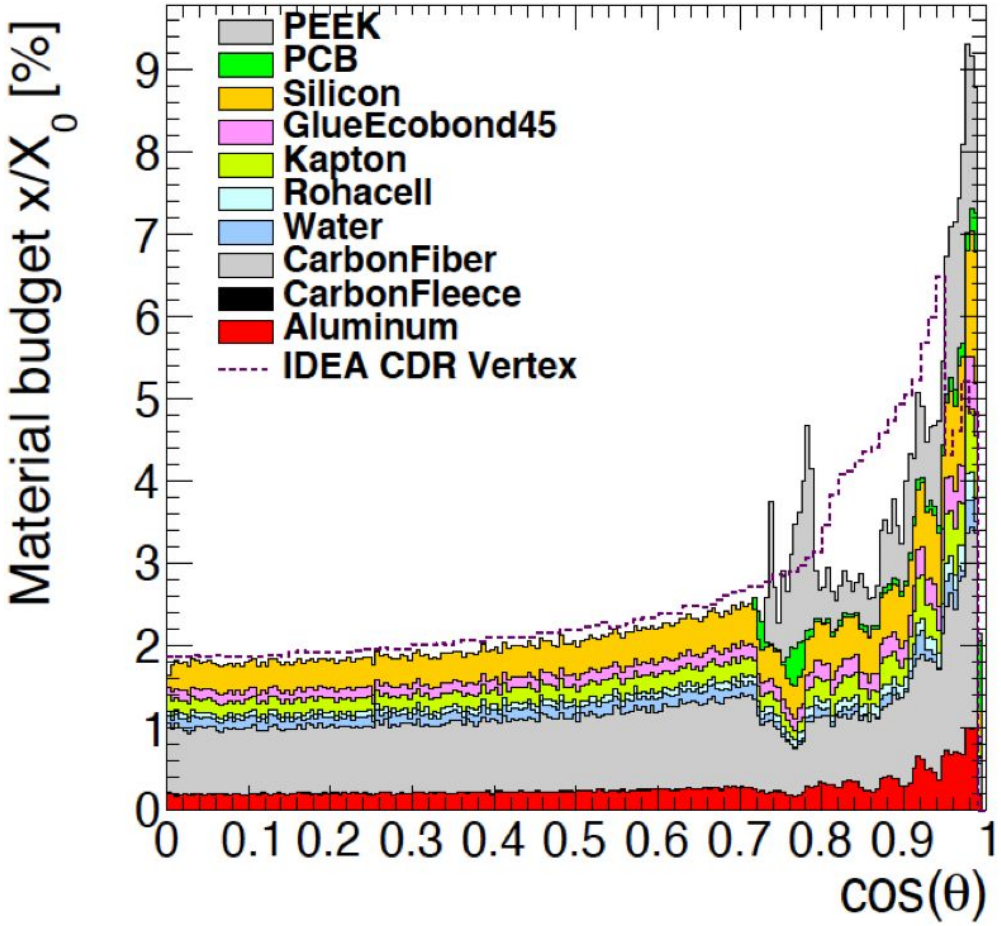
Integration with MDI

Development with the FCCee MDI accelerator group

- Integration with **realistic local support,** cooling and electrical services
- Mockup to be build at LNF to demonstrate the interface with the machine and the mixed cooling
  - air cooling for vertex
  - water cooling for internal tracker



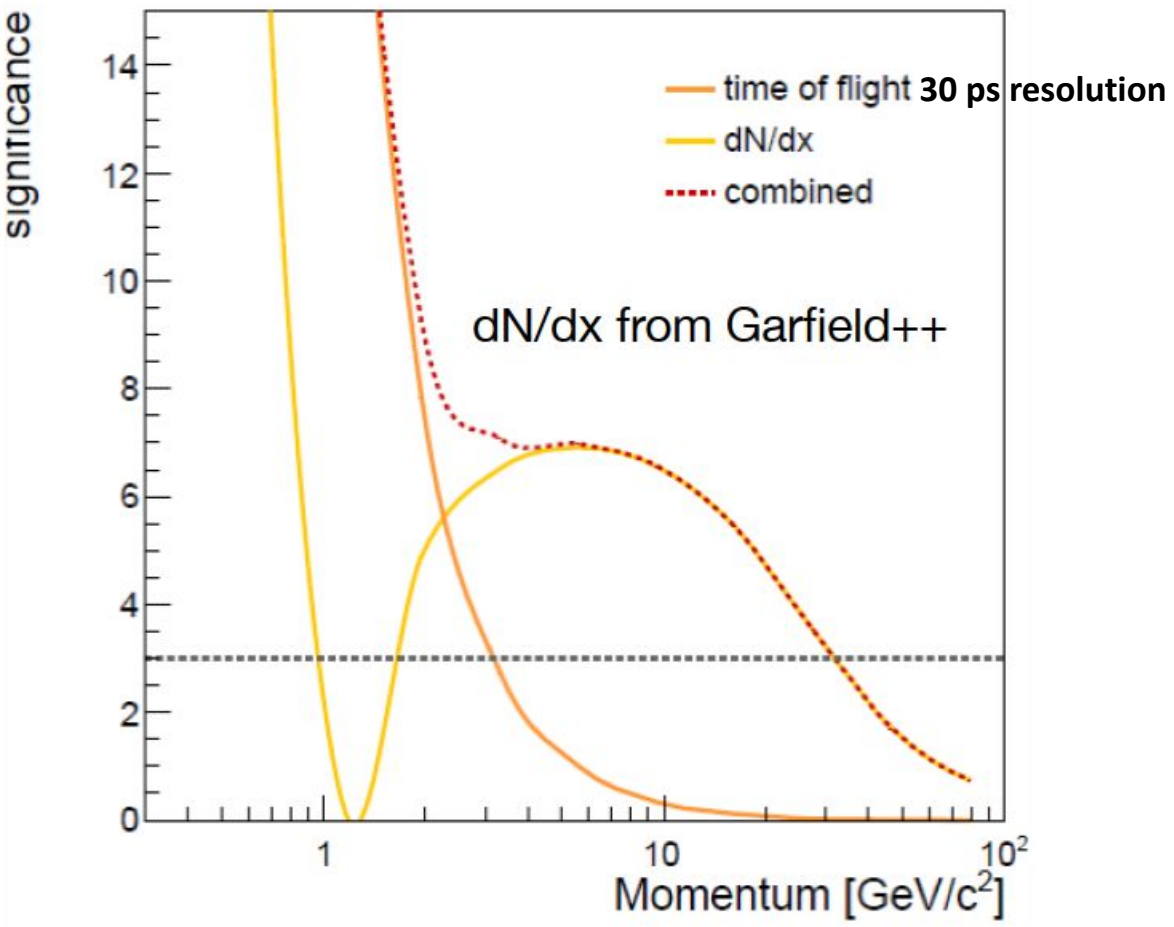
All details in F. Palla's talk in accelerator session!



TOF measurement in Si Wrapper

- Particle IDentification is essential for many physics measurements
- Needed on a wide momentum range
  - $B_s^0 \to D_s K$ has K up to 30 GeV/c
  - K for flavour tagging in $b \to c \to s$ decay chains are pretty soft
  - useful in tau physics for Vus measurements in $\tau \to K\nu$

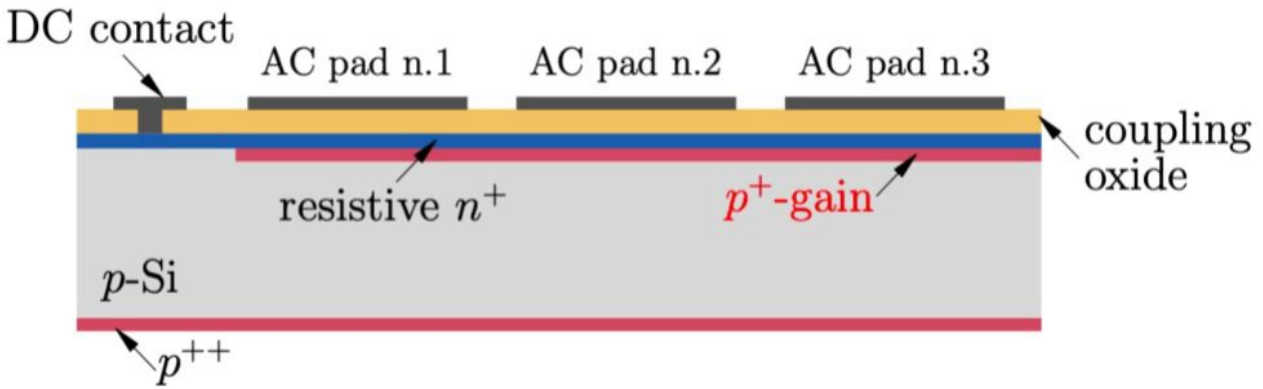
- **dN/dx** measurements in Drift Chamber provides 3σ separation up to 30 GeV/c
- Confusion region about 1 GeV/c can be covered by **TOF** measurement with resolution **<100 ps**

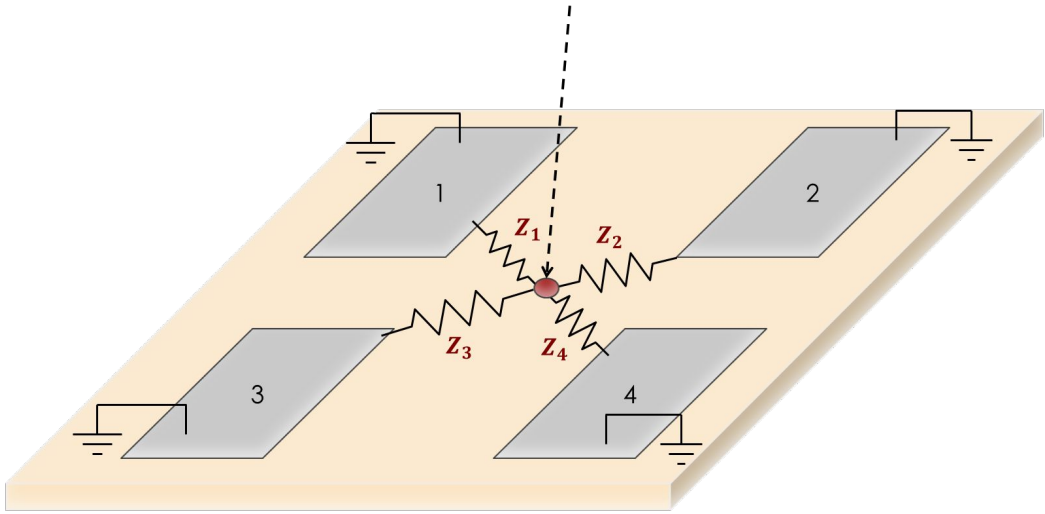


Can it be implemented in the Si Wrapper without compromising the spatial resolution?

Resistive Silicon Detectors (RSD)

- LGAD detector with **continuous gain layer**
- Charge collection through **resistive n-layer**
- Readout by induction on **AC coupled pads**
- Fully active detector
  - avoids inefficient regions due to the insulation between pixels needed in LGAD sensors
- Charge sharing defined by the relative impedance of the path between the charge deposition and readout electrodes
  - pad pitch >> lateral dimension of charge deposit
  - sharing is deterministic (in low pitch pixel detectors is dominated by Landau fluctutations)
  - resolution depends on the S/N ratio of the readout electronics

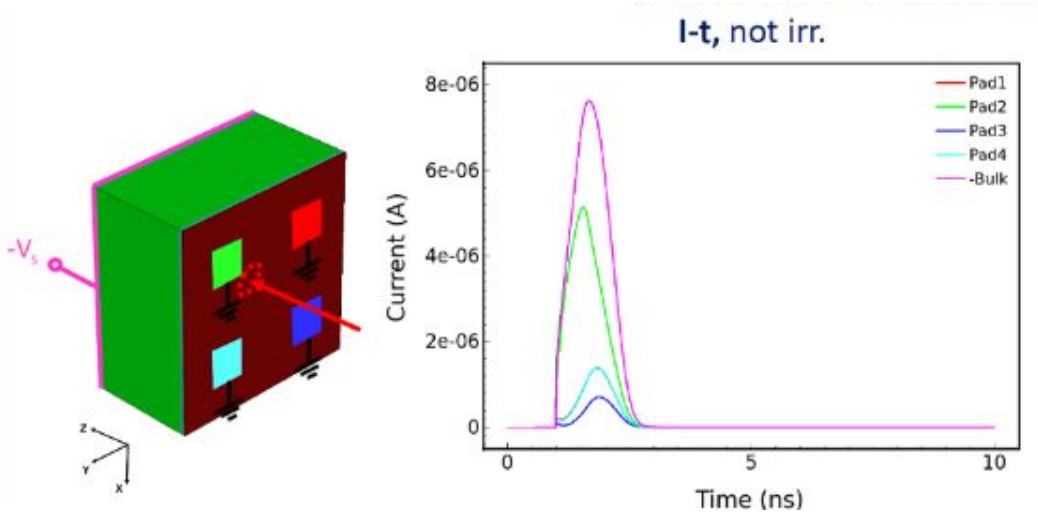




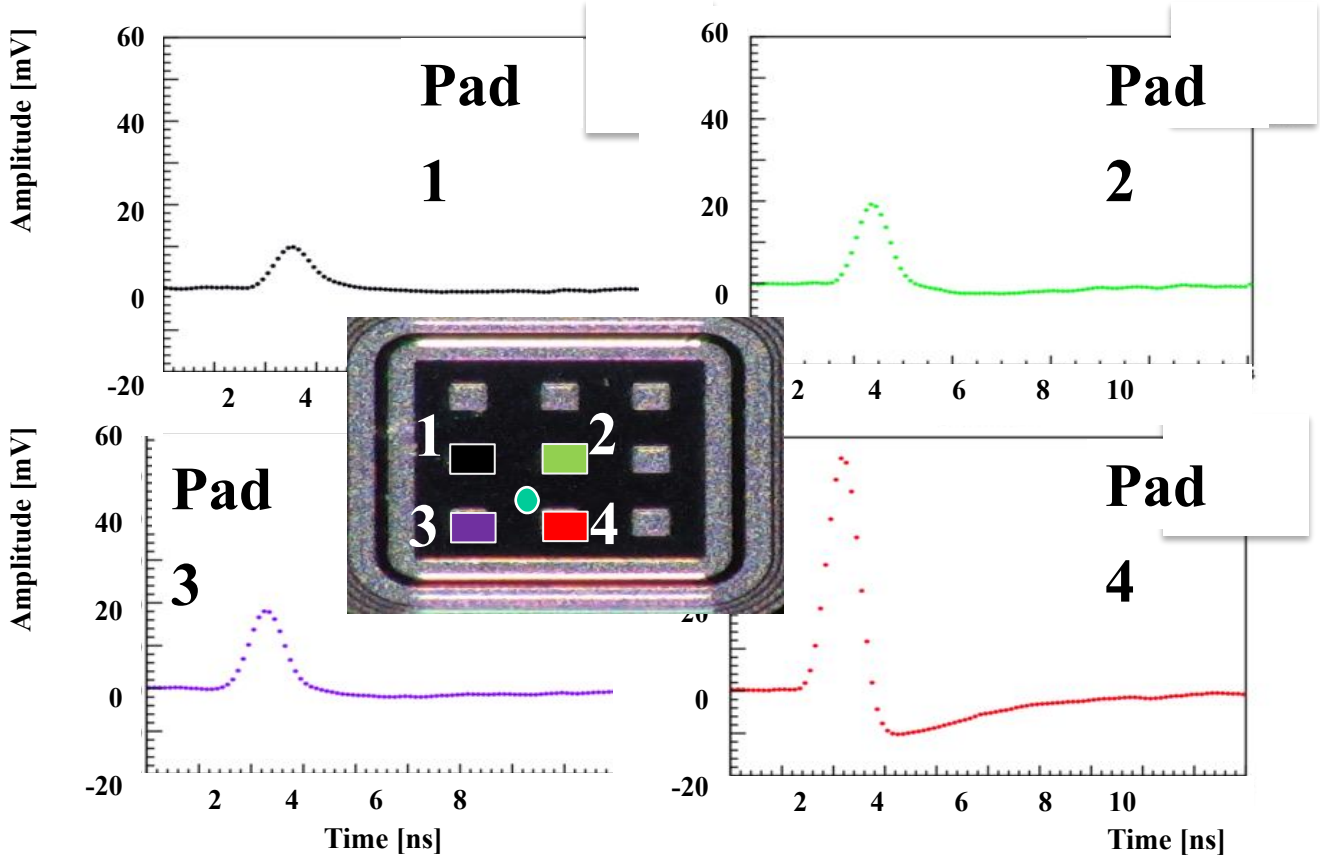
$$S_i = \frac{1/Z_i}{\sum 1/Z_i}$$

RSD: Signal sharing example

TCAD Simulation model...

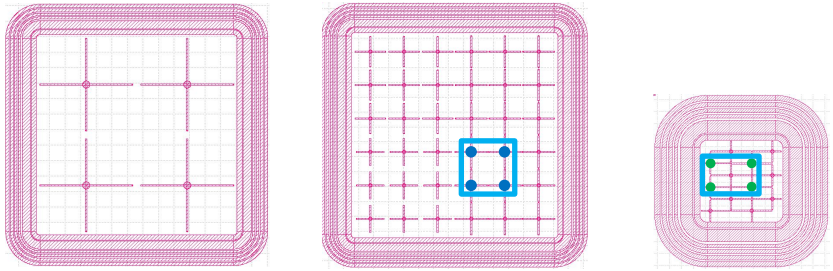


...and reality



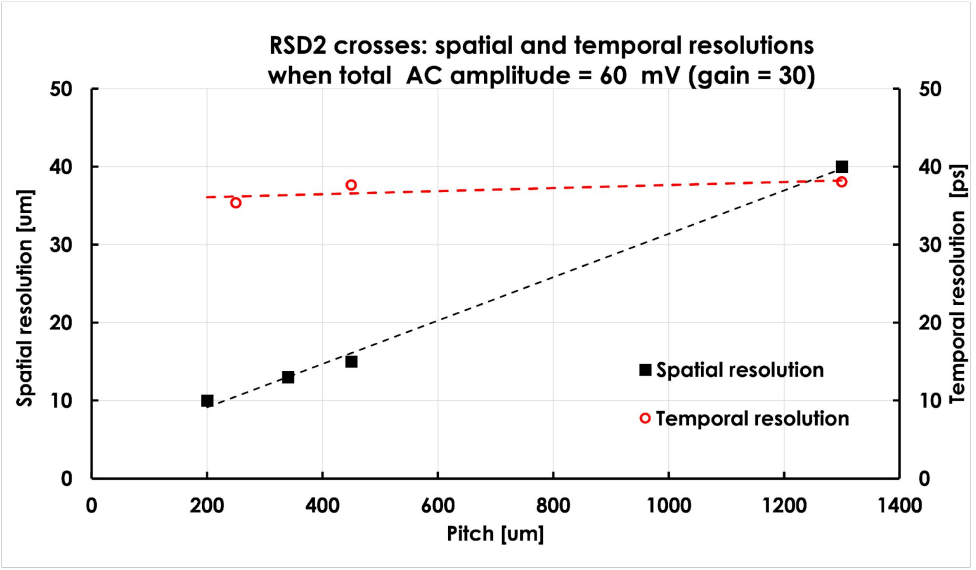
RSD: Prototype performance

- Spatial resolution << pixel pitch
  - 10 μm achieved in lab tests with 200 μm pixel pitch
  - more space in readout pixel cell to implement precision TDC
- Timing resolution about independent from pixel pitch
- Drawbacks:
  - hybrid detector (but bump-bond pitch is easily achievable commercially)
  - effective pitch is >2 readout pitch: particle flux limited by pixel size
- Suited for Si Wrapper:
  - particle density at 2 m from the interaction region should not be a concern at e^+e^- colliders
  - no need to push for extremely low material: hybrid detectors are acceptable



$1.3 \times 1.3\ mm^2$ $450 \times 450\ \mu m^2$ $200 \times 340\ \mu m^2$

Cross-shaped electrodes



Summary and outlook

- The IDEA tracker layout poses different challenges for the different silicon trackers:
  - Extremely high resolution and low-mass are needed for the vertex detectors
  - System issues are the focus topics for the large area detectors
  - Depleted Monolithic CMOS pixel detectors are a cost-effective and high-performance solution
- **ATLASPIX3** (AMS/TSI 180 nm) is a well-developed full-size sensor:
  - Already a possible solution for the bulk of the detector silicon area
  - It is used to investigate integration and system issues
- **ARCADIA** (LF 110 nm) provides a global platform for fully-depleted CMOS sensors
  - The sensitive area has been developed and detector performance appears very promising
  - Fine granularity and low power make it suitable for the vertex trackers
  - Periphery needs to implement trigger logic, command decoder, 1.28 Gbps serializers...
- **Resistive Silicon Detectors** are an extremely interesting option for the Silicon Wrapper:
  - Micrometric spatial resolution even with coarse granularity: reduced number of channels
  - Provide a TOF layer supplementing the drift chamber particle ID
- Plenty of **fascinating electronic design and sensor development** will be needed to arrive to build a state-of-art detector within the time scale of future e^+e^- factories
- At the same time, it is possible to **address system aspects with already existing detectors**

BACKUP

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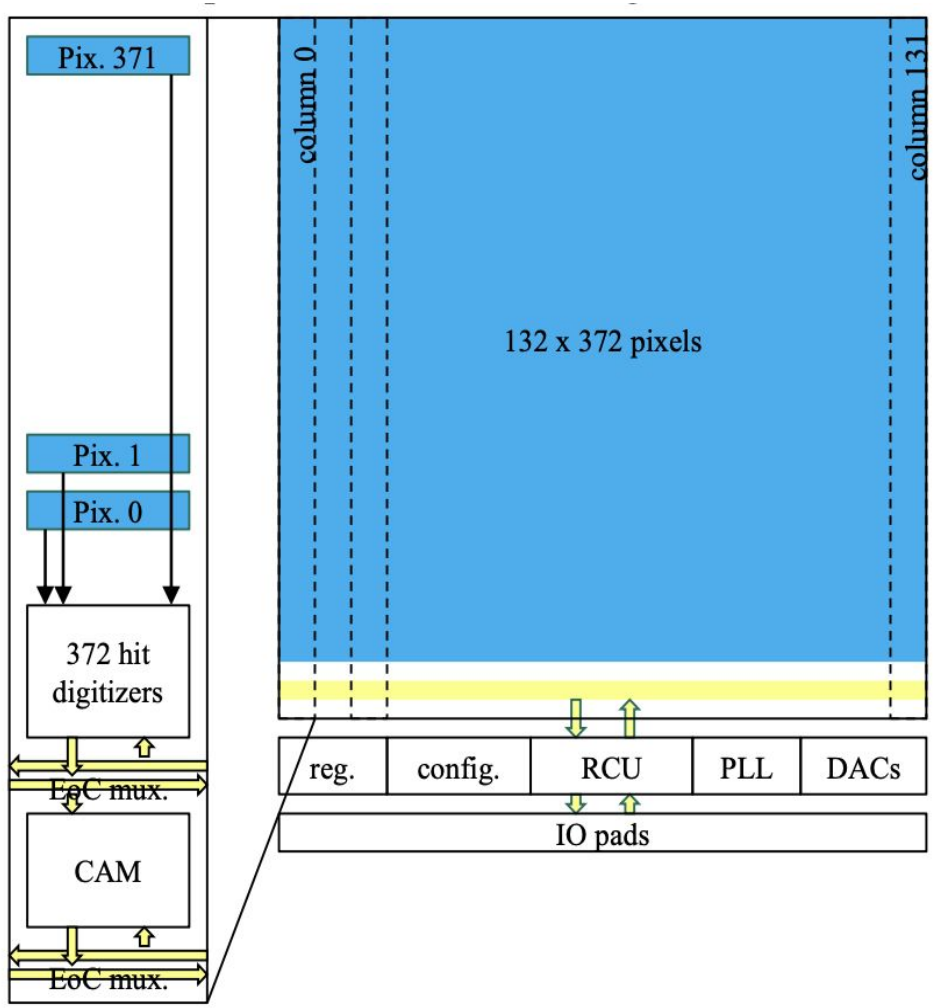
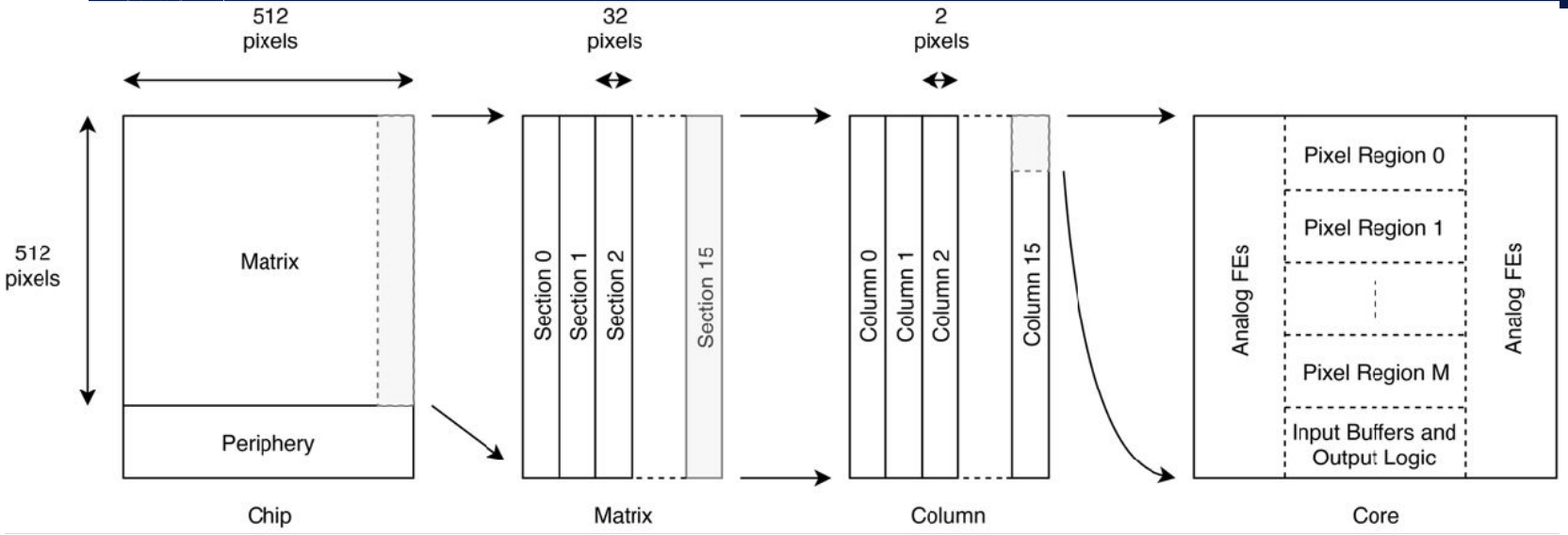
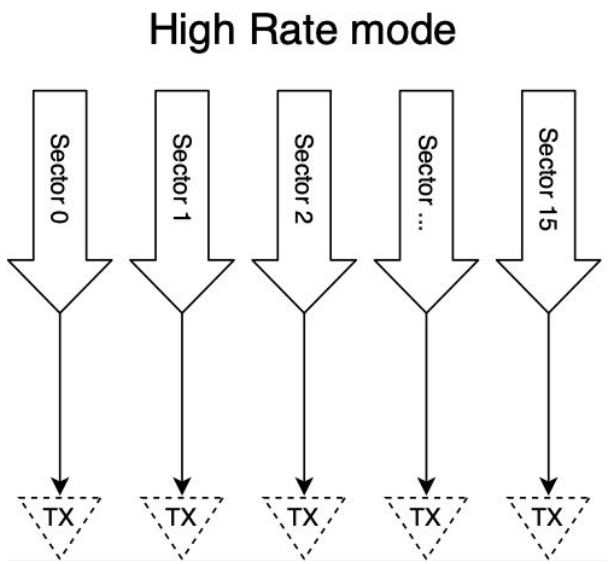
ATLASPIX3 Readout Architecture

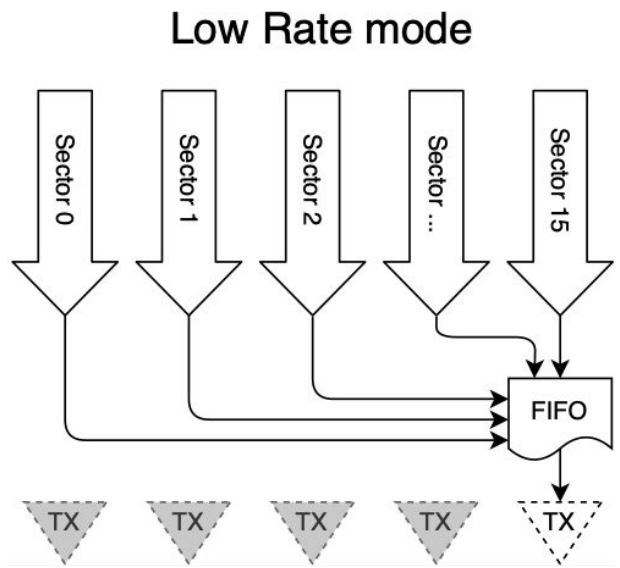
- **Chip architecture**
  - organized in 132 columns, each with:
    - 372 pixels
    - **372 hit digitizers** (HDs)
    - **80 content addressable memory cells** (CAM)
    - **two end-of-column multiplexers** (EoC mux)
  - **digital part** (HDs, CAM, EoCs) in **chip periphery**, separated from analog pixels electronic (CSA and comparator)
  - chip periphery also contains the readout control unit (RCU), the clock generator, configuration registers, DACs, linear regulators and IO pads
  - **triggerless** and **triggered** readout
    - two EoCs
    - 372 hit buffers for triggerless RO
    - 80 trigger buffers for triggered RO



ARCADIA: MD3 Architecture







- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm^2 (post-layout simulations, to be demonstrated: test-beam in late 2023)
- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.