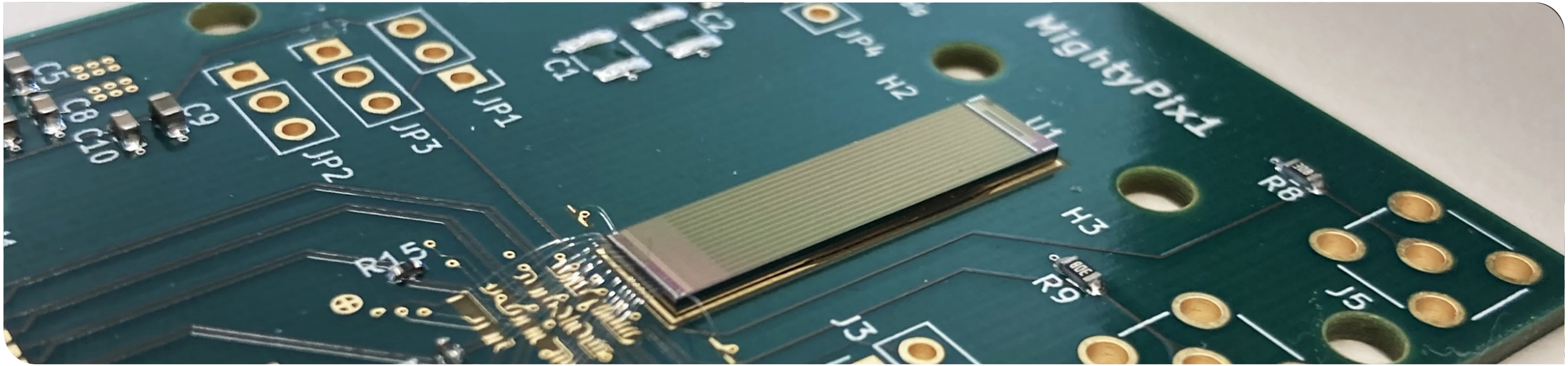
MightyPix

Update on the HV-CMOS chip for LHCb's Mighty Tracker

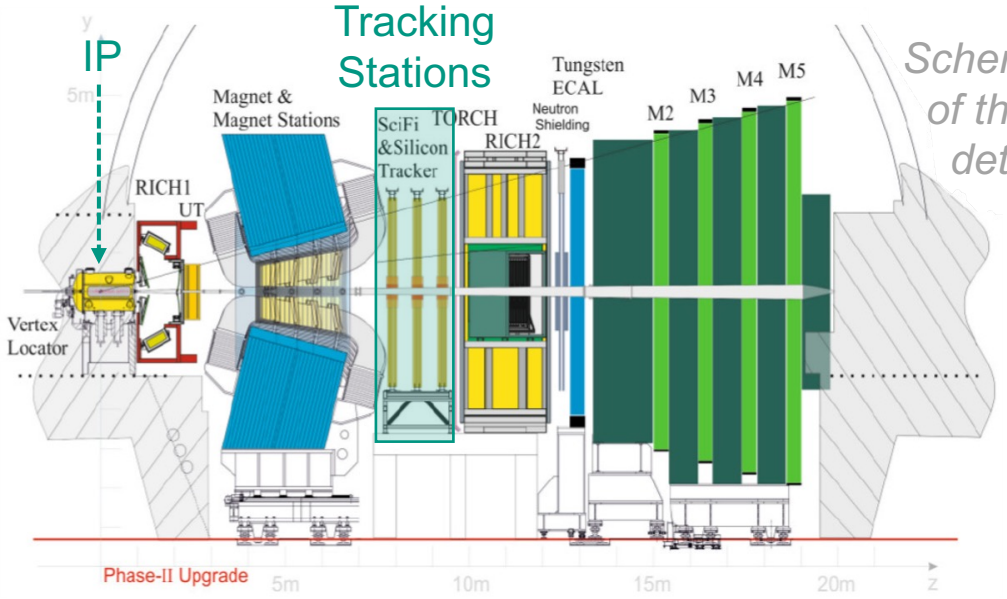
Toko Hirono, Richard Leys, Ivan Perić, **Sigrid Scherl***, Nicolas Striebig

**sigrid.scherl@cern.ch*

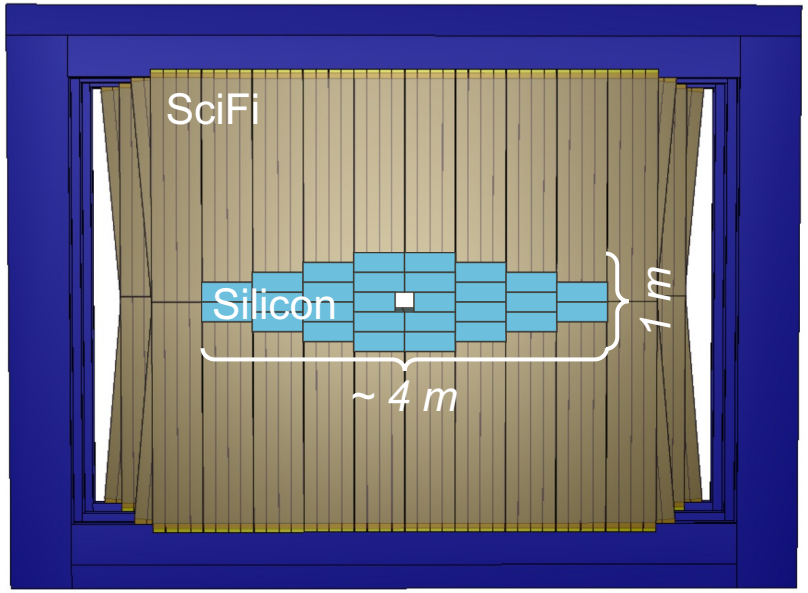


The Mighty Tracker

- New hybrid tracker for LHCb High Luminosity upgrade [1]
- Outer parts: Scintillating Fibre (SciFi) Tracker
- Inner parts: HV-CMOS pixel chip **MightyPix** → Good granularity and radiation hardness



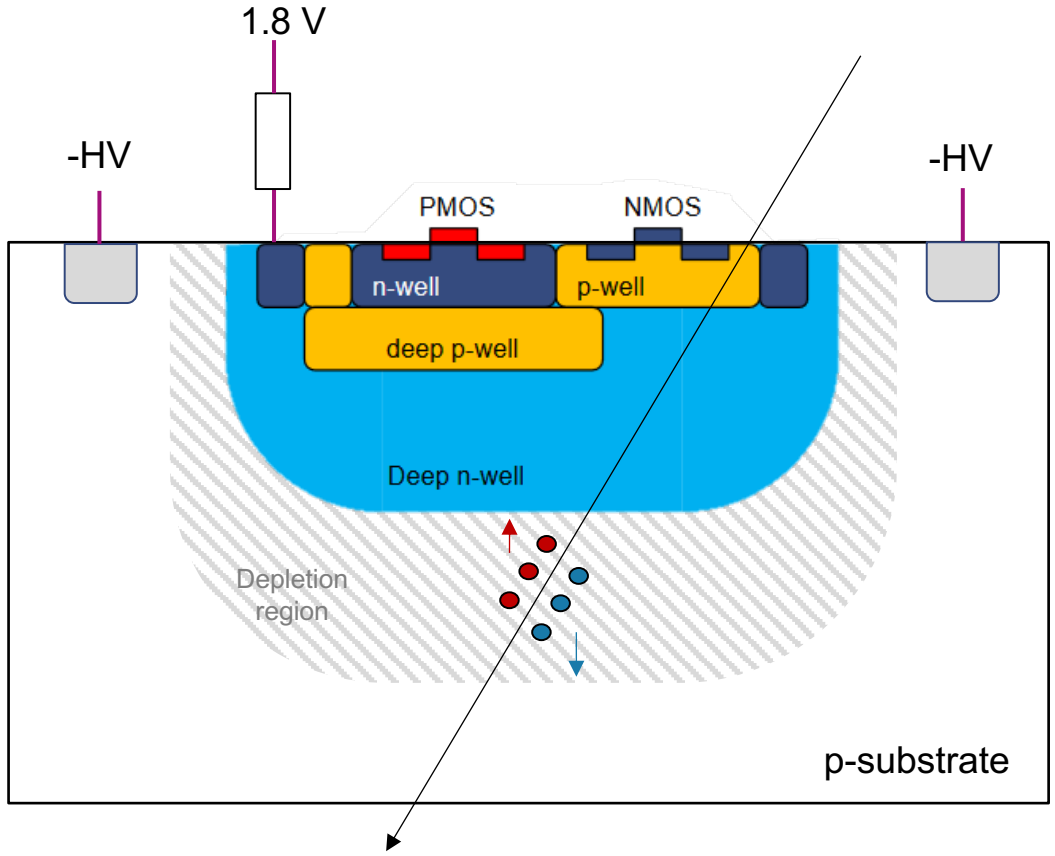
Schematic side view of the HiLumi LHCb detector. [1]



Schematic front view of of the Mighty Tracker. [1]

HV-CMOS

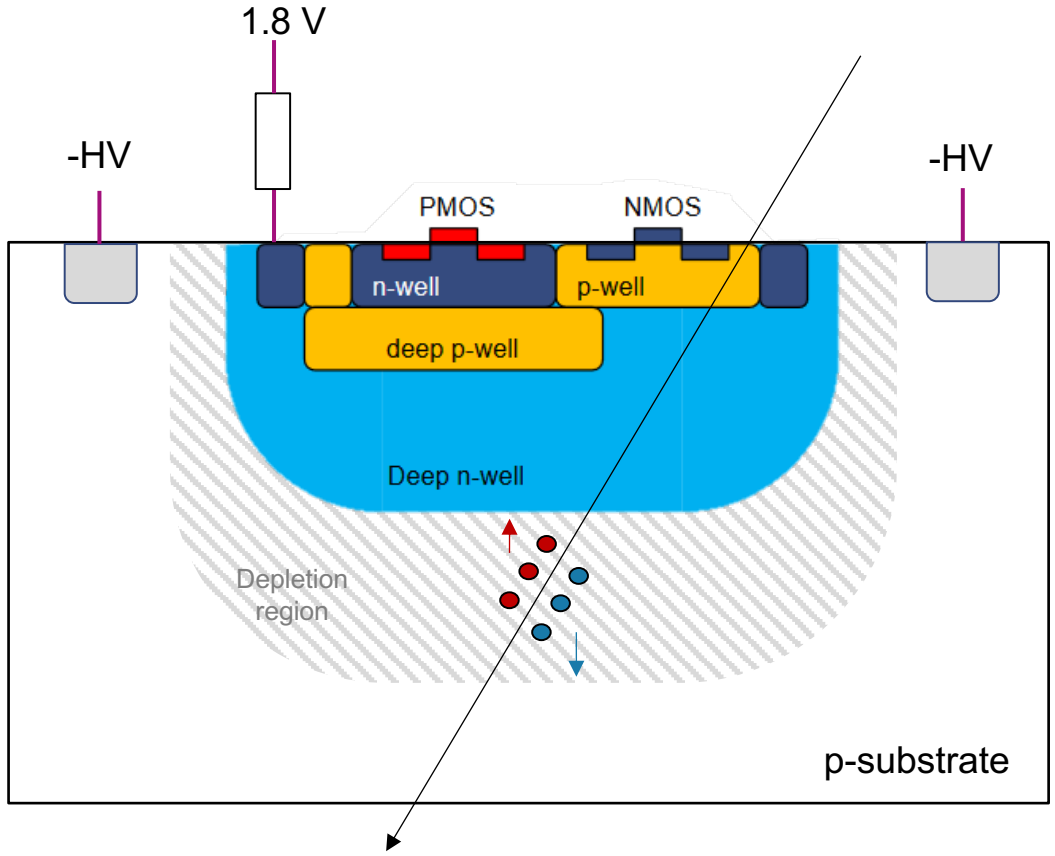
- HV-CMOS = High Voltage Complementary Metal-Oxide-Semiconductor
- Sensors also called HV-MAPS = HV Monolithic Active Pixel Sensors
- **Advantages:**
  - Very thin ~ 700 µm down to 50 µm
  - Radiation hard
  - Fast charge collection via drift
  - Cheaper than hybrid
  - Fabricated in standard CMOS process



Working principle of HV-CMOS sensors.

HV-CMOS

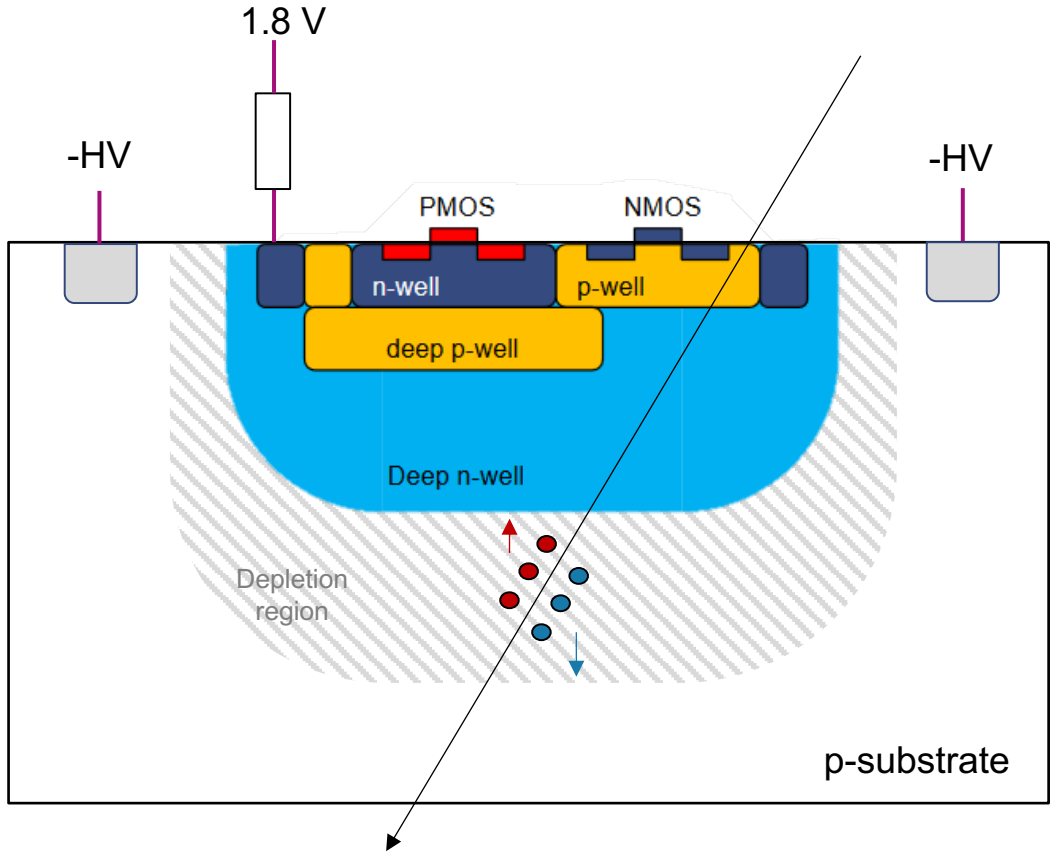
- Sensing element and readout circuit on same chip
- High reverse bias (~ 200 V) creates thick depletion region between deep n-well and p-substrate
- n-well/p-substrate diode acts as sensor
- Readout electronics isolated from high voltage by deep n-well
- Photons and charged particles create electron/hole pairs, collected via drift



Working principle of HV-CMOS sensors.

HV-CMOS

- **Quadruple-well process**
  - PMOS and NMOS transistors are placed in shallow wells
  - PMOS isolated by additional deep p-well
  - High voltage can be applied between substrate and deep n-well



Working principle of HV-CMOS sensors.

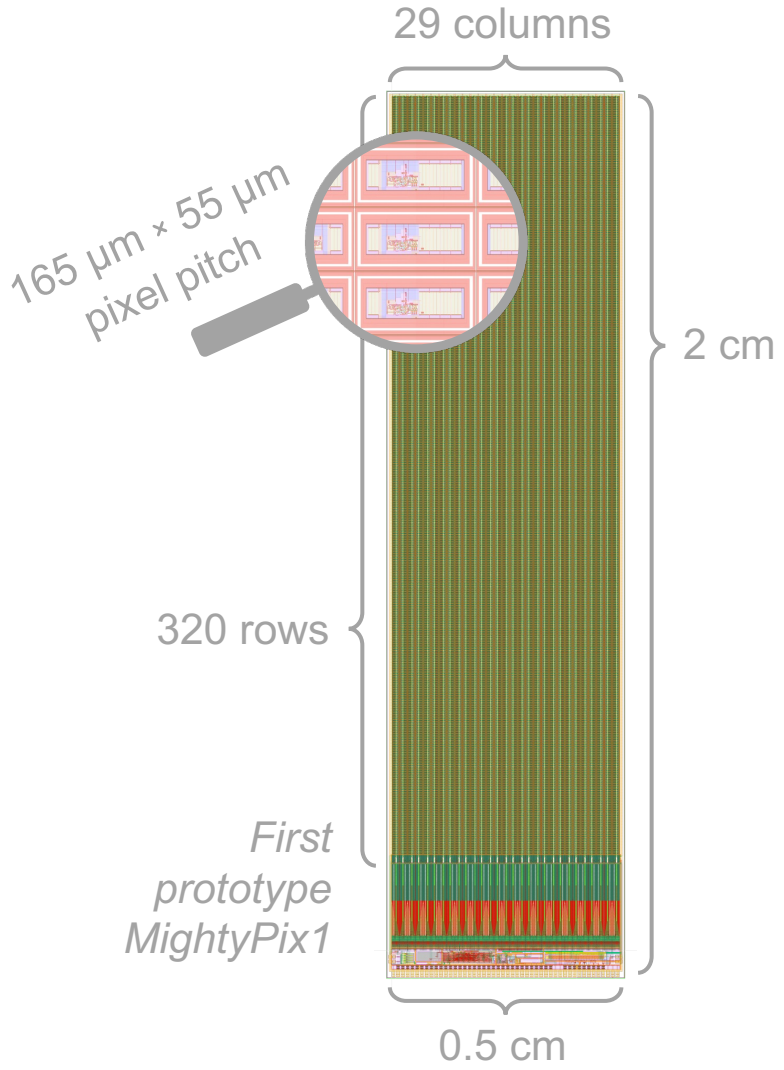
MightyPix

- Based on knowledge of previous HV-CMOS chips
  - ATLASPix *(Proposed for CERN's ATLAS experiment)*
  - MuPix *(Used for PSI's Mu3e experiment)*
- Final design requirements for MightyPix
- First prototype: **MightyPix1**

Parameter	Required Value
Chip size	$\sim 2\ \text{cm} \times 2\ \text{cm}$
Sensor thickness	$200\ \mu\text{m}$
Pixel size	$< 300\ \mu\text{m} \times 100\ \mu\text{m}$
Inactive area	$< 4\%$
Time resolution	$< 3\ \text{ns}$
Power consumption	$< 0.15\ \text{W/cm}^2$
NIEL[3]	$6 \times 10^{14}\ 1\ \text{MeV}\ \text{n}_{\text{eq}}/\text{cm}^2$
Data transmission	$\leq 4 \times 1.28\ \text{Gbit/s links per chip}$

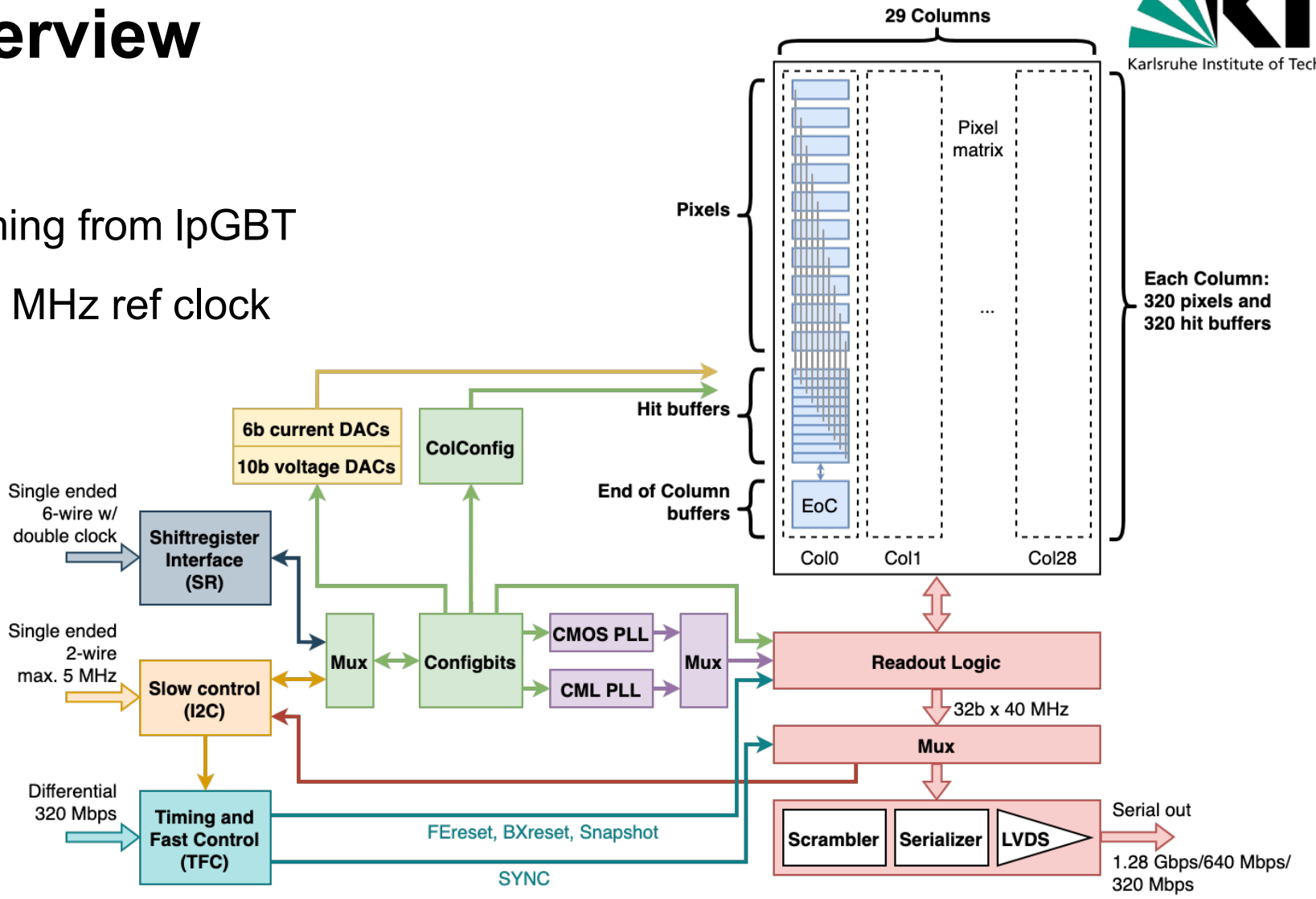
MightyPix1: Overview

- **Implementation:** TSI 180 nm process
- **Submission:** in May 2022
- **Chip size:** ~ 2 cm x 0.5 cm → Full length, ¼ of final width
- **Pixel matrix:** 29 columns, 320 rows
- **Pixel pitch:** 165 µm × 55 µm
- **Inside pixel:** CMOS amplifier and CMOS comparator
- **Data format:** 2 x 32 bit words per hit
- **Output rate:** 1.28 Gbit/s going to lpGBT



MightyPix1: Overview

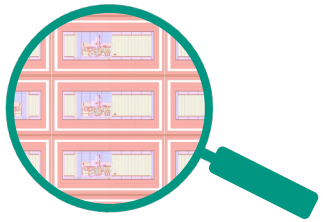
- **Clock generation:**
  - External 40 MHz coming from lpGBT
  - Internal PLLs with 40 MHz ref clock
- **Bias voltages:**
  - Integrated 10 bit voltage DACs
- **Digital interfaces:**
  - Slow Control (I2C)
  - Timing and Fast Control (TFC)
  - Shift Register (SR)



MightyPix1 Block Diagram (Source: Nicolas Striebig, KIT)

MightyPix1: Analogue Part

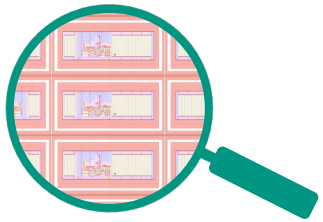
- **Pixel content:**
  - N-well charge collecting anode
  - CMOS Charge Sensitive Amplifier (CSA)
  - CMOS Comparator
  - Threshold tune DAC
  - RAM for tune bits



Schematic of the MightyPix1 Analogue Pixel (Source: Ivan Perić, KIT)

MightyPix1: Analogue Part

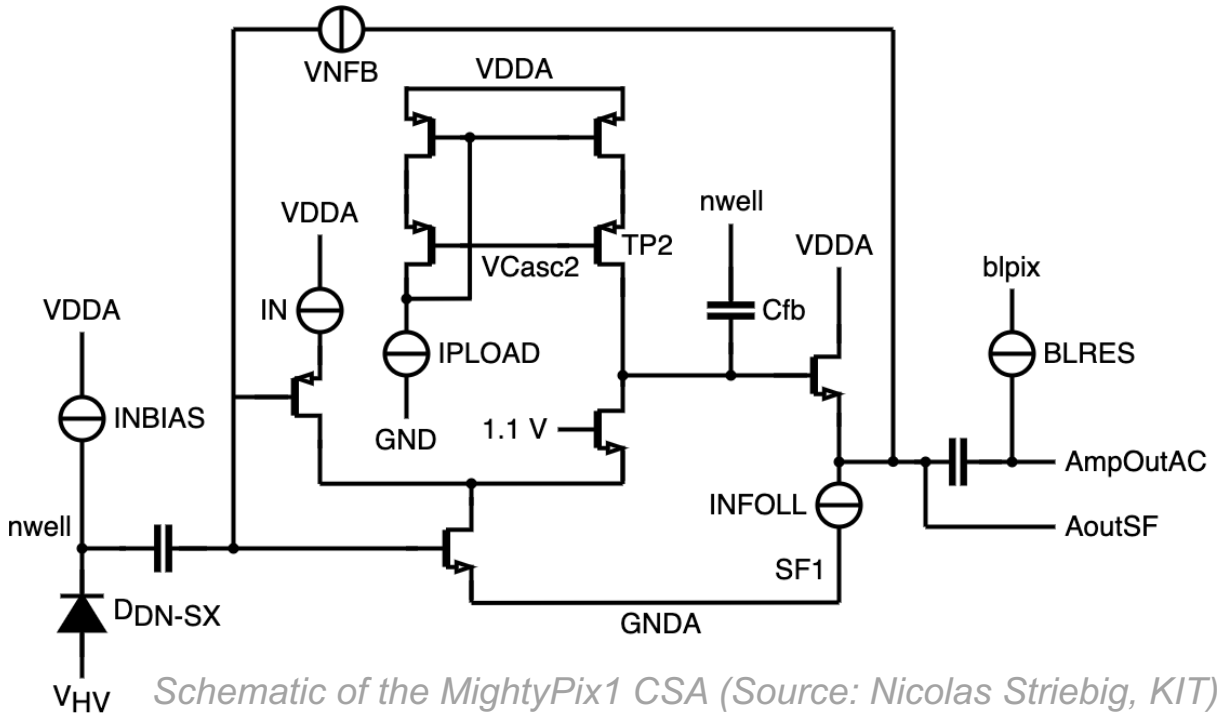
- **Hit detection:**
  - Charge collected by pixel n-well
  - Converted to voltage signal by Charge Sensitive Amplifier
  - Analog voltage pulse shaped and converted to digital signal by comparator
  - Hit information stored in hit buffer



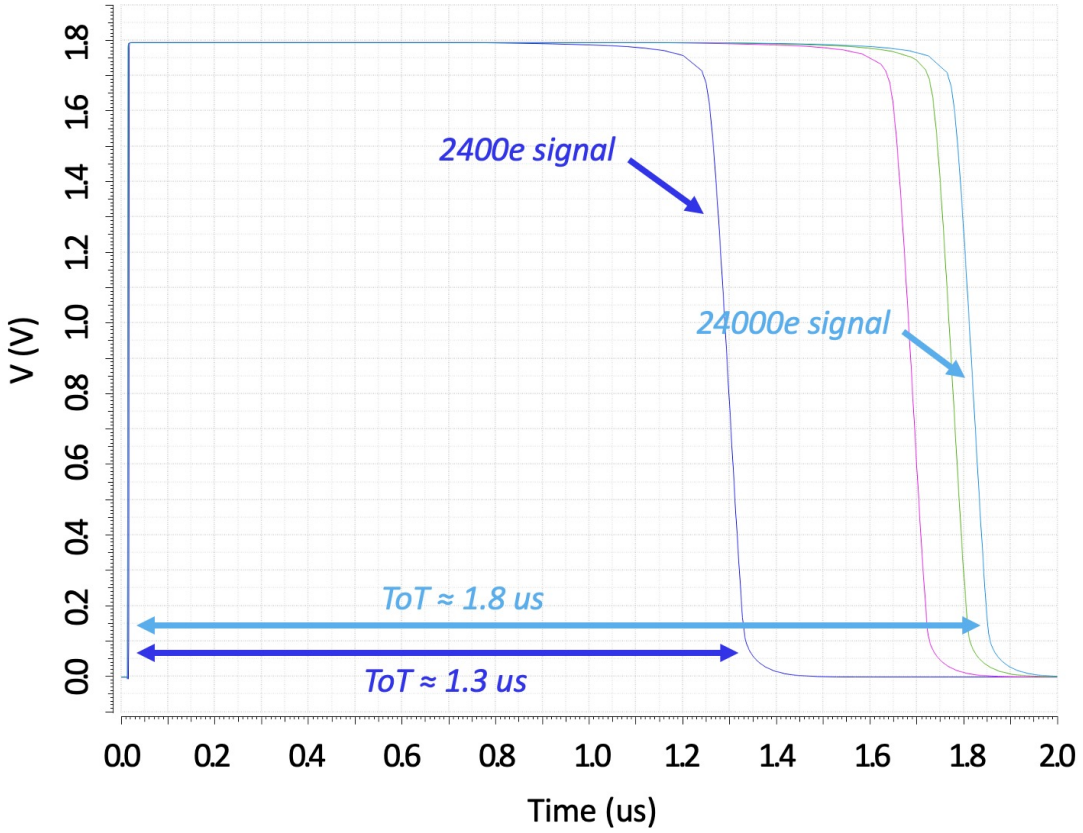
Schematic of the MightyPix1 Analogue Pixel (Source: Ivan Perić, KIT)

MightyPix1: Amplifier

- CMOS type amplifier inside pixel
- Equivalent Noise Charge: 67 e^- *(88 fF pixel capacitance)*
- Time walk: 2.4 ns *(2400 e^- to 24000 e^- signals)*

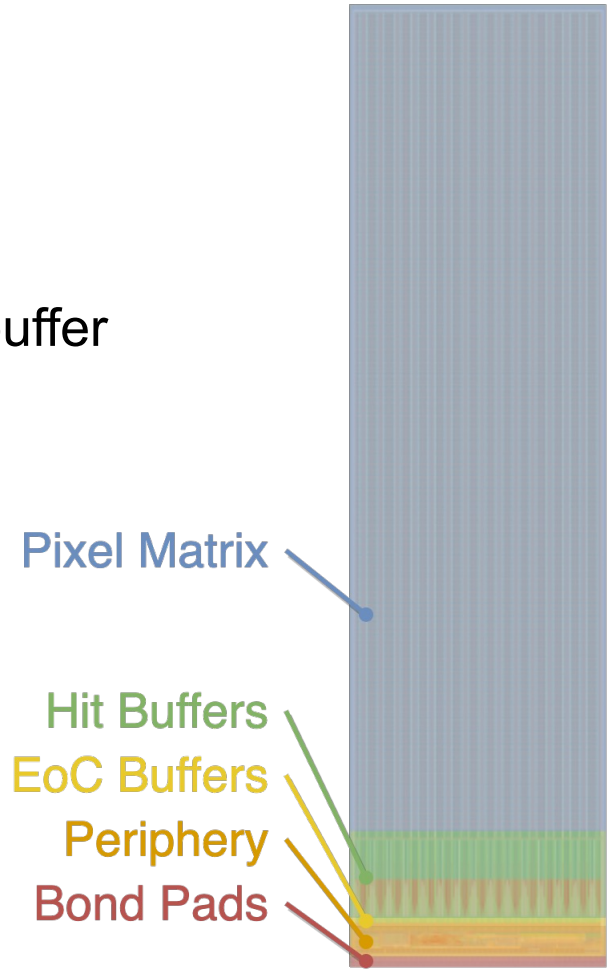


Schematic of the MightyPix1 CSA (Source: Nicolas Striebig, KIT)



MightyPix1: Digital Readout

- Readout driven by Readout Control Unit (RCU) FSM
- **Working principle:**
  - Every pixel has one hit buffer, where hit is stored
  - Data loaded from highest active hit buffer to End of Column (EoC) buffer
  - Data read from EoC buffer
  - For every hit a 2 x 32 bit data word is generated
  - Parallel scrambler analogue to VELOPix (optional)
  - Data sent to serialiser tree and sent off-chip



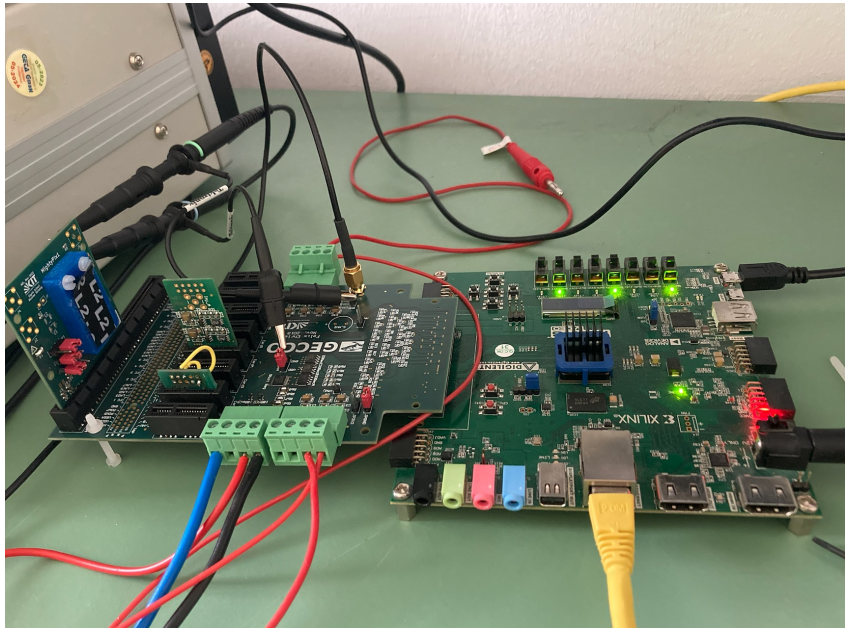
MightyPix1: LHCb Specific TFC Signals

- LHCb sends Timing and Fast Control (TFC) signals to all FE modules

- **BXReset:** Reset internal BXcounter to synchronise chips to same BX
- **Snapshot:** Capture number of received TFC commands (partially implem.)
- **FEReset:** Reset all modules except TFC receiver, BXcounter, chip configuration registers
- **Cal:** Could be used to control an on-chip injection circuit (not yet implem.)
- **Sync:** Chip outputs sync pattern, configurable via configuration register

Measurements: First results with MightyPix1

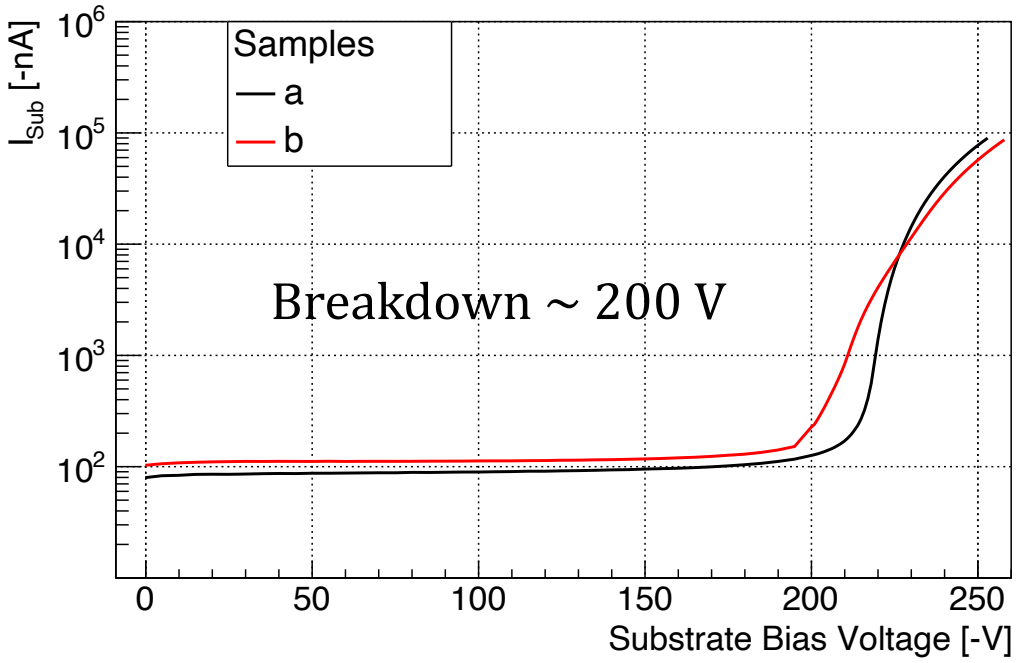
- First measurements started this summer
- Successfully tested basic functionalities and newly implemented digital interfaces
- Test beam with irradiated chips next year



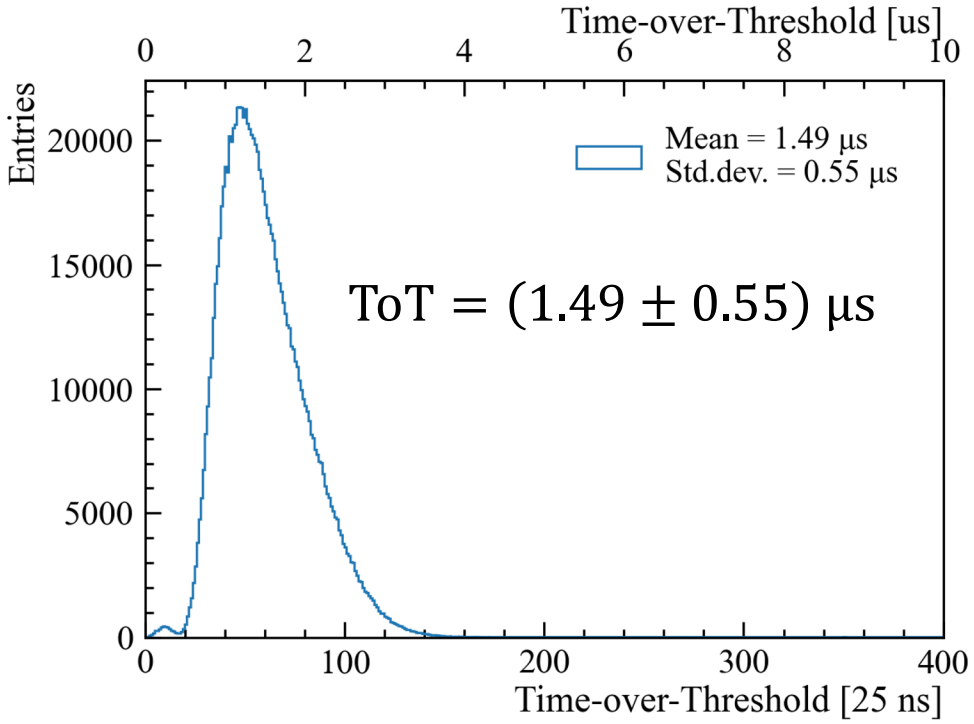
GECCO Setup at KIT for measuring MightyPix1

Measurements: First results with MightyPix1

- IV-curve to Measure Breakdown Voltage
  (J. Hammerich, University of Liverpool)

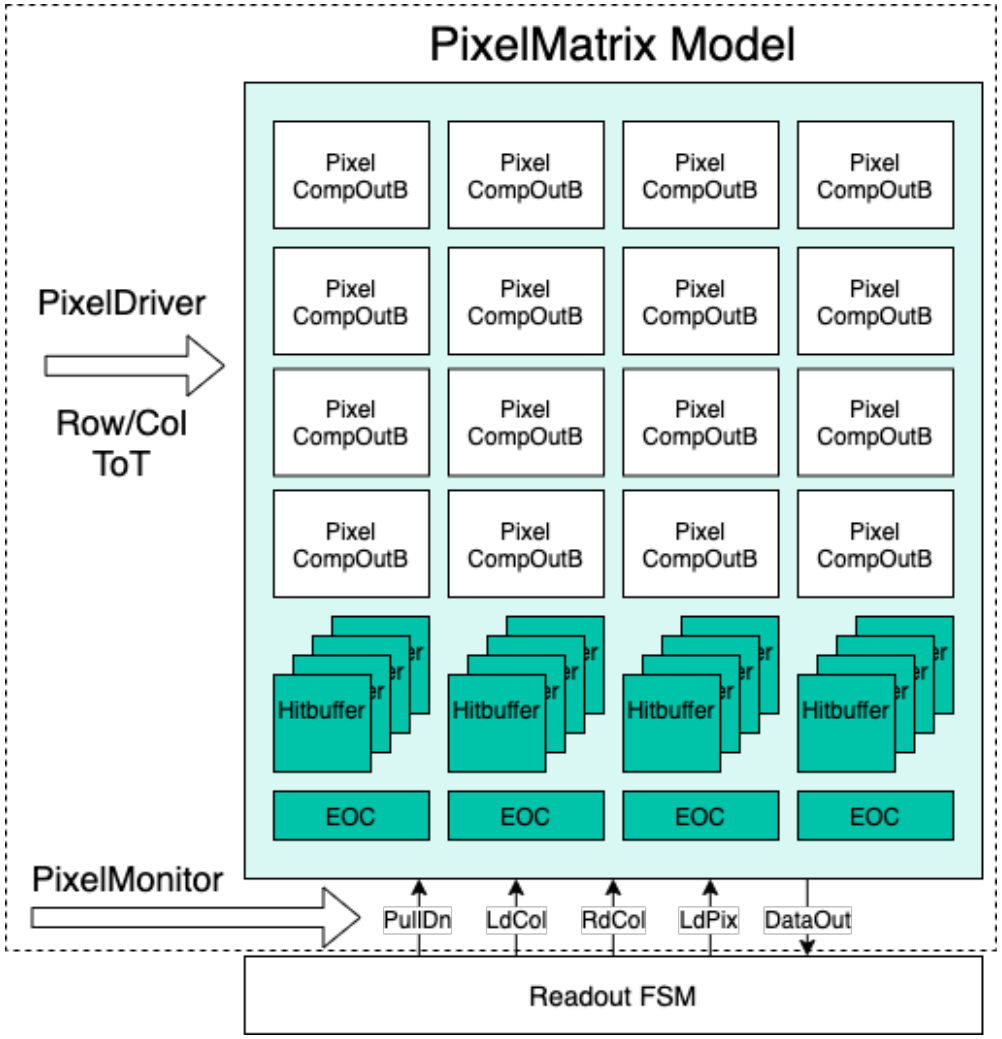


- Sr-90 ToT Measurement
  (L. Dittmann, University of Heidelberg)



Simulations: Efficiency of MightyPix1 Readout

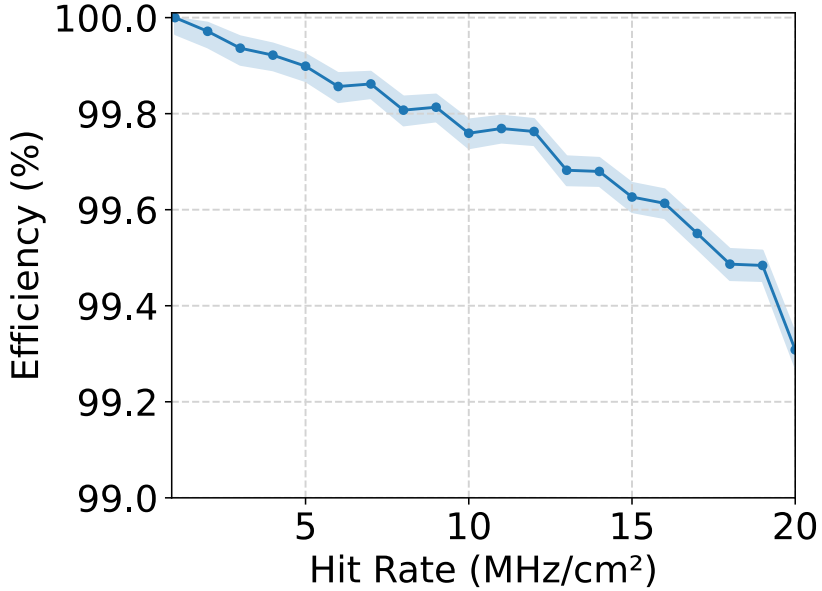
- ***Can MightyPix1 handle hit rates at LHCb?***
- Maximum hit rate at Mighty Tracker: 17 MHz/cm^2
- Test readout system in simulations
- Model of pixel matrix + synthesised digital design
- Simulated 500 000 events for different hit rates
- Fixed ToT to 2 us *(as worst-case scenario)*
- Limits to efficiency set by experiment:
  - Can maximally send 23.75 MHz/cm^2 off-chip through 1.28 Gbit/s readout link
  - Hits must be read out within 89.1 us, afterwards BXID repeats

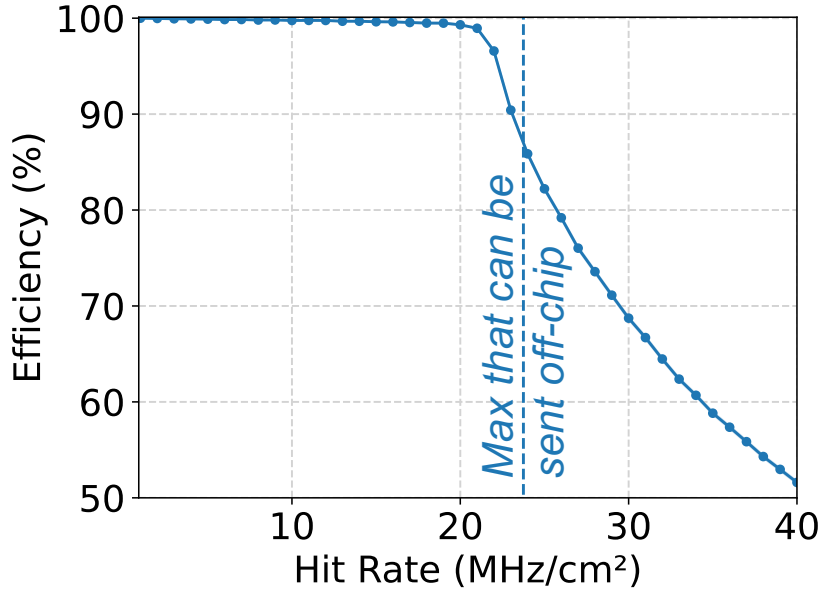


MightyPix1 Pixel Matrix Model (Source: Nicolas Striebig, KIT)

Simulations: Efficiency of MightyPix1 Readout

- Simulated efficiency of MightyPix1 readout mechanism > 99% up to 20 MHz/cm^2
- Drop at 21 MHz/cm^2 as readout times reach 89.1 us
  → Hit buffers not read out fast enough → new hits are missed

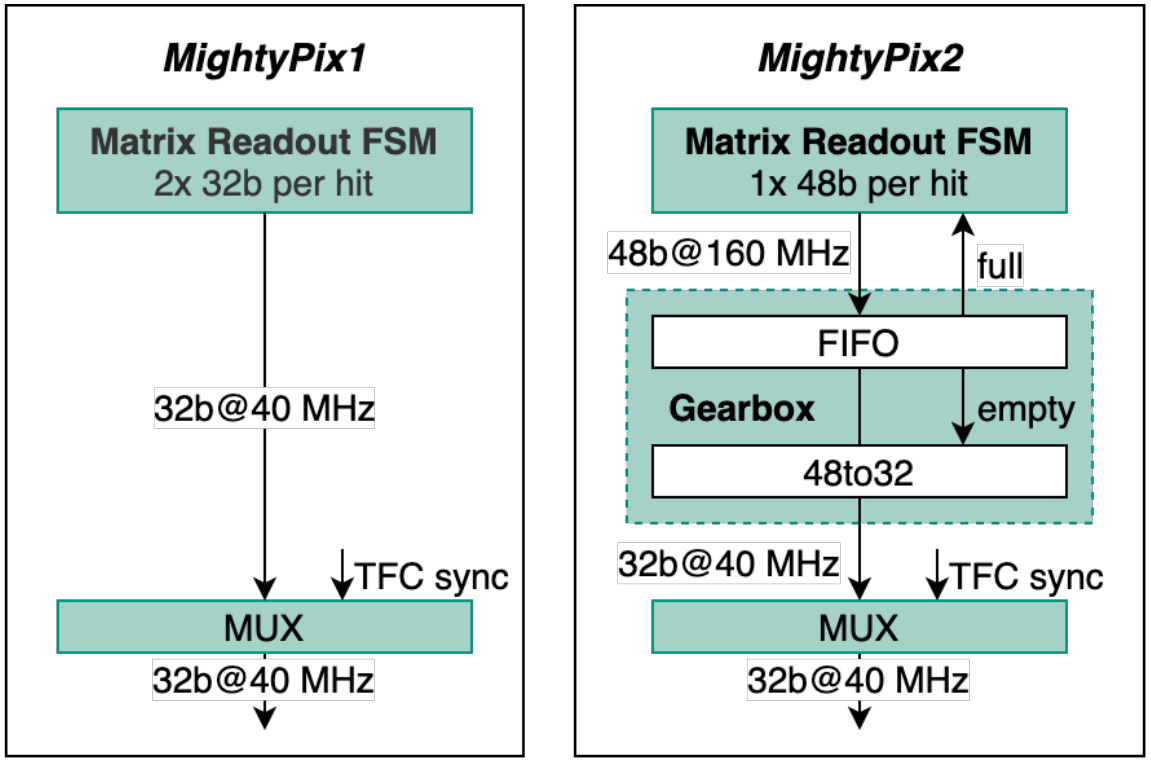




- *How can we speed up readout and increase efficiency?*

Towards MightyPix2: New Readout

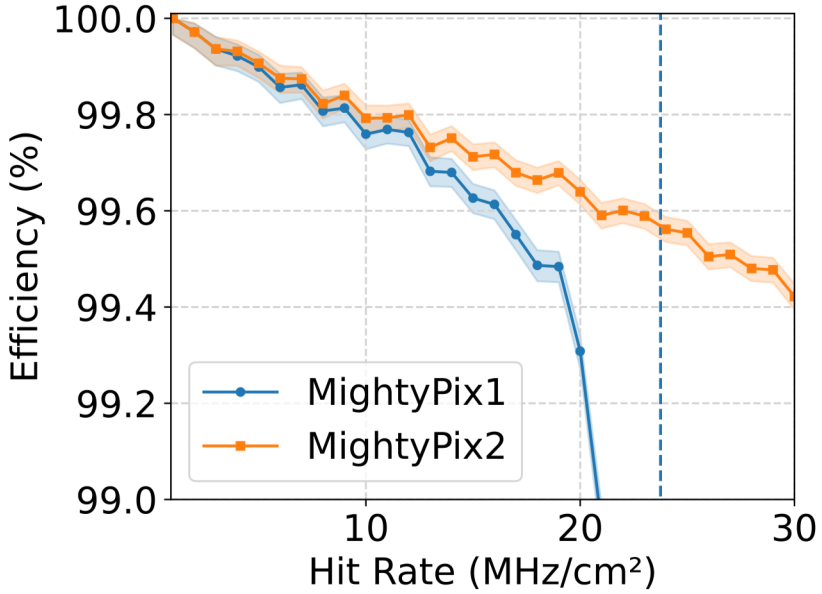
- Cannot increase readout link speed
- **Decrease data size:**
  - 2 x 32 bits per hit → 1 x 48 bits per hit
  - Can send **up to 31.66 MHz/cm²** off-chip
- **Increase speed of readout FSM:**
  - 32 bit at 40 MHz → 48 bit at 160 MHz
  - Hit buffers read out faster, less hits missed
- **New gearbox:**
  - FIFO of depth 16 stores hits before they're sent off-chip
  - Fit hit words into 32 bit format (1 hit = 1.5 x 32 bit)

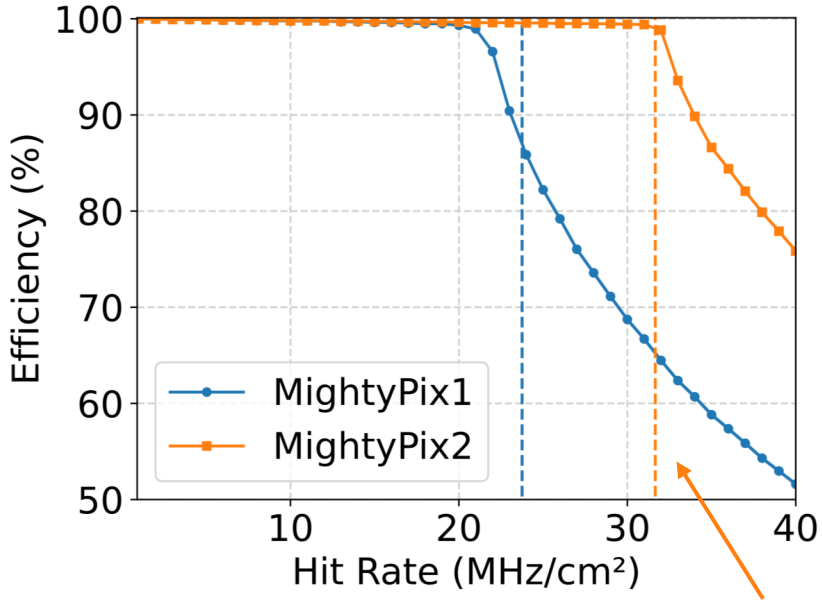


Improved Readout for MightyPix2
(Source: Nicolas Striebig, KIT)

Towards MightyPix2: Efficiency of New Readout

- Simulated efficiency of improved readout mechanism > 99% up to 31.66 MHz/cm^2
- Drop at 31.66 MHz/cm^2 as 1.28 Gbit/s readout link works at full capacity





Towards MightyPix2: Additional Features

- Fully compliant TFC interface
  - Improved Interface: Link training phase and lock phase, tolerant to transmission errors
  - Implementation of last TFC command (snapshot)
- Fast chip configuration
- Increased pad size
- Serial powering
  - Integrated Shunt-LDO Regulators for VDDA and VDDD

Summary

- MightyPix1
  - First monolithic active pixel sensor compatible with LHCb
  - Measurements in progress, basic functionalities tested successfully
  - Simulation of the readout mechanism show > 99% efficiency up to 21 MHz/cm^2
- MightyPix2 design in progress
  - Discussions on new features in progress
  - Simulations of improved readout mechanism shows > 99% efficiency up to 31.66 MHz/cm^2

References

[1] The LHCb Collaboration, Framework TDR for the LHCb Upgrade II - Opportunities in flavour physics and beyond, in the HL-LHC era, Tech. Rep. CERN-LHCC-2021-012, LHCB-TDR-023, CERN, Geneva (2021).

Backup

MightyPix1: Focused Ion Beam Surgery

- A load signal for the chip config was not connected correctly
- Fix idea: make one cut and one connection → Focused Ion Beam surgery
- First attempt by UK company did not work
- Second attempt by company in Netherlands worked!