A large area CMOS pixel sensor for particle detection

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on behalf of

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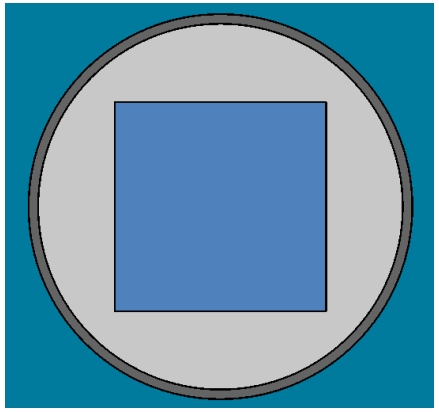
Outline

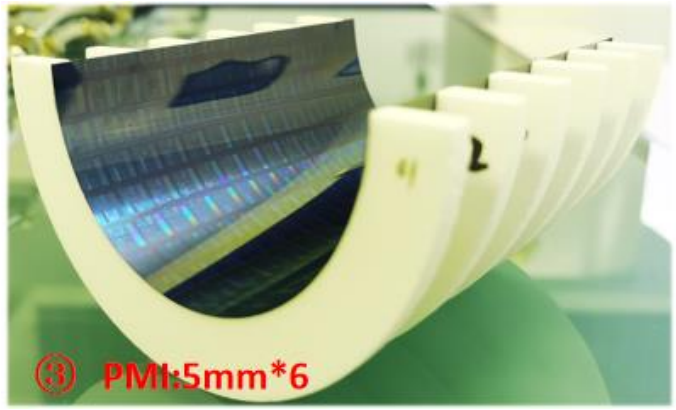
- **Motivation**
- **Wafer-scale CMOS pixel sensor R&D**
  - Architecture
  - Pixel circuit
  - Digital control and data processing
  - Prototype chip
  - Readout electronics
  - Wafer thinning and bending
- **Summary**

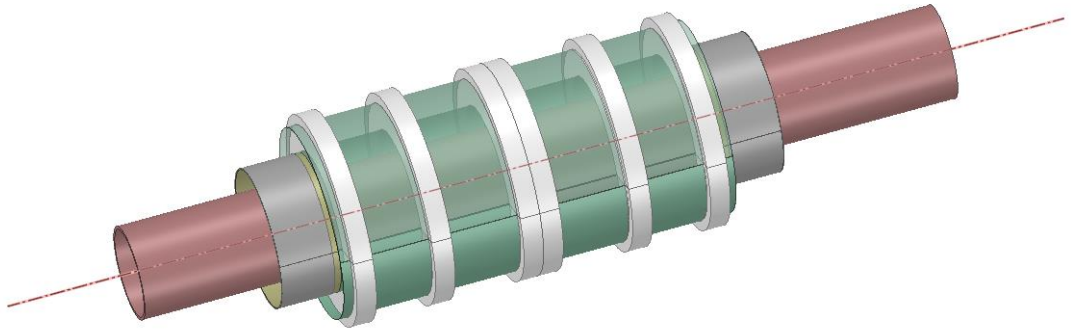
Motivation

- **Wafer-scale CMOS pixel sensor using stitching technology**
  - A wafer can be scribed into one die
- **Attractive features contributing to low material budget**
  - Bending with very thin thickness (~ 50 μm)
    - ✓ Less support material
    - ✓ Need few chips to make a barrel
  - Low power consumption
    - ✓ The power mainly concentrated on both sides
    - ✓ Cooling outside the sensitive area
    - ✓ Less electronics required
- **High potential for particle detection**
  - Being developed @ CERN for the ALICE-ITS3
  - For the inner tracker of BESIII, CEPC ....



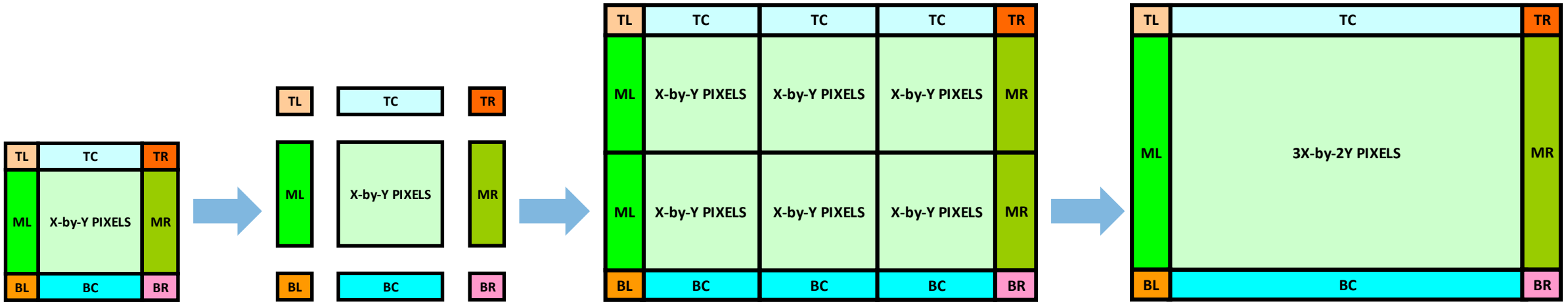
wafer





Wafer-scale CMOS pixel sensor

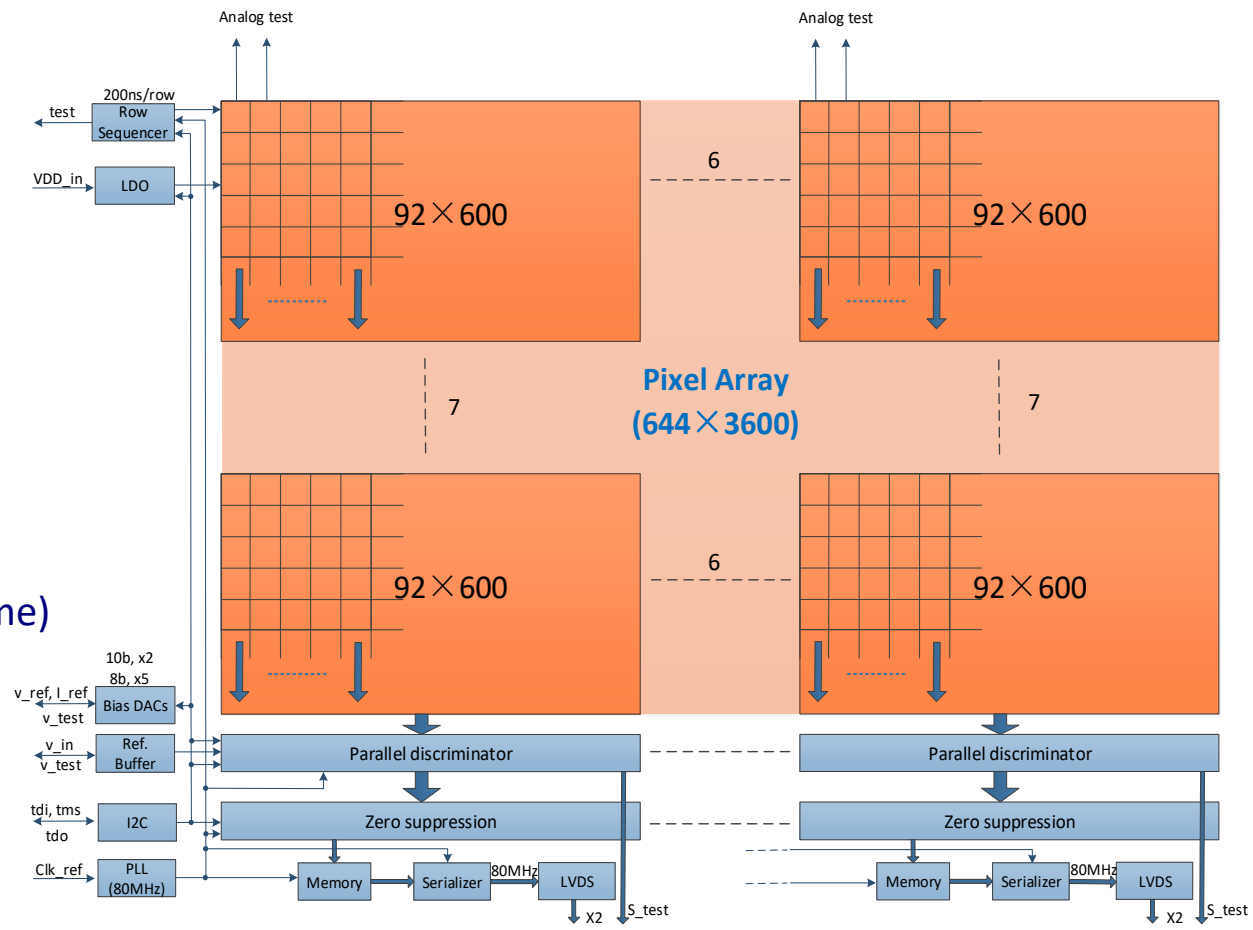
- The reticle size of the chip is about few cm^2
- Stitching technique merges multiple structures to realize larger chip
- Stitching components
  - 9 segments: TL, TC, TR, ML, MC, MR, BL, BC, BR
  - 2-D stitching to make wafer-scale



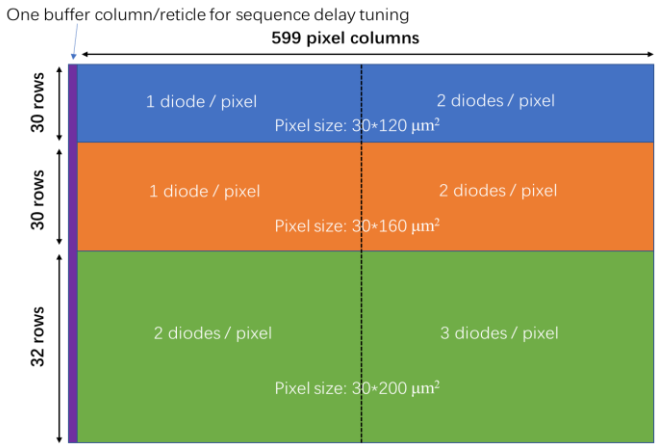
Reticle size

Chip architecture

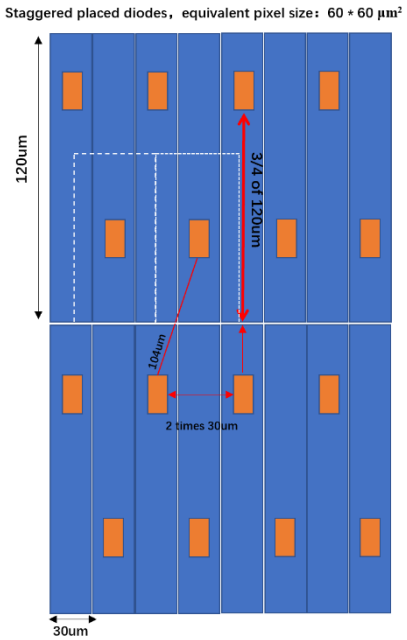
- **350 nm CIS process**
  - Epitaxial layer: thickness 14 µm, resistivity 500 - 2kΩ·cm
  - 4 metal layers
  - No deep P-well: PMOS cannot be used in pixel circuit
- **Total size**
  - ~11×11 cm^2 (only one die in a wafer)
- **Pixel array (42 segments)**
  - Basic pixel array: 92 rows × 600 columns
  - After stitching: 644 rows × 3600 columns
  - Rolling shutter readout mode (200 ns/row, ~129 µs/frame)
- **Full functional chip**
  - Analog test point for pixel array
  - Column-level discriminator
  - On-chip zero suppression
  - Interface: Bias DAC/Buffers/I2C/PLL/LVDS/LDO ……
- **Submitted in Feb 2023**

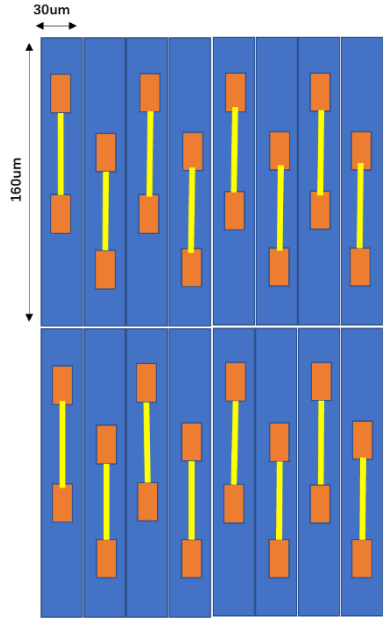


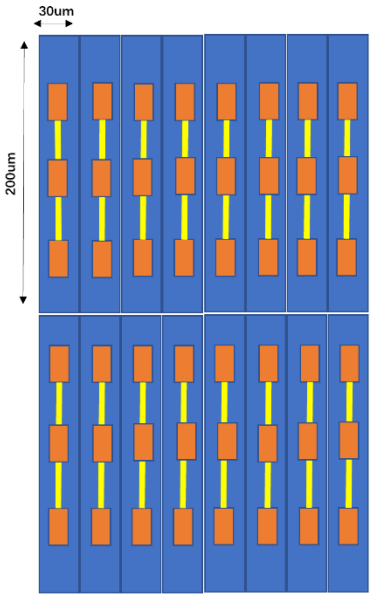
Pixel architecture and column readout



Basic pixel array with 6 submatrices

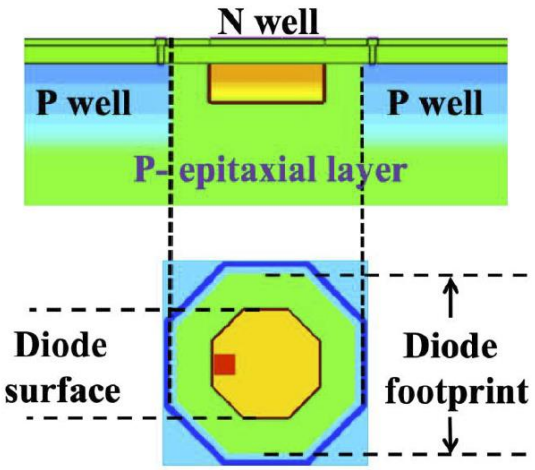






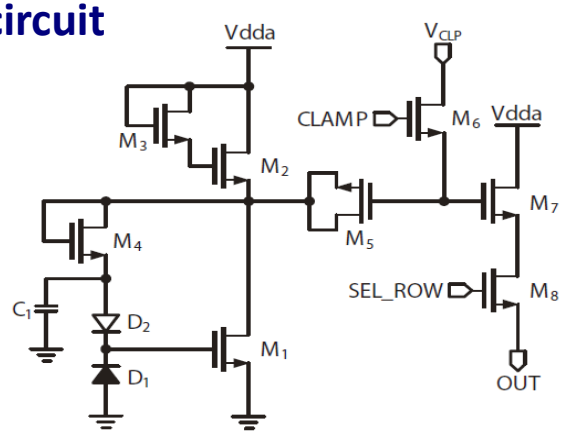
- **Rectangular pixels: increased readout speed**
  - rϕ : 30 μm
  - Z : 120/160/200 μm
- **6 submatrices:** study charge collection and charge sharing
  - Different pixel sizes and diode arrangements
- **Octagonal diode:** 20 μm²
- **Diode surface/footprint:** 0.1

3 different diode arrangements are used

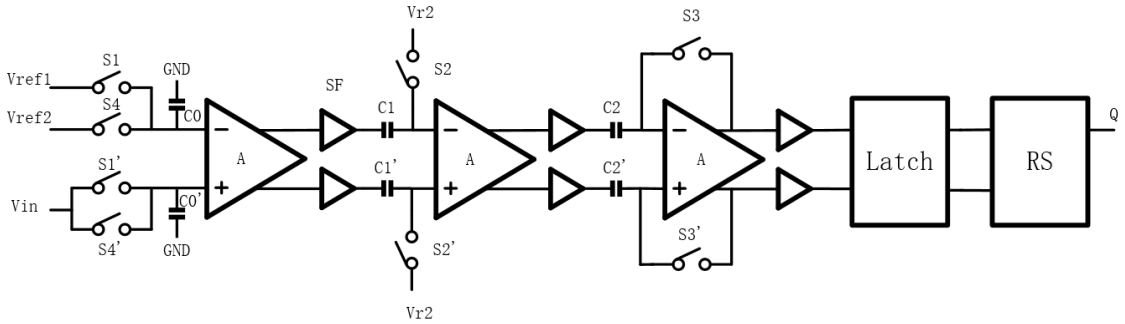


Pixel architecture and column readout

In-pixel circuit



Column-level discriminator



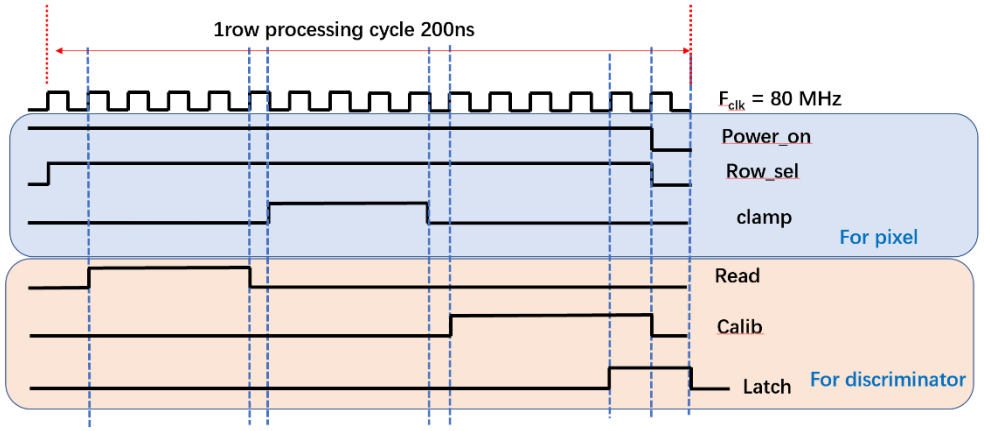
Diodes No.	Amp. Gain	SF	CVF [µV/e⁻]
1	14	0.8	135
2	13.5		75
3	11		40

*Reference: A.Dorokhov, "Optimization of amplifiers for Monolithic Active Pixel Sensors", IPHC

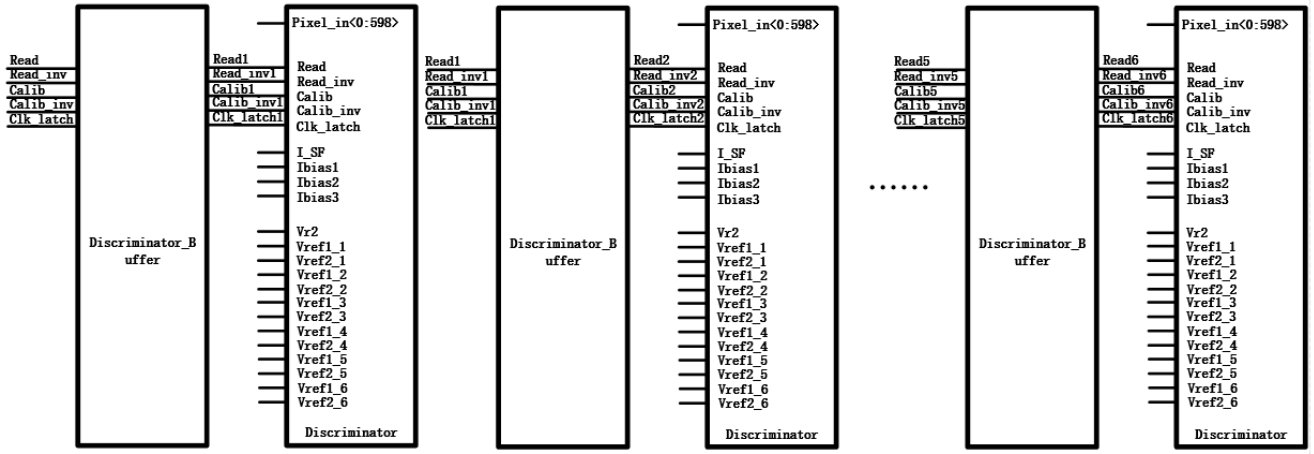
Discriminator performance:

- ❑ Auto-zeroed architecture
- ❑ Threshold: V_{ref1}-V_{ref2}
- ❑ Power consumption: 134 µW
- ❑ Area: 30×290 µm^2
- ❑ Thermal noise: 158 µV

Pixel architecture and column readout



Timing for pixel and discriminator: 200ns @ 80 MHz clock



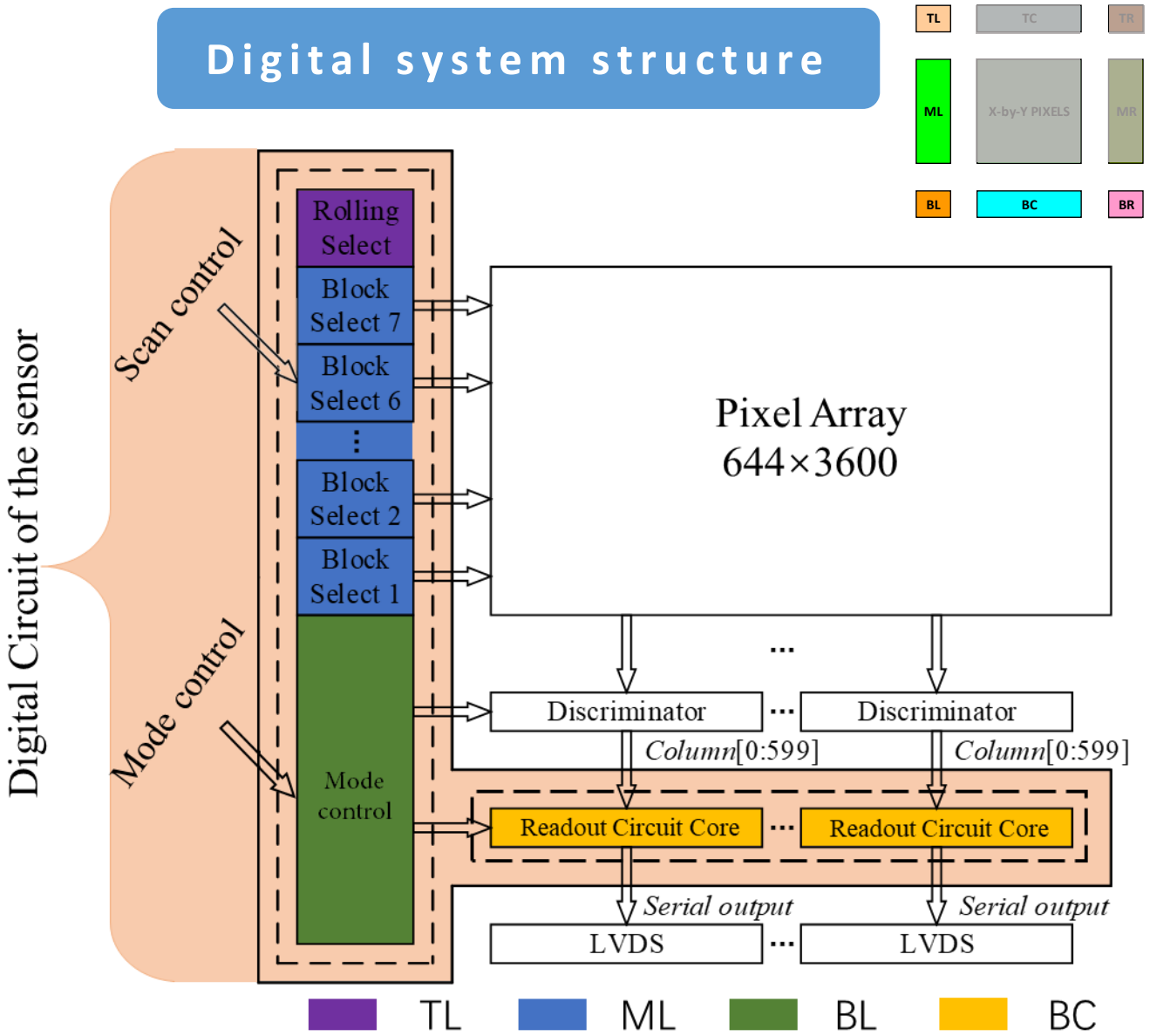
Combination of total 3600 column-level discriminators

- **Basic clock 80MHz**
  - 200 ns/row
  - Readout time: ~ 129 µs/frame
- **Power consumption**
  - ~ 25 mW/cm^2 (pixel matrix area)

- **Every 600 columns driven by one buffer**
  - Improve driving capability, reduce delay time, keep timing matching
- **Threshold voltages Vref1 & Vref2 are divided into 6 groups**
  - Increase driving capability, reduce settling time

Digital control and data processing

Digital system structure



Functions

Scan control

- Provide rolling shutter sequence
- 7 segments with 92 rows each

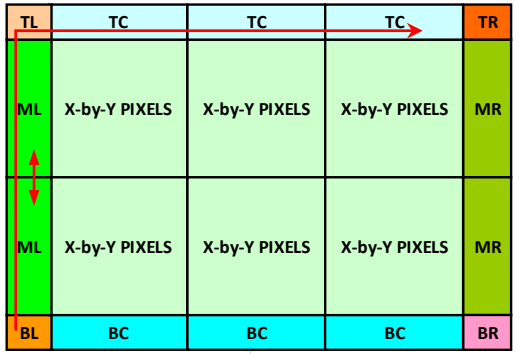
Mode control

- Integrate interactive interface
- Change working mode & generate control signal

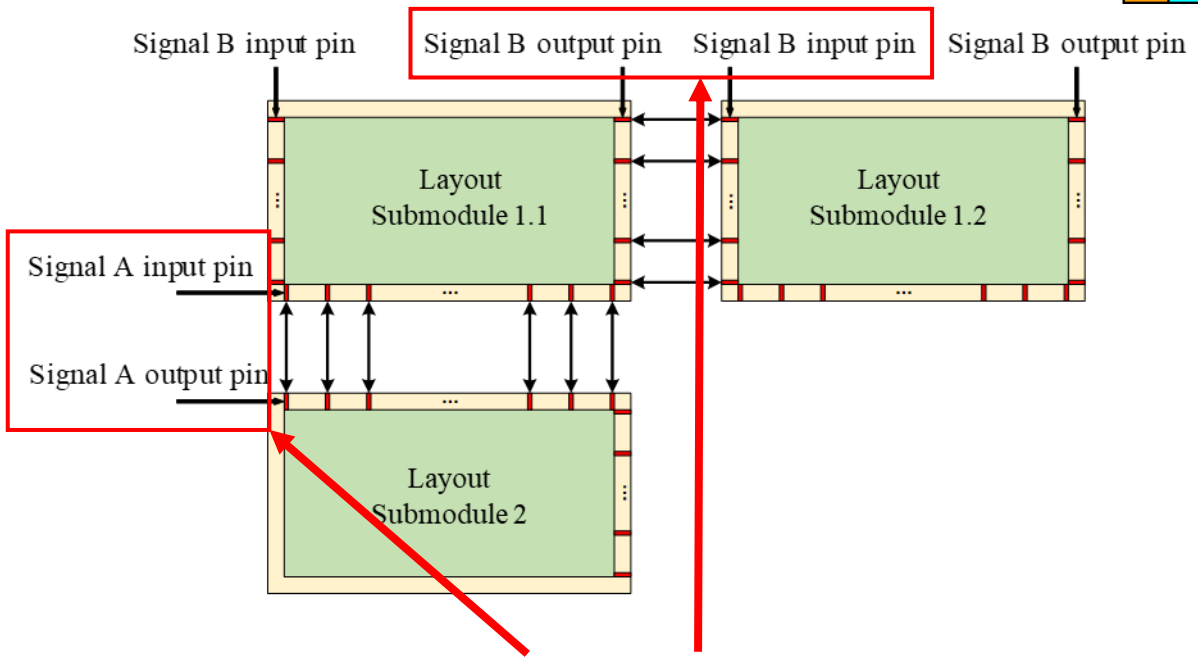
Readout circuit

- zero suppression, storage and serial output
- Composed of 6 segments with 600 columns each

Digital control and data processing

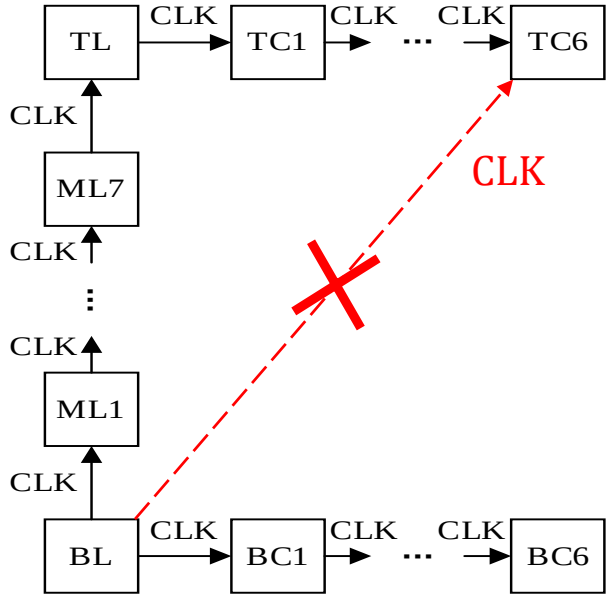


Signal transmission between segments



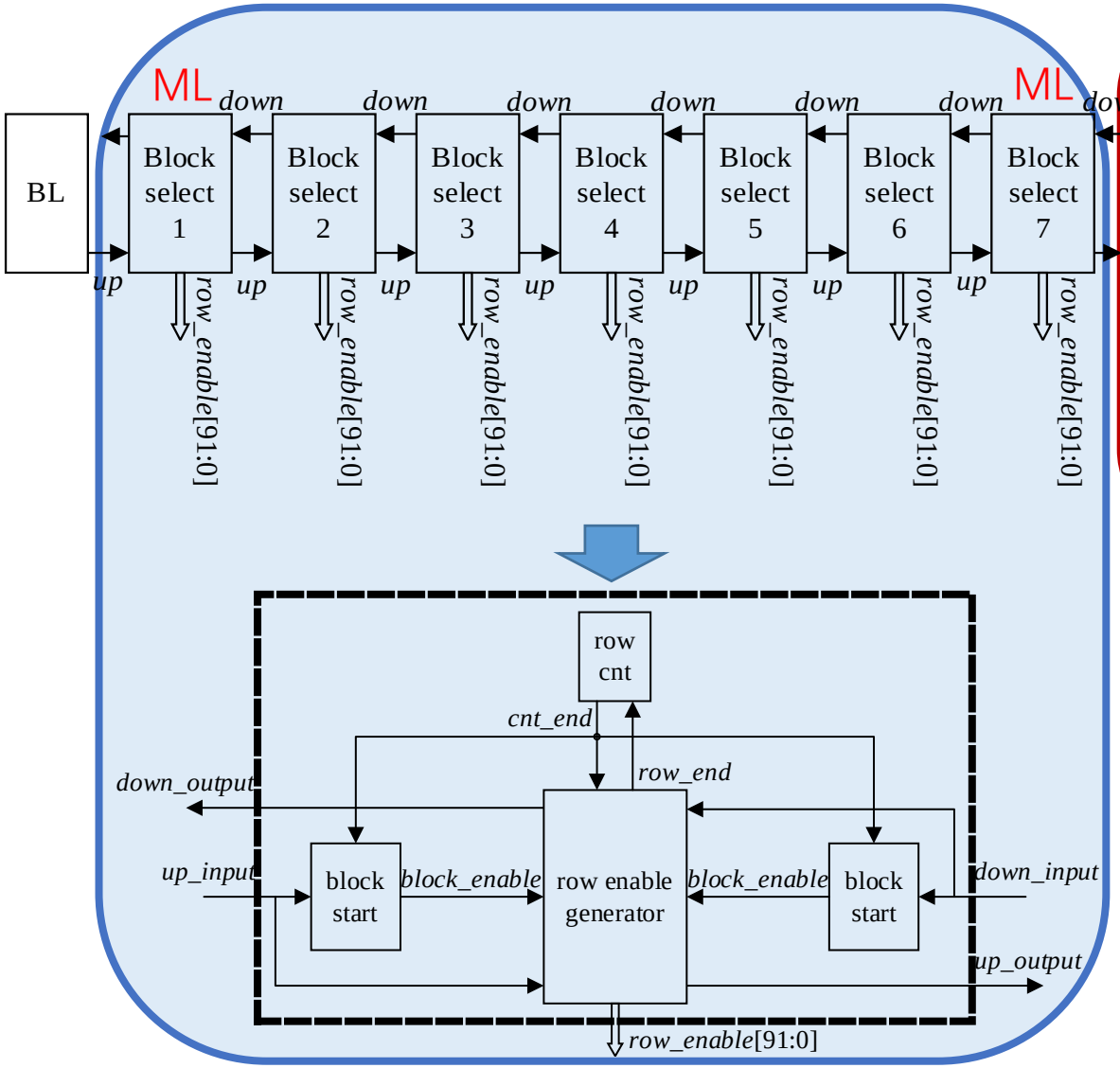
Pin-position between sub-modules MUST be matched

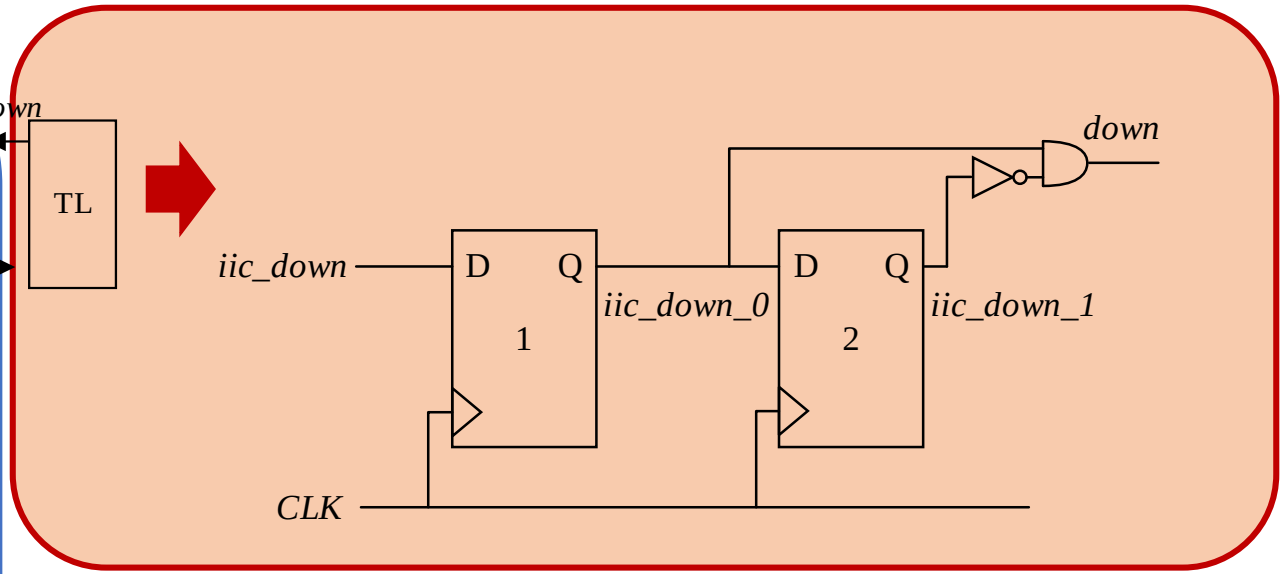
Place & route in long distance



Cross-module signal transmission route MUST be carefully planned

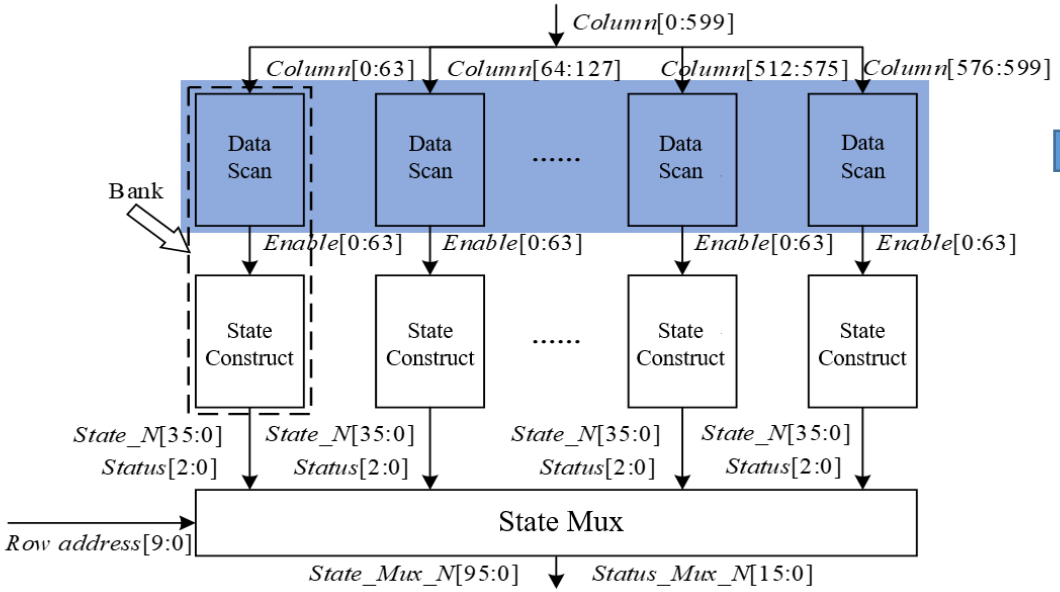
Digital control and data processing – scan control

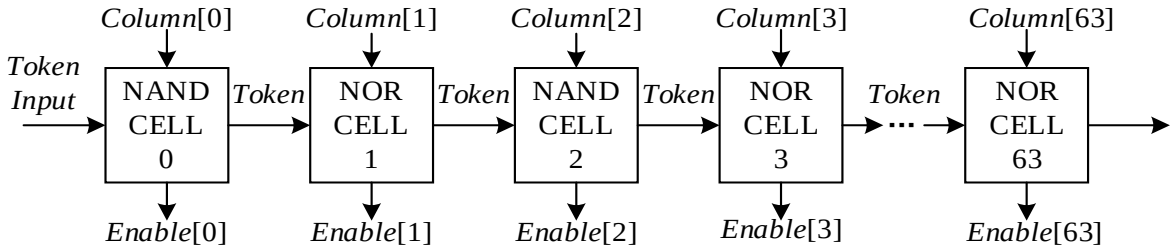


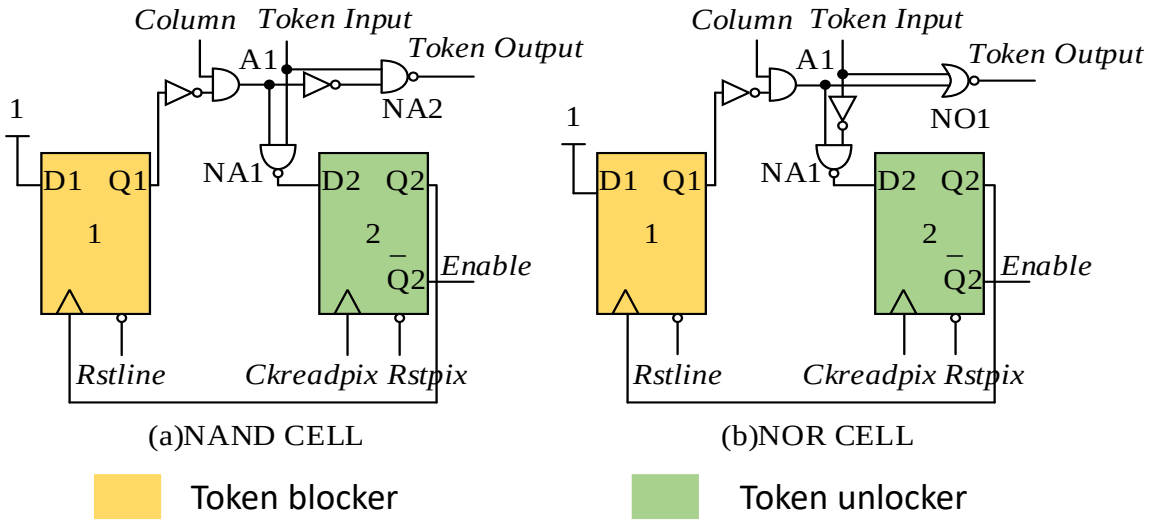


- 7 segments of ML to scan 644 rows
- Each segment is the same
- Two kinds of readout timing: top-down/bottom-up

Digital control and data processing – readout circuit

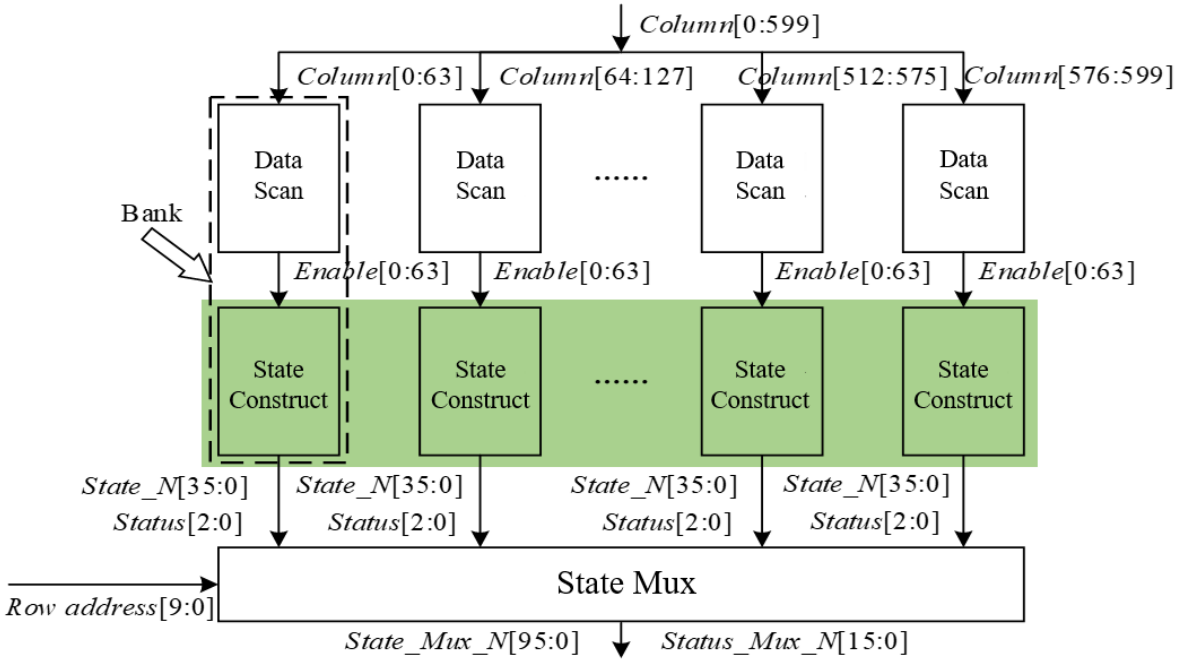


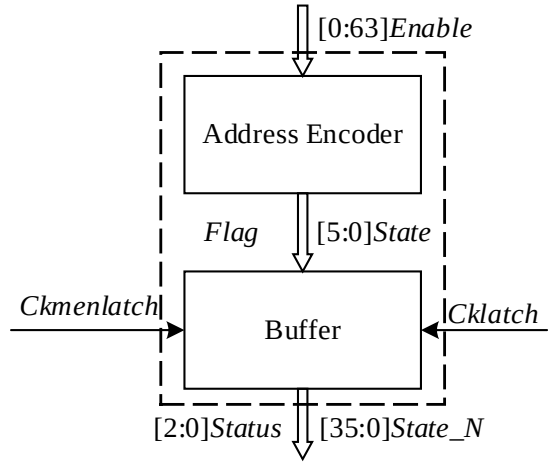




- The column outputs are divided into 10 groups, each group consisting of data scan and state construct.
- **Token blocker:** if there is a signal in the column, the token is blocked.
- **Token unlocker:** if the token is blocked, 'enable' is valid and the token is unlocked after the next input arrives.
- Through the token chain, the hit is readout one by one with a 64-bit data format.

Digital control and data processing – readout circuit





- **Address encoder:** encode the 64-bit wide Enable signal into a 6-bit wide state.
- **Data buffer:** collect all the states in a bank and encode into status.

State

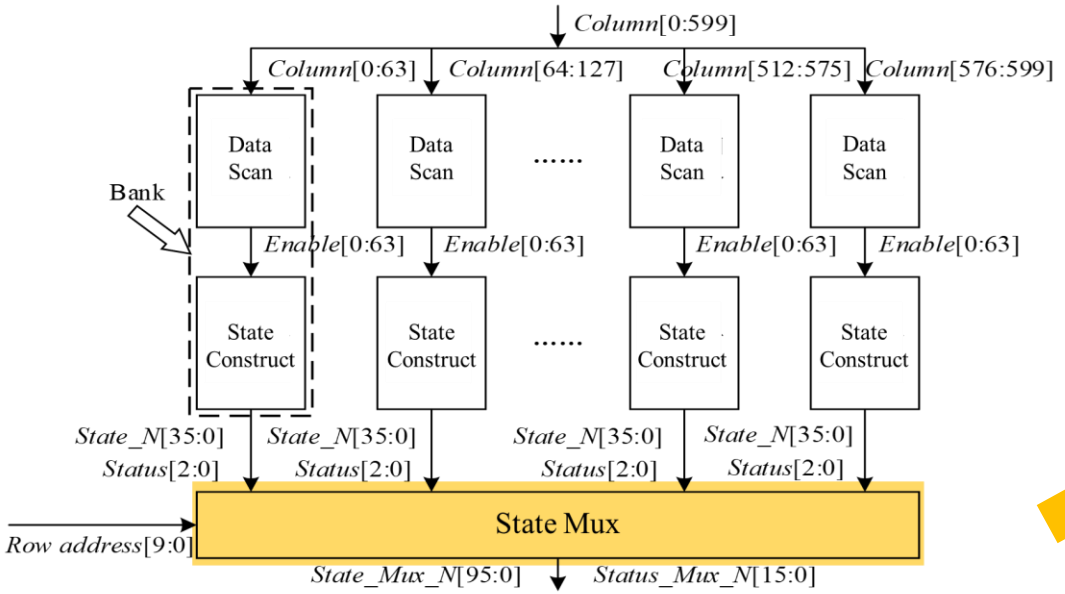
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0										
Mark						Address of BANK				Address in BANK					

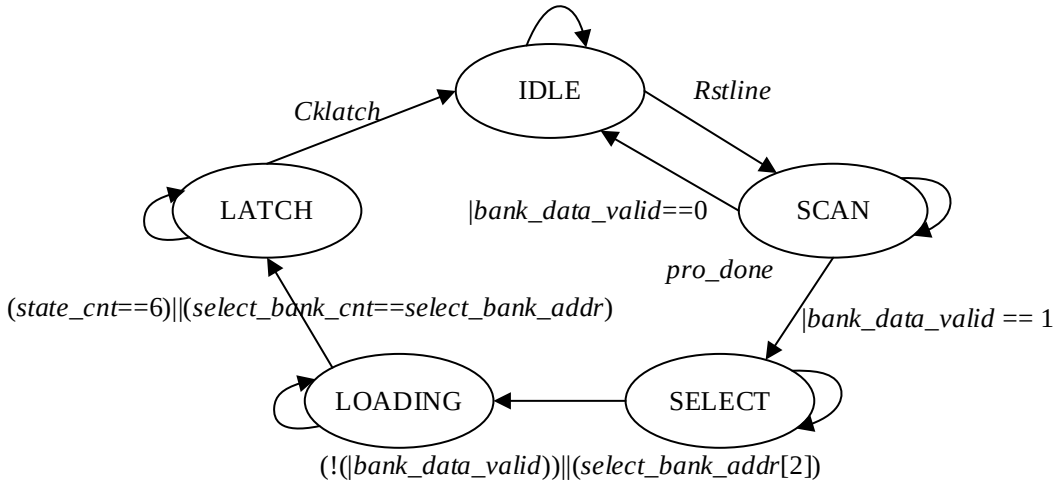
Status

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	0													
Mark			Number of State			Row address									

To be encoded Already encoded

Digital control and data processing – readout circuit





- **State mux:** Add Row and BANK address to status and state, respectively
- **Data compression ratio:** according to the physics environment, there are maximum 40 pixels in a column of reticle. 77: 1

State

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0										
Mark						Address of BANK				Address in BANK					

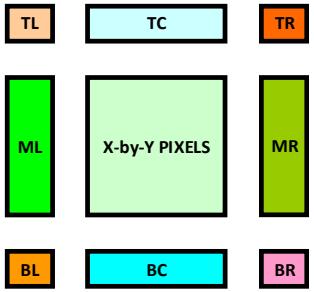
Status

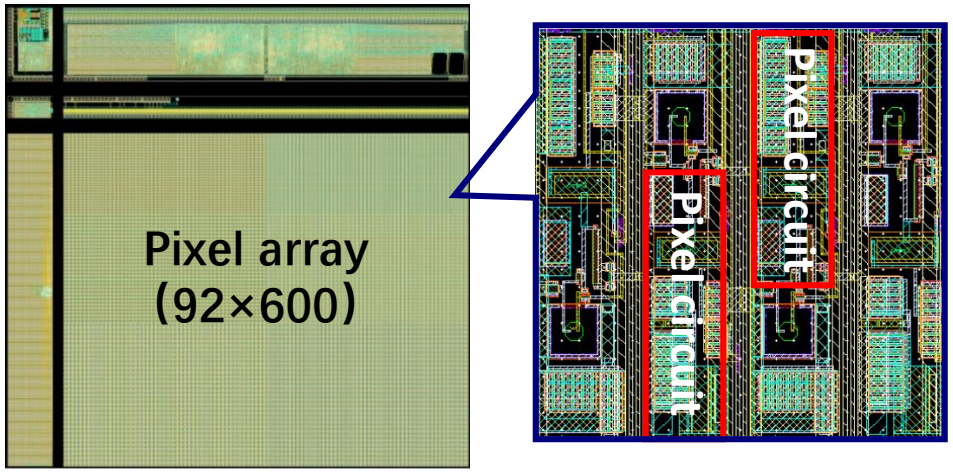
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	0													
Mark			Number of State			Row address									

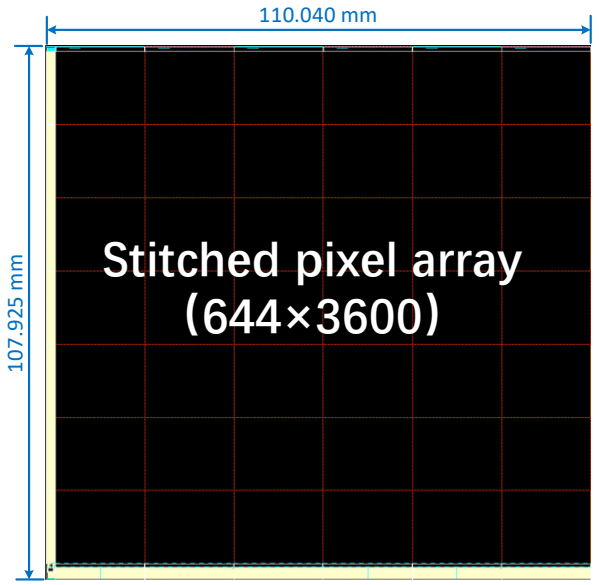
Encode during state mux Already encode

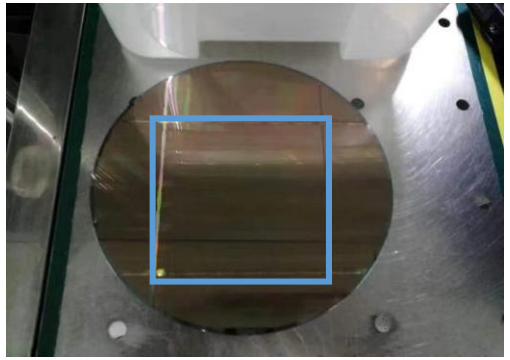
Prototype chip

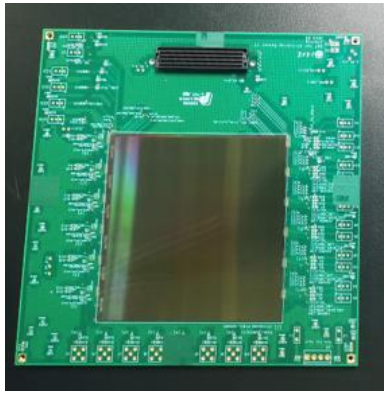
- **Reticle floorplan**
  - Area: ~ 2 × 2 cm^2
  - 9 groups of modules
    - TL,TC,TR,ML,MC,MR,BL,BC,BR
    - Pixel array in a reticle: 92 × 600
- **Stitching**
  - Area: ~ 11 × 11 cm^2
  - Pixel array
    - 7 rows and 6 columns
    - Total pixel array: 644 × 3600







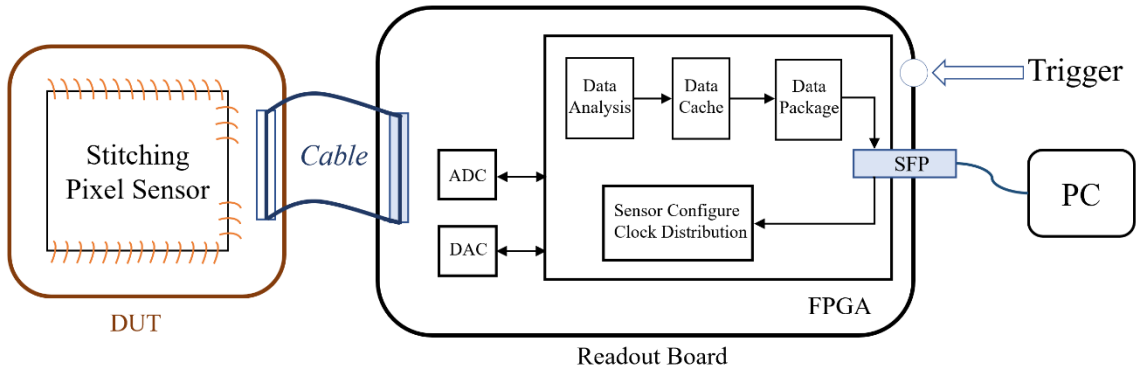


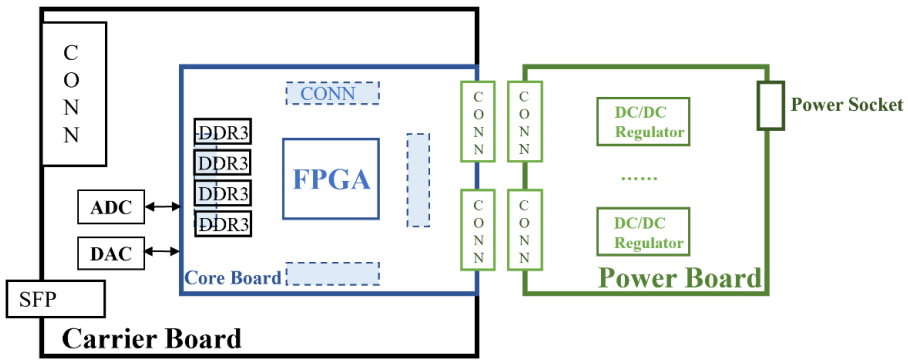


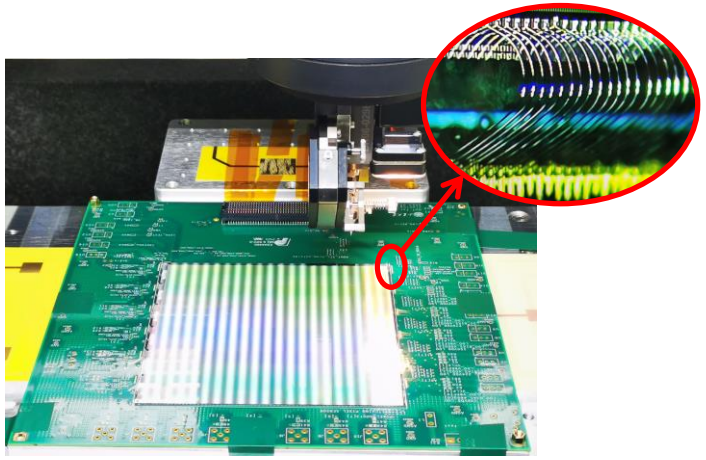
8 inch wafer
(die size 11 cm × 11 cm)

Readout electronics

- **DUT board**
  - Few components, connector, wire bonding
- **Readout board**
  - FPGA core board: XC7K325T, DDR3
  - Carrier board: ADC, DAC
  - Power board: supply different voltages
  - The chip is under testing

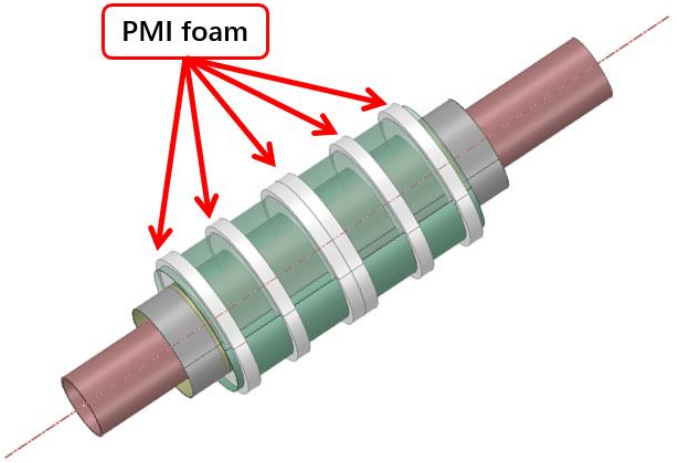


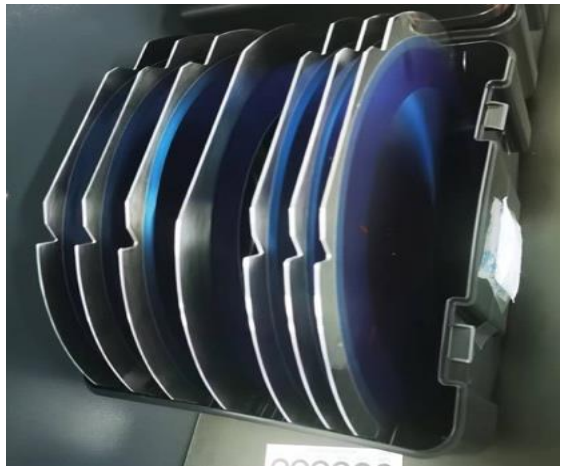


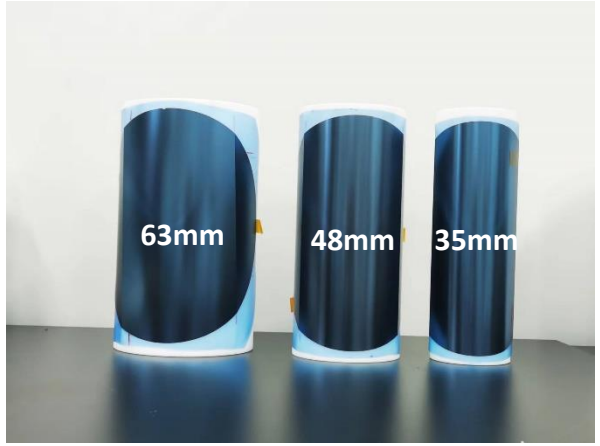


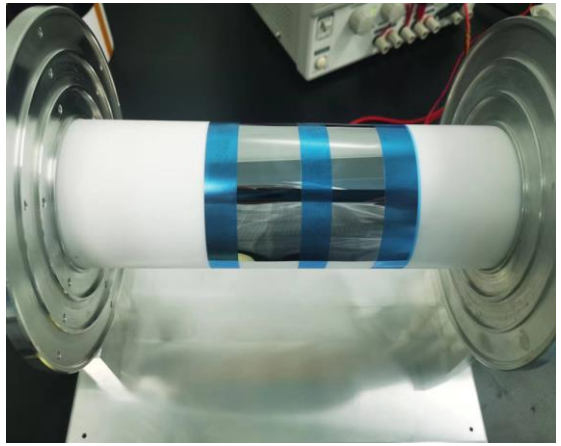
Wafer bending and bonding study

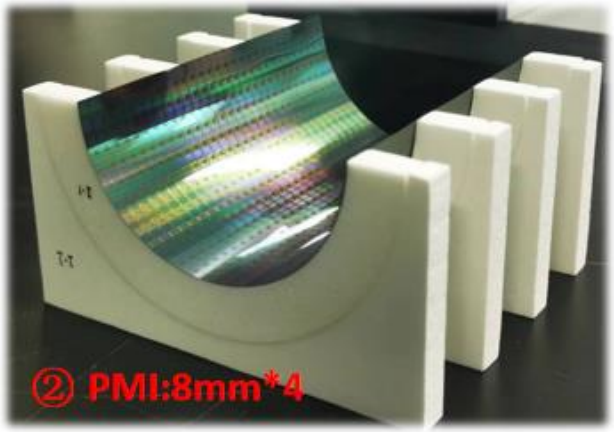
- **Dummy wafer is thinned down to 50 µm**
- **Wafer bending with different radii**
- **Ring support**
  - Wafer bending and fixed with glue
  - PMI: high strength, low material, mass density is about 0.05g/cm^3

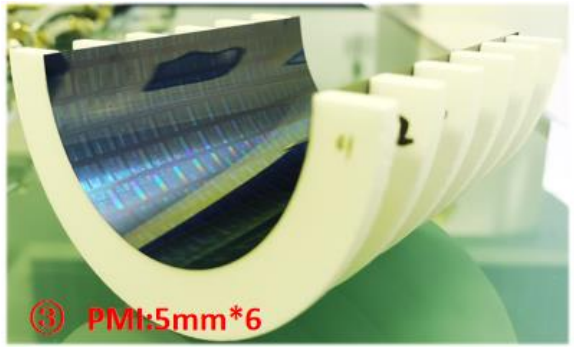








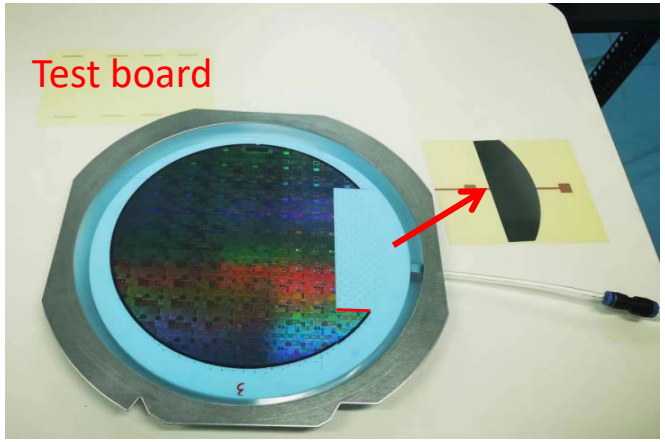


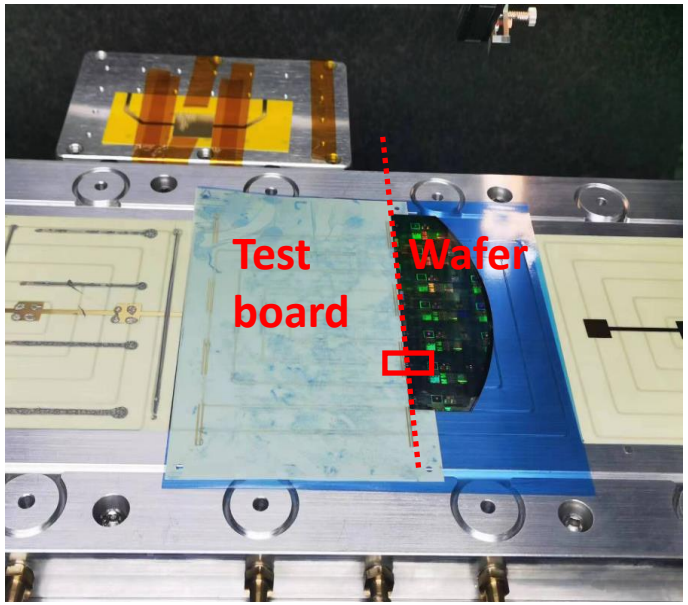


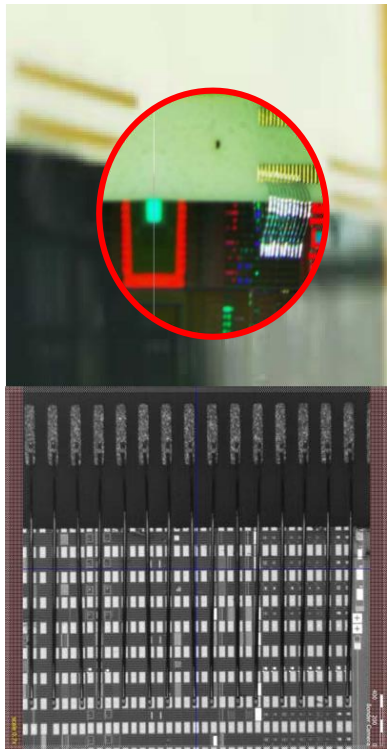
Wafer bending with radii 63mm, 48mm and 35mm

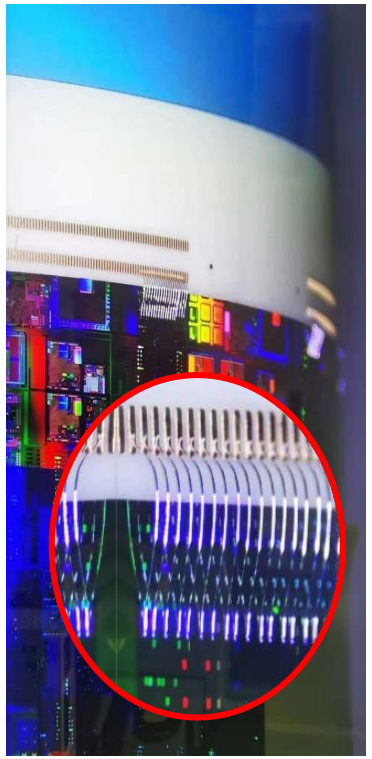
Wafer bending and bonding study

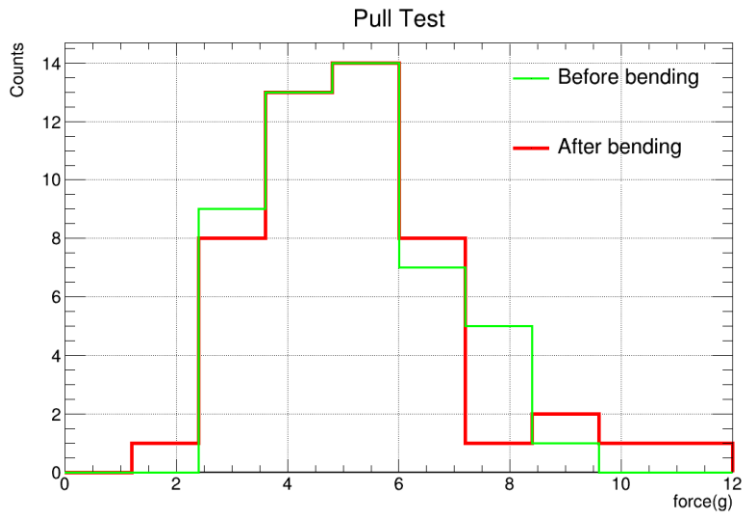
- **Wire bonding with thinned dummy wafer**
  - Dicing a part of dummy wafer
  - Wire bonding with test board
  - The wire shape doesn't change after bending
  - The pull test shows not much change











Summary

- The thinned wafer-scale CMOS pixel sensor will have extremely low material budget, having a high potential for the inner tracker.
- A wafer-scale prototype sensor has been developed, and now is under testing.
- Wafer thinning and bending have been done, and they perform well so far.

Acknowledgements

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Thanks