Status of the ARCADIA project for the implementation of innovative CMOS monolithic sensors

CEPC 2023

23-27 October 2023, Nanjing

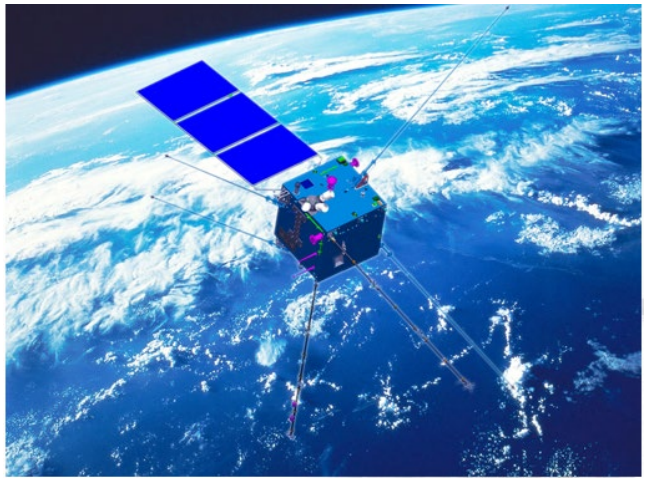
Davide Falchieri

INFN Bologna, Italy

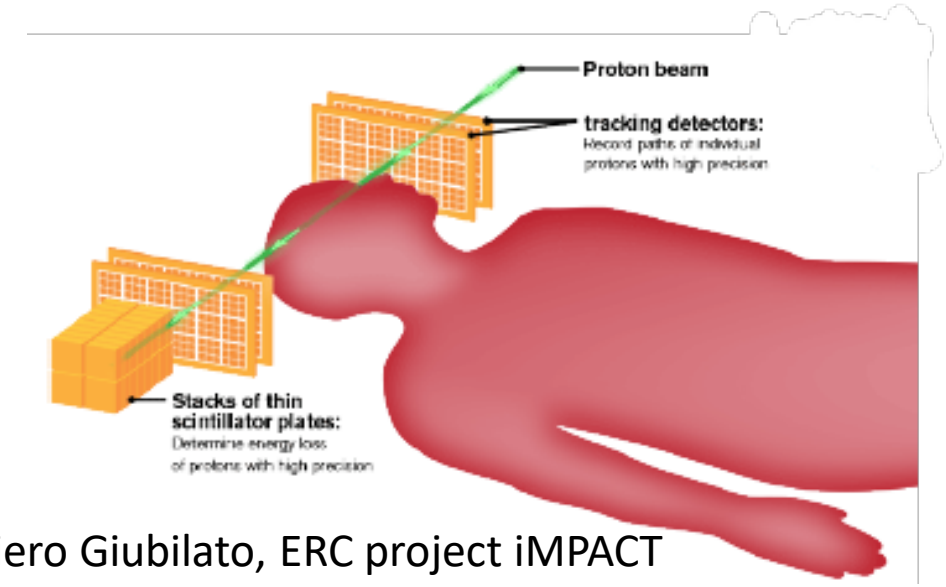
on behalf of the **ARCADIA collaboration**

Motivations of Arcadia

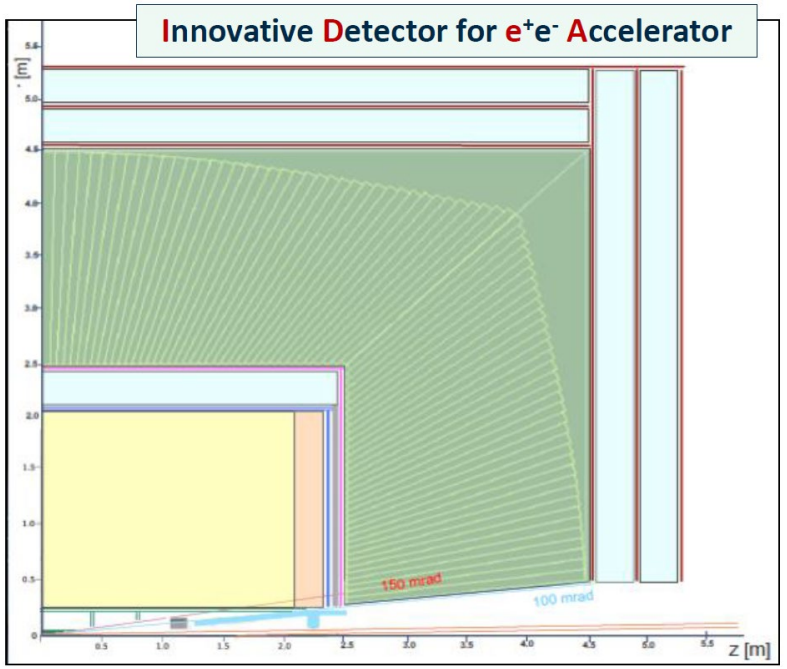
- Large-area **monolithic pixel detectors for particle tracking**: low power, high-rate capability, low cost per unit area, low material budget
- Target **applications**:
  - medical imaging (e.g. Proton Computed Tomography)
  - astro-particle detection on satellites
  - high energy physics experiments



CSES-01 http://cses.roma2.infn.it

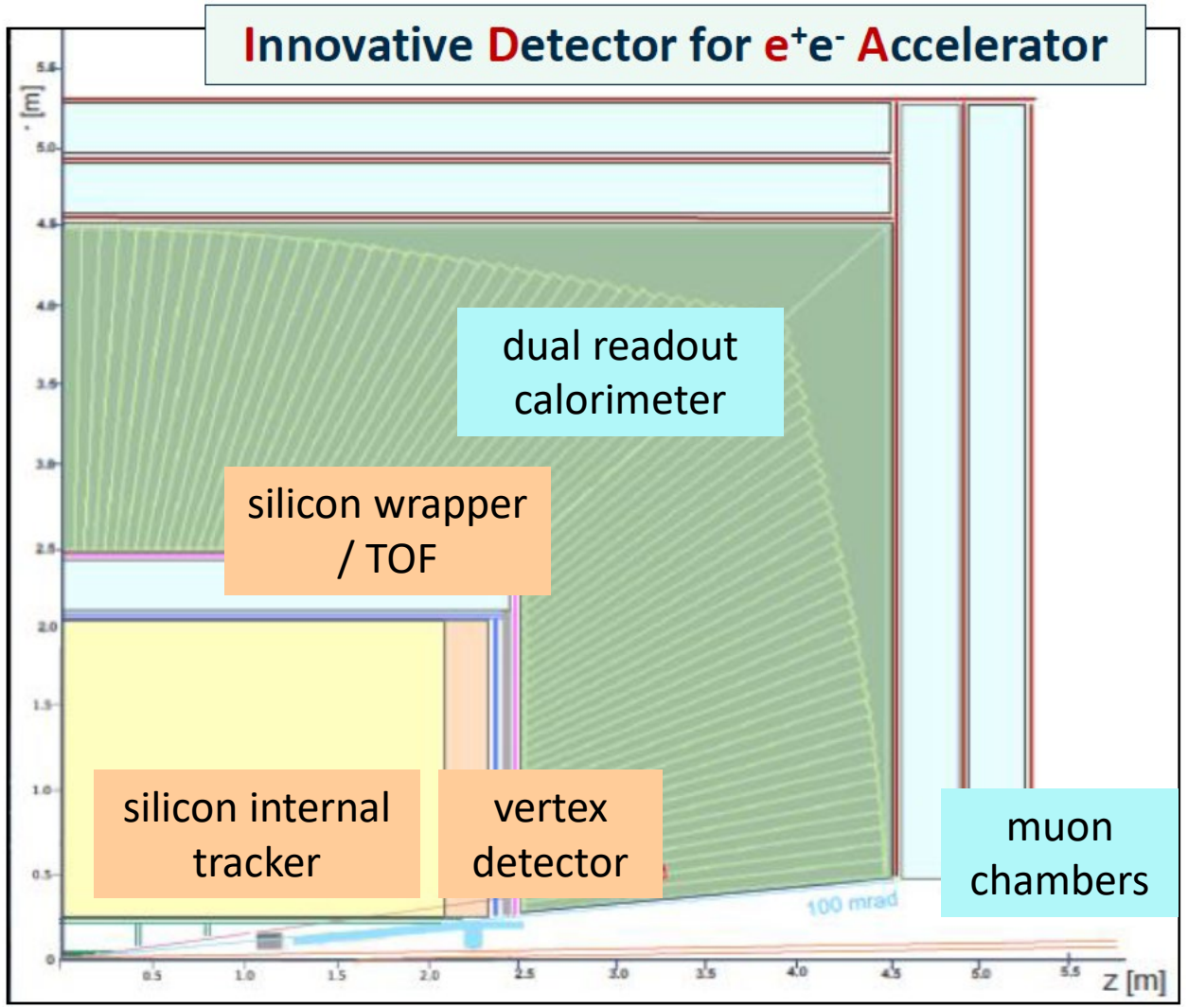


Piero Giubilato, ERC project iMPACT



IDEA

The IDEA concept



Arcadia is designing possible solutions for high precision silicon detectors:

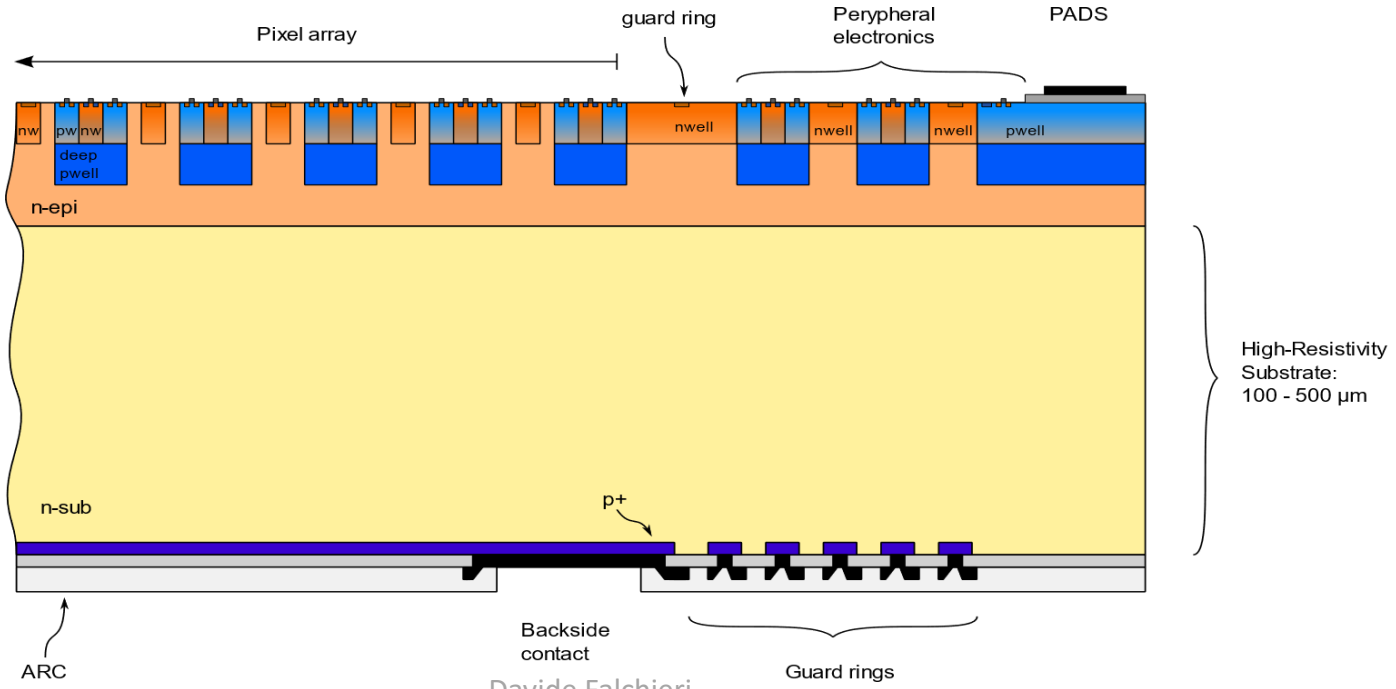
- vertex detector
  → pixel detectors (FDMAPs)
- silicon internal tracker
  → strip detectors (FDMAMs)
- silicon wrapper / TOF
  → pixel detectors with fast timing

Arcadia:

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

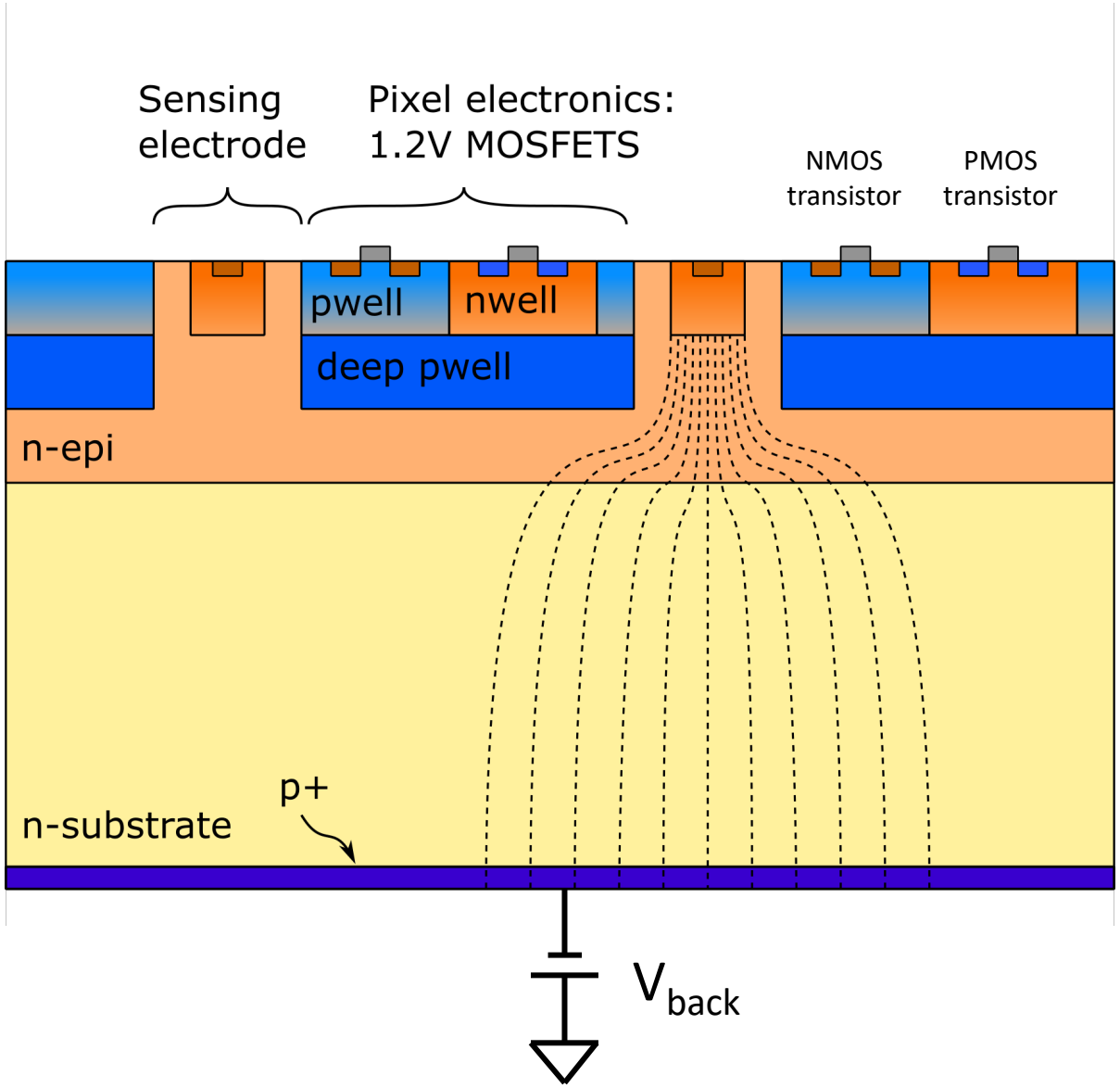
Fully Depleted Monolithic Active Pixel CMOS sensor technology platform:

- active sensor thickness in the range 50 μm to 500 μm;
- operation in **full depletion** with fast charge collection by **drift**
- **small collecting electrodes** for optimal SNR
- scalable readout architecture with ultra low-power capability (**O(10 mW/cm^2)**)
- compatible with standard CMOS fabrication process
- technology: **LF11s 110 nm CMOS node** (quad-well both PMOS and NOMS), high resistivity bulk
- custom patterned backside, patent developed in collaboration with L-Foundry

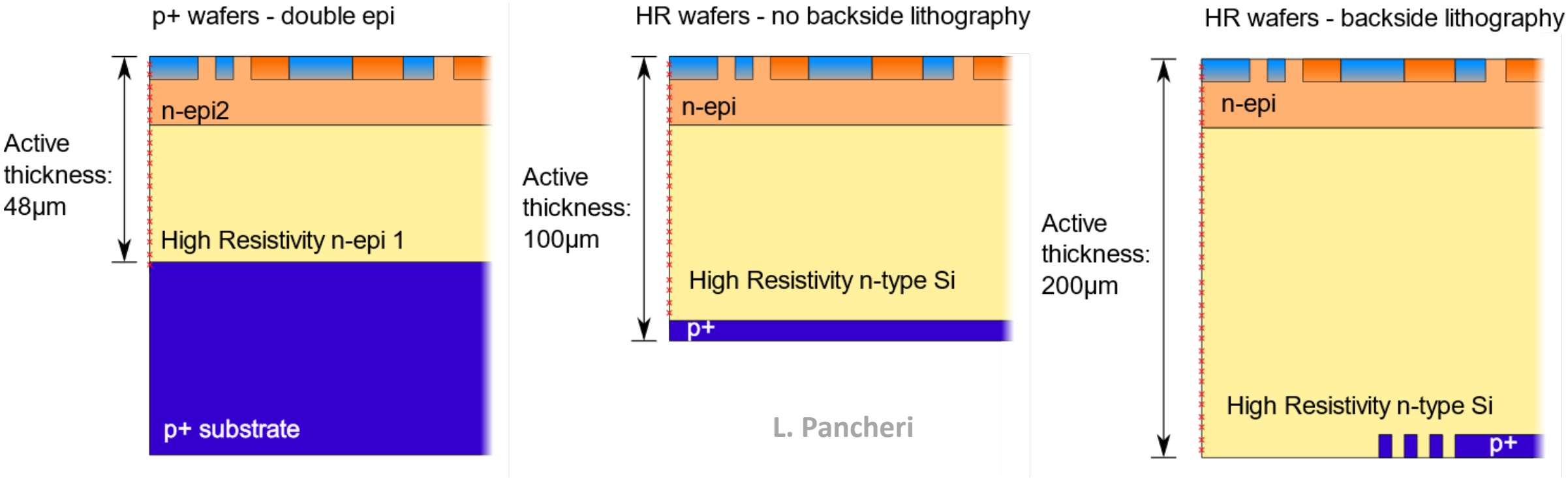


Sensor concept

- n-type **high resistivity** active region
- reverse-biased **junction at the bottom**: depletion grows from back to top
- **n-epi** layer: reduce **punch-through** current between p+ and deep pwells
- **sensing** electrodes can be biased at **low voltage** (< 1V)
- nwells with electronics shielded by **deep pwells**



Wafer post-processing: starting material and backside process

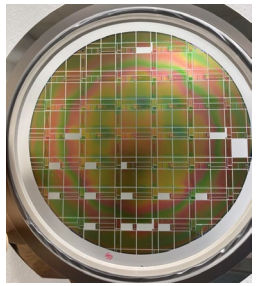


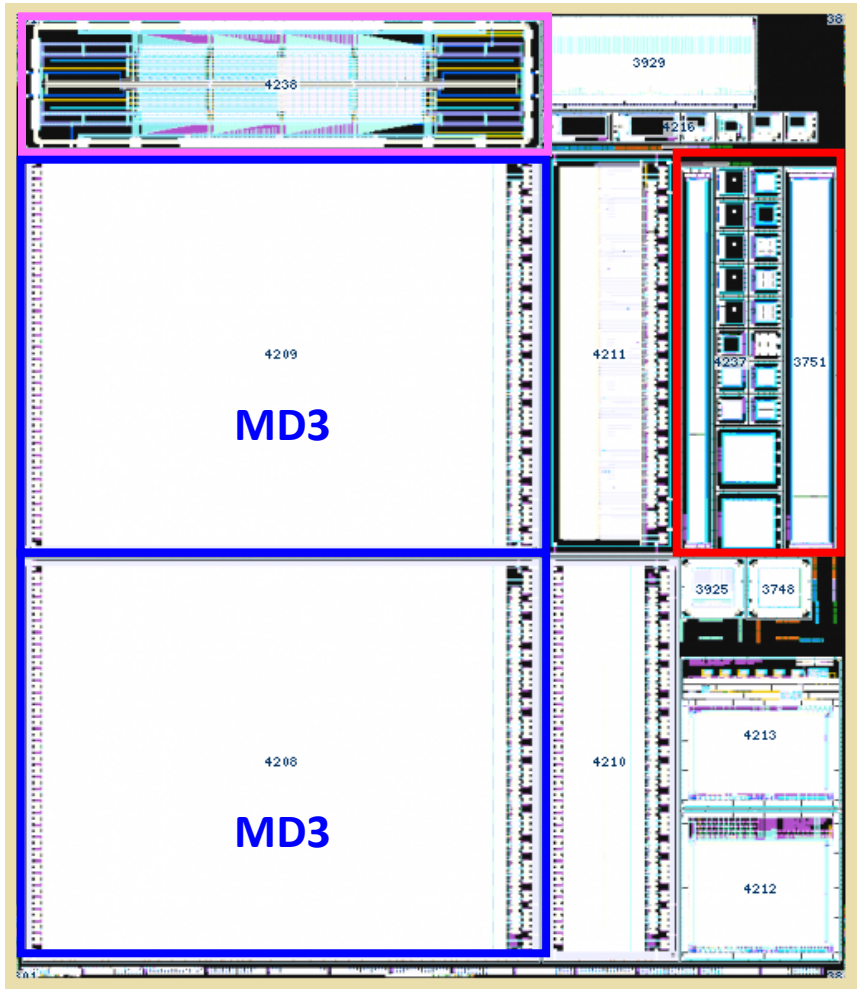
type 1:
p+ starting substrate:
thinning down to a 100 µm total thickness,
active thickness below 50 µm

type 2:
post-processing: thinning, then back-side **p+ implantation** and laser annealing, no patterning on backside

type 3:
post-processing: thinning, **lithography**, backside **p+ implantation** and laser annealing, insulators and **metal** deposition

Arcadia technology demonstrators





Arcadia 3rd engineering run
(silicon received in middle 2022)

List of produced devices:

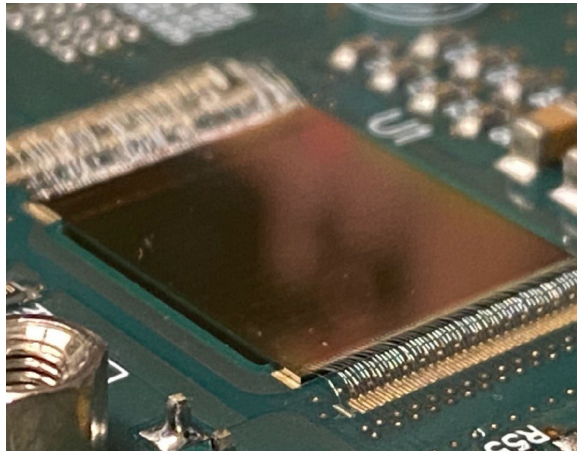
- **main demonstrator MD3**: pixel sensor built with an array of **512 x 512** 25-µm pitch **pixels**
- small **pixel arrays** with different **pitch** (10 µm – 25 µm – 50 µm) with and w/o active readout
- **strip detectors** with and w/o active readout
- **ASTRA** 64-channel ASIC for Si-strip readout
- **test structures** for sensors characterization and process qualification
- low power **MATISSE** (ultra low power front-end for space instruments)
- **HERMES**: small-scale demonstrator for fast timing
- X-ray multi-photon counter
- MADPIX: CMOS LGAD multi-pixel active demonstrator chip for fast timing

Arcadia Main Demonstrator – chip floorplan

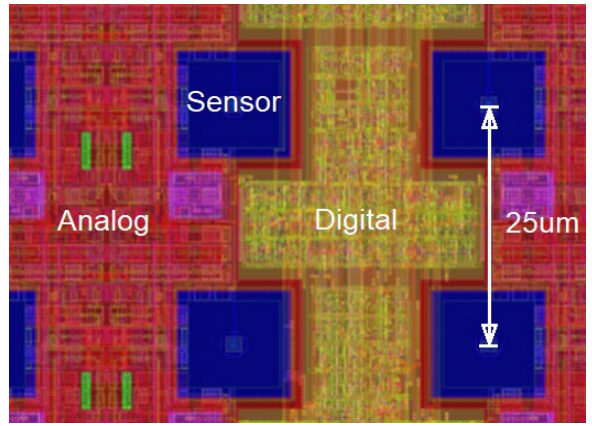
M. Rolo

top padframe: auxiliary supply, IR drop measure

bottom frame: stacked power and signal pads



512 x 512 pixel sensor bonded on PCB



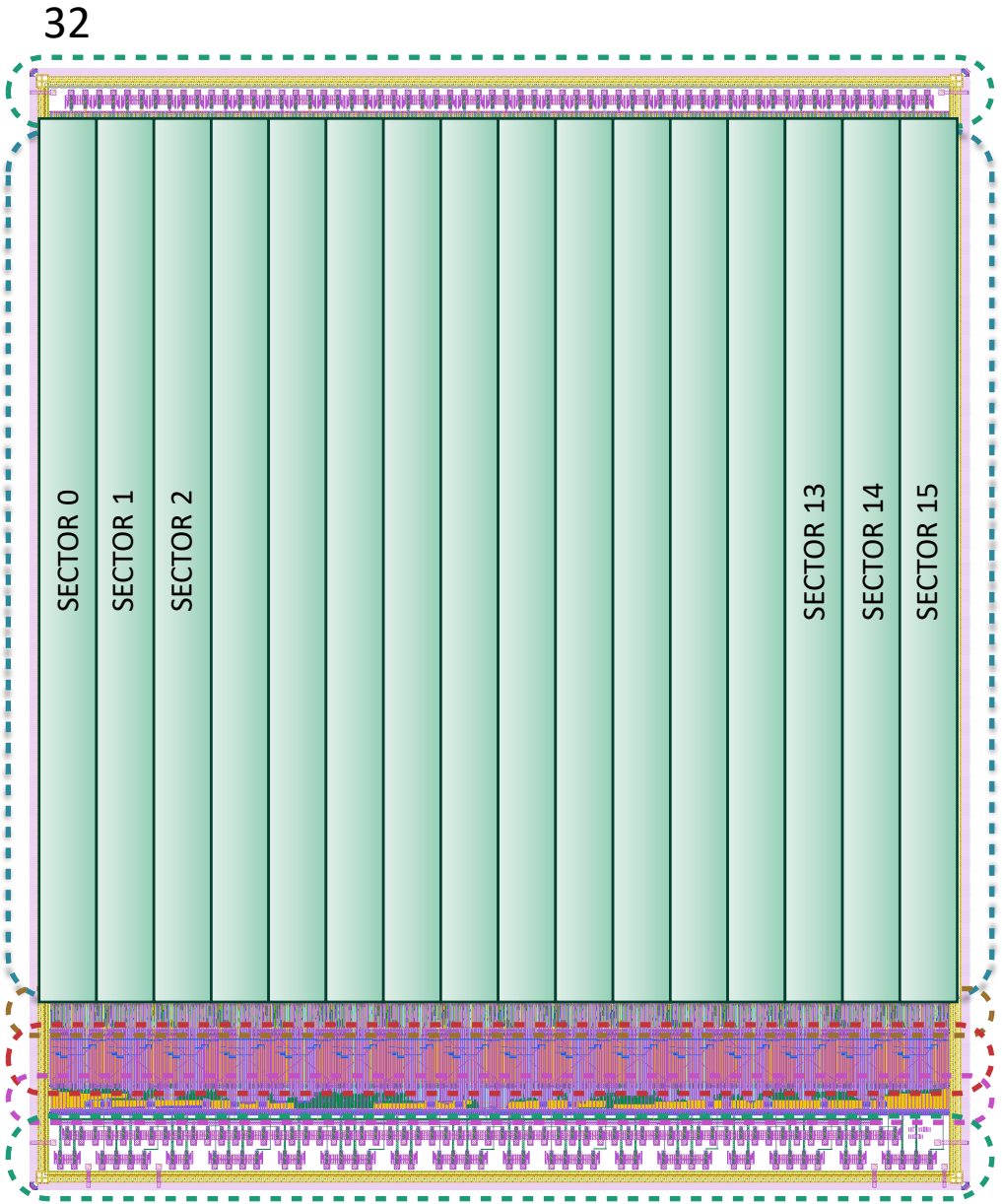
detail of pixel layout

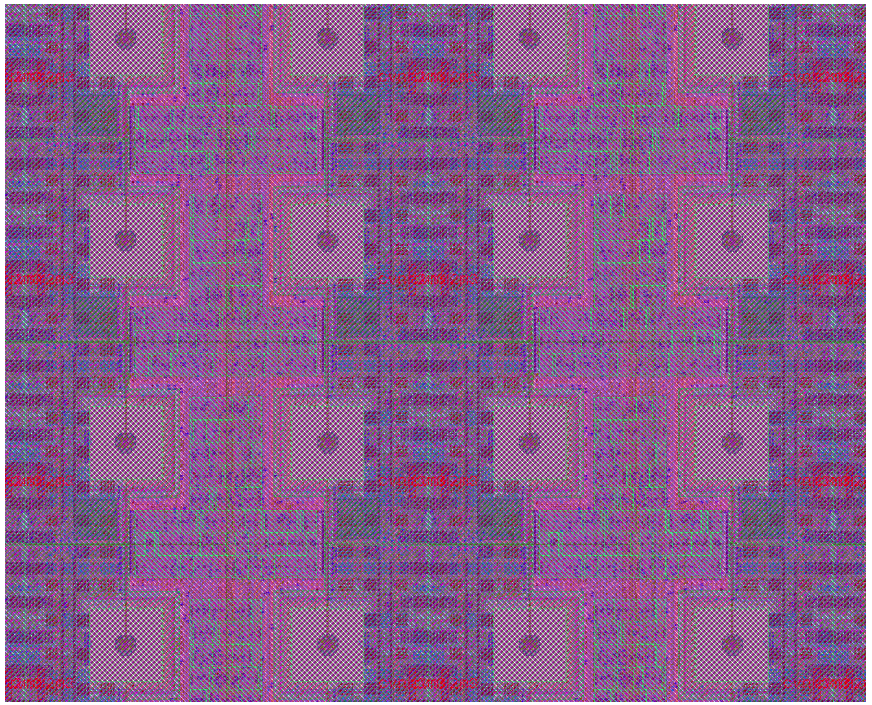
end of sector:
reads and configures one section

sector biasing:
generates I/V biases for sections

periphery:
SPI slave, registers and pixels configuration, 8B/10B encoding, 320 MHz DDR serializers

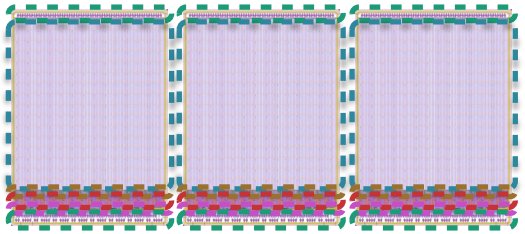
Arcadia Main Demonstrator – chip integration



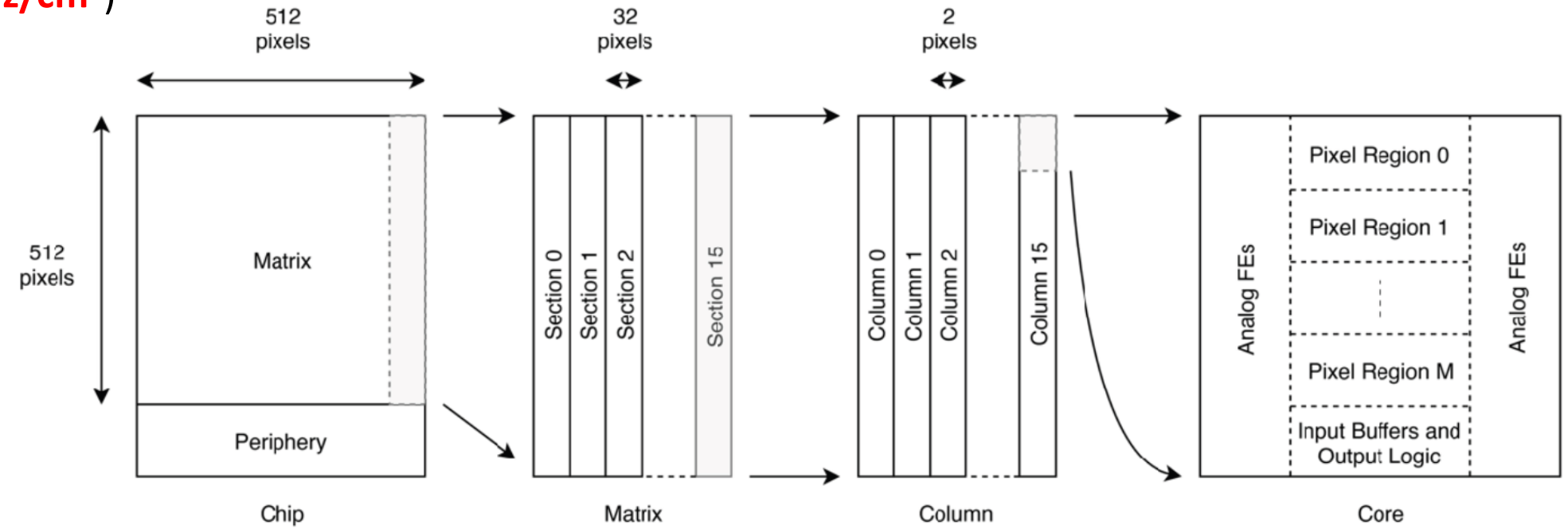


- the matrix is composed of 16 identical Sectors (32x512), each of which contains 16 Double Columns
- triggerless data-driven readout with low-power asynchronous architecture with **clock-less pixel matrix** integrated on a **power-oriented flow**
- power: 10 – 30 mW

Main demonstrator: chip architecture



- pixel size: 25µm x 25µm. Array core area: 1.28cm x 1.28cm → "**side abuttable**" and one-direction **stitching** compatible
- **pixel** electronics: **analog and digital**. In-pixel threshold and data storage
- architecture: **event-driven:** pixels detecting events (charge pulses) send their address and a 8-bit timestamp to the periphery (binary readout)
- low **power** (**as low as 10 mW/cm^2**) and high **event rate** (**as high as to 100 MHz/cm^2**)



M. Rolo

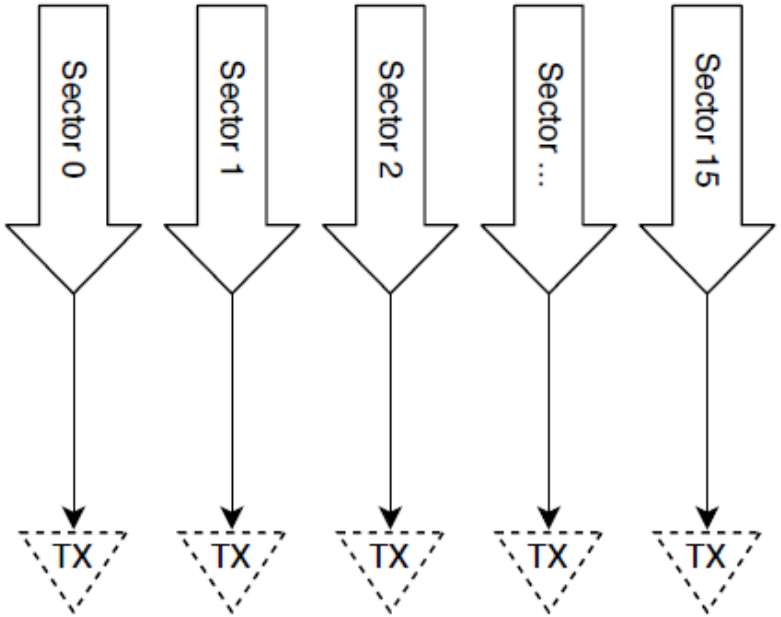
Arcadia-MD3: peripheral dataflow

- each sector has an independent readout and output link when operating in **High-Rate Mode**
- sector data is sent out (with 8B/10B encoding) via dedicated 320MHz DDR serializers
- in **Low-Rate Mode**, the first serializer processes data from all the sections. The other serializers and C-LVDS TXs are powered off, in order to reduce power consumption

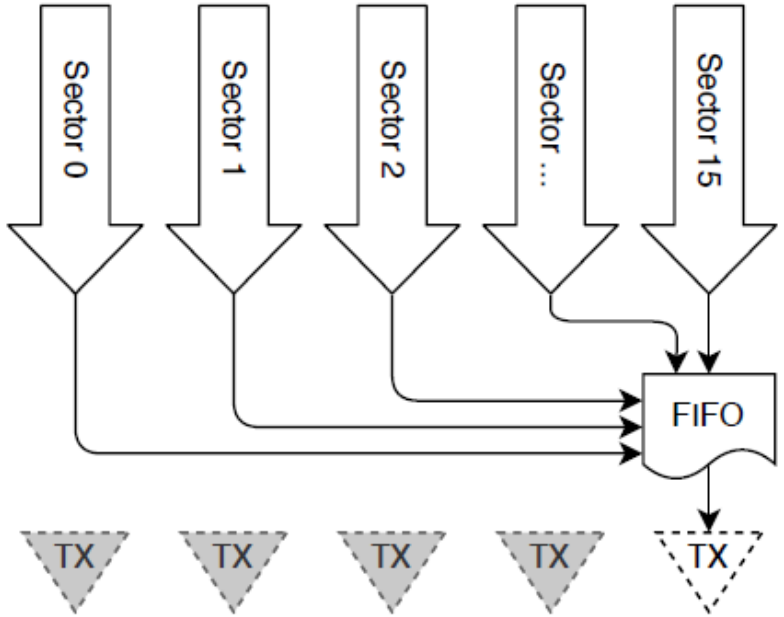
high-rate mode

measured value:
17-30 mW/cm²

(to be verified at high rates up to 100 MHz/cm²)

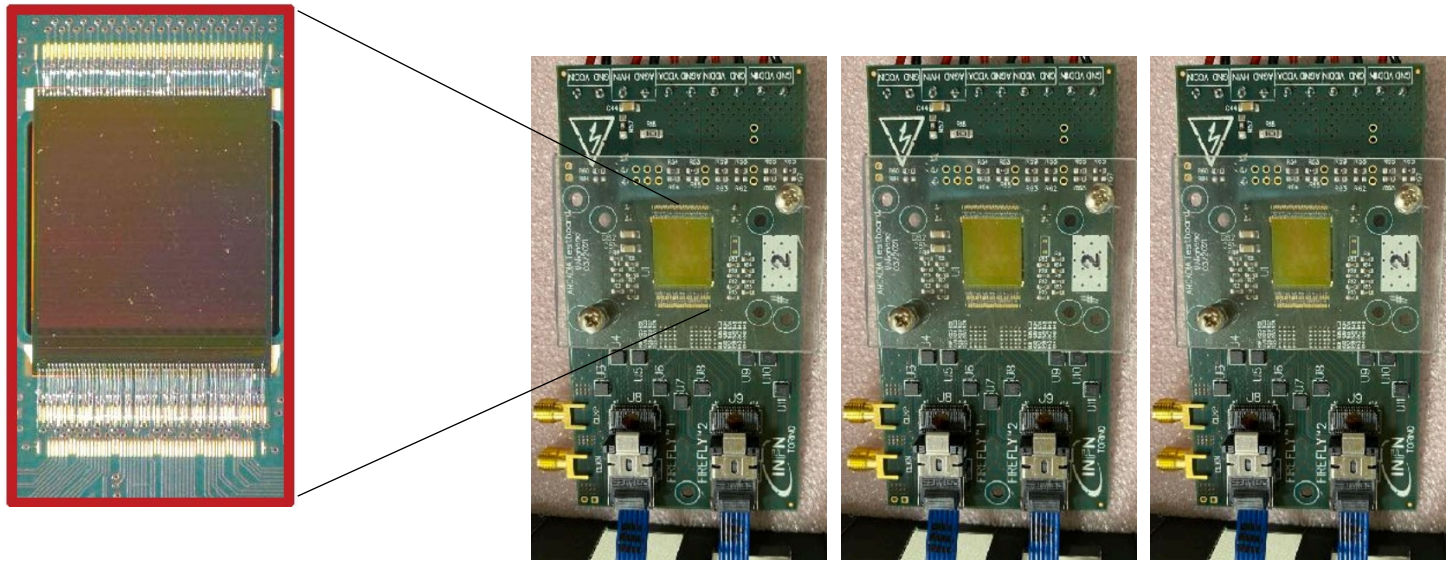


low-rate mode



measured value:
10 mW/cm²

Front-end board and DAQ

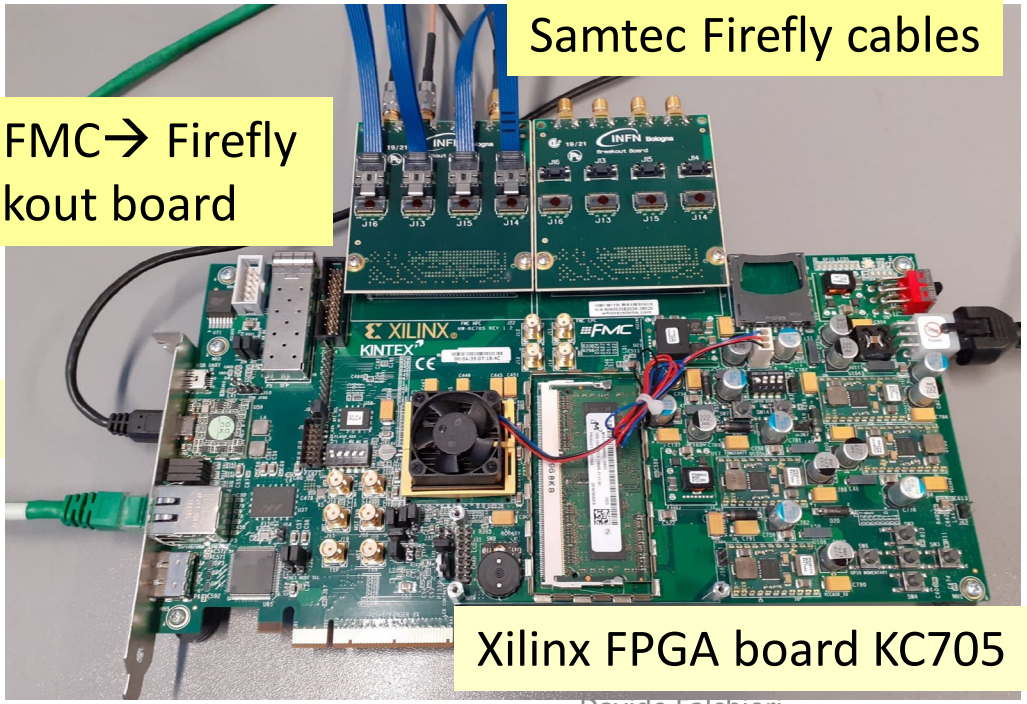


Arcadia front end board

PCB through-hole for matrix Back Side Illumination

Samtec Firefly cables

custom FMC→ Firefly breakout board



Xilinx FPGA board KC705

1 Gb ETH

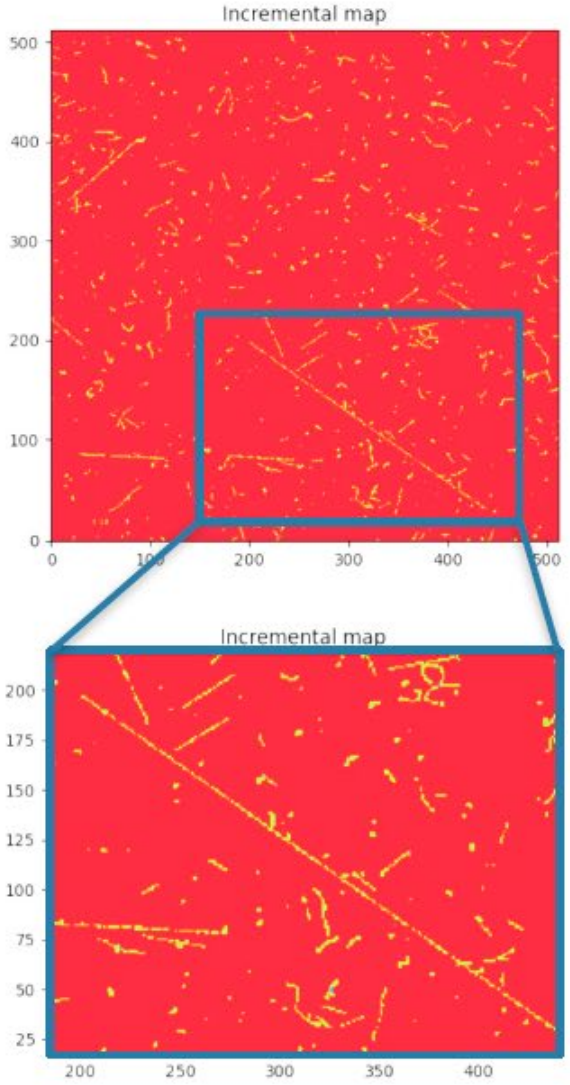
CERN Ipbus

The **FPGA**:

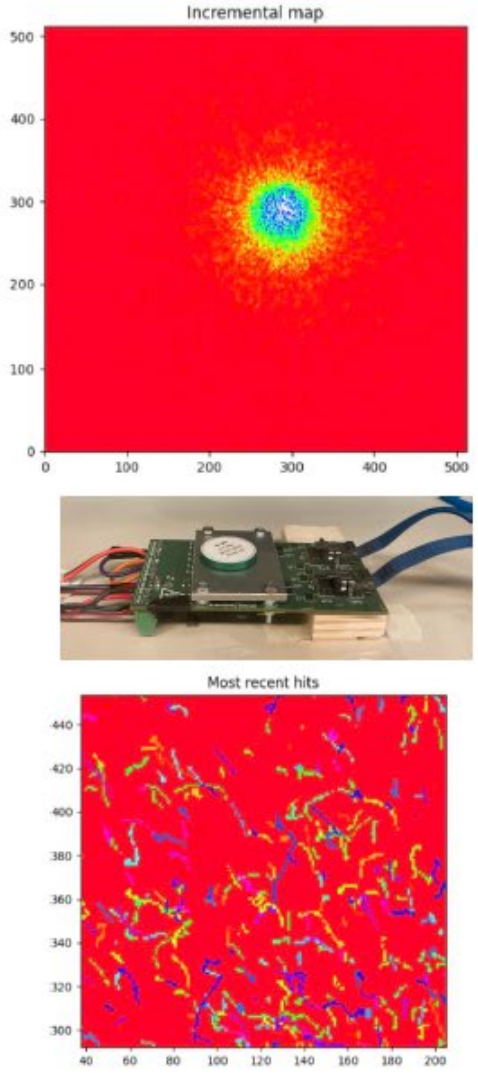
- manages the SPI interface
- extracts hits from the 16 input lanes and stores them locally, before they are sent to a PC using the Ipbus protocol
- can work both in data-push mode or in triggered mode

Main prototype: charged-particle detection

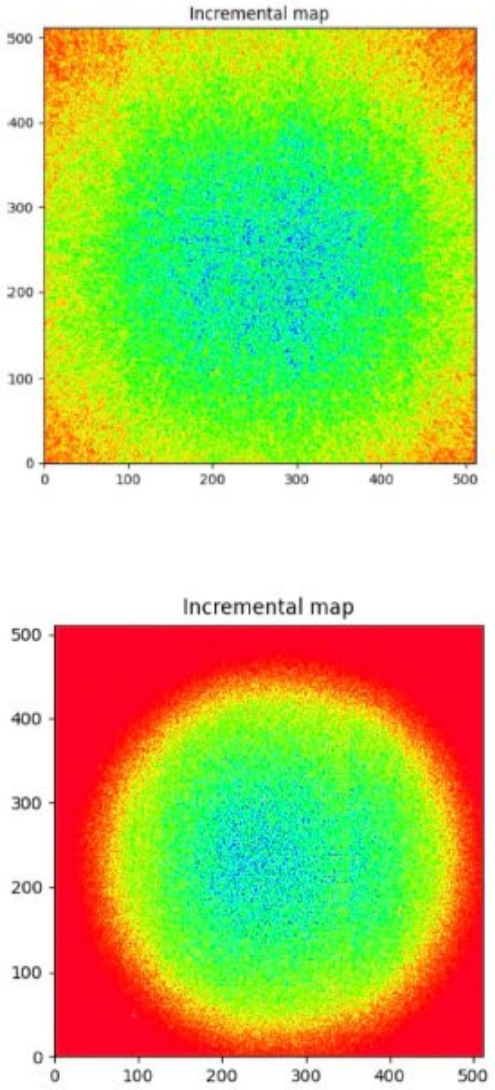
cosmic rays (tilted sensor)



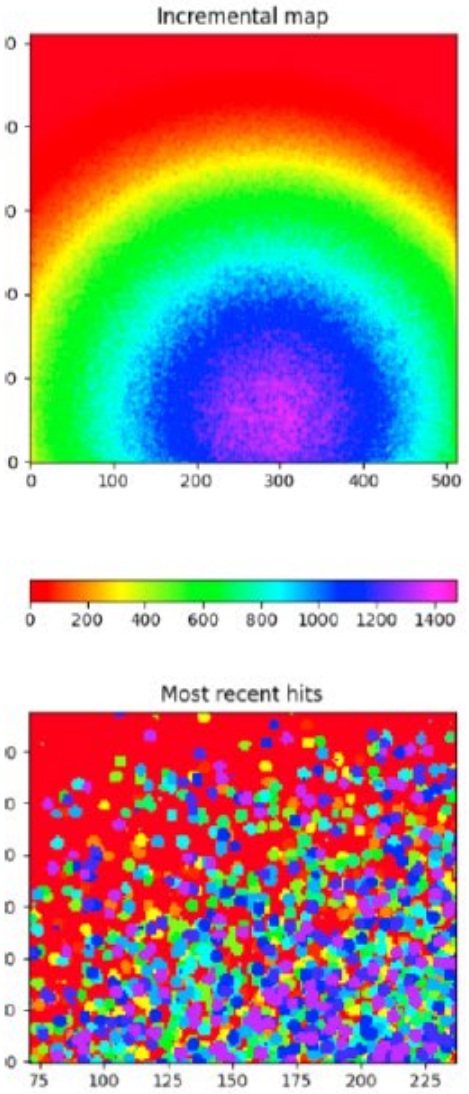
Sr90 (collimated 1 mm)



Sr90 (uncollimated)



Am241

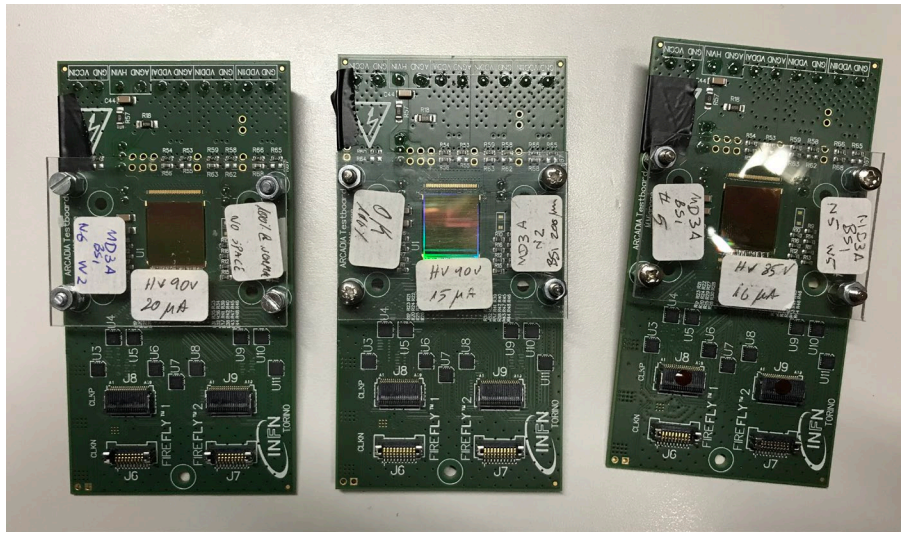


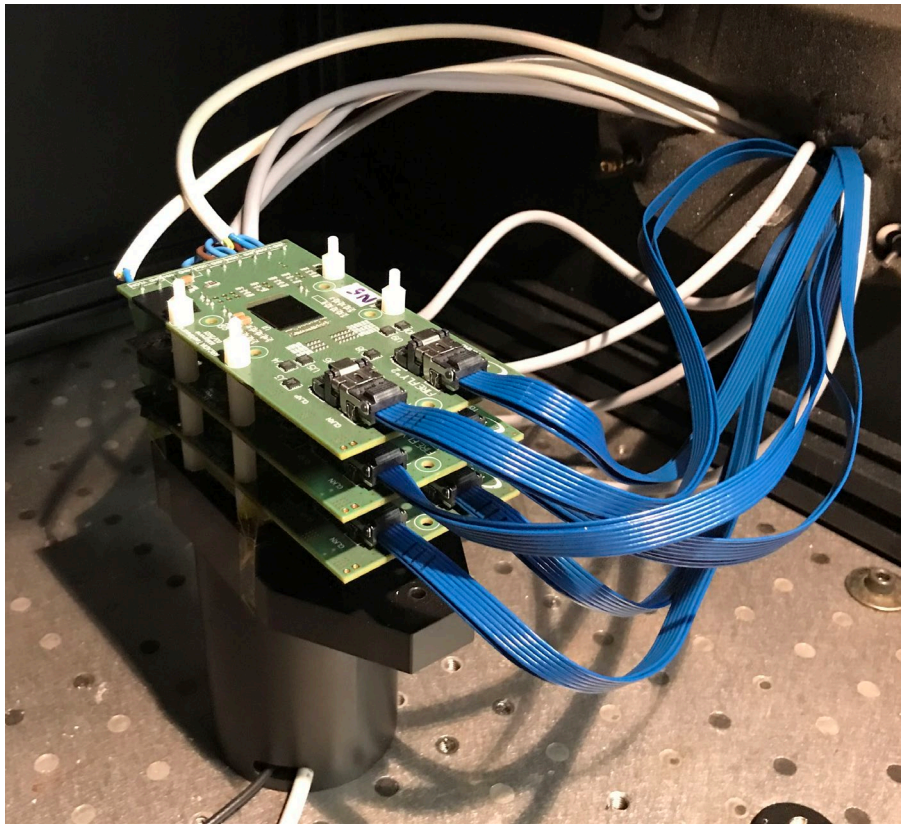
Arcadia MD3 cosmic data: setup

system mounted in a black box
typical HV = - 90 V
typical leakage current = 20 μA
threshold = 25 DAC (290 e-)

System very stable:

- 1 week of data taking, unattended, in stable condition
- no specific activity for parameters optimization





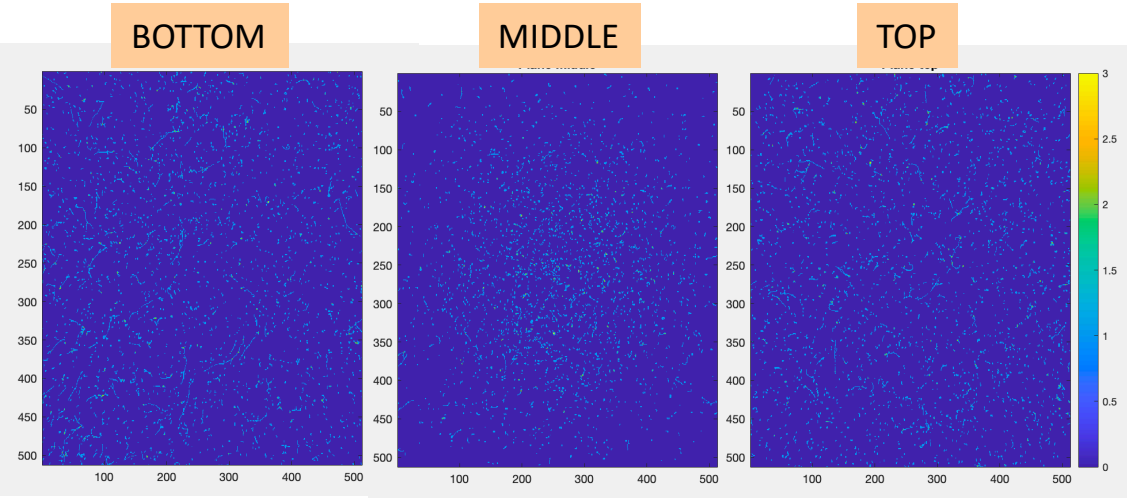
R. Santoro

Cluster size

MPV = 4 pixels

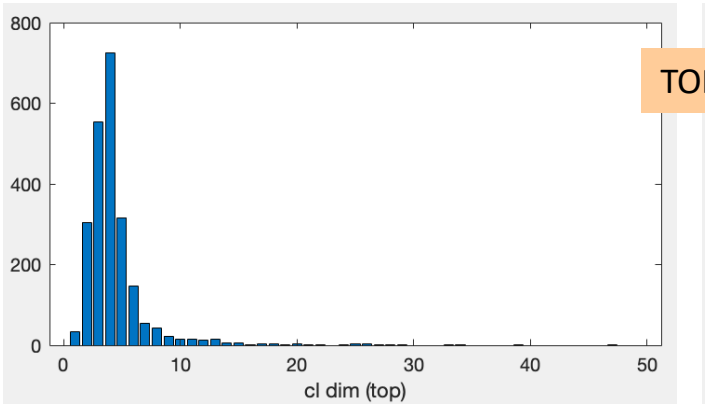
more than 90% of clusters
with less than 6 fired pixels

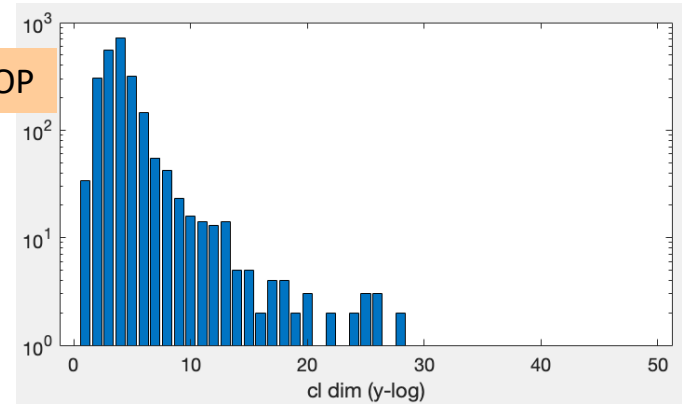
matrices with synchronized data

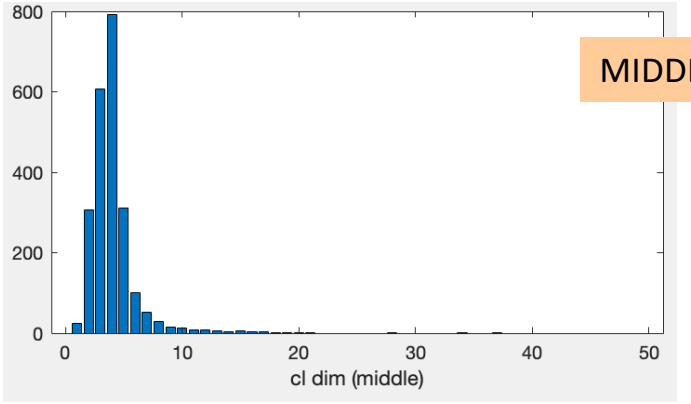


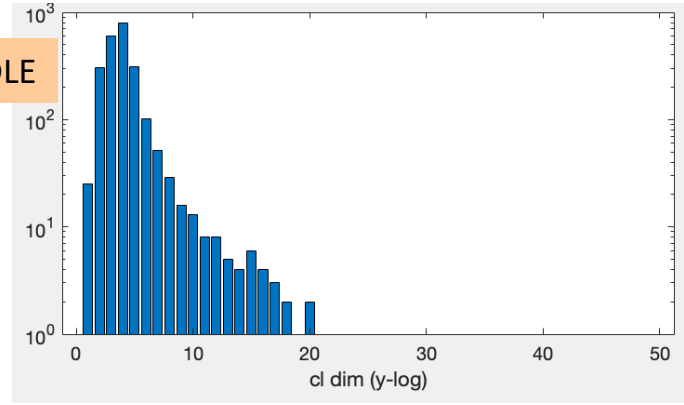
linear scale

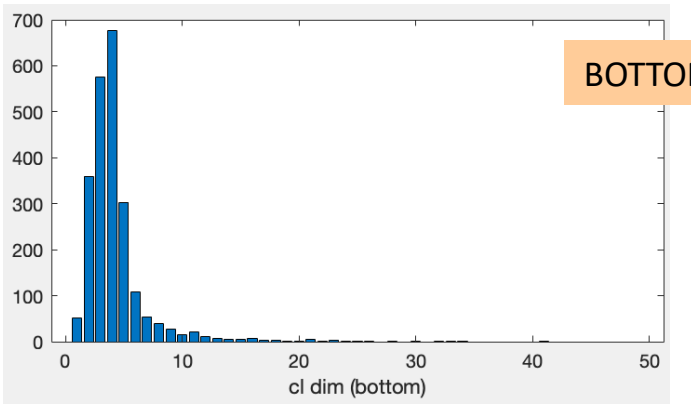
log scale

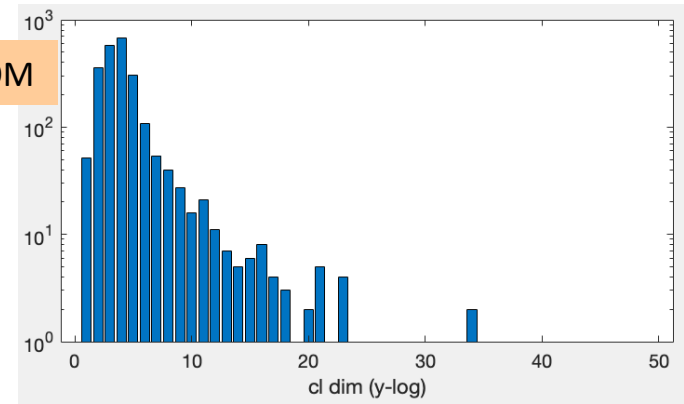












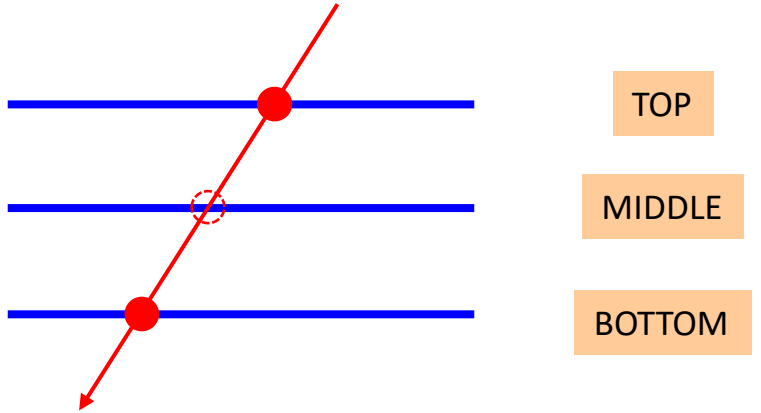
R. Santoro

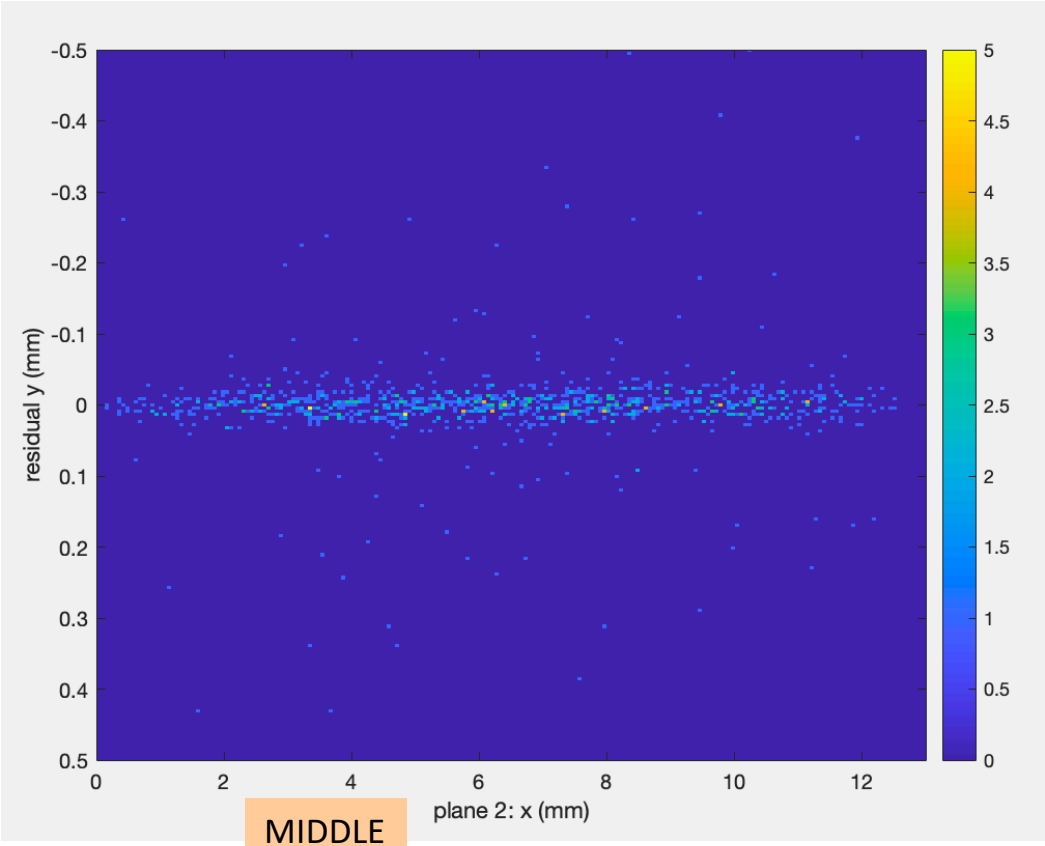
Residuals

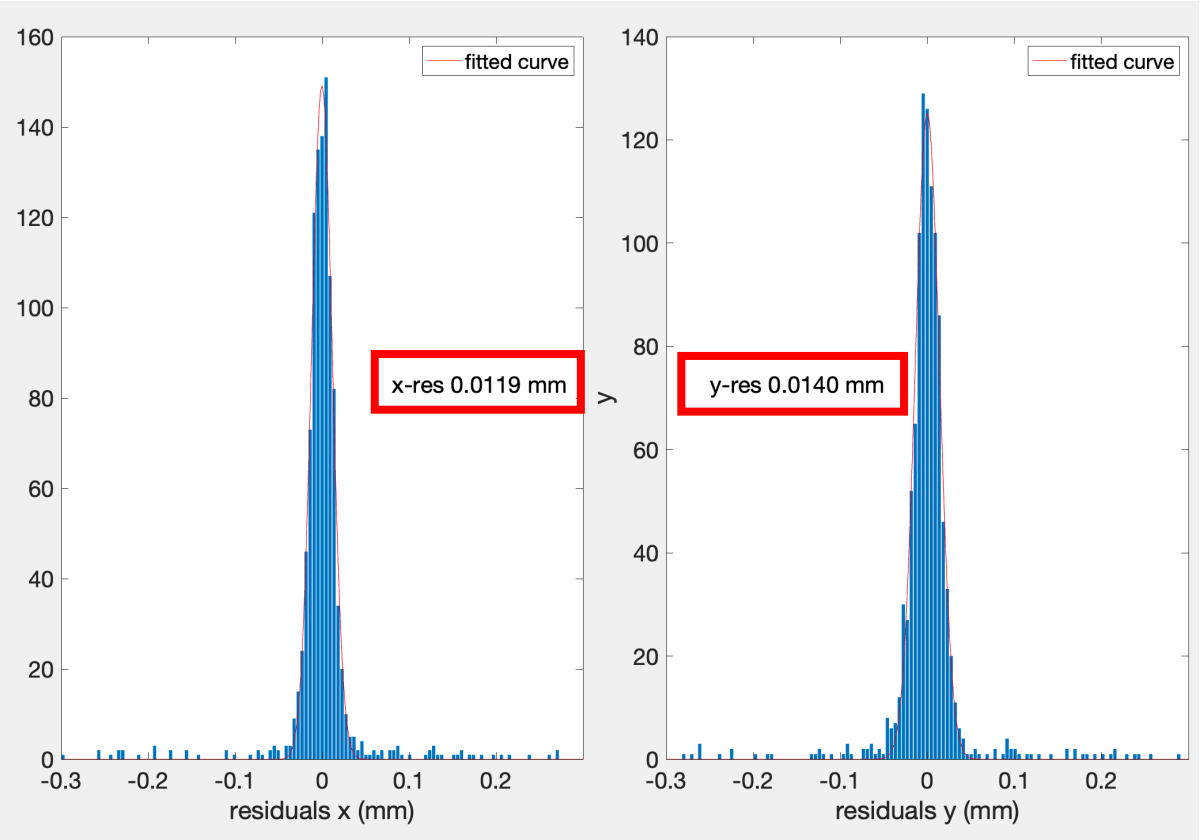
Selection criteria:

- 1 cluster per plane
- Δt <= 10 clock cycles
- cluster dimension <= 4 in tracking planes (top and bottom)

Selected $\approx 46\%$ of the synchronized events





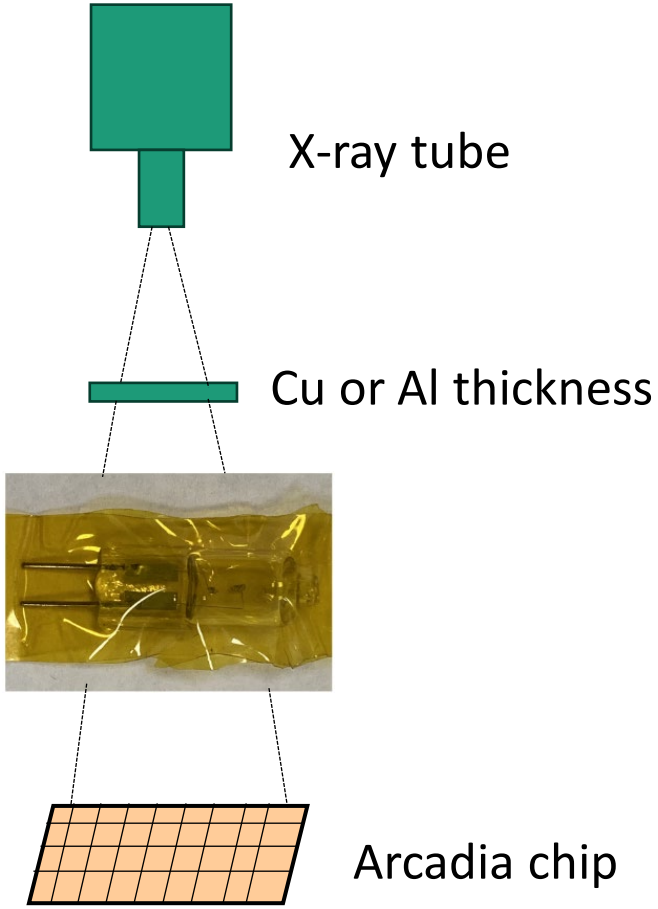


R. Santoro

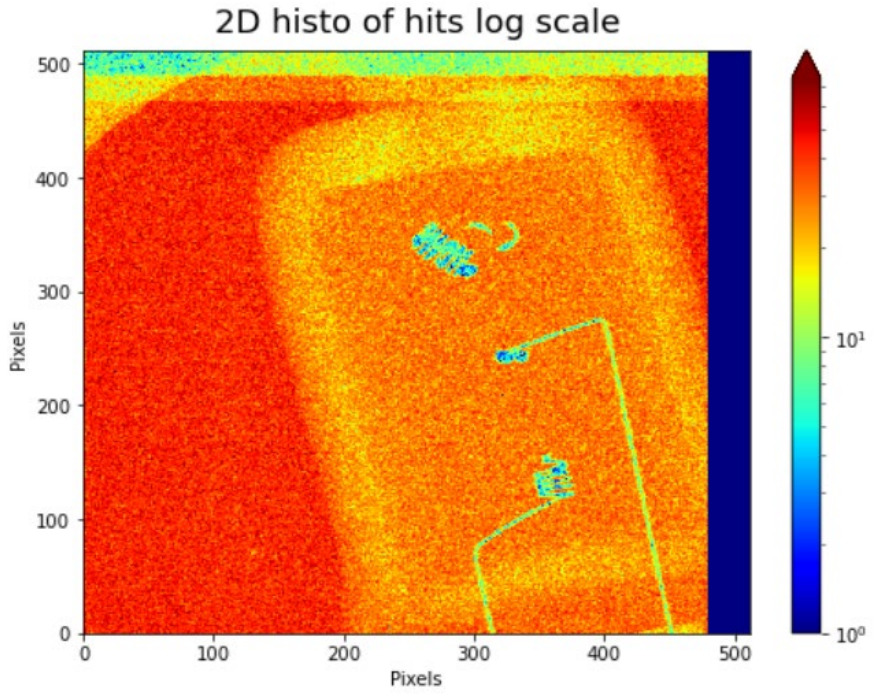
X-ray tube and CT with Arcadia MD3

S. Ciarlantini, C. Bonini, D. Chiappara, P. Giubilato

- X-ray setup (2-10 mA, 40 kV)
- radiography samples and CT reconstruction (stepper motor)
- samples directly placed closed to the backside of Arcadia (BSI)

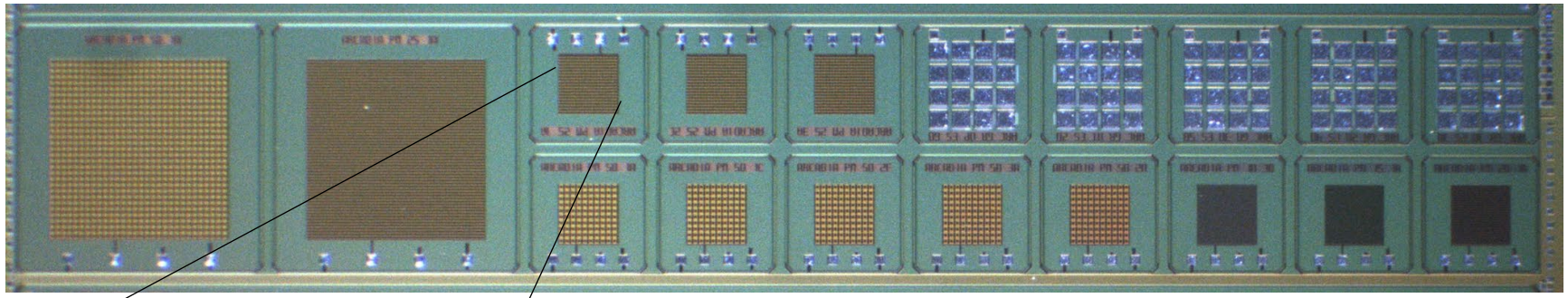


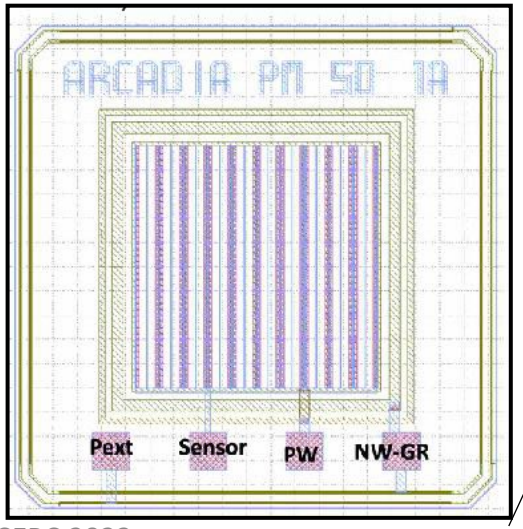
light bulb



thickness: ~8 mm, height: 2.29 cm, glass + metal

Pixel / strip test structures



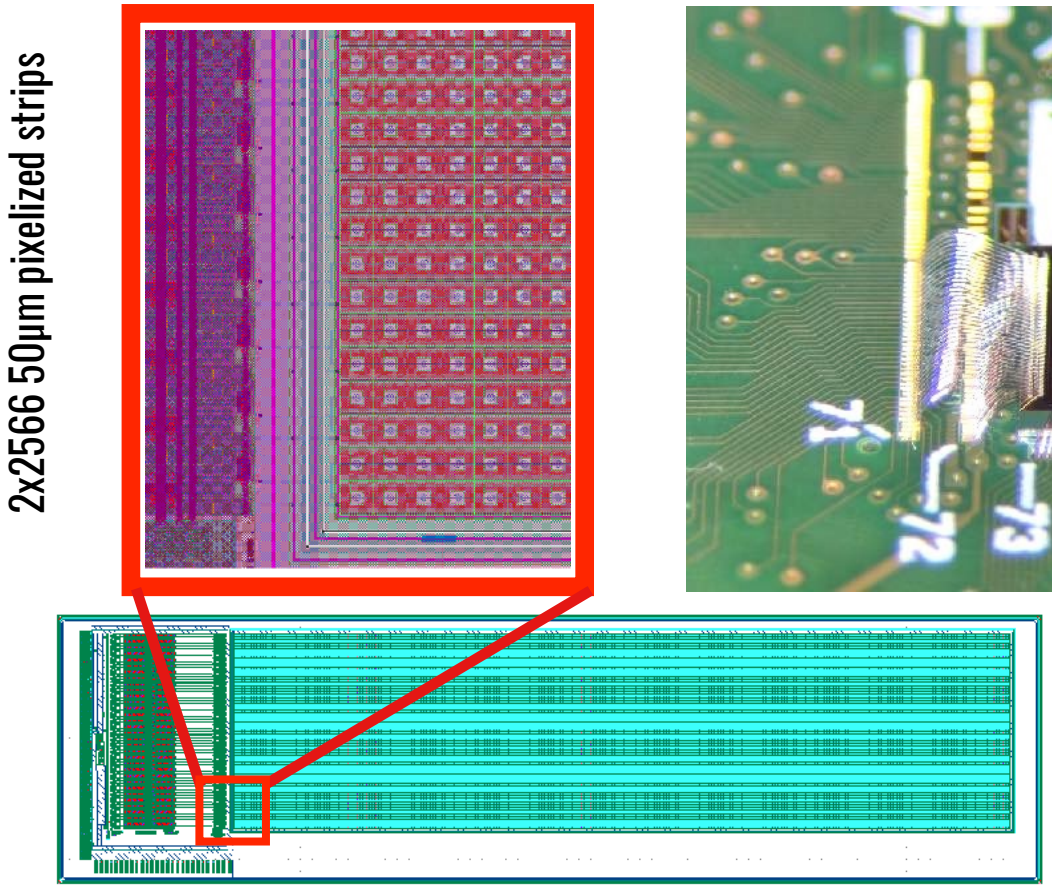


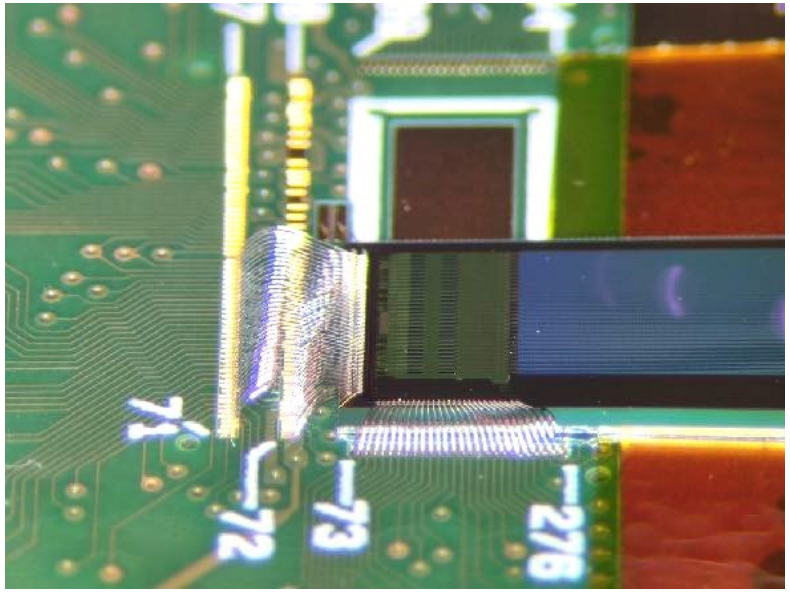
strip flavours:
- 25 μm pitch pixelated
- 25 μm pitch continuous
- 10 μm pixelated

pixel flavours:
- pseudo-matrices of 1x1 and 2x2 mm^2 (all the sensor nodes are connected in parallel)
  - 50 μm
  - 25 μm
  - 10 μm

FDMAMs (Fully Depleted Monolithic Active Microstrips)

CMOS monolithic strip block and readout electronics (active sensor area: 12800 x 3200 μm^2)



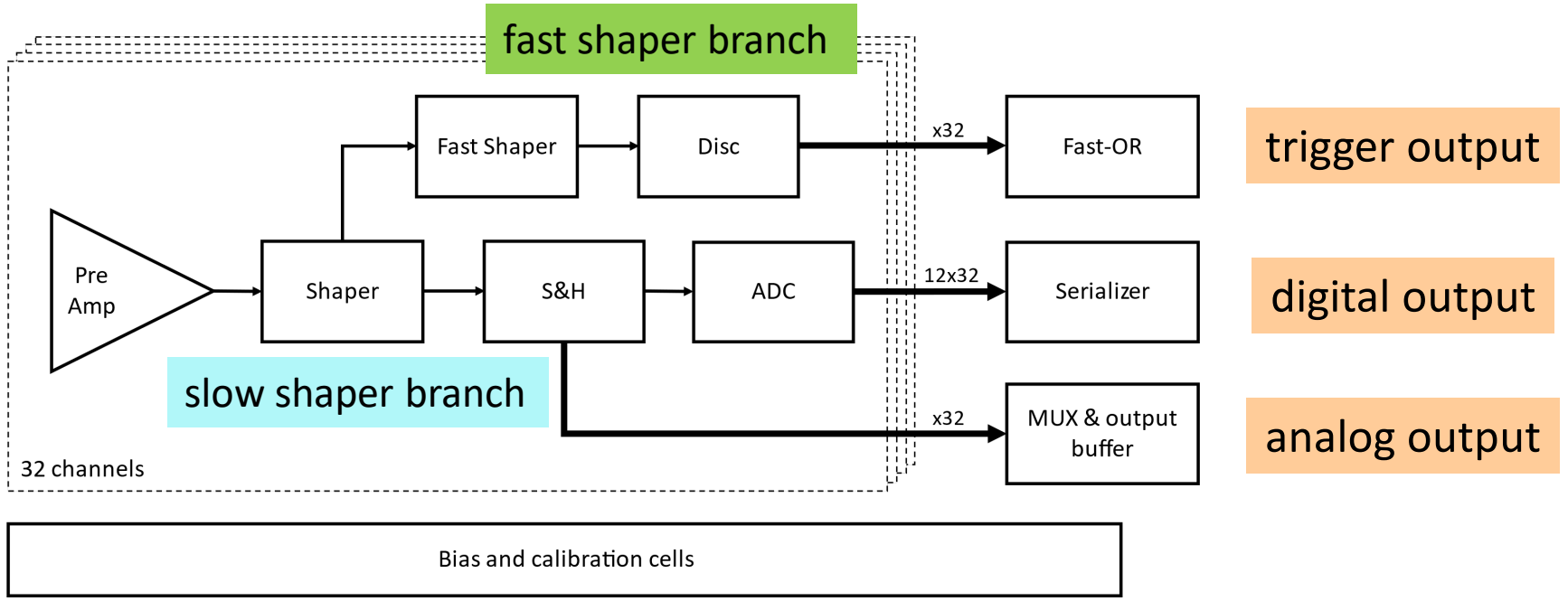


L. Pancheri

FDMAMs (Fully Depleted Monolithic Active Microstrips)

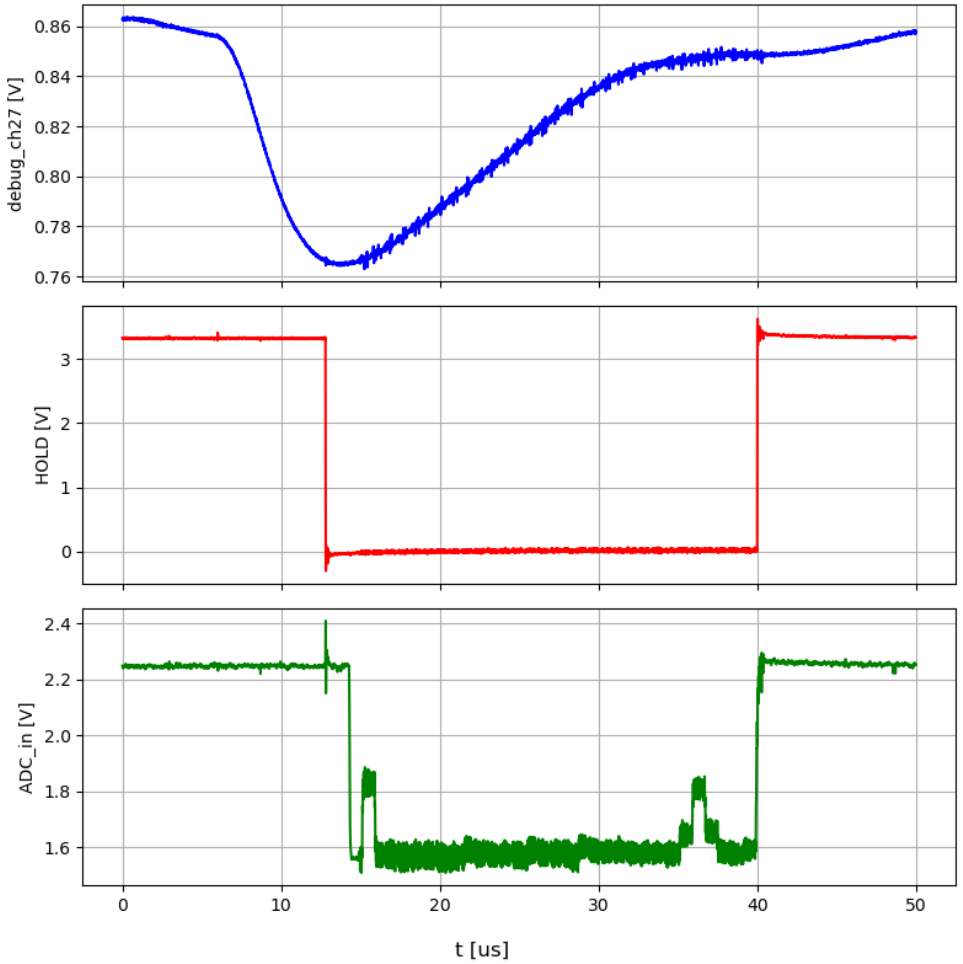
- **preamp**: CSA + testpulse injection circuit
- slow shaper branch for charge measurement with externally controlled S&H circuit
- **readout**:
  - analogue: mux-differential output buffer
  - digital: Wilkinson ADC and serializer
- **trigger output**:
  - fast shaper branch with fast-OR output

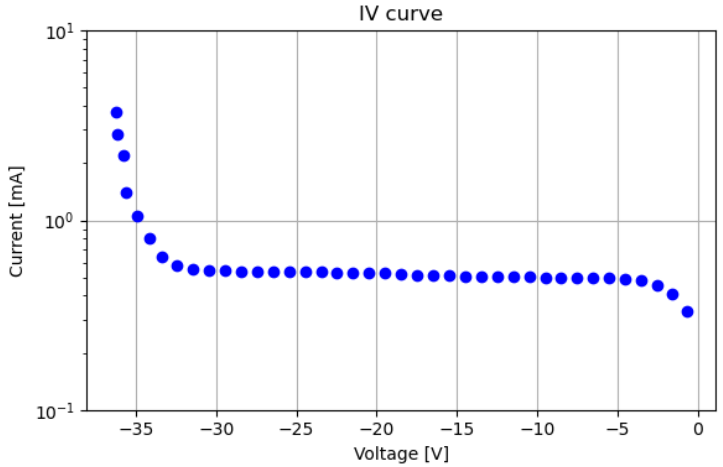
the same readout of the ASTRA chip is integrated into silicon in FDMAMs



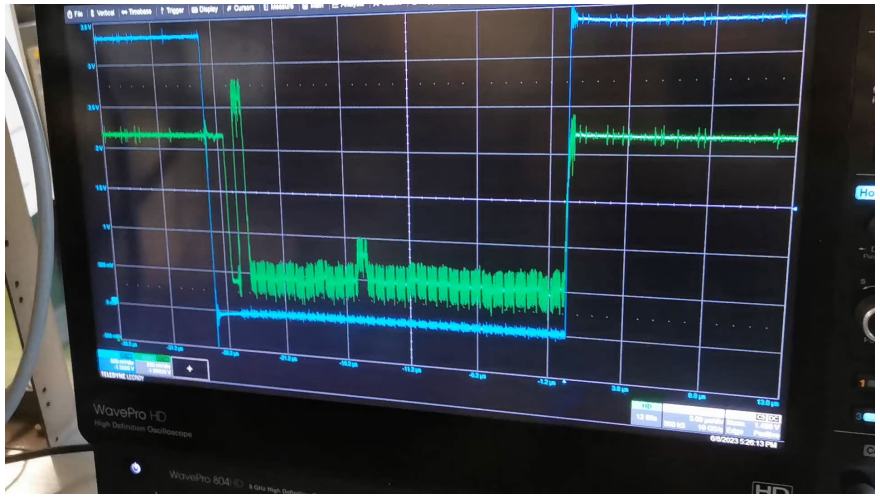
FDMAMs (Fully Depleted Monolithic Active Microstrips)

tests with Sr90

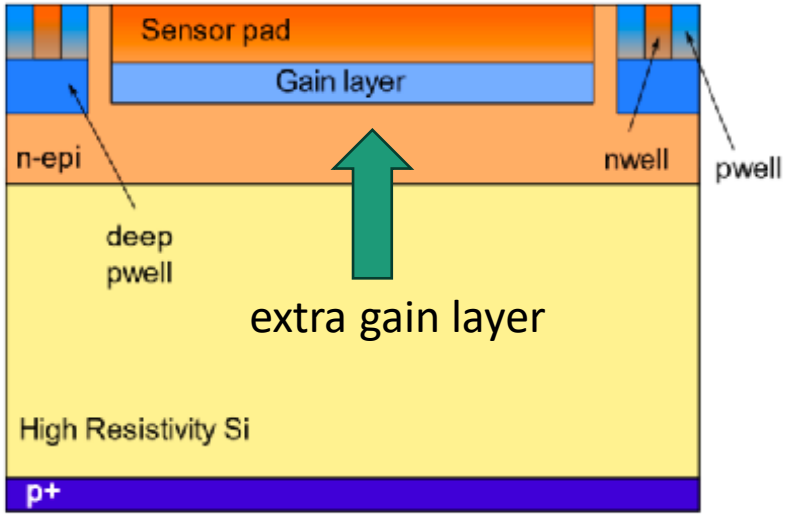


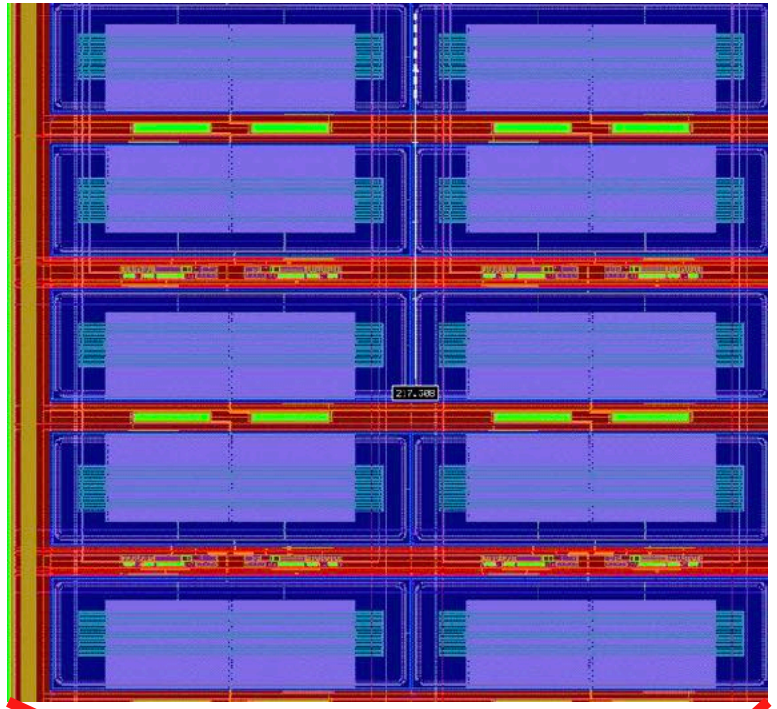


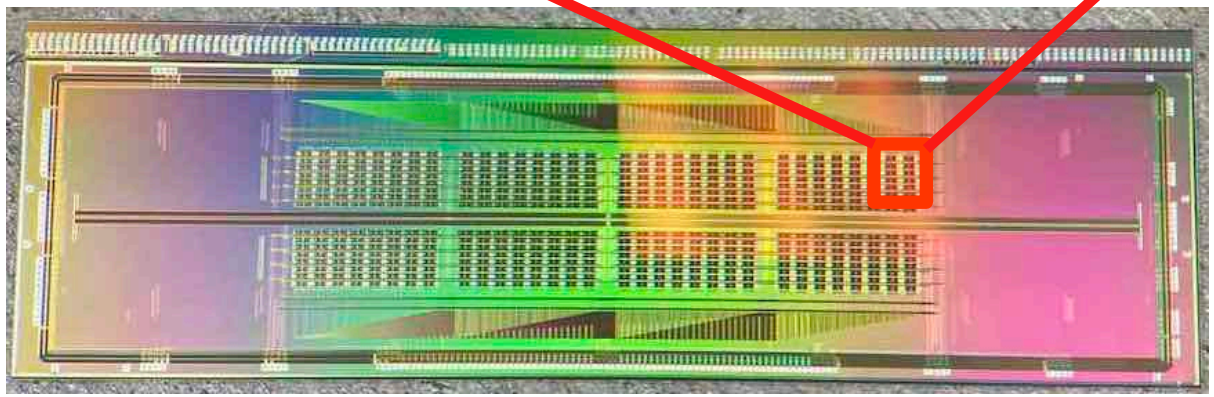
- ASTRA FastOR signals provides trigger to the FPGA
- FPGA sends HOLD signal and then starts readout of analogue MUX



MadPix CMOS LGAD multi-pixel prototype



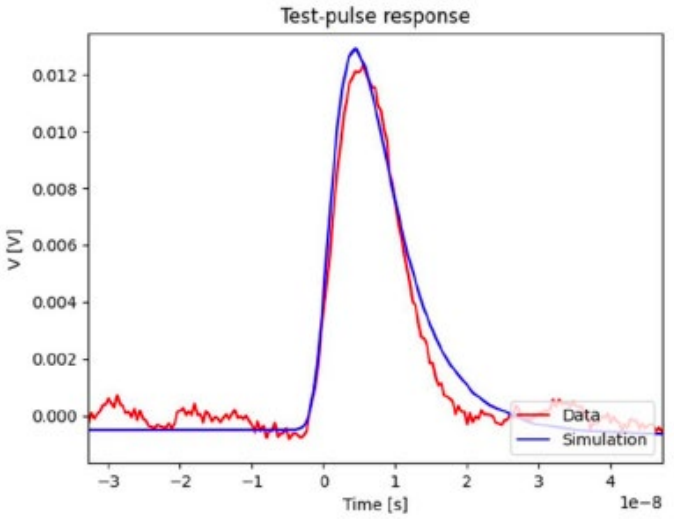


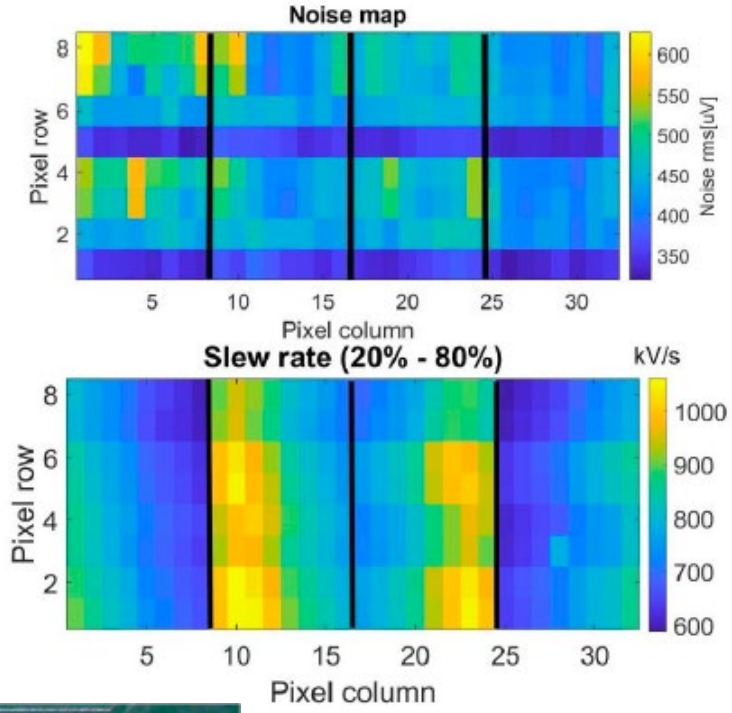


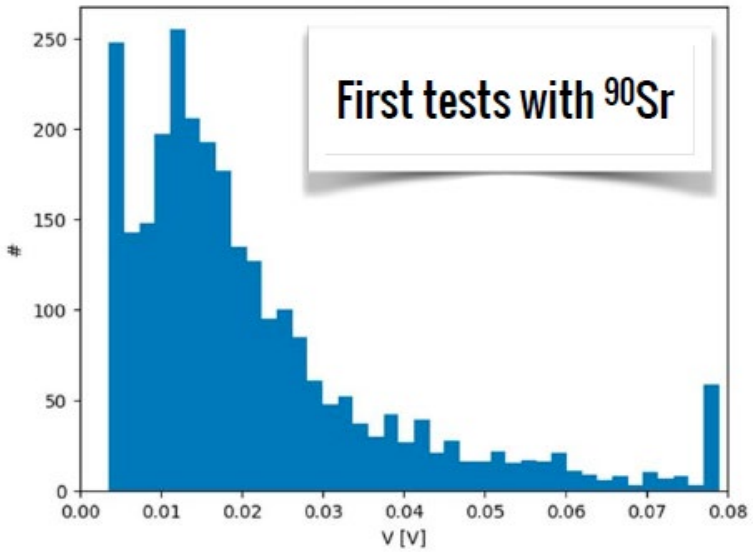
- some of the HR and p+ wafers implement **an extra gain layer** added to the sensor
- first small-scale demonstrator 4 x 16 mm^2
- 8 matrices (64 pixels each) implementing different sensor and front-end flavours
- 250 x 100 mm^2 pixel pads
- 64 analogue outputs on each side, rolling shutter of single matrix readout

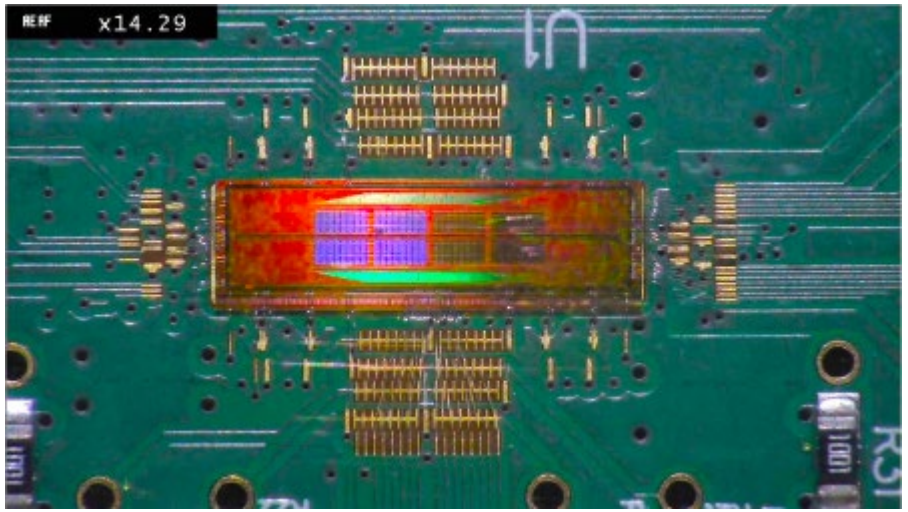
MadPix CMOS LGAD multi-pixel prototype

- noise and slew-rate characterization with external testpulse
- scans with Sr90 source
- happening now: test-beam for evaluation of timing performances









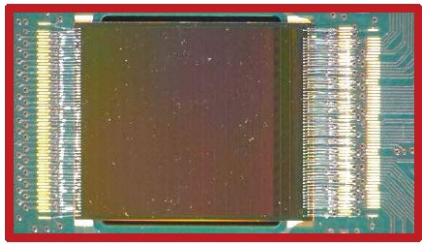
Arcadia: status and outlook

Characterization:

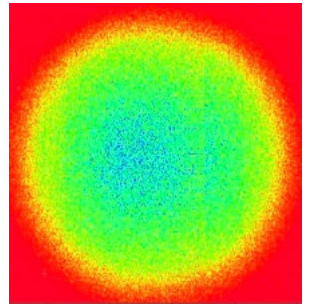
- extensive **testing** (first test beam foreseen in the next months)
- **3-layer telescope** → tracking performance measurements
- extended **radiation hardness characterization** on test structures and on main demonstrators

Design:

- **sensors with high timing resolution** (particle TOF – upgrade of ALICE experiment at CERN): CMOS sensors with gain layer for fast timing



ARCADIA

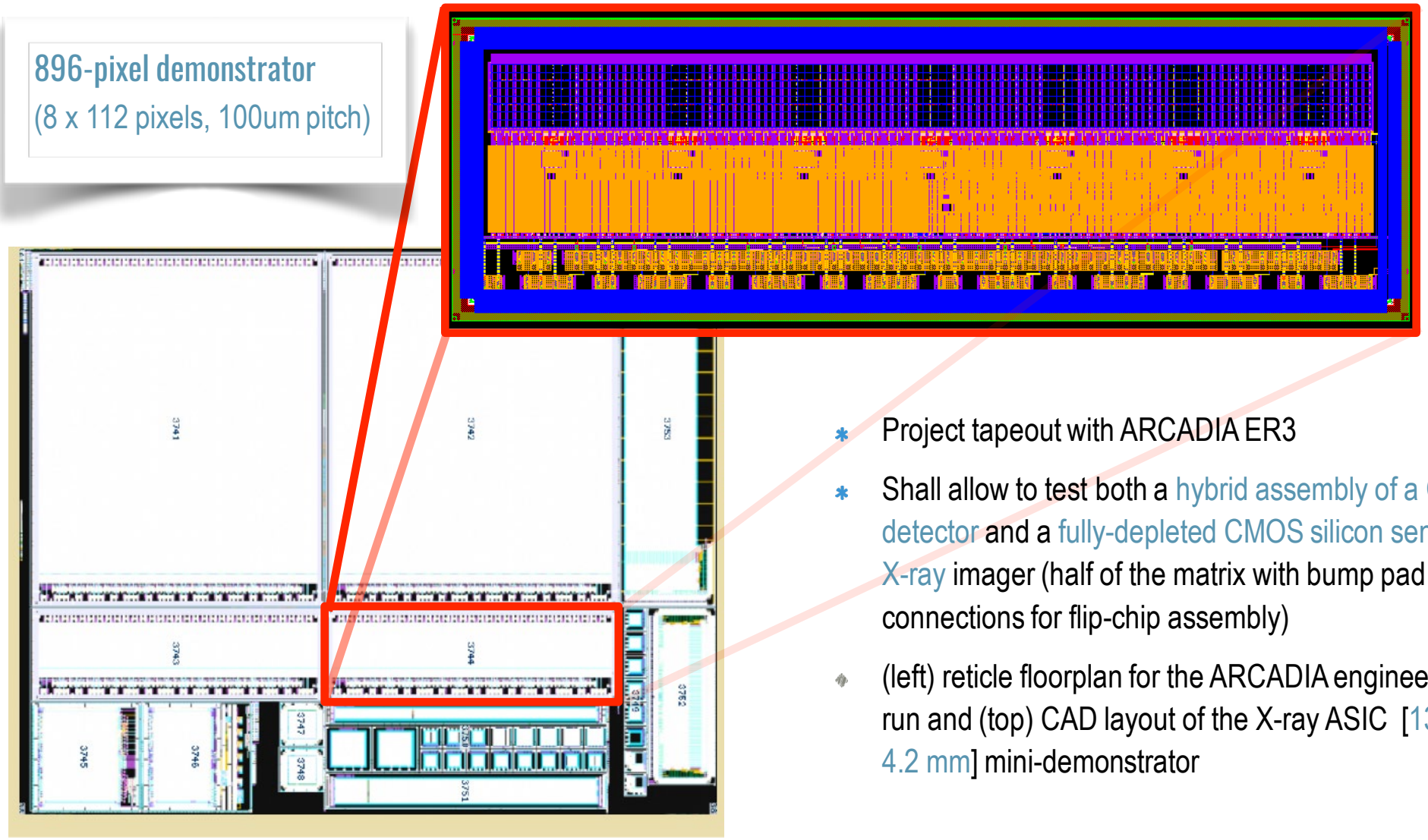


Thanks for your time

Backup

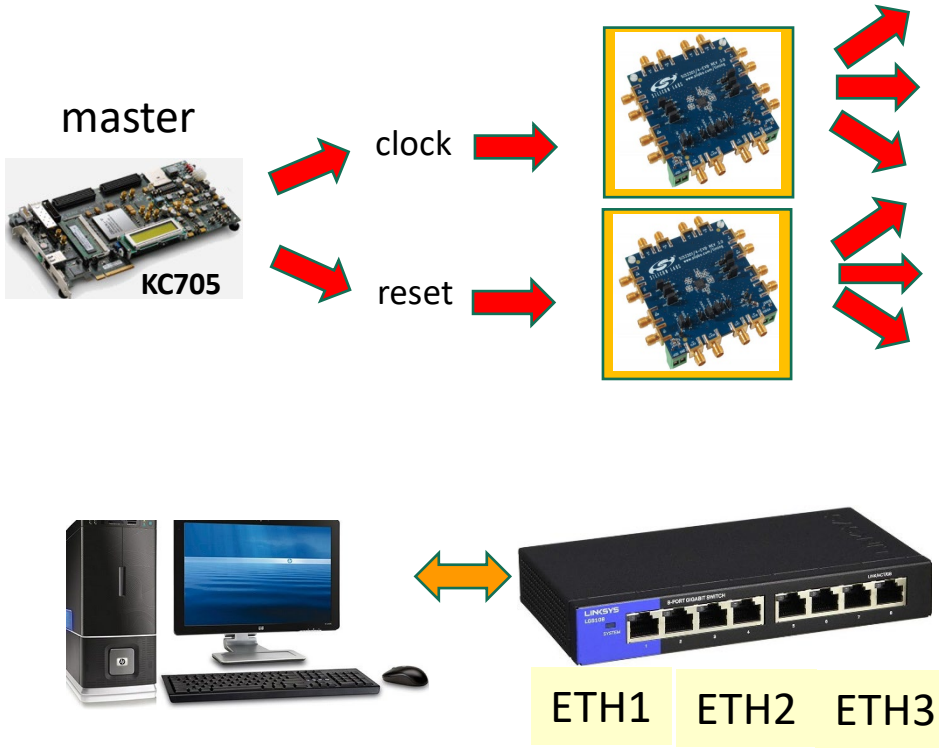
X-ray photon counting demonstrator

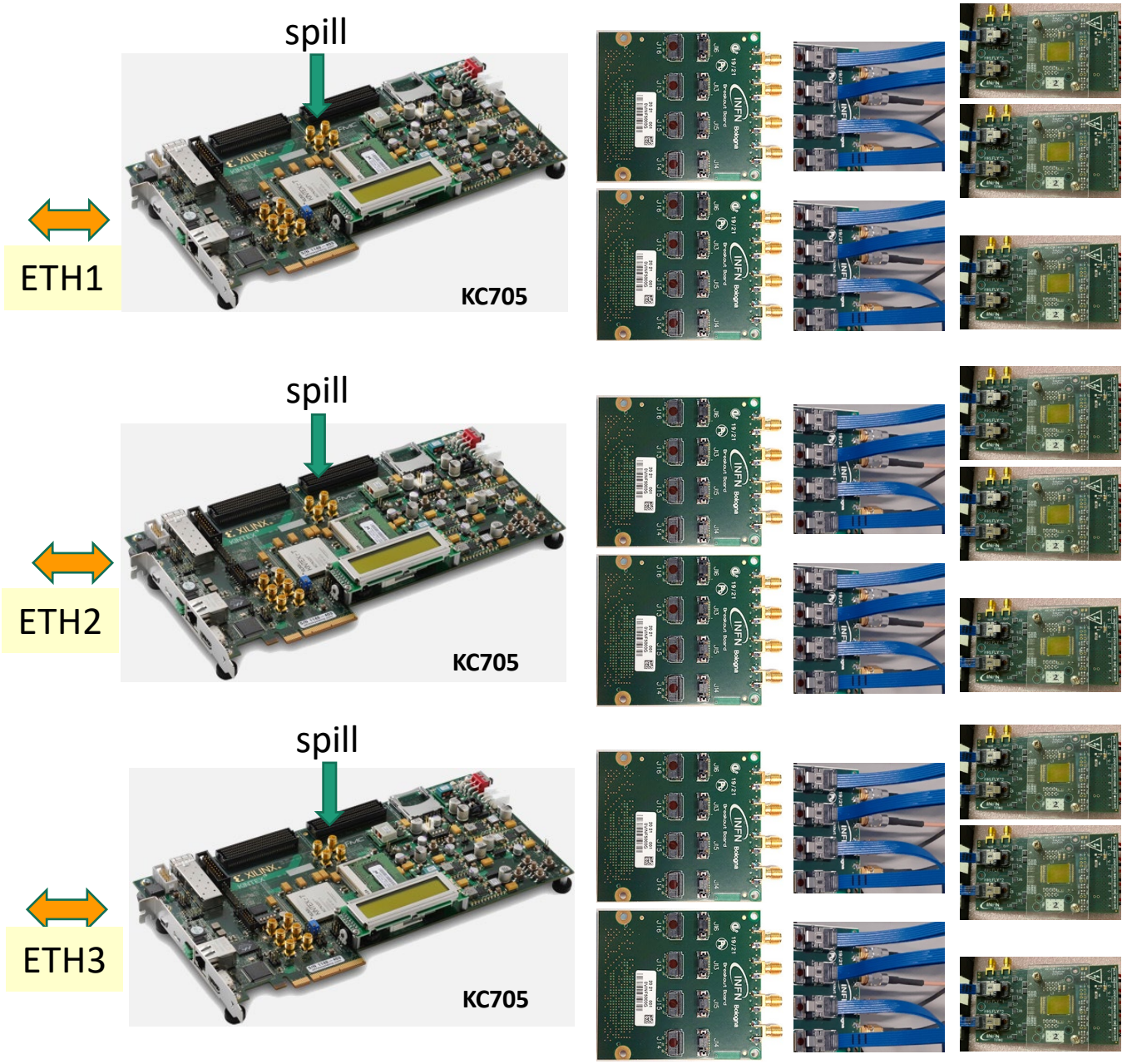
896-pixel demonstrator
(8 x 112 pixels, 100um pitch)



- Project tapeout with ARCADIA ER3
- Shall allow to test both a hybrid assembly of a CdTe detector and a fully-depleted CMOS silicon sensor X-ray imager (half of the matrix with bump pad connections for flip-chip assembly)
- (left) reticle floorplan for the ARCADIA engineering run and (top) CAD layout of the X-ray ASIC [13.4 x 4.2 mm] mini-demonstrator

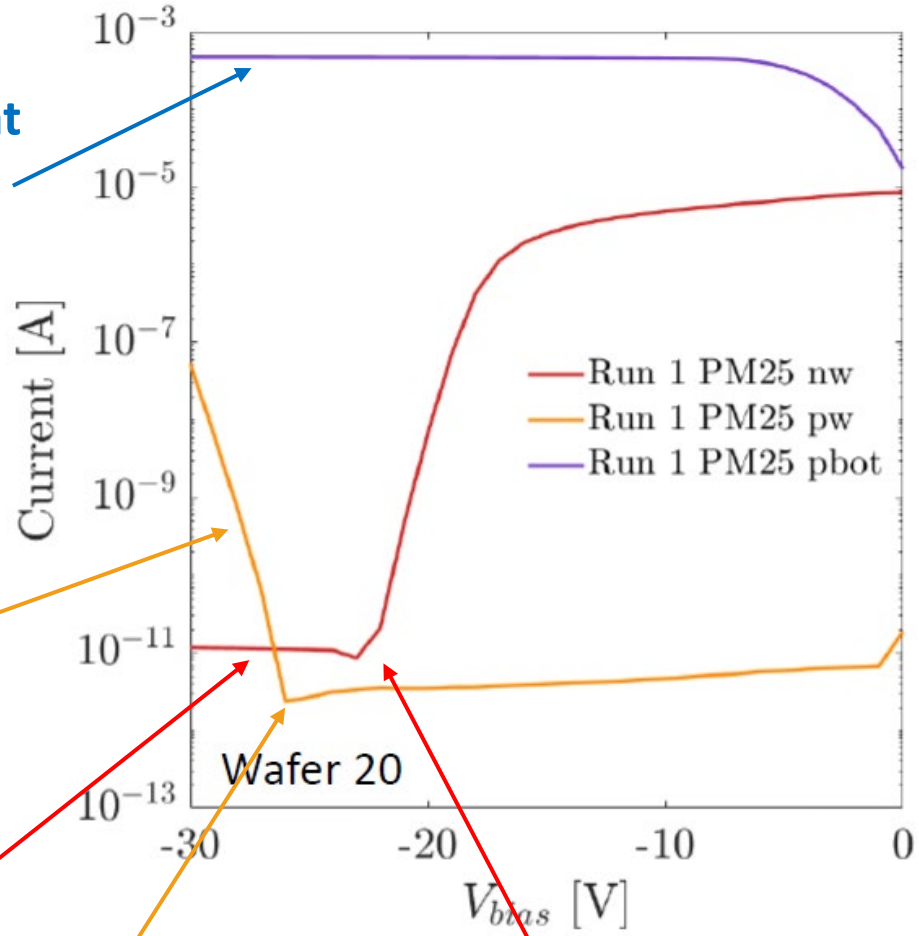
Telescope/test beam





Sensor characteristics - IV curves

Backside bias current (thermal generation at the dicing line)



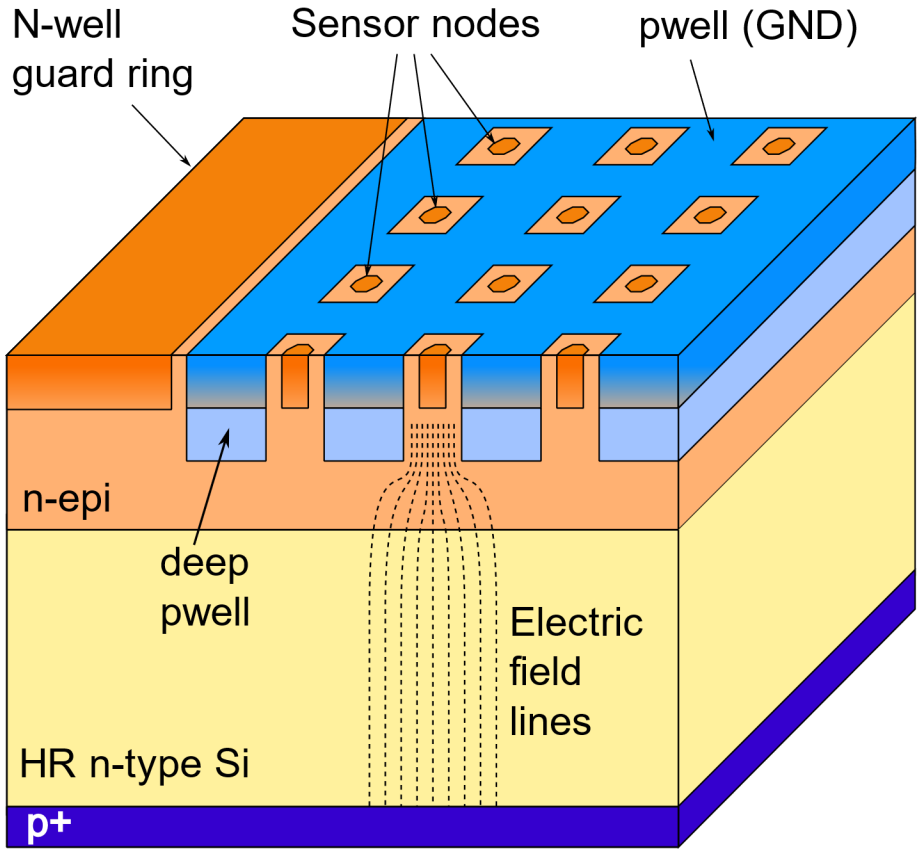
Pwell Punch-through current

Pixel dark current

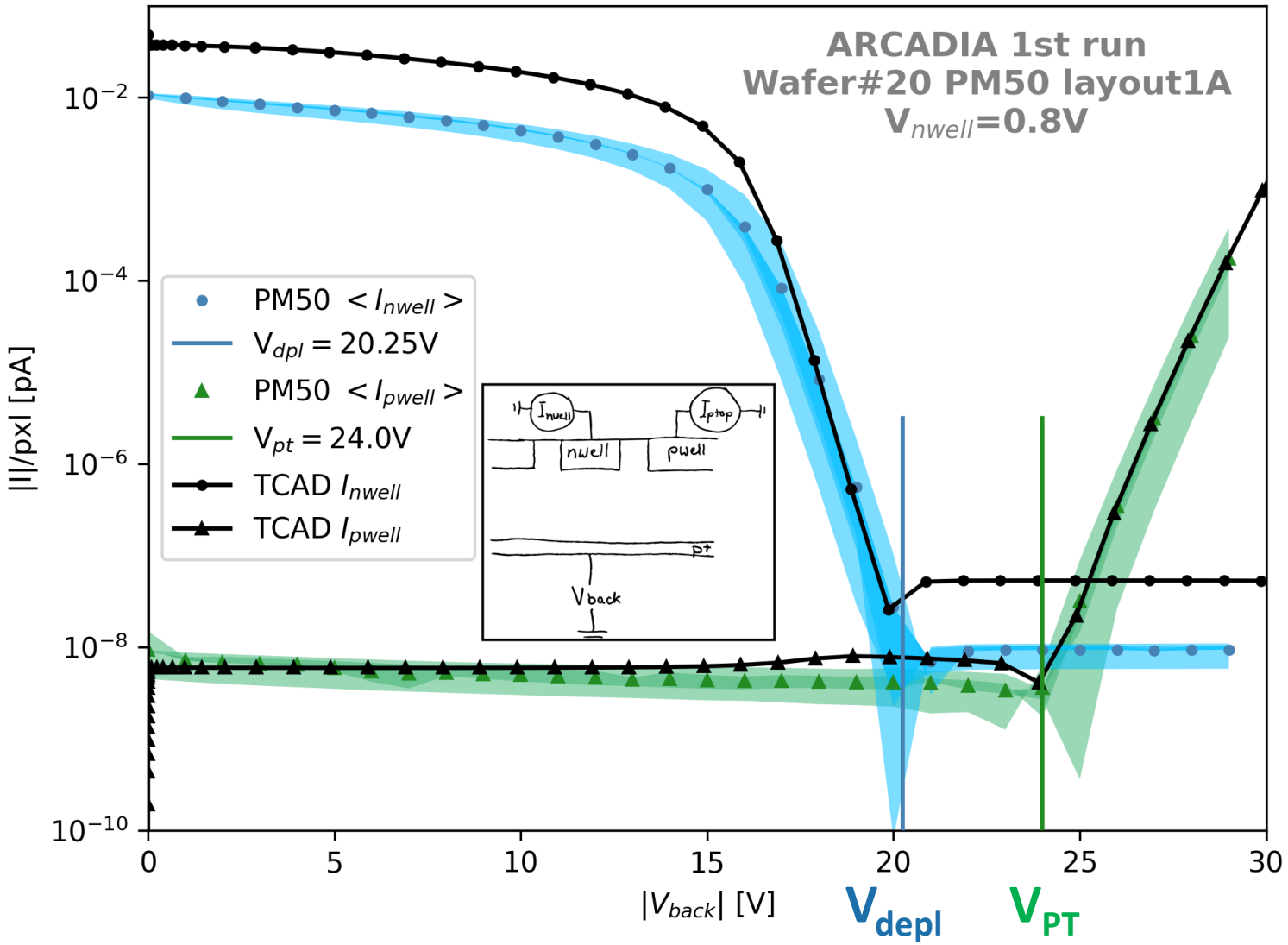
Punch-through onset voltage V_{PT}

Full depletion voltage V_{depl}

Measured on pixel test structures (arrays of pixels connected in parallel)



Pixel Current-Voltage curves – comparison with TCAD models



Experimental data acquired for different pixel layouts

Intra-wafer and inter-wafer variations were evaluated

Process parameters in **TCAD simulations** adjusted on experimental results

C. Neubüser

MD1 characterization: gain and noise