Karlsruher Institut für Technologie

CEPCPix1: A HVCMOS pixel sensor for CEPC experiment

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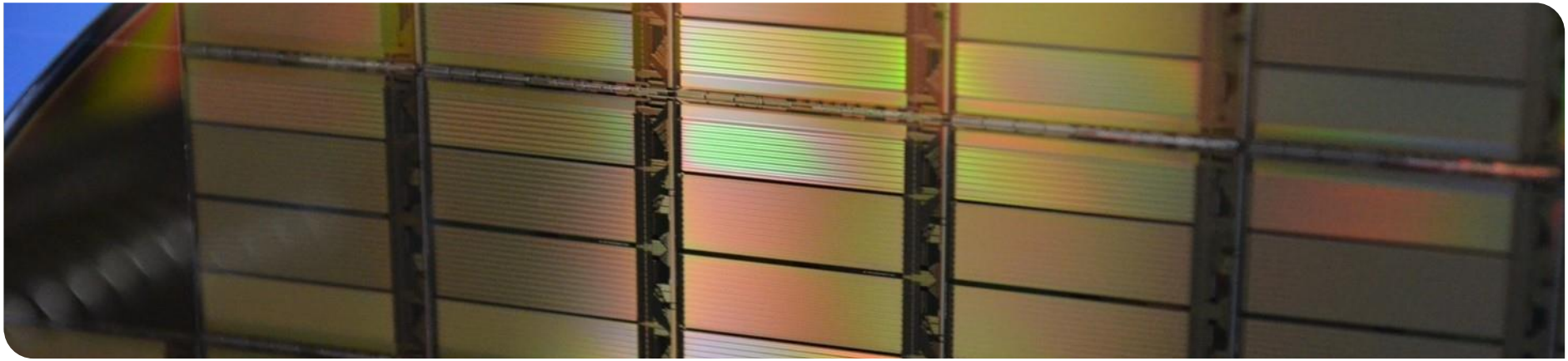


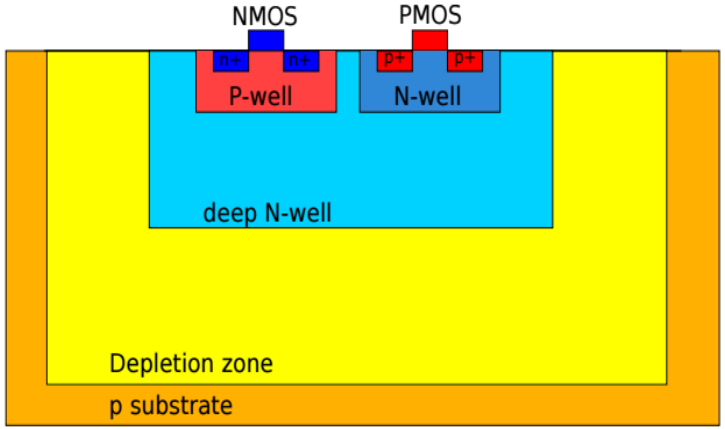
55nm High Voltage CMOS Technology

- We have submitted the dedicated CEPC design in August with 55nm HVCMOS technology
- An area of 1.25 x 1.25 mm is reserved for our design

- The 55nm logic technology combines improved performance and reduced power consumption with increased design possibilities and cost efficiencies.
- The maximum voltage for HV transistors is 32V
- Low voltage power supply is 1.2V
- Deep n-well to p-substrate should have higher breakdown
- Metal layers 1 – 5 can be used for fine pitch routing
- There are tree more thick metal layers, suitable for power

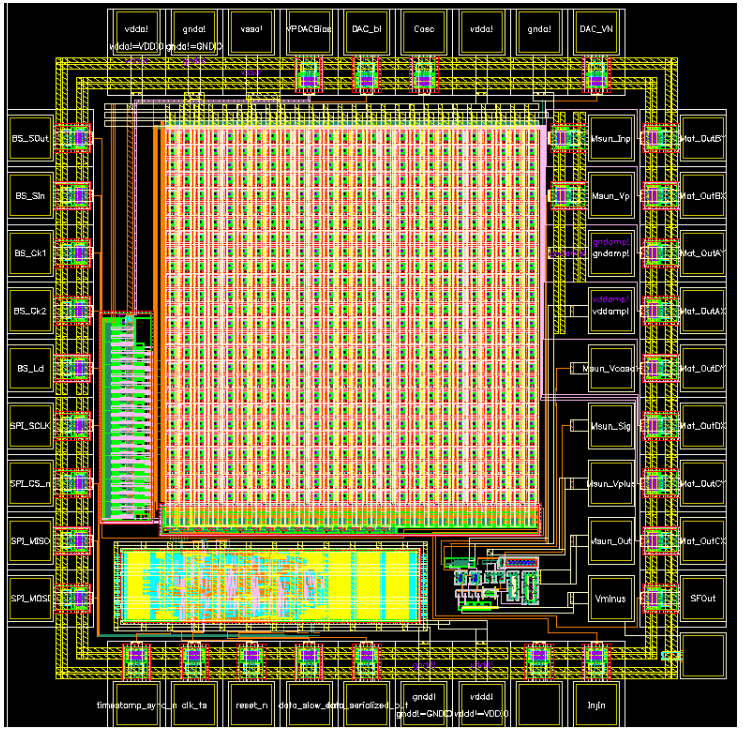
HVCMOS introduction

- Sensor and readout electronics could be produced in one chip.
- High reverse bias accelerate the charge collection by drift.
- High reverse bias creates thick depletion region between deep n/well and p substrate
- N-well/p sub diode works as sensor. Electronics embeded in deep n-well.
- Substrates from 300Ωcm to ~20kΩcm
- Could be produced in standard technology, eg. 180nm, 65nm, 55nm.
- Radiation tolerance.



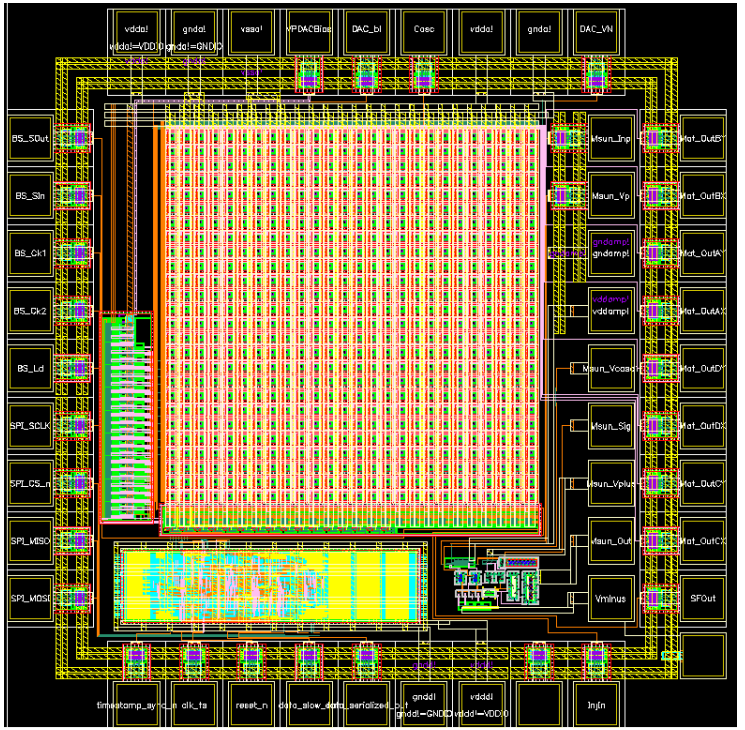
CPECPix1: Overview

- Implemented in 55nm process
- Submitted in August 2022
- Chip size: ~ 1.25 mm × 1.25 mm
- Pixel matrix: 26 columns (2 digital + 24 analog), 26 rows
- Pixel:
  - 25 µm × 25 µm
  - PMOS amplifier and NMOS comparator
- Bias voltages:
  - Integrated 8-bit voltage DACs
  - Can be supplied externally



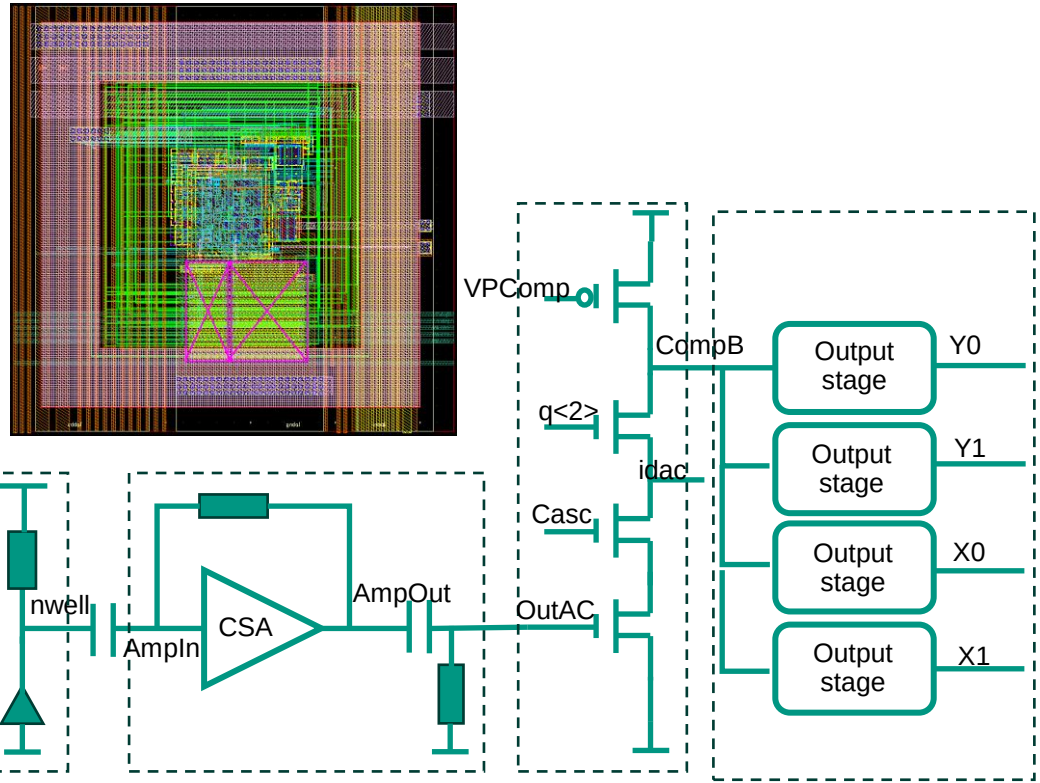
CPECPix1: Overview

- Timestamp measurement:
  - Two columns use digital encoding of pixel address and 24 columns use analog encoding of addresses
  - leading & trailing edge timestamp
  - Address double check for hit consistency
- Digital Readout FSM:
  - Polling readout of 4 hit channels
  - Compatible with test mode
- Digital Interface
  - Synchronous serialized slow output
  - Asynchronous serializer
  - SPI configuration



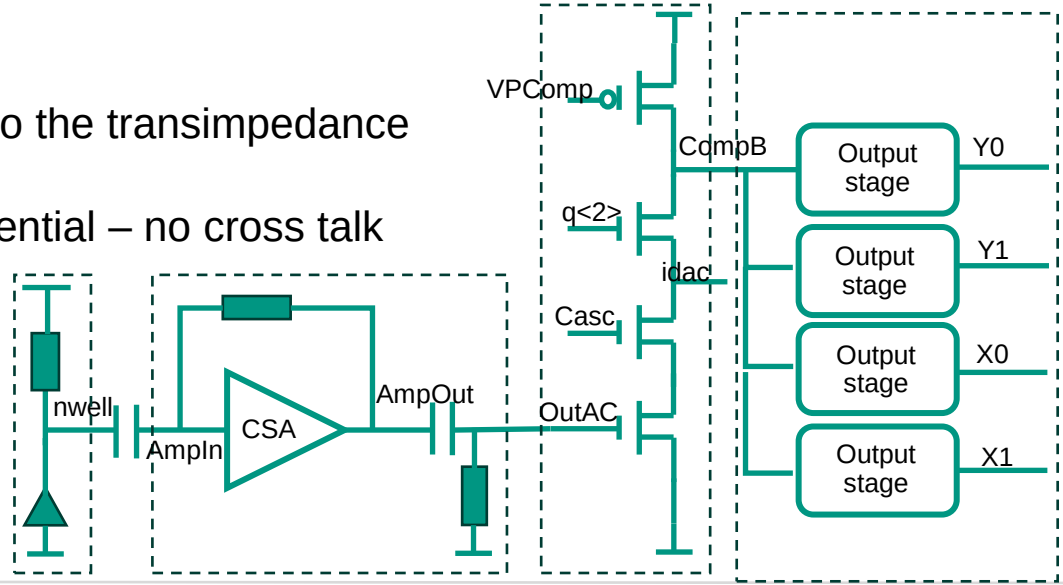
CPECPix1: Pixel Electronics

- Pixel electronics contains
  - Sensor diode
  - Charge Sensitive Amplifier (CSA)
  - CR filter
  - Comparator
  - RAM and tune DAC
  - Output stages



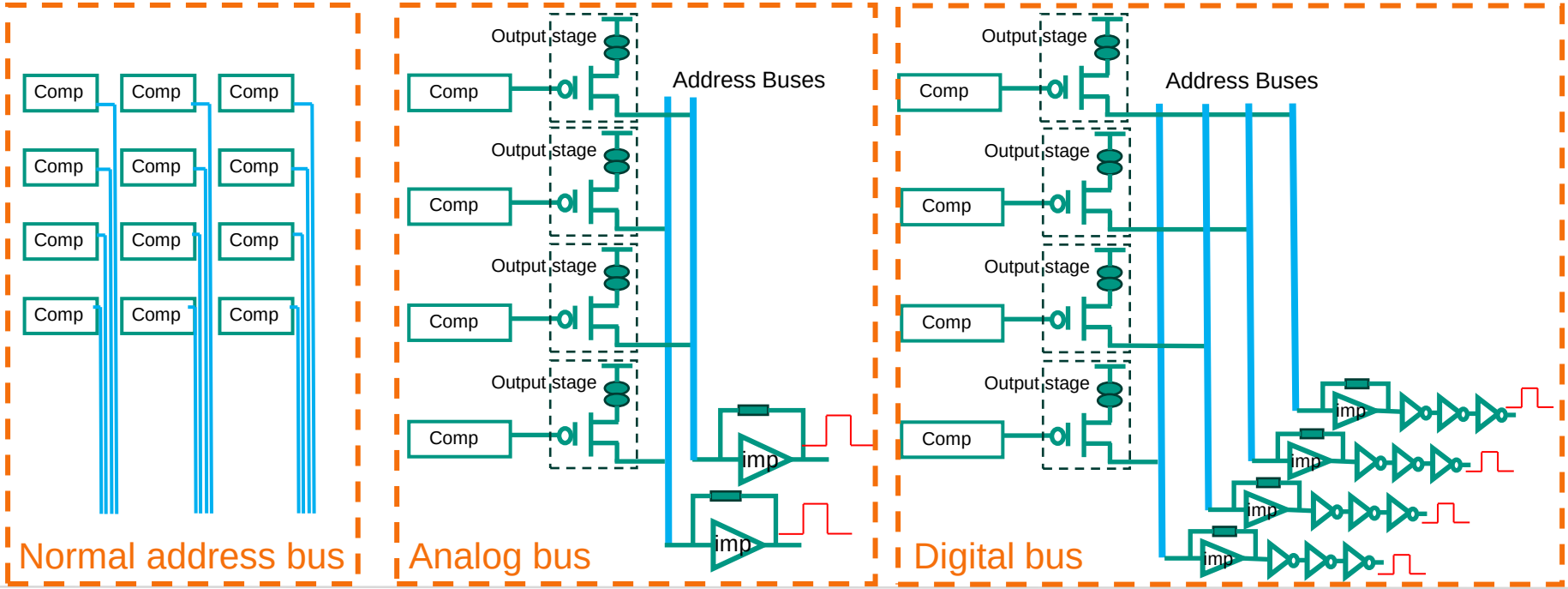
CPECPix1: Pixel Electronics

- Work principle
  - Charge collected by pixel n-well
  - Converted to voltage signal by Charge Sensitive Amplifier
  - Analog voltage pulse shaped and converted to digital signal by comparator
  - Output stage generates current
  - Current is sent via address line to the transimpedance amplifier outside matrix
  - Address lines have constant potential – no cross talk



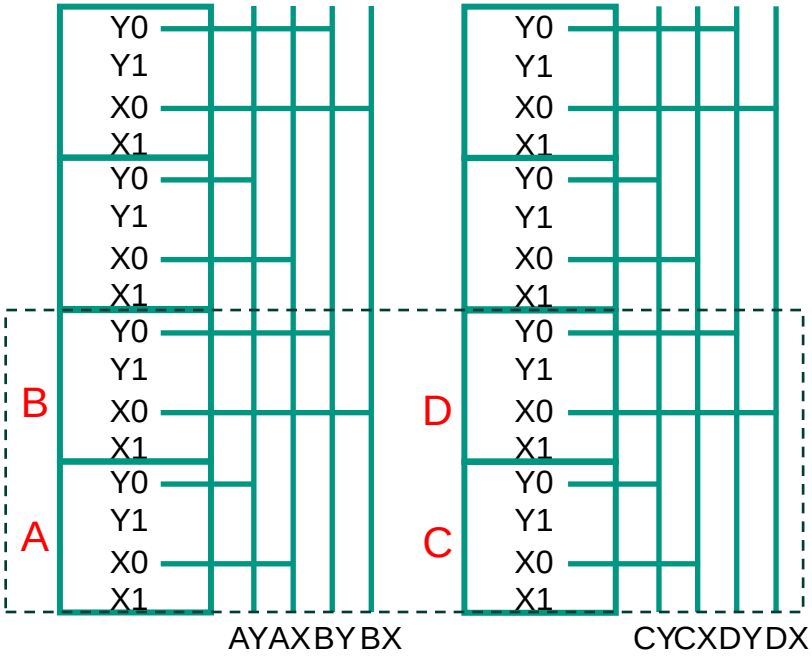
CPECPix1: Address bus

- Compare different address buses.
  - Less address buses as before version
  - Number of address buses << number of pixels



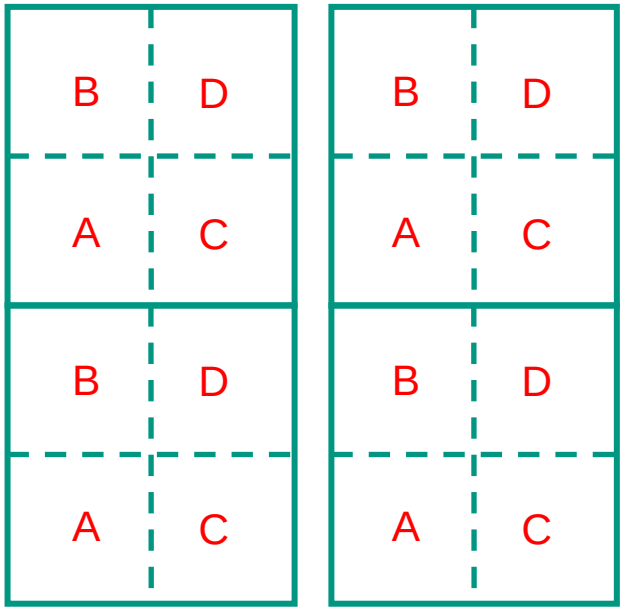
CPECPix1: Address group (Analog Part)

- Since the pixels are small, we expect 4-pixel clusters
- If we had just one hit bus line, we could not measure the amplitude of 4 pixels of a cluster
- Now I explain analog encoding
- To allow amplitude measurement of 4 pixels in a cluster, we foresee 8 address lines for whole matrix (2 per group for x and y) – AY, AX, BY, BX, CY, CX, DY, DX
- Addresses are encoded as amplitudes
- The pixel output stages are connected alternately to A, B or C, D



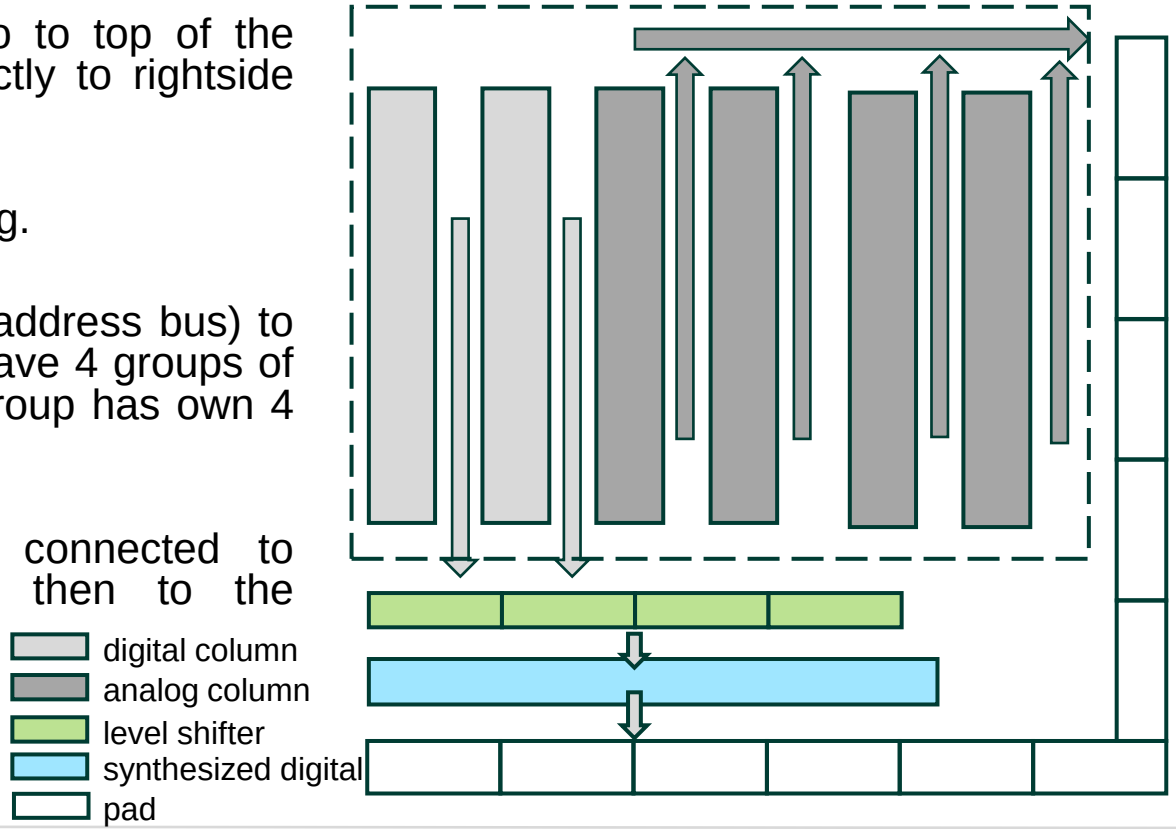
CPECPix1: Address group (Analog Part)

- For example: four columns of pixel
- In different columns the pixel Ax has different amplitudes and in different row Ay has different amplitudes.
- The address encoding is done in the way, that if 4 neighbour pixels are hit, the received code corresponds one of the pixels
- In the case of 4-pixel clusters, by examining the A, B, C, D address signals we can obtain pixel row and column by measuring amplitudes and signal amplitudes by measuring pulse width.



CPECPix1: Address hit bus to pad connection

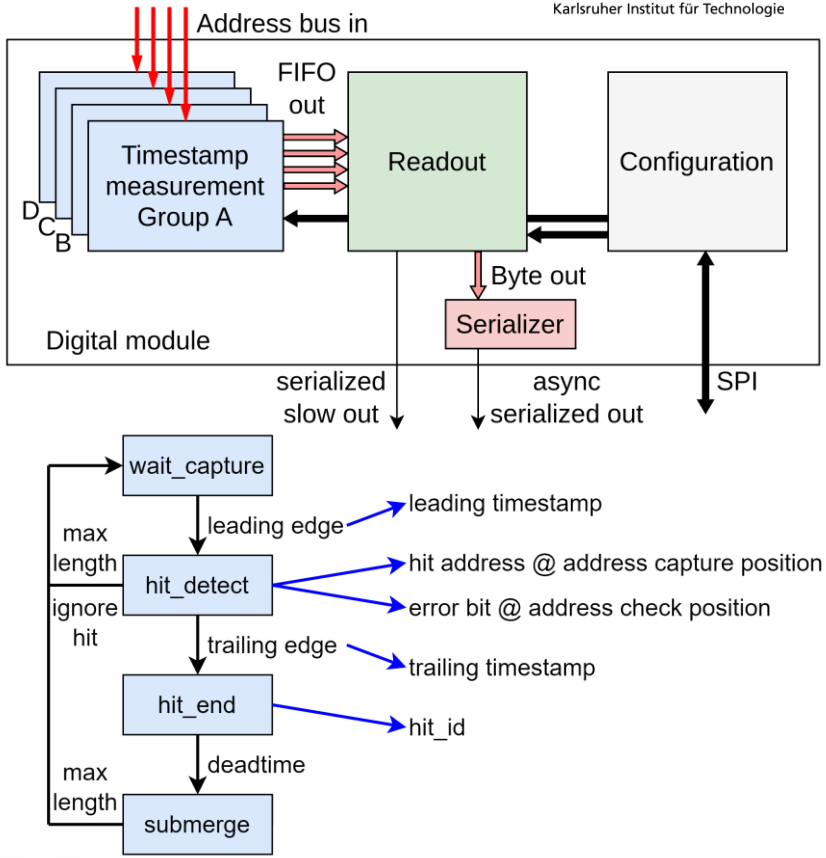
- Analog hit address lines go to top of the chip and then connect directly to rightside pads.
- Now I explain digital encoding.
- We use 4 bit digital signal (address bus) to encode pixel address. We have 4 groups of pixels A B C D and every group has own 4 bit address bus.
- Digital address lines are connected to voltage level shifter and then to the synthesized digital part.



CEPCPix1: Digital Readout

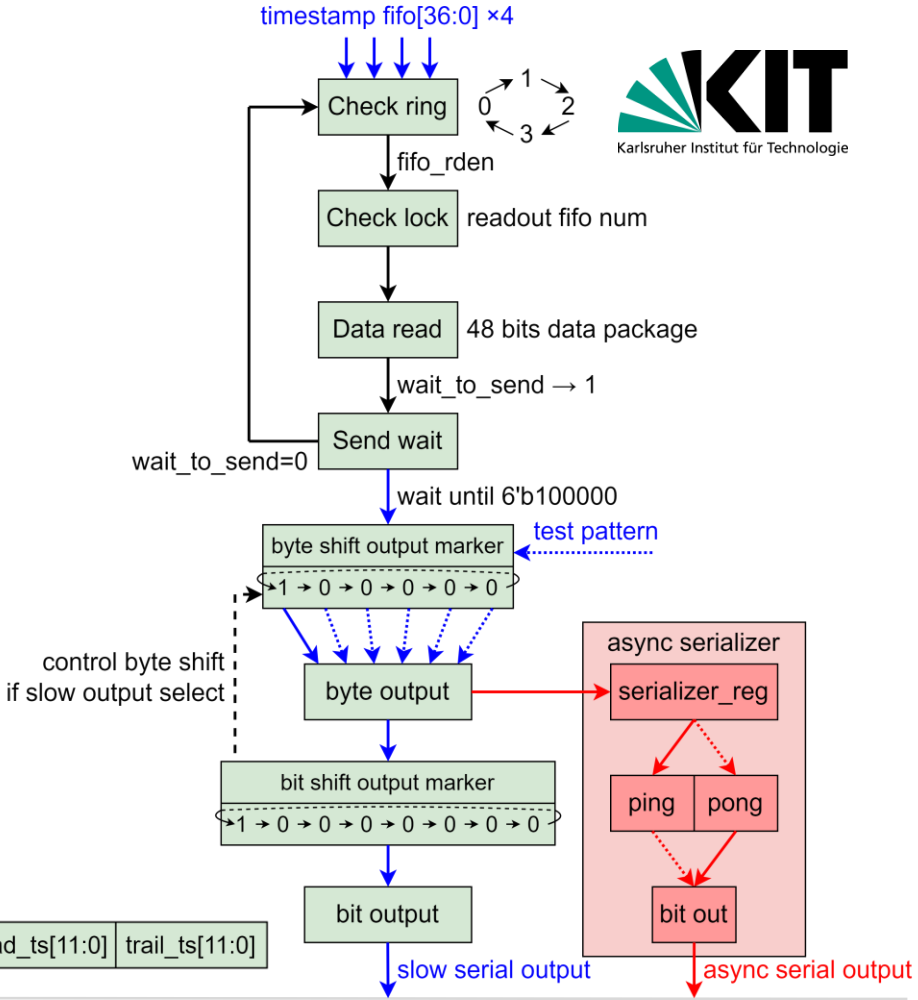
- Timestamp measurement
  - Timestamp bin size 5 ns
  - Make an OR logic on 4 address bit input
  - Hit pulse width ~ 1 µs
    - Set a detect max length parameter
    - Ignore too long pulse
    - Set an address check position parameter
    - Double check address at leading edge
    - Error bit for overlapped or too short pulse
  - Submerge FSM until detect max length
    - Shield spurs hit, control data rate
  - Output fifo for each timestamp channel
    - 37 bits fifo bit width

error_bit	addr[3:0]	hit_id[7:0]	lead_ts[11:0]	trail_ts[11:0]



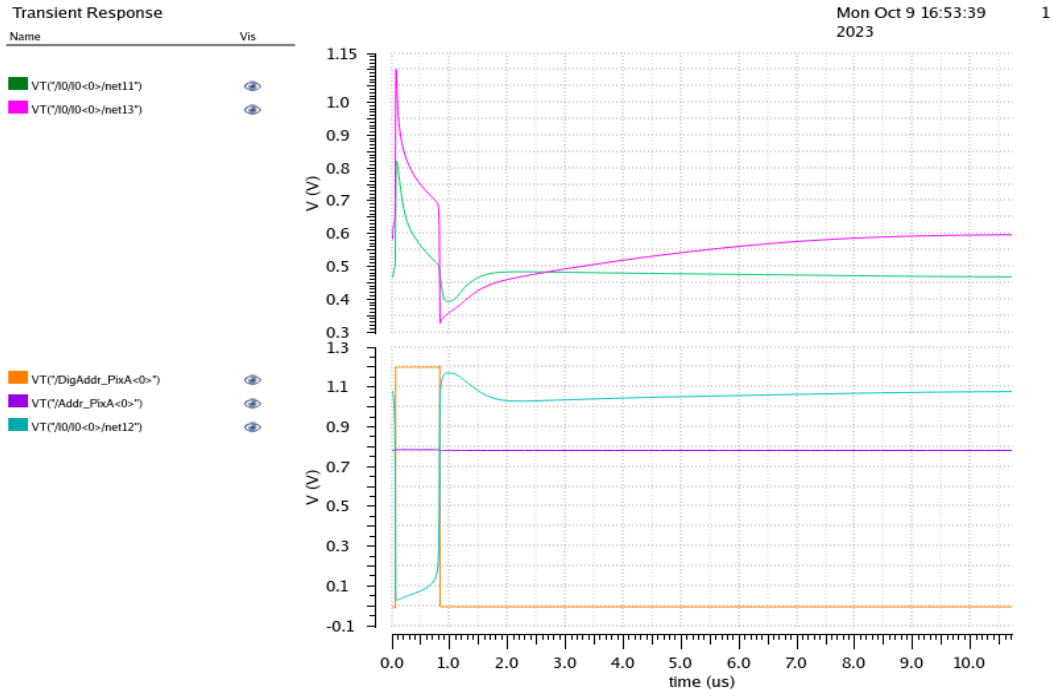
CEPCPix1: Digital Readout

- Data readout
  - Polling readout from 4 timestamp fifo
  - Mode select
    - Hit data
    - Test pattern: fixed or counter
  - 48 bits data package to readout interface
- Readout interface
  - Mutual exclusive output selection
  - Slow serial output
    - 48 to 8 to 1
  - Asynchronous serializer output
    - 8 to 1 serializer
    - Ping-pong register to cross clock domain



Header[5:0]	pack_marker[1:0]	chn_num[1:0]	1'b0	error_bit	addr[3:0]	hit_id[7:0]	lead_ts[11:0]	trail_ts[11:0]

Simulation results



Conclusion

- HVCMOS introduction and 55nm HVCMOS technology

- CEPCPix1: Analog Part
  - 4 output stages in each pixel electronics
  - Address lines have constant potential → no cross talk
  - Special design in pixel to reduce analog and digital buses
  - Group 4-pixel cluster and use different amplitudes of pixel A in each group to cope with charge sharing

- CEPCPix1: Digital Readout Part
  - Hit pulse from address bus capture rising and falling edge of time stamp
  - Several design to solve overlap problem
  - Two mutually exclusive interface (asnychronous interface is 8 times faster than main clock)

Thank you!