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Research progress on multichannel，high precision TDC based on VDL technology

As the key component of time measurement electronics, Time-to-Digital Converter (TDC) has become a research hotspot in high energy physics, nuclear medical imaging and radiation detecting. Many TDC topologies have been proposed during the past two decades to realize sub-100 ps time resolution, among which vernier delay loop (VDL) is the most appropriate considering the performance, the design complexity and the possibility of implementation under less elaborate process.

Recently, we have designed 2 TDC ASIC prototypes under 180-nm CMOS process. In 2022, a high-precision TDC with eight identical channels was proposed. The asynchronous time interval measurement is implemented with one channel for the Start event and another channel for the Stop event, which can make use of a technique known as the sliding scale to effectively improve the linearity of TDC. Aiming to realize high resolution and large dynamic range at the same time, the proposed TDC adopts the three-step structure. As the first step, a binary counter is used to count up the number of clock cycles between Start and Stop. And then the time intervals between Start/Stop and corresponding rising edges of reference clock is measured by the multiphase clock interpolation circuit. The finest step is performed with the vernier delay loop structure, which is used to measure the residual time of the last step. The vernier measurement is realized with two Delay Locked Loops (DLLs) whose unit delay is slightly different, so we can get a fine resolution of 41.7 ps. Testing results showed that this TDC can get the single-shoot resolution of 56.2 ps with the clock frequency of 100 MHz, the DNL and INL are better than 0.4 LSB and 3.8 LSB respectively.

Earlier this year, we designed a 6-channel time-amplifier based TDC. This new TDC is also based on the multi-step architecture mentioned above, in which the residual time of the second measuring stage is broadened by 5 times and then delivered to the third stage. The time resolution can be raised to 8.3 ps while other performances may deteriorate. This chip was taped out in September and will be tested soon.

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