Test of CMOS chip using 55nm process

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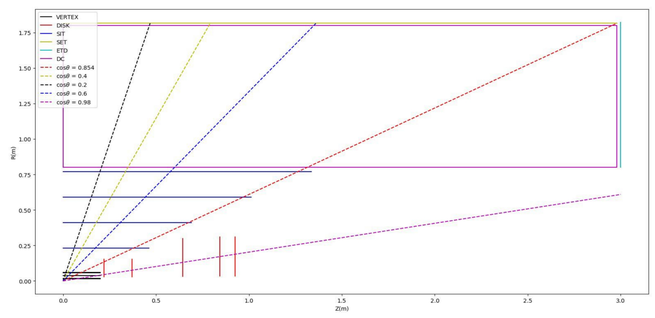
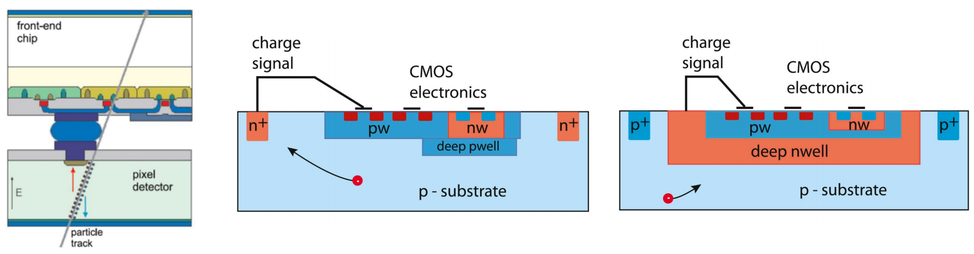
1 Introduction

CEPC plans to utilize a large-area, fine-pitch, low-material, fast-readout and economic silicon-based tracker system to achieve exceptional spatial resolution.



An alternative tracing system conceptual design.

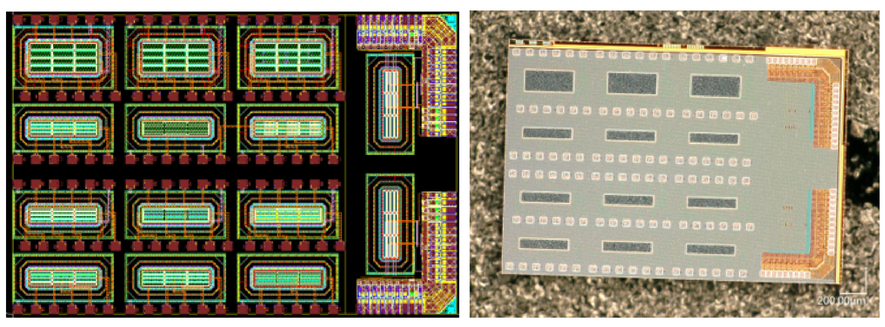
CMOS technology presents an appealing solution due to its high performance and cost-effectiveness. Compared to hybrid silicon pixel sensors, the CMOS process allows for a smaller size while guaranteeing a lower amount of material budget. It is also a potential candidate for future upgrades to other experiments, i.e., the LHCb Upstream Tracker. Unlike many CMOS processes that require modifications and enhancements to generate sufficient signal, the commercially available high resistance wafer based High Voltage CMOS (HVCMOS) is intrinsically radiation hard and has large capacitance for signal acquisition. The potentially lifting noise and power consumption of HVCMOS, compared to the small-electrode CMOS, are tolerable for large area tracker. Moreover, the HVCMOS production process has further developed in domestic foundry recently, could be customized commercially.



Hybrid silicon pixel sensor small-electrode CMOS high-voltage CMOS basic structure

2 MPW submission

The 1st design was submitted in October 2022 for MPW with 55nm low leakage process. 12 layout designs integrated on a chip with an area of 3×2 mm^2. Each array contains 12 pixels, which minimum size is 25×150 μm^2 or 50×150 μm^2, varying with or without P stop between them. Simple charge sensitive amplifier structure was also added. Though the high resistance substrate was not yet available, a similar deep N well separating the transistors and the sensor part. The 2nd design has also been submitted in August 2023, which will be the real validation of the sensor with high resistance wafer. The updated analog amplifier, switch circuit and variant diode structures were added in this version.



The 1st layout design of CMOS chip and its production sample.

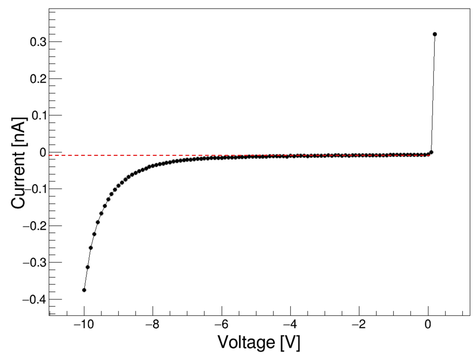
3 Lab test set up

The preliminary test, mainly IV and CV test, is based on production sample from the 1st design. In order to stably measure reliable sensor characteristics for different pixel array to prove the behavior whether is good diode like or not. The chip was tested by connected to probes in a thermostatic and magnetic shielded probe station. The Keithley 2470 source-meter was used as a bias source meantime could measuring current with a stable accuracy of 1 pA, and the capacitance of pixel array was measured by E4980A LCR instrument with an accuracy of several tenth fF approximately. The accuracy is sufficient for a single small diode of $0.1 \sim 0.2$ pF and a leakage current of 10 pA in estimation.

The IV and CV test probe station.

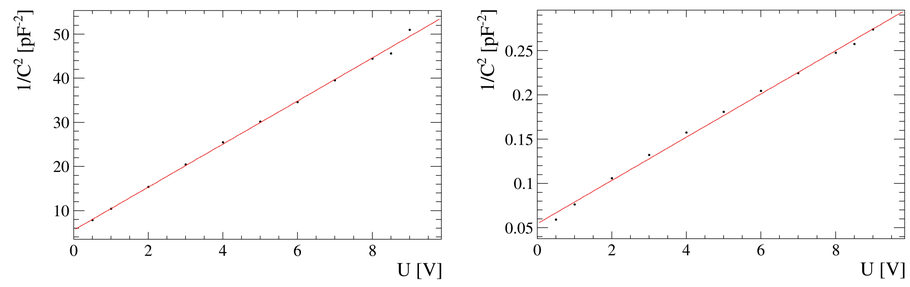
4 IV/CV results || Discussion

The IV test results show very good diode behavior with low leakage $\sim$ 10 pA for all diode design, as expected. It is obvious that there is clear positive conduction, and gradually reverse breakdown begins as voltage increases to -9V $\sim$ -10V. Significant improvement in reverse breakdown voltage is expected with the use of high resistivity substrate and high voltage process.



A typical IV test result, the leakage as low as $\sim$ 10 pA.

The CV test results are comparable for different diode design The capacitance tends to stabilize as the diode is depleted and is proportional to the number of pixels in parallel After subtracting the external capacitance of the testing system, around 0.5 pF, a good linear relationship between pixel array capacitance in inverse square and voltage can be obtained. For single small pixel, the calculated capacitance is compatible with predictions $0.1 \sim 0.2$ pF.



An example of CV test result, where the left plot shows a single pixel and the right for the result of ten pixels in parallel. Note that the external capacitance of $\sim$ 0.5 pF has been subtracted.

As a conclusion, first test results from CMOS chip show that the technology of 55 nm process with low leakage is promising. The preparation for test the HVCMOS in the near future is ongoing:

- IV/CV test under different conditions.
- Prepared laser system to verify pixel size and spatial resolution.
- Using nucleon beam in SNC, DESY or CERN to investigate real response of the HVCMOS chip to the MIP, and also study the radiation resistance.