Exploration of a 55nm HV-CMOS process for the CEPC silicon tracker

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ABSTRACT

To explore process for next generation HV-CMOS pixel sensors, a prototype was designed and submitted in August 2023 using a 55nm HV-CMOS technology with a 1kΩ·cm substrate. This prototype includes a guard ring with a width of 170μm, a 32×20 pixel-matrix, and 5 diode arrays. The pixel matrix comprises 6 flavor charge sensing diodes with a constant pixel size of 40μm×80μm. Charge sensing amplifier and discriminator are integrated in pixels. The peripheral block includes row/column selection, bias DACs, a bandgap reference, and readout buffers.

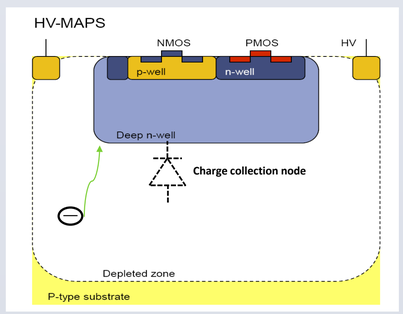
INTRODUCTION

Monolithic Active Pixel Sensors (MAPS) utilizing a specialized High-Voltage CMOS technology (HV-CMOS) have proven to be a promising choice for the CEPC silicon tracker. By applying a high reverse bias voltage (> -50V) to a highly resistive substrate (>a few hundreds of Ω·cm), it becomes possible to create a depletion depth of a few tens of microns. This results in superior time resolution and enhanced radiation hardness compared to standard CMOS processes.

Over the past decade, the development of HV-CMOS MAPS has primarily focused on the 180/150 nm processes. Transitioning to a smaller technology node not only enhances the current design's performance (power dissipation, readout speed, TID, etc.) but also opens up new possibilities. With a smaller technology node, more transistors and functionalities can be integrated into each pixel.

PROCESS SPECIFICS

- 55nm High-Voltage CMOS process;
- 1kΩ·cm p-type substrate;
- Custom designed IO;
- Core power: 1.2V;
- Triple-well process: n/p/deep n-well;
- Deep n-well/p-substrate breakdown Voltage > 50V;
- 10-metal layers is possible for fine pitch routing, including 2 thick metal layers for power;



Layout of the submission

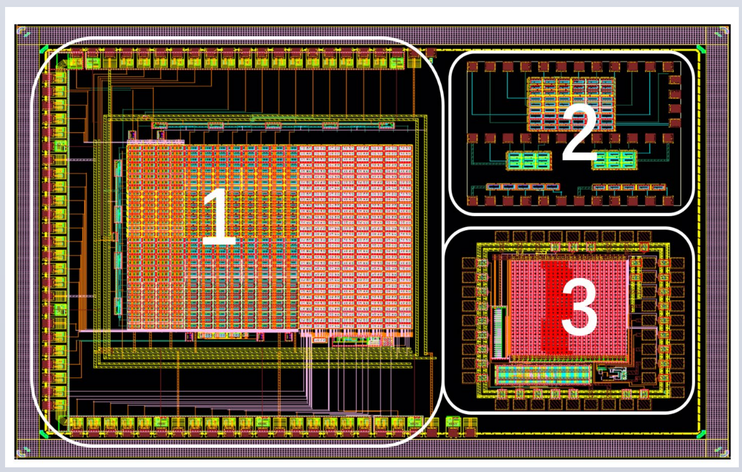


Figure: layout of the first submission on the 55nm HV-CMOS process. 3 independent sections are included for different purpose. The whole chip size is 4mm×3mm.

- 1st section: a 32×20 pixel matrix comprises various diodes and in-pixel amplifier and discriminator design for process validation;
- 2nd section: 5 diode array for charge sensing diodes I-V/ C-V study;
- 3rd section: a 26×26 pixel matrix with relative digital readout periphery for new electronics structure study; (Hui Zhang's talk & Ruoshi Dong' poster)

Guard ring & pixels

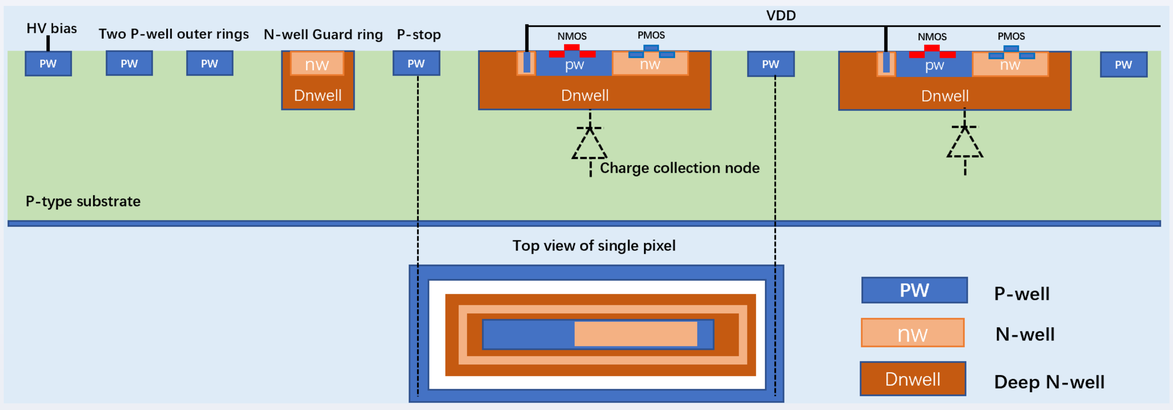


Figure: Cross-section and top view of the guard ring and pixel design.

Table: 6 flavor charge sensing diodes comprised in the section 1&2.

Diodes flavor	Specifications	
Pix_D10core	Single DNW size: 30μm×70μm, distance between two diodes 10μm	With P stop
Pix_D10core_wps		Without P stop
Pix_D15core	Single DNW size: 25μm×65μm, distance between two diodes 15μm	With P stop
Pix_D15core_wps		Without P stop
Pix_D20core	Single DNW size: 20μm×60μm, distance between two diodes 20μm	With P stop
Pix_D20core_wps		Without P stop

Charge Sensing Amplifier & Discriminators

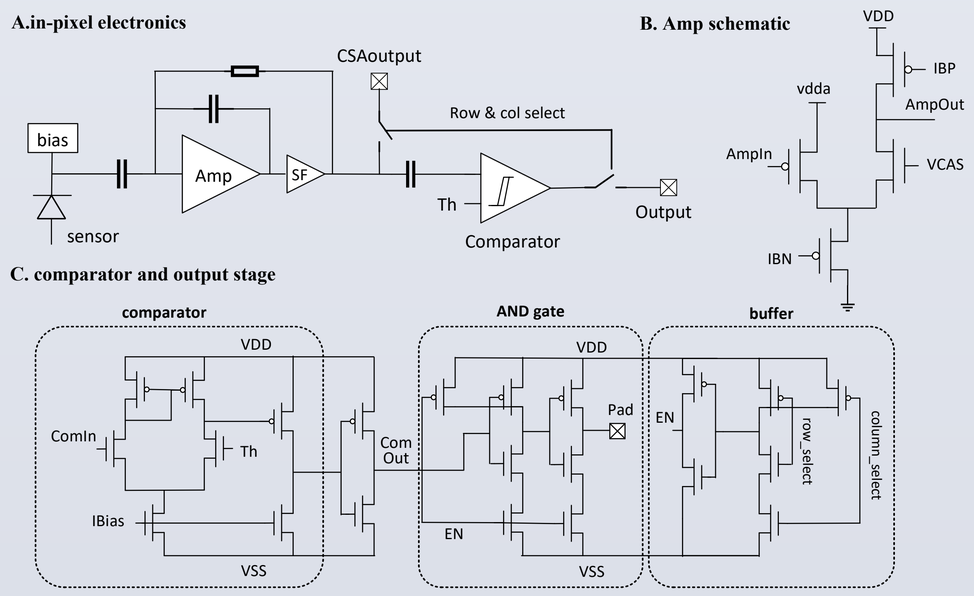


Figure: One version in-pixel electronics in the 1st section (two different versions in total). Both the analogue and digital signals are output.

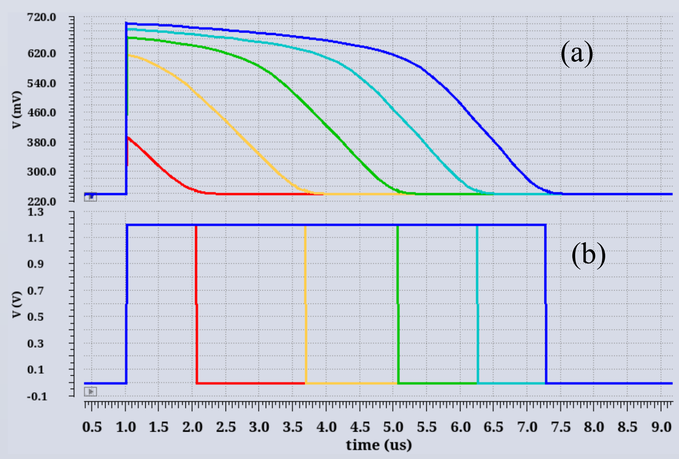


Figure: Output transients voltage of the output of (a) CSA, (b) the discriminator for different charge varied linearly between 2ke⁻ and 18ke⁻ in 4ke⁻ steps (simulation results, C_{input}= 150fF)

CONCLUSION AND PERSPECTIVES

The initial submission utilizing the 55nm HV-CMOS process was completed in August 2023. It incorporated various versions of charge sensing diodes, in-pixel electronics, and readout structures. Currently, efforts are underway for preparation of design validation. The forthcoming test results are anticipated to offer vital insights, serving as essential benchmarks for the future advancement of HV-CMOS pixel sensors for the CEPC tracker.