Introduction to Belle II TRG system

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on behalf of the Belle II TRG group

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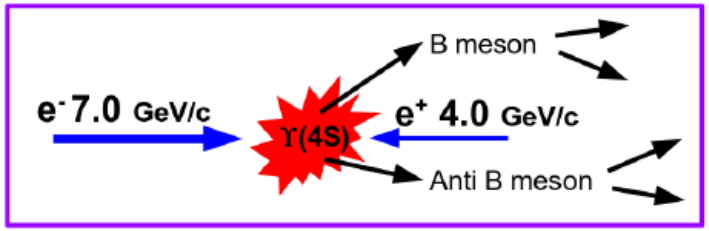
Outline

- Introduction: SuperKEKB, Belle II, Trigger and DAQ
- Belle II Level-1 Trigger (TRG) system:
  - Electronics device
  - Sub-triggers: CDC, ECL, TOP, KLM
  - Global triggers: Global Reconstruction Logic (GRL) and Global Decision Logic (GDL)
  - Upgrade plans
- Summary

SuperKEKB

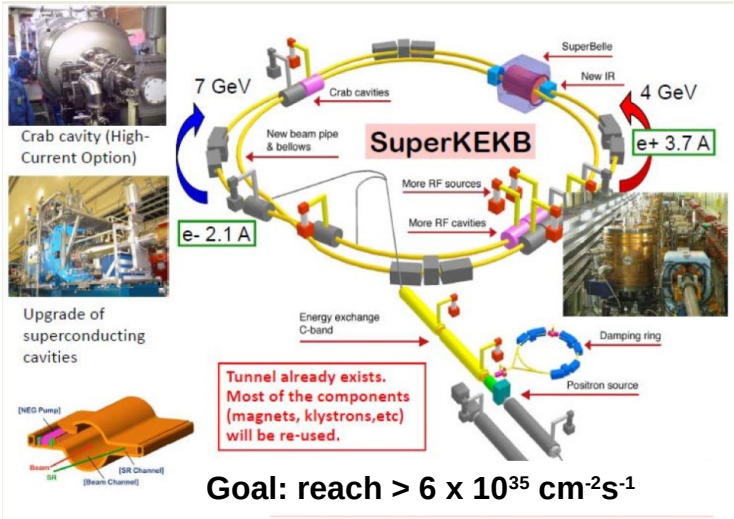
- SuperKEKB: Upgraded from KEKB.
  - More than 30 times larger luminosity of KEKB with nano beam scheme.

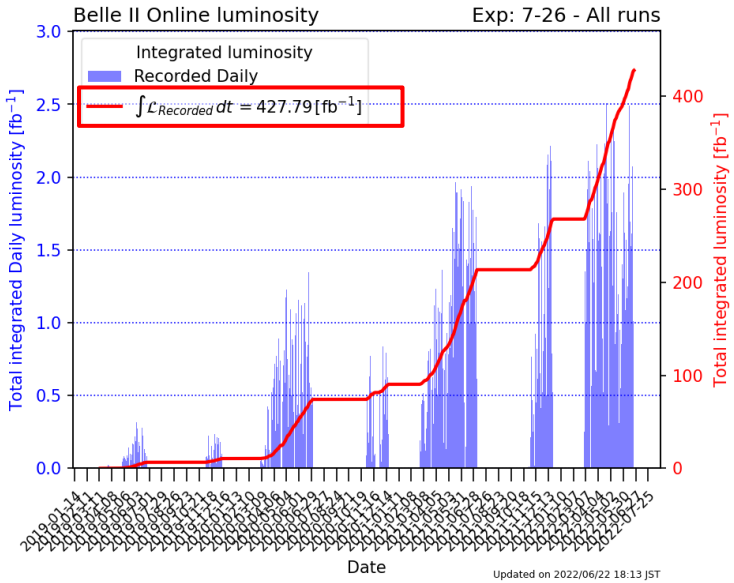
- Asymmetric energy collider:
  - 7.0 GeV e^- and 4.0 GeV e^+ for Y(4S) $\rightarrow B\bar{B}$.



- Luminosity achievement:
  - L_{peak} = 4.65 x 10^{34} $cm^{-2}s^{-1}$.
    World record. ~Two times of KEKB record with much smaller beam current.
  - L_{int} = ~427 fb^{-1} up to Jun. 2022.

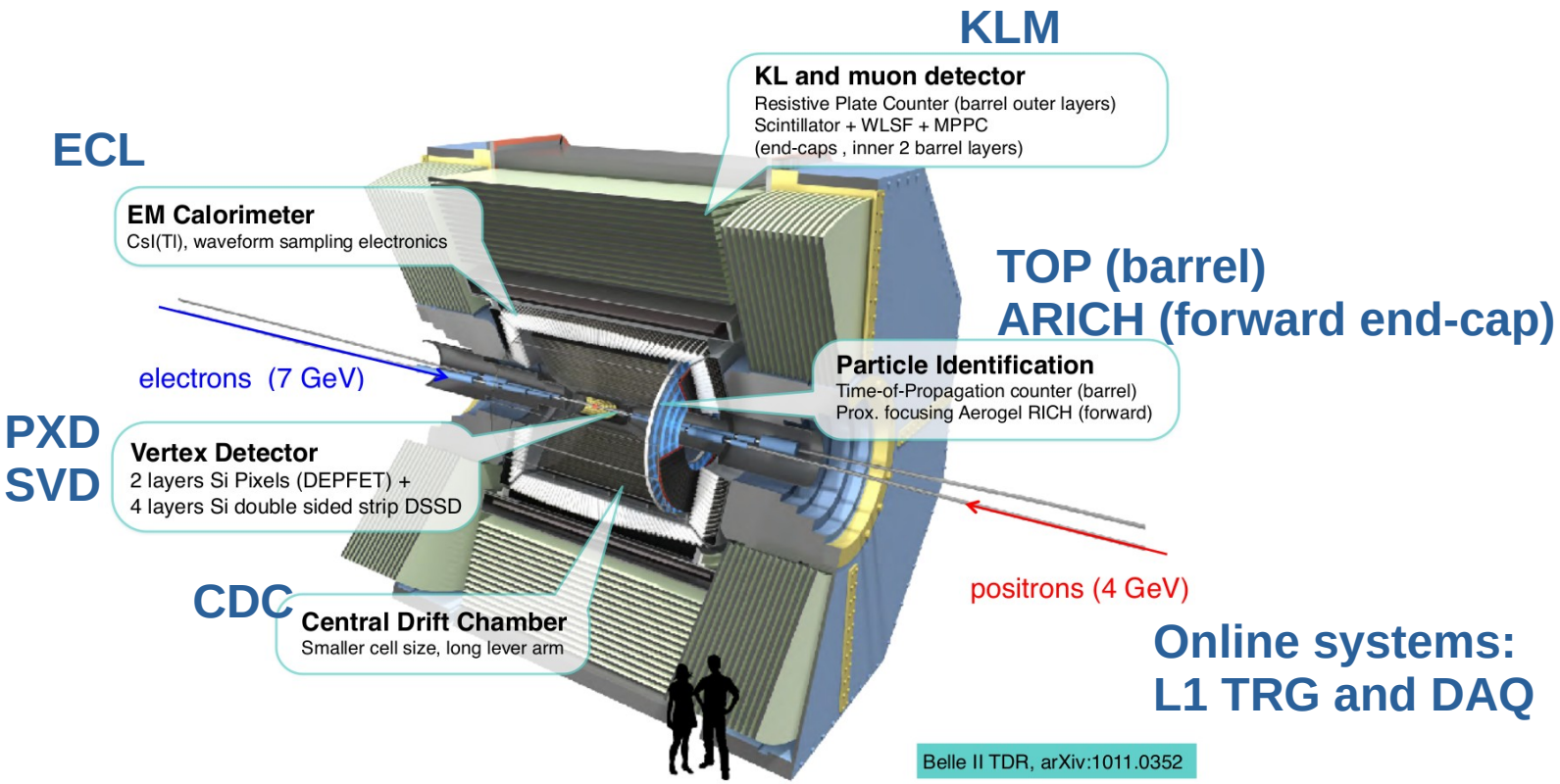
- Will resume beam collision in 2024 with PXD full installation.





Belle II detector

- Belle II: Newly-designed sub-detectors set to improve detection performance.

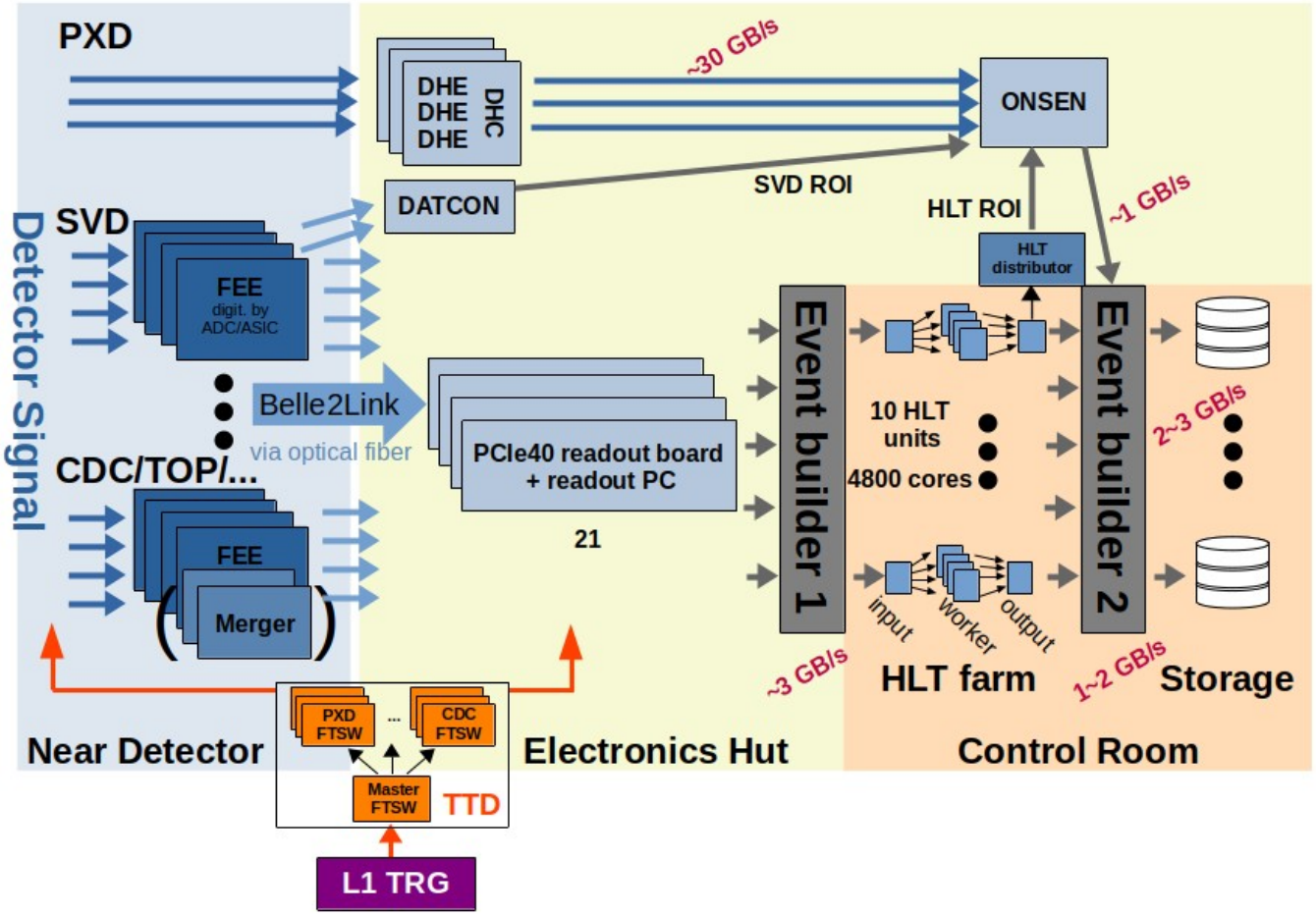


- Physics target of Belle II:
  - Rare B, τ, charm physics, Dark Matter search, CP Violation.

- Requirement for data taking:
  - High L1 trigger rate (~30 kHz), high background, and large event size.

Belle II DAQ system

- Common readout system for each sub-detector (except for PXD)
- Timing and trigger distribution (TTD) for trigger signal from L1 TRG.
- Pipeline readout
- Target: 30 kHz trigger rate and raw event size of 1 MB.



Belle II TRG system

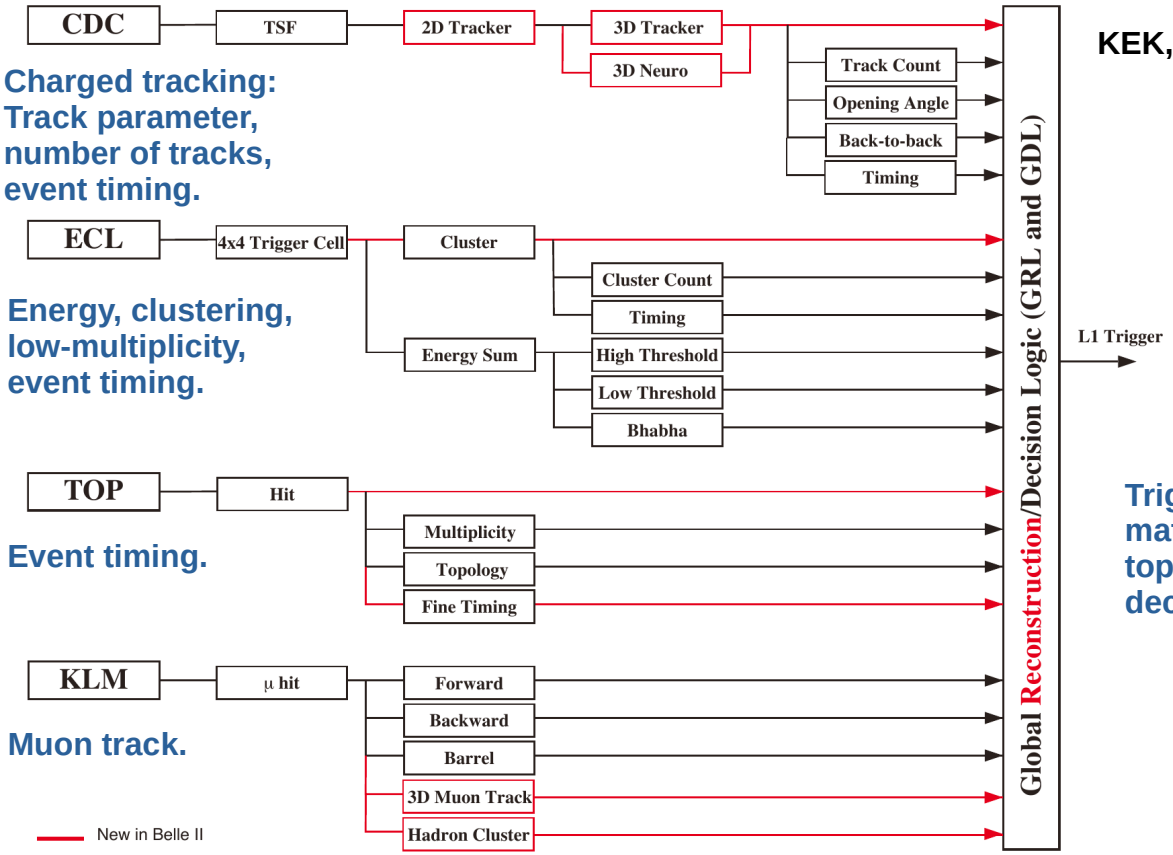
- Provide L1 trigger signal to DAQ using FPGA chips for real-time processing on detector raw data.
- Why L1?
  - Buffer storage are not enough for all data due to high event rate and short bunch spacing in collider experiment.
- 4 sub-trigger systems + 2 global trigger systems.

KEK, NTU, FJU, NUU, KIT, TUM, MPI, KU, KMI Nagoya, U. of Tokyo

Hanyang U., BINP, Notice co.

U. Pittsburgh, Hawaii U.

Virginia Tech., Hawaii U.



Conditions and requirements for TRG

- Requirements:
  - Overall latency < 4.4 μs.
  - ~100% eff. for hadronic events.
  - Max 30 kHz @ $8*10^{35}$ $cm^{-2}s^{-1}$
  - Timing precision: < 10 ns
  - Event separation: 500 ns

- Physics processes in interest:

- Examples of technical challenges so far:
  - Low-multiplicity trigger mainly based on ECL, but contamination from noise, beam bkg or Bhabha.
  - Energy trigger with high eff. but high rate too.
  - Injection bkg.
  - Drawback of track trigger at endcap.
  - High track trigger rate due to crosstalk noise.
  - Latency budget due to transmission or complicated logics.
  - .....

Phase2 Lum. Record

Process	C.S. (nb)	R@L=5.5x10^{33} (Hz)	R@L=8x10^{35} (Hz)	TRG logic
Upsilon(4S)	1.2	6.6	960	CDC 3trk(fff) ECL high energy(hie) ECL 4 clusters(c4)
Continuum	2.8	15.4	2200	
μμ	0.8	4.4	640	CDC 2trk(ffo) etc
ττ	0.8	4.4	640	
Bhabha	44	242	350 *	ECL Bhabha(bhabha, 3D bhabha)
γ-γ	2.4	13.2	19 *	
Two photon	13	71.5	10000	CDC 2trk(ffo) etc
Total	67	357.5	~15000	

Universal Trigger boards: UT3 and UT4

- Most of the major logics in Belle II TRG are implemented in these two Universal Trigger boards.
  - Different from Front-End electronics, TRG device requires FPGA with large amount of logic cells and IO bandwidth due to the complexity of the algorithm design.

- Interface:
  - QSFP optical link.
  - Lemo and RJ45 for clock input from accelerator.
  - LVDS.
  - VME 6U: Power, slow control, flash memory access.

Belle II UT3

Xilinx Virtex-6
xc6vhx380t, xc6vhx565t
11.2 Gbps with 64B/66B

Belle II UT4

Xilinx UltraScale
XCVU080, XCVU160
25 Gbps with 64B/66B

Data transmission protocol

- Data transmission in TRG: Xilinx and Altera FPGA MGT, QSFP module, and MPO cable.
- The original plan was to use the open-source Aurora protocol, but large latency was introduced and exceeded the L1 limit (4.4 μs).
- Belle II CDCTRG developed an user-defined transmission protocols:
  - Smaller latency than Aurora's: **Latency reduction is critical for L1!**
  - User-friendly interface.
  - 8B/10B and 64B/66B encoding.
  - Support various Xilinx and Altera MGT.
  - Bit error rate < 10^{-18} /s with few weeks BERT.
  - Flow control and synchronization.

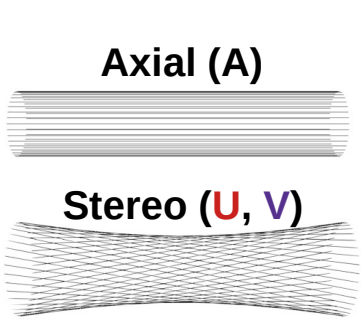
Latency comparison using UT3 (Virtex-6 GTX and GTH)

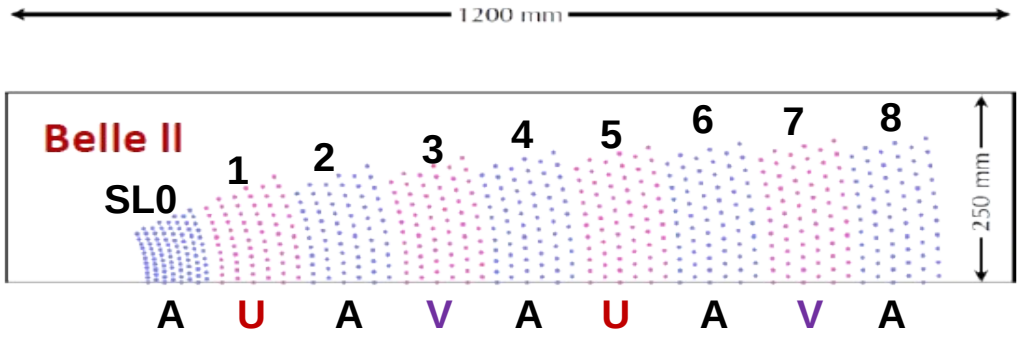
Protocol	Lane rate	user_clk	Link type	Latency (ns)
Aurora 8B/10B	5.08 Gbps	254 MHz	GTX-GTX	185∼190
Raw-level 8B/10B	5.08 Gbps	254 MHz	GTX-GTX	132∼136
	5.08 Gbps	254 MHz	GTH-GTX	132∼136
	5.08 Gbps	254 MHz	GTH-GTH	91∼95
	5.08 Gbps	254 MHz	GTX-GTH	91∼95
Aurora 64B/66B	10.16 Gbps	158.75 MHz	GTH-GTH	296∼302
Raw-level 64B/66B	11.176 Gbps	169.33 MHz	GTH-GTH	106∼112

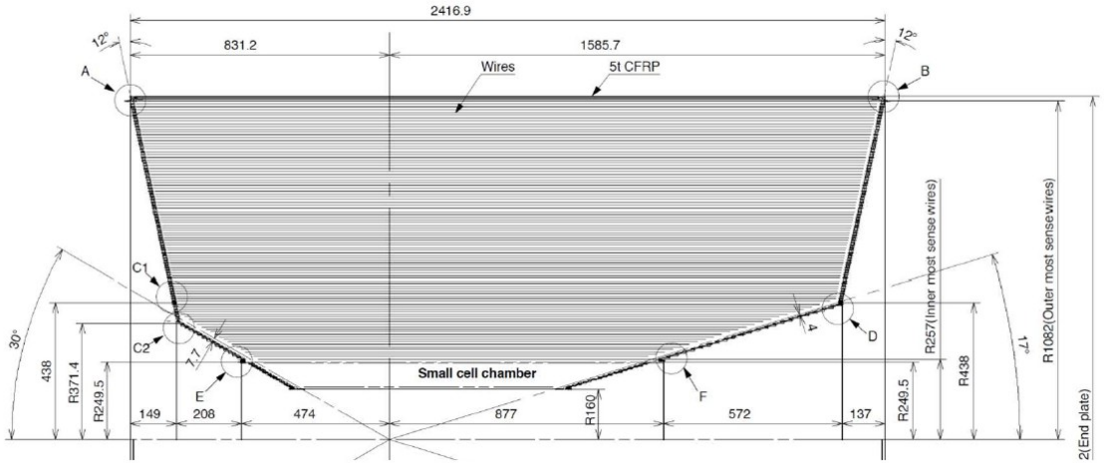
- For **UT4**:
  - Up to 25 Gbps using 64B/66B.
  - Much smaller latency than the ones in the left table (even by a factor of 2, < 100 ns).

Central Drift Chamber (CDC)

- About 14 thousand of sense wires and mixture of He and ethane as ionization gas.
- Gas atoms' ionization will accumulate charges on sense wires when charged particles go through.
- An alternative **AUAVAUAVA** wire configuration for 3D information:
  A: Axial super-layer (SL) parallel to z-axis
  U, V: Stereo SL with two small stereo angles.

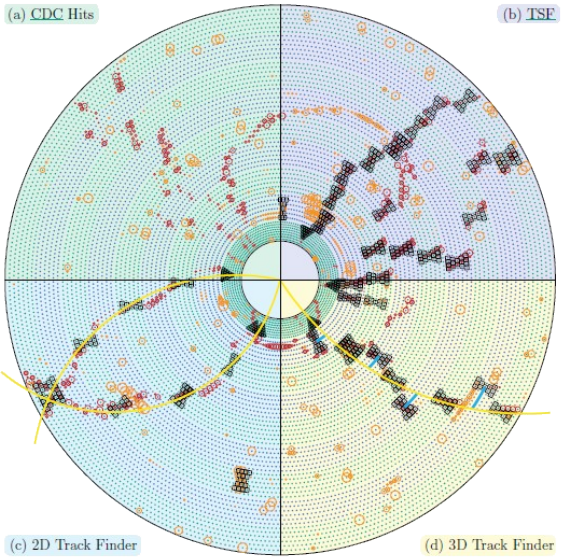






CDCTRG

- Track Segment Finder (TSF): Basement of all track trigger.
  - Collection of specific shape of wires within a SL.
  - Simplify the tracking algorithm design in L1.
- Tracker: 2D full track, 3D, Neural 3D (NN), and short tracker in Global Reconstruction Logic (GRL).
- Event Timing Finder (ETF): also based on tracking results.

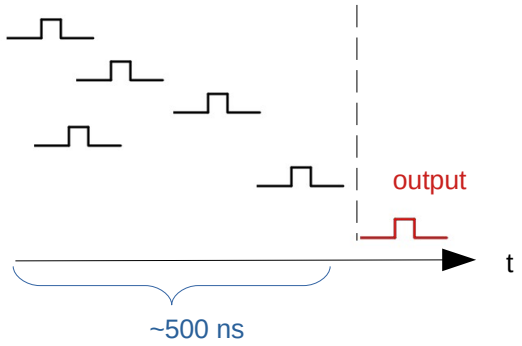


Fonrt-End
Xilinx Virtex-5

Merger
Altera Arria2

Universal Trigger board: UT3 and UT4

Drift time:
For the wire hits in CDC from the same track, their signals would appear within a ~500 ns window.

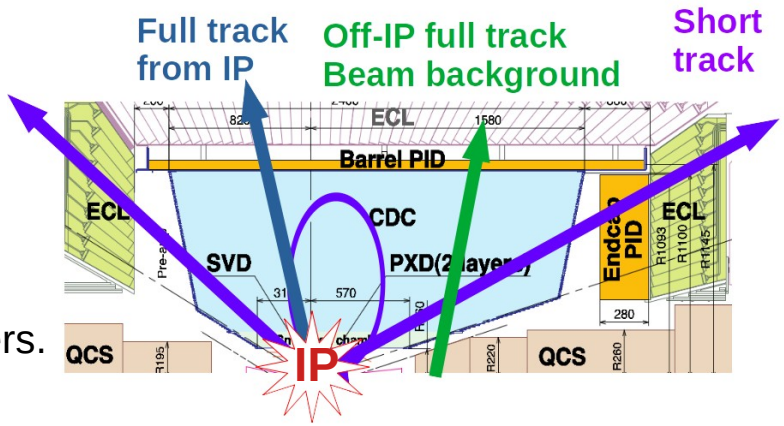


2D full tracker

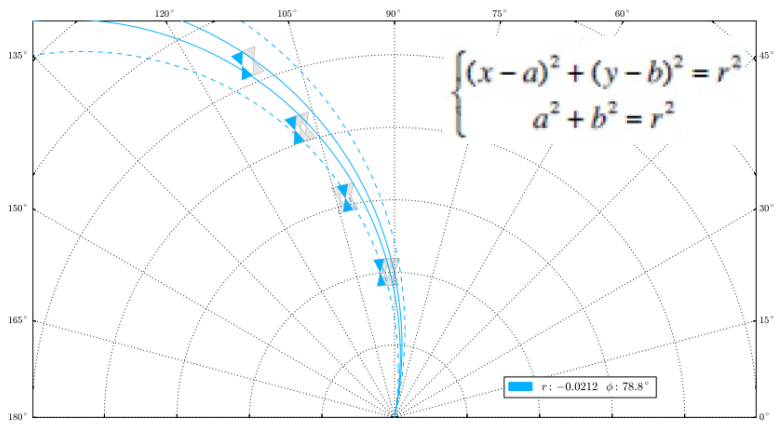
T.-A. Sheng. Master thesis
https://doi.org/10.6342/NTU201802022
Ping Ni. Master thesis

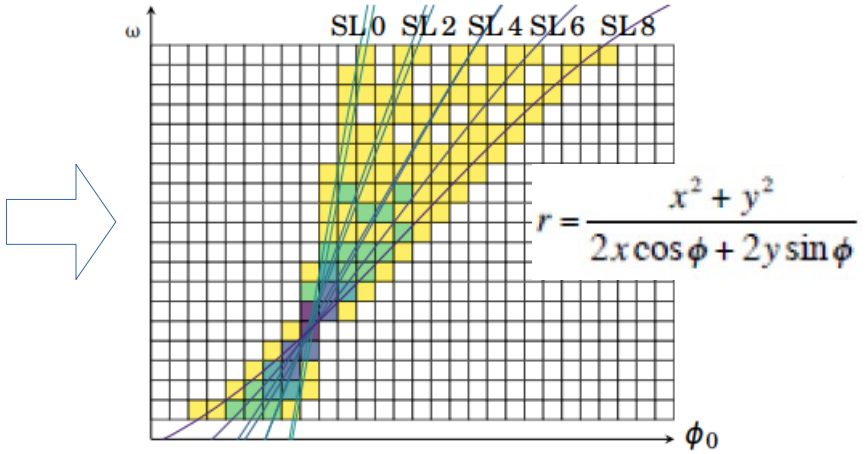
- Full track: The charged tracks which go through all of the layers of CDC and reach barrel region of ECL.

- 2D algorithm: Hough transformation.
  - Assuming a circle.
  - TS from 5 Axial SL are transferred into 5 lines in the conformal plane.
  - Find the peak, which corresponds to track parameters.



- Very high eff. Utilization:
  - 3-track: Hadronic events.
  - 2-track with back-to-back or opening angle: di-muon or tau events.



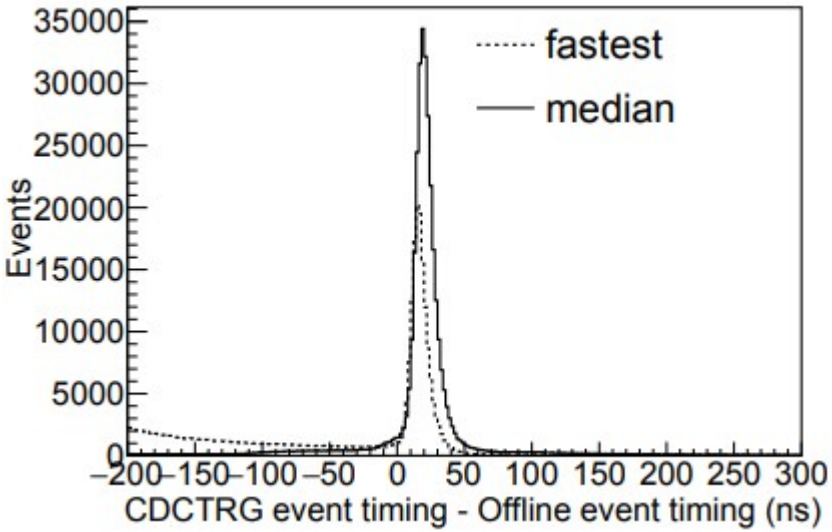


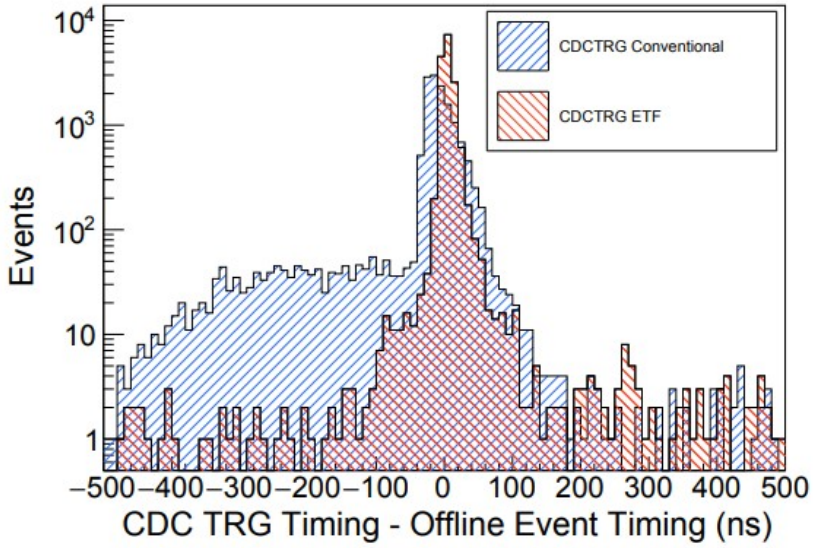
Event Timing Finder

E. Won, H. Moon, J.Korean Phys.Soc. 80 (2022) 2, 117-122
Yuki Sue et al 2022 J. Phys.: Conf. Ser. 2374 012103

- The original design is based on a histograming method by collecting the timing of TS.
  - However, too many fake TS due to crosstalk noise from CDC.

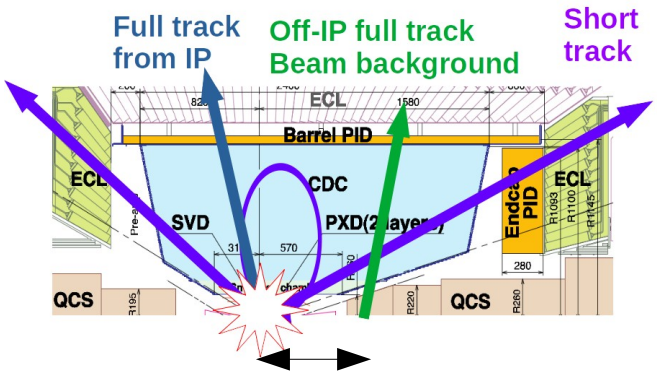
- New method: Use the 2D tracking result to pick up the TS associated with tracks, and find the fastest timing among wires.
  - Resolution: 20 ns → 10 ns.
    - Became usable for L1 timing.
  - Eff. for hadronic events: 87.2% → 94.2%.



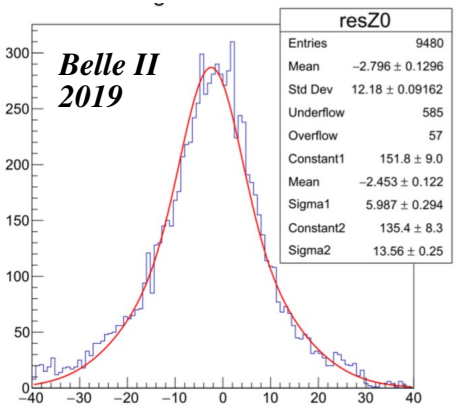


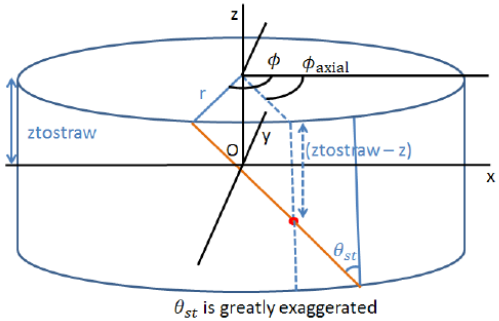
3D tracker

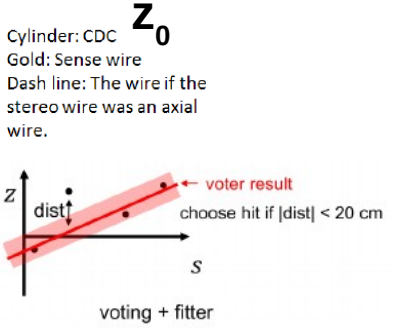
- Purpose: find the longitudinal displacement of a track (z_0) to separate the off-IP track, e.g. beam background.



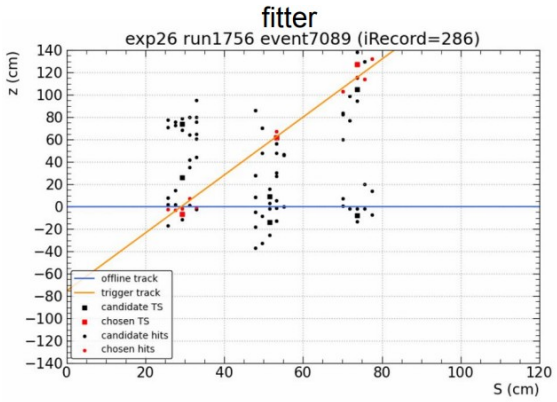
- Based on the 2D track, and perform fitting on the 4 stereo SL TS.
  - Presently, the resolution is not good enough for L1 utilization.

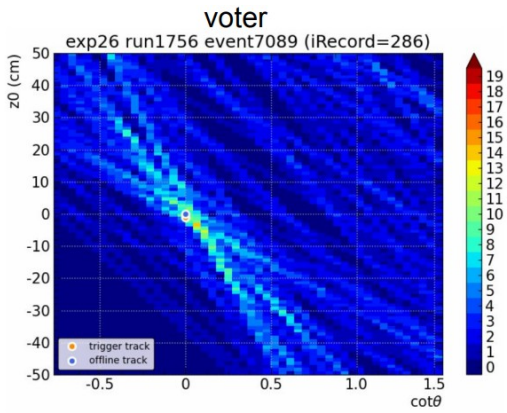






- New method under development with new electronics:
  - To improve the robustness against noise hits.



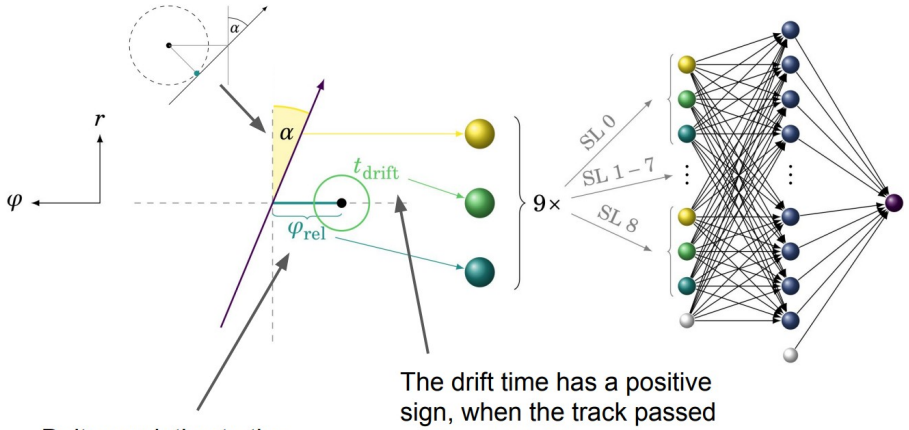


Neural z trigger

Karlsruher Institut für Technologie

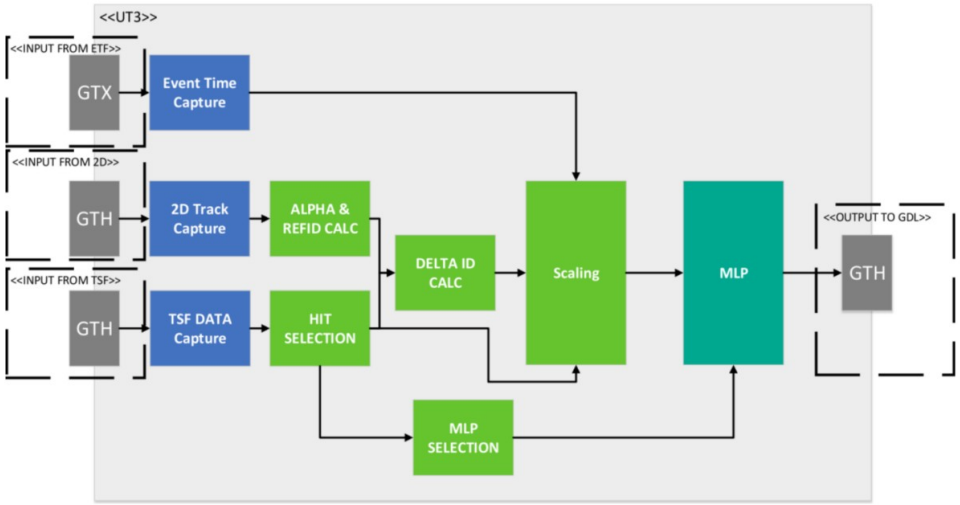
S. Neuhaus et al 2015 J. Phys.: Conf. Ser. 608 012052
Kai Lukas Unger et al 2023 J. Phys.: Conf. Ser. 2438 012056
F. Meggendorfer, DPG Conference 2021
Thesis: S. Skambraks, S. Pohl

- In addition to the conventional 3D tracker based on fitting method, Belle II has a Neural Network 3D tracker (NN) running in parallel in the system.
- Input the 2D tracker and stereo TS info
  - Crossing angle, drift time, φ relative to 2D Track .
  - Obtain z_0 and θ.



Delta φ relative to the 2DTrack. For Axial TS this is 0.

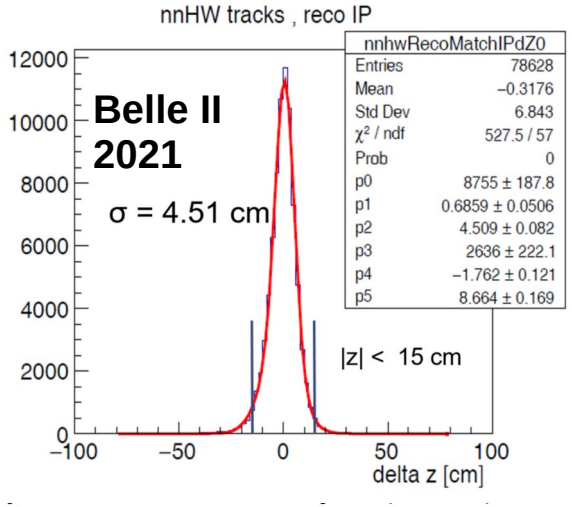
The drift time has a positive sign, when the track passed on the right side, and a negative sign if it passed on the left.



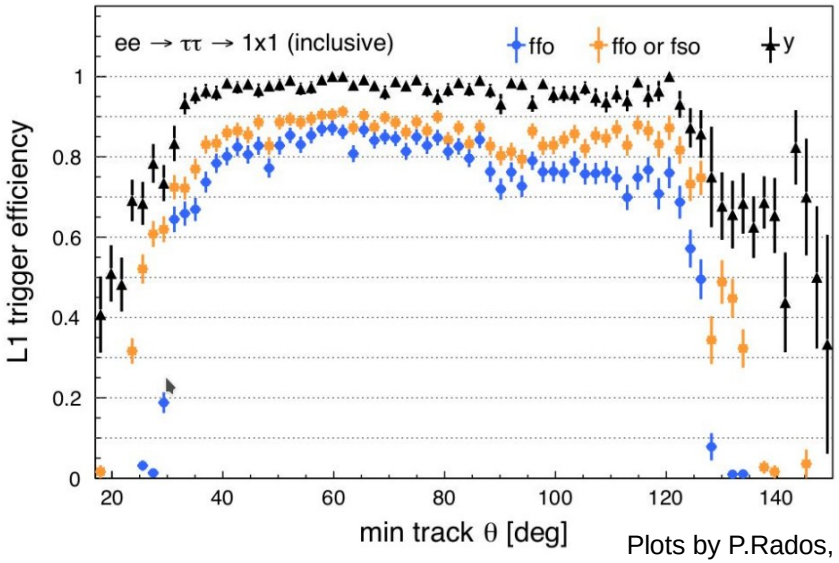
Neural z trigger (cont'd)

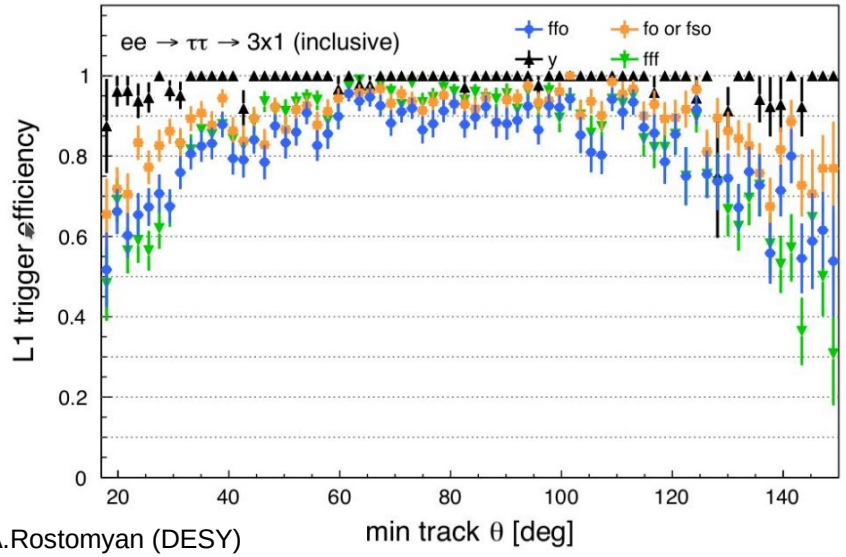
S. Neuhaus et al 2015 J. Phys.: Conf. Ser. 608 012052
Kai Lukas Unger et al 2023 J. Phys.: Conf. Ser. 2438 012056
F. Meggendorfer, DPG Conference 2021
Thesis: S. Skambraks, S. Pohl

- z_0 resolution is very good.
  - Will be more improved with updated network along with new data.
- The ambitious single-track-trigger with z_0 and pt requirement to reduce bias.
  - Thanks to the good performance of Neural trigger, its L1 trigger rate is acceptable.



ffo: full-to-full opening angle > 90°
fso: full-to-short opening angle > 90°
y: single-track from Neural



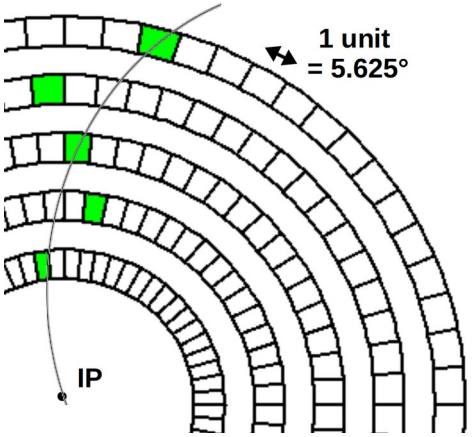


Plots by P.Rados, A.Rostomyan (DESY)

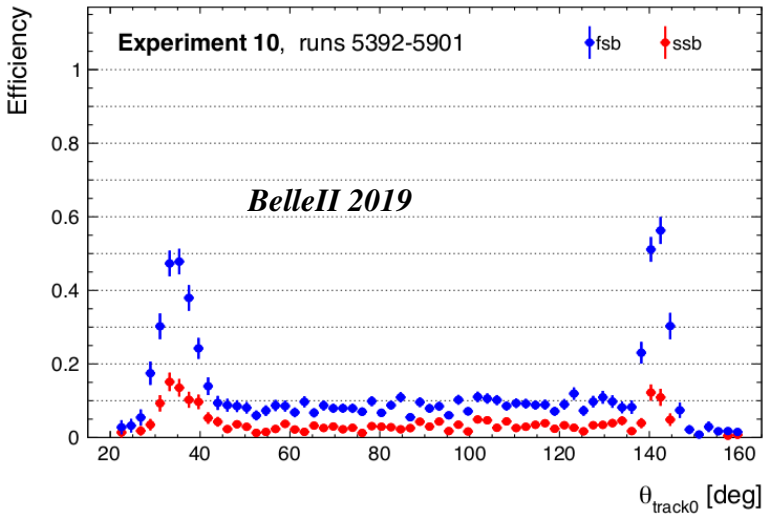
Short tracker in GRL

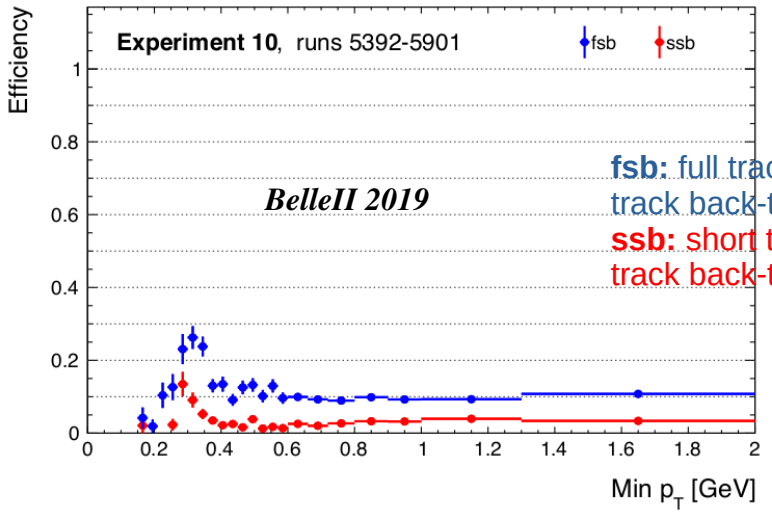
- The logic is implemented in part of the global trigger (GRL).
  - Use the TS of inner 5 SL (3 axial, 2 stereo).
  - Pattern recolonization over a 64 x 5 array. Simple design.
    - Consider the resource of FPGA device.

- Improve the angular acceptance of CDCTRG toward endcap.
- Also the curling-back tracks within the chamber: low-pt.



2 tracks ee→ττ events



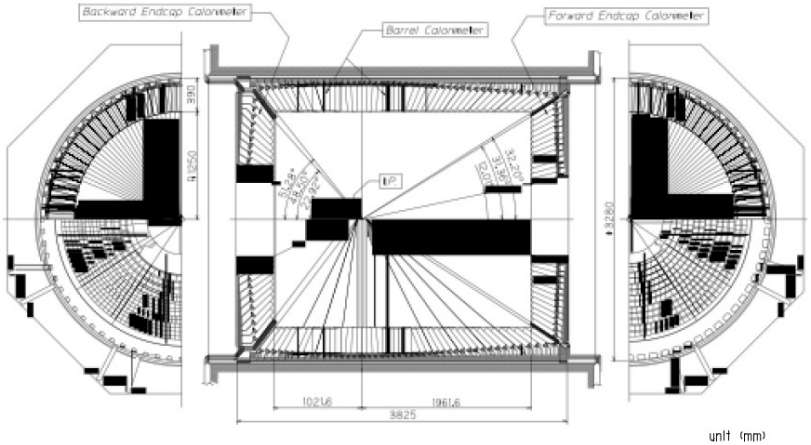


fsb: full track short track back-to-back
ssb: short track short track back-to-back

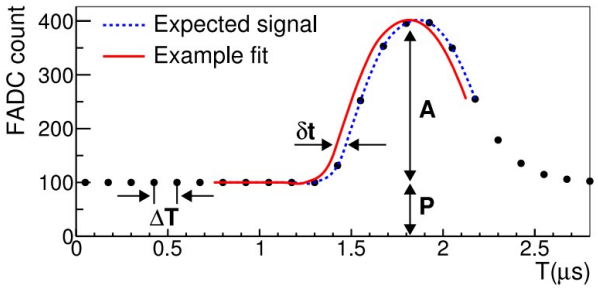
ECLTRG

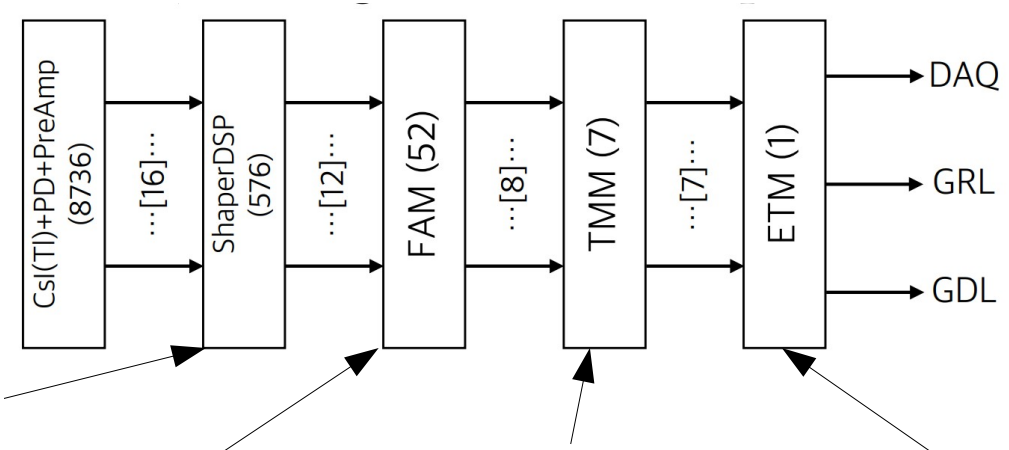
I. S. Lee et al., IEEE TNS, vol. 67, no. 9, pp. 2143-2147, Sept. 2020
S.-H. Kim et al 2017 J. Phys.: Conf. Ser. 928 012022

- Belle II ECL:
  - 8736 CsI(Tl) crystals



- ECLTRG data flow:





ShaperDSP: Fast-shaping signals from neighboring 4x4 crystals are merged as a Trigger Cell (RC).

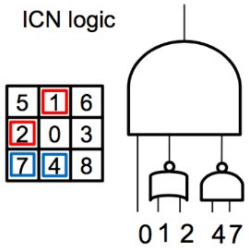
FAM: FADC analysis module. Xilinx Kintex-7 FPGA. Receive TC info and perform fitting.

TMM: Merger. Xilinx Kintex-7 FPGA.

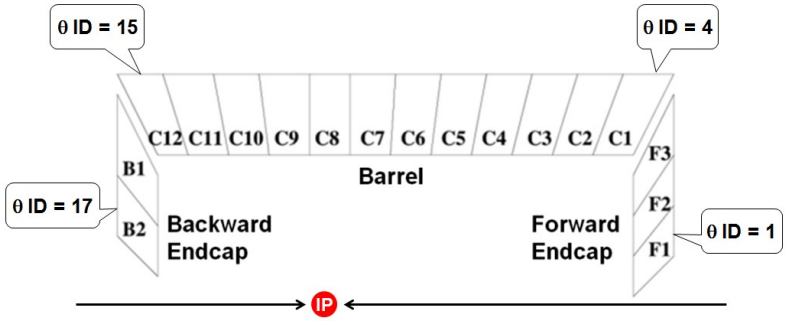
ETM: Energy&Timing Measurement using universal trigger board.

ECLTRG ETM

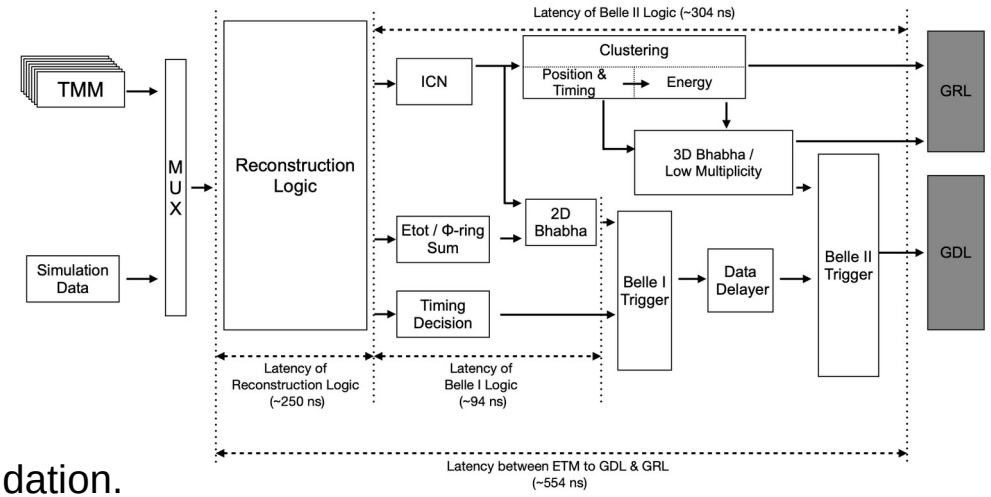
- S. Lee et al., IEEE TNS, vol. 67, no. 9, pp. 2143-2147, Sept. 2020
  S.-H. Kim et al 2017 J. Phys.: Conf. Ser. 928 012022



- Triggers from ETM:
  - Energy sum > 1 GeV.
  - Clustering.
  - Low-multiplicity trigger and Bhabha: Clusters region, opening angle, and enerygy requirements.
  - Event timing: Major timing source in L1 TRG.

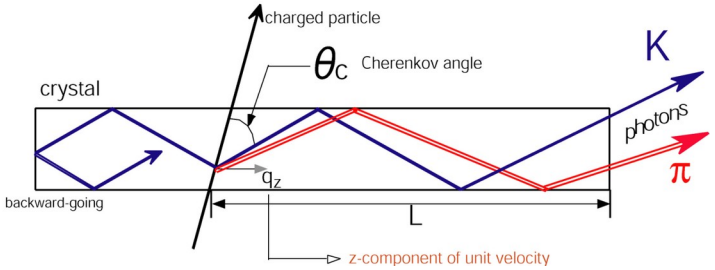


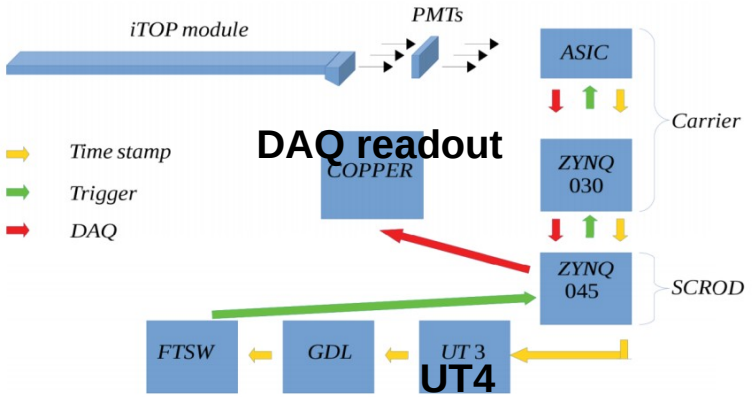
- Performance:
  - The energy sum trigger has the best performance for most of physics. e.g. hadronic (~100%), tau, etc.
  - Since track trigger from CDC cannot handle endcap, low-multiplicity highly relies on ECL trigger.
  - But the trigger rate is easy to go too high as ECL is easy to be affected by background.
  - CDC-ECL matching in GRL is under validation.

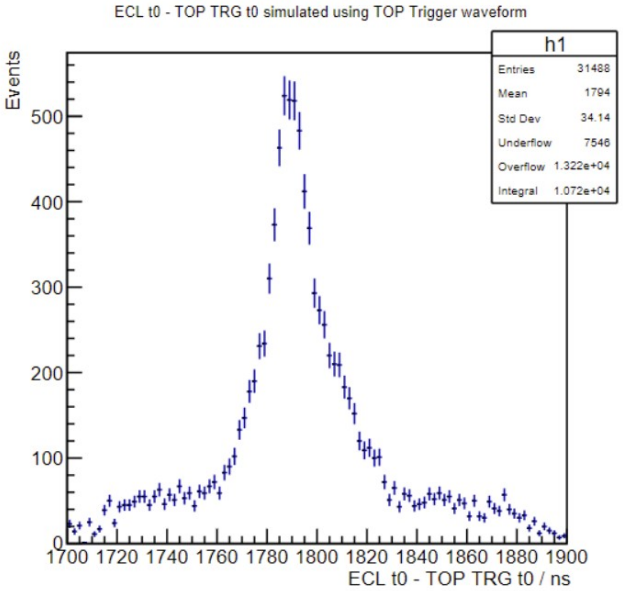


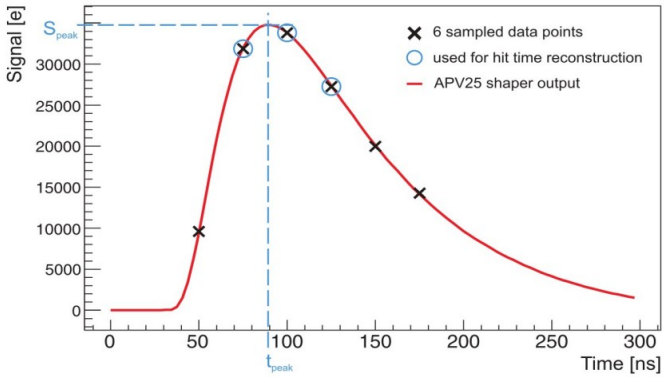
TOPTRG

- TOP: Utilizing Internally Reflected Cherenkov Light within the quartz bar (iTOP module) for PID in barrel.
- Also for L1 event timing measurement based on real-time likelihood analysis on the waveform.
- Timing resolution of hadronic event:
  - Eff. is only ~34% due to overwhelming number of beam-related background photons.
  - Utilization of CDC-TOP matching is under study.





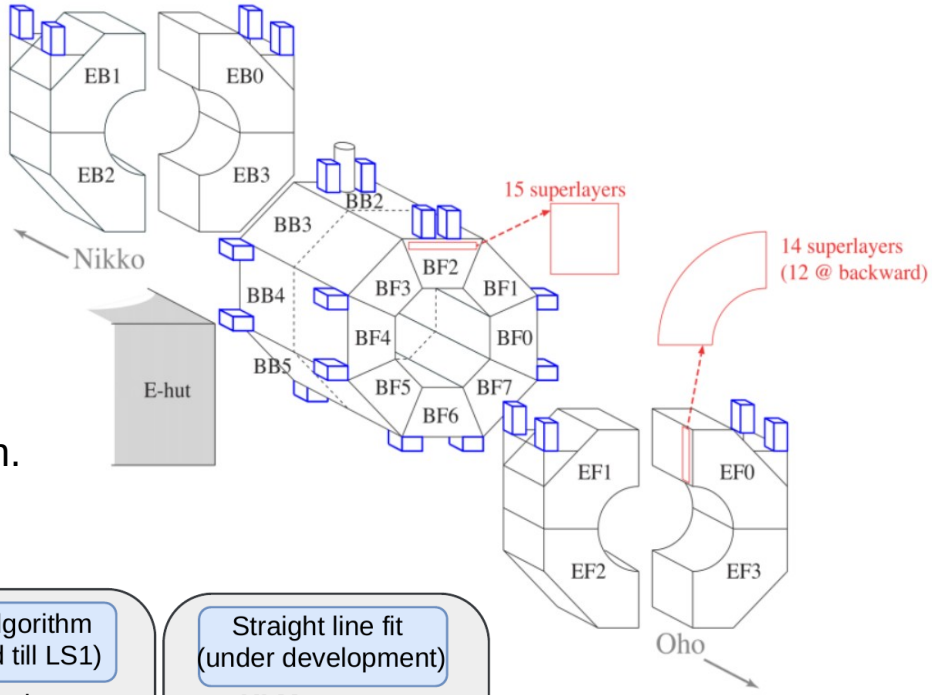




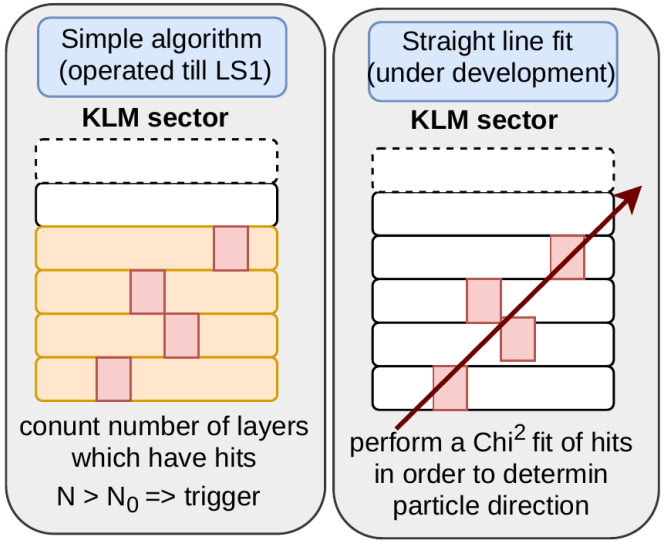
KLMTRG

- KLM: Scintillator strips and Resistive Plate Counters (RPC) in different regions.

- Present logic design:
  - Coincidence of hits in multiple layers.
  - back-to-back.
  - High eff., and the overall trigger rate is not very high. Cosmic occupies a certain fraction.
  - CDC-KLM matching in GRL.

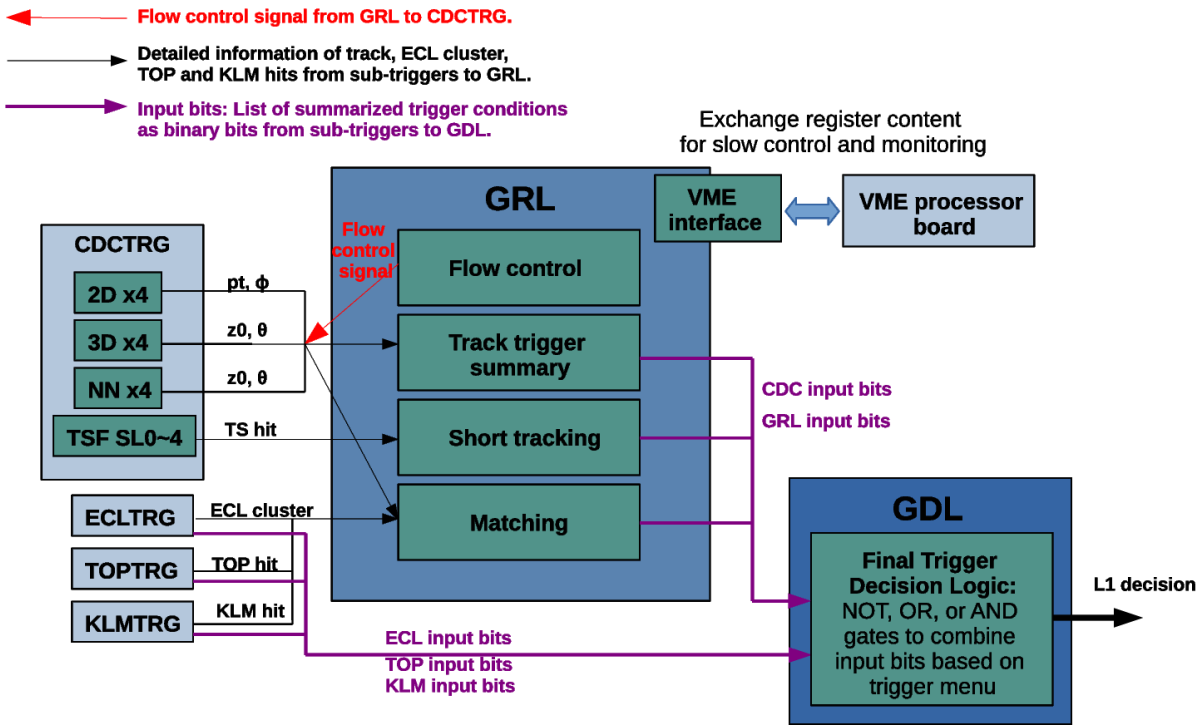


- New logic under development:
  - Straight line chi^2 fitter.
  - Expect to be able to separate cosmic event.



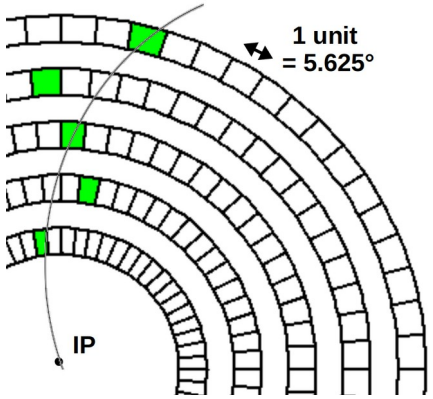
Global Reconstruction Logic

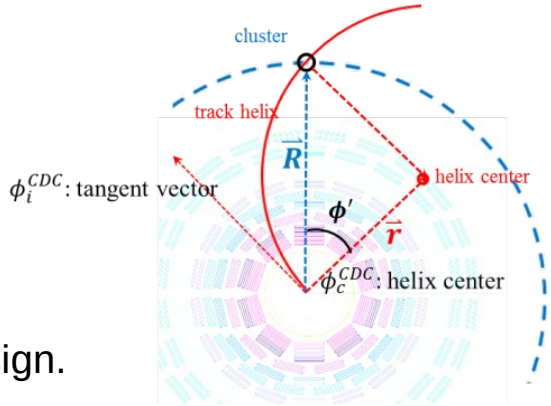
- Global Reconstruction Logic (GRL):
  - Master of the entire CDCTRG system: GRL receives the track output from each separated pieces, and provides summary:
    - Short tracking, track counting, back-to-back, opening angles, etc.
  - GRL also receives the output from other sub-triggers in form of physics objects: ECL cluster, KLM hit, TOP hit, and it performs matching between CDC track and those other sub-triggers.



Global Reconstruction Logic: trigger list

- GRL has strong flexibility of trigger combinations:
  - Track counting from 2D and 3D: single-track, 2-track, 3-track.
  - Short tracking.
  - back-to-back, opening angle > 90°.
    Between full to full, full to short, and short to short.
  - Matching between 2D full tracks and others: Using track parameter to calculate Δϕ with LUT.
    - CDC-ECL
    - CDC-TOP
    - CDC-KLM
    - ECL-KLM
  - Track-cluster back-to-back.
  - Tau trigger with machine learning.

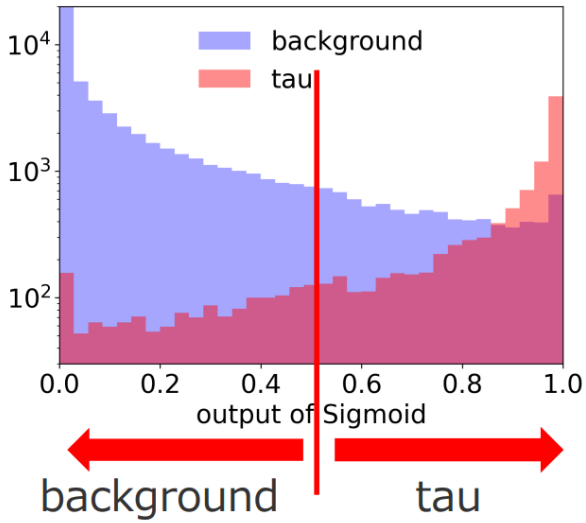




- Many of them were not in the original plan of Belle II TRG design.

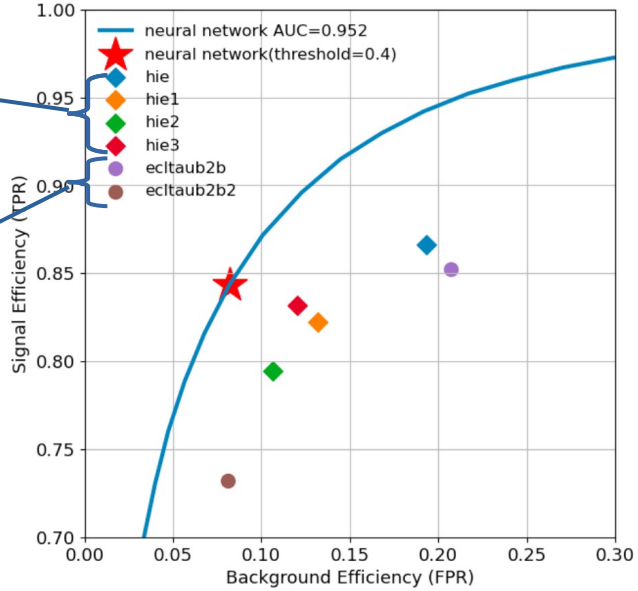
Global Reconstruction Logic: ML tau trigger

- GRL receives the cluster information from ECLTRG.
  - Input the position and energy information of clusters to a Neural Network, and determine if it is a tau event or not.
  - A kind of topological application.
  - Based on hls4ml.
  - Validated and will be implemented in 2024 runs.



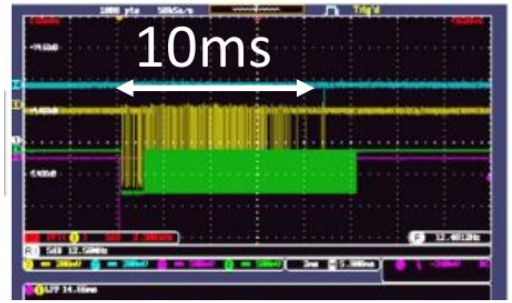
hie: ECL energy sum

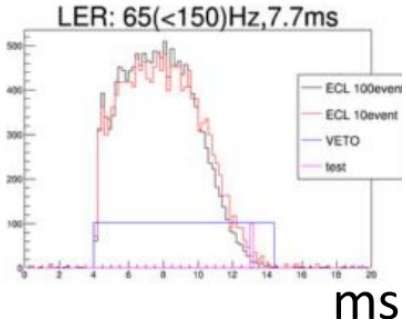
ecltaub2b: ECL cluster based logic

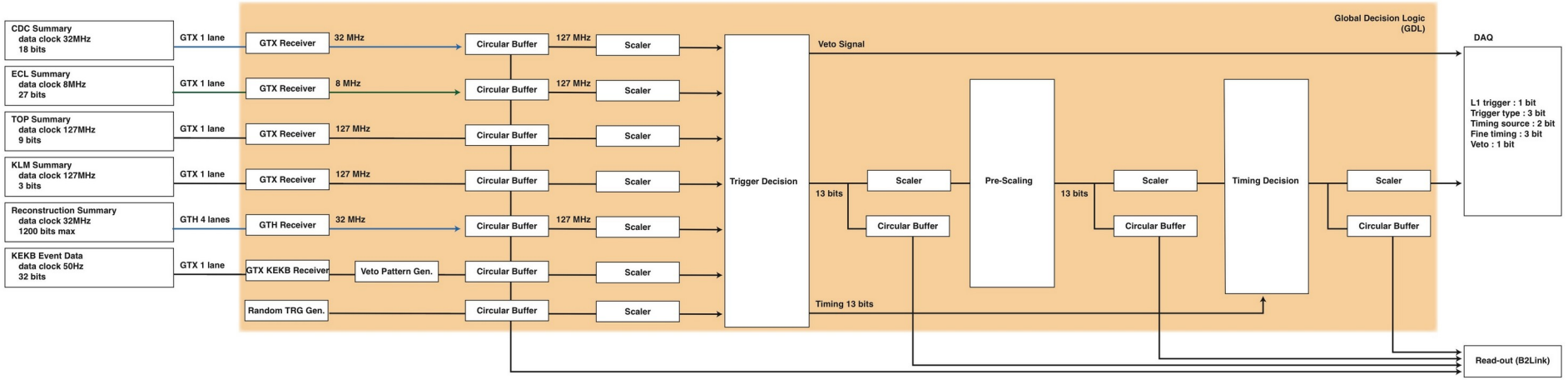


Global Decision Logic

- Global Decision Logic (GDL):
  - GDL receives the summarized sub-trigger info in forms of "trigger bit".
  - Latency adjustment on the input trigger bits.
  - Trigger decision: Or or AND gate to combine input bits into final L1 trigger menu, and the final decision will be sent to DAQ system.
  - Pre-scale on trigger bits.
  - Injection veto from accelerator.
  - Event timing decision:
    from TOP, ECL, and CDC.







Trigger menu for Belle II physics

- **Hadronic event: BB-bar and qq-bar (q=u,d,s,c)**
  - High multiplicity. ~100% eff.
  - While keeping high eff., need to reduce systematics.
    - 3-track
    - 2-track + opening angle > 90°
    - ECL energy sum > 1 GeV
    - 4 ECL clusters

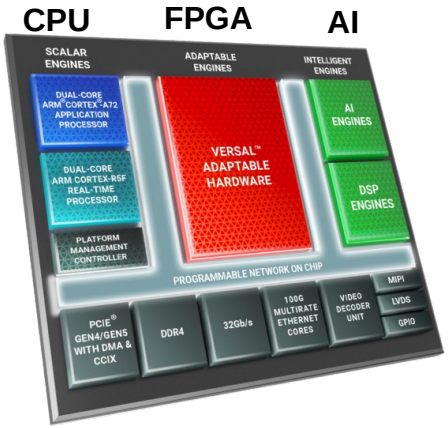
- **τ event**
  - 1 or 3 charged tracks.
    - 2-track (full or short) + opening angle > 90°
    - ECL energy sum > 1 GeV
    - 3 ECL clusters, 1 of E > 300 MeV
    - CDC-KLM matching

- **Dark sector, Low-multiplicity**
  - 1 or 3 charged tracks.
    - 2-track + opening angle > 30°: Z'
    - CDC-KLM matching: Z'
    - 1 ECL cluster, energy sum > 1 GeV: single photon, axion, ALP
    - 1 ECL cluster, energy sum > 0.5 GeV, barrel: high mass dark photon
    - ECL cluster back to back, energy sum < 2GeV: two-photon fusion, ALP
    - 1 ECL cluster, energy sum > 2 GeV, endcap: π^0 form factor, ISR

Future trigger board UT5 with Xilinx Versal

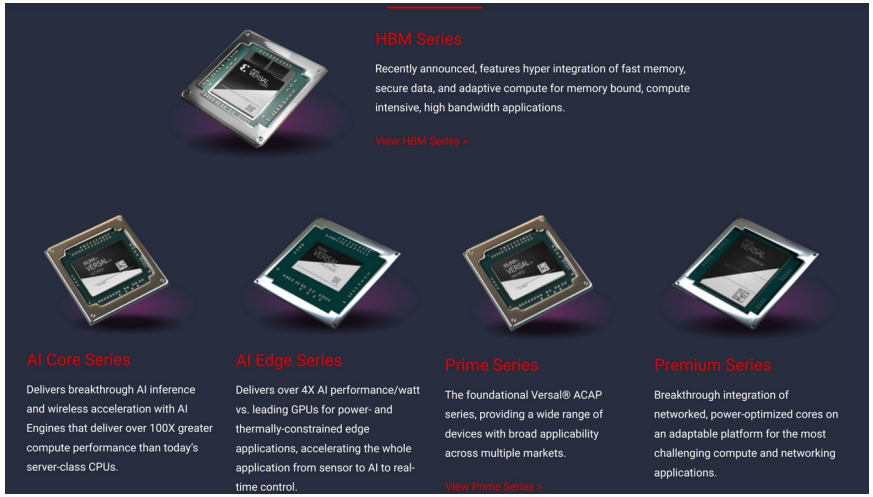
- Xilinx Versal ACAP: Candidate of FPGA selection for the next generation of trigger device.
  - FPGA together with other external tools integrated into a SoC.

source: Xilinx website

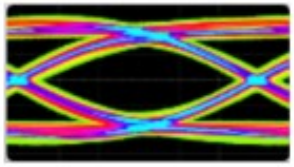


- For Versal, what are we interested in?
  - Stronger FPGA.
  - AI engine for machine learning inference.
  - Higher transmission bandwidth with PAM4.
    - Suitable for the L1 TRG's purpose.

- Now, Belle II, Energy Frontier, and E-sys group in KEK IPNS are collaborating for new Trigger board's R&D based on Versal devices.

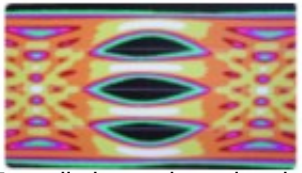


NRZ
(Non-Return-to-Zero)



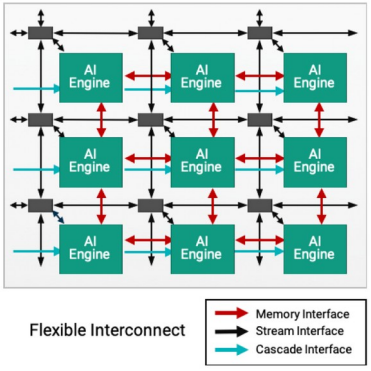
Limit: ~25 Gbps

PAM4
(Pulse Amplitude Modulation)

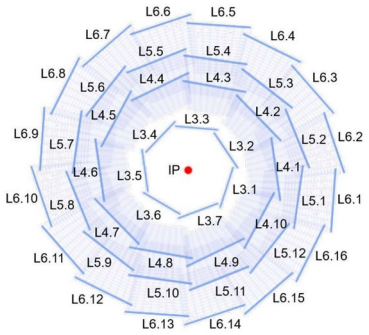


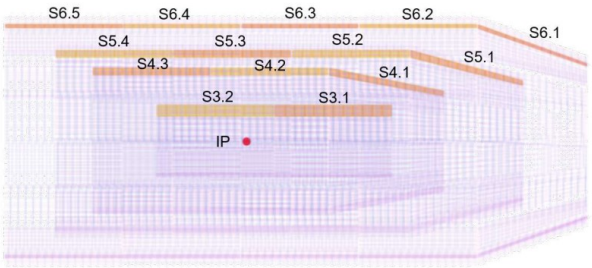
Four distinct voltage levels.
Two bits per clock cycle.

AI engine

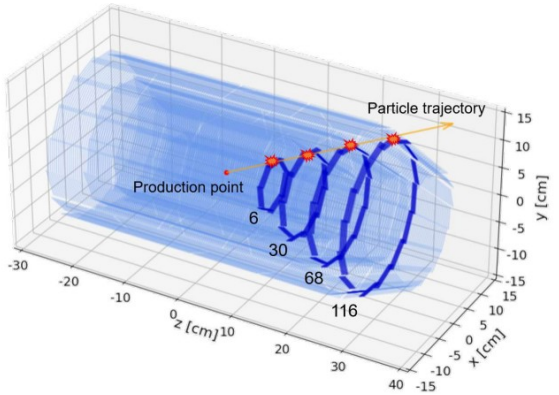


SVDTRG





T. Shimasaki, "Msater thesis, The University of Tokyo, 2023

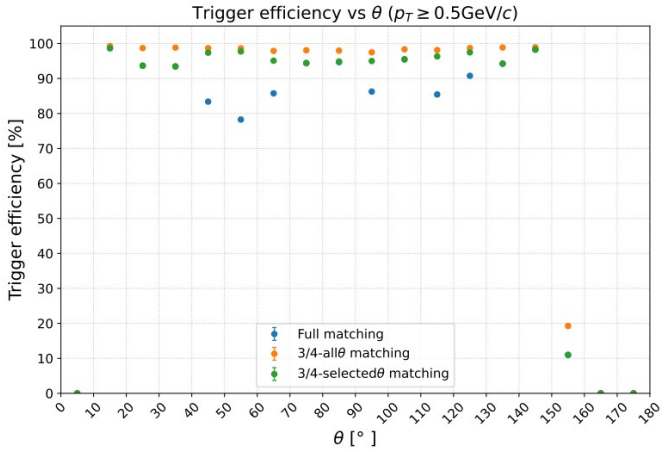


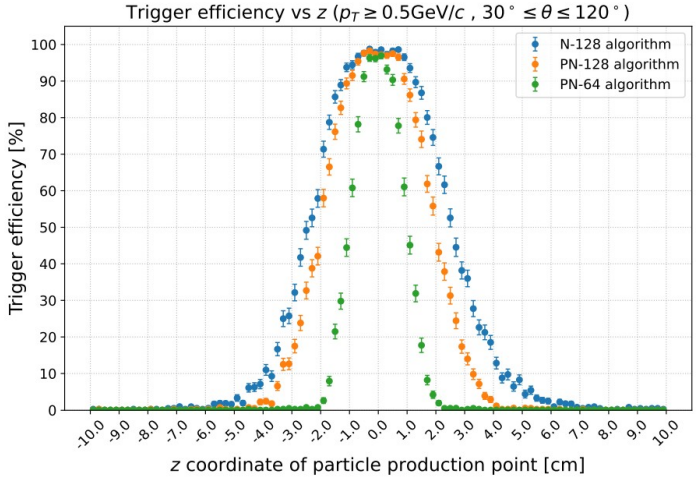
- A brand new idea to include the inner Silicon Vertex Detector (SVD) in the L1 TRG system.
  - Enhance the power of off-IP track rejection.
- Firmware design:
  - Obtain the hit pattern among all cells.
  - Match with pre-defined patterns stored in table.

Encode

Online hits $00110110 \cdots 011 \cdots 010 \cdots 110 \cdots 011$

A pattern of the table $00000010 \cdots 010 \cdots 010 \cdots 010 \cdots 000$



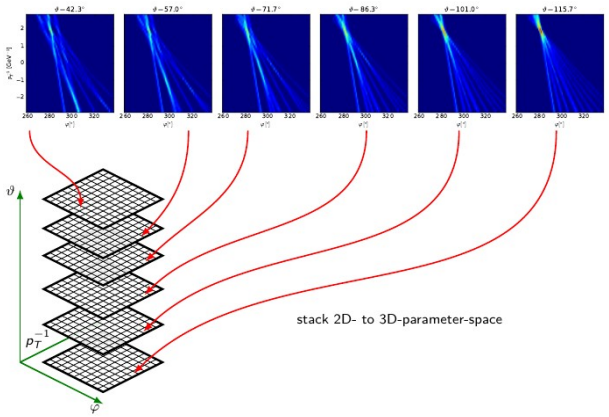


More new ideas are ongoing

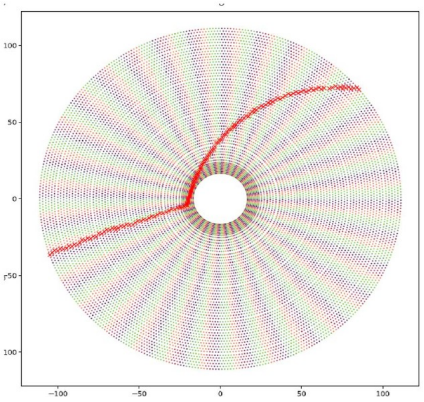
Karlsruher Institut für Technologie

S. Skambraks. Thesis

2D → 3D Hough tracking:

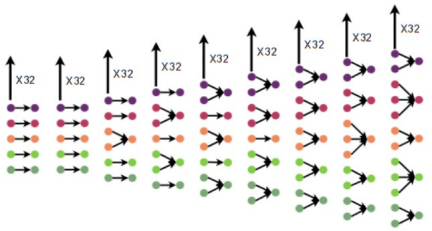


Displaced tracking with CNN:



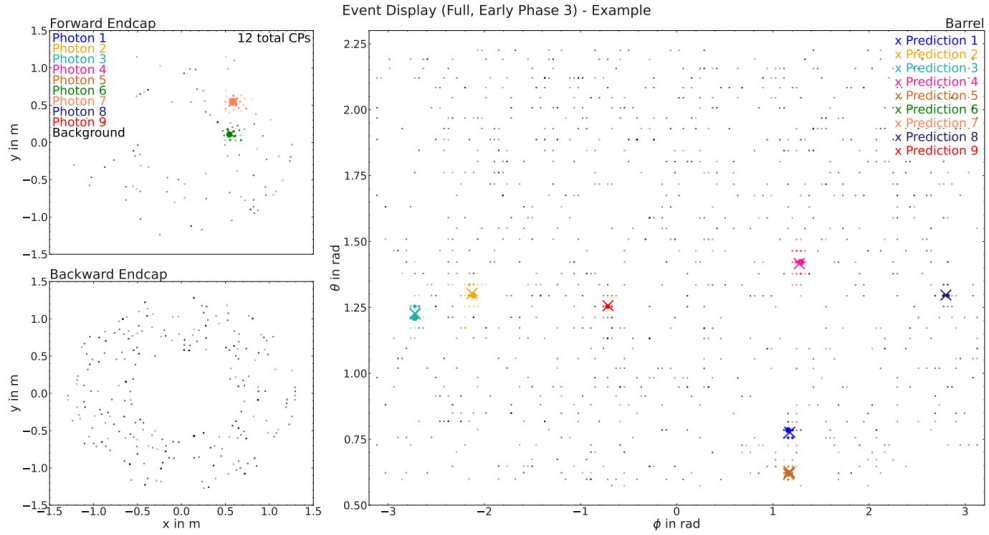
Aglining methode ploted on the CDC cross-section

SL	0	1	2	3	4	5	6	7	8
Sense wires	160	160	192	224	256	288	320	352	384
/ 32	5	5	6	7	8	9	10	11	12

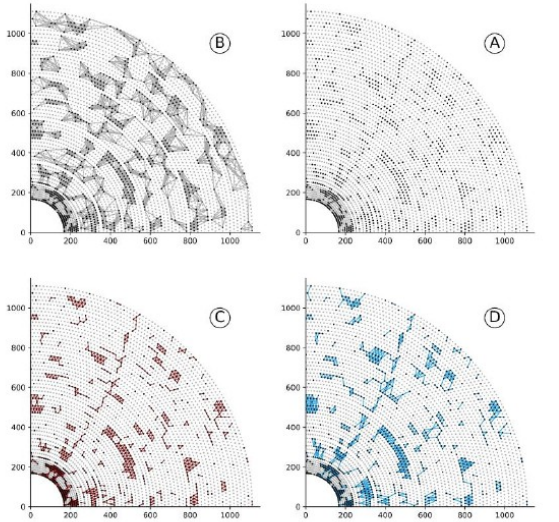


Proposed aglining methode with a agning width of 5 within each segment

ECL clustering with GNN:



Tracking with GNN:



Dataset: displaced_processed_simulated_2_tracks_0_nominal-phase3

Summary

- Belle II TRG system performs real-time event selection based on the 4 detectors' input and FPGA chips.
  - CDC, ECL, TOP, KLM, and global trigger systems.
- TRG logics includes tracking, calorimeter, muon, event timing, and matching between sub-triggers.
- For the future upgrade with increasing luminosity, new algorithms require stronger robustness again noise and background to reduce the overall L1 trigger rate, and the R&D of new FPGA device is ongoing.