

MAPS-based Upstream Tracker for LHCb Upgrade II

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Introduction

LHCb detector (Fig. 1) is dedicated to the flavour physics studies, serving as a forward general-purpose detector:

- Forward **single-arm spectrometer** with a unique coverage in pseudo-rapidity ($2 < \eta < 5$)
- Observing 40% of the **heavy quark** production cross-section in 4% of the solid angle
- Precision measurements in the **beauty and charm** sectors
- Also study of QCD, EW, heavy ion collisions, etc.

Upstream Tracker (UT) is located upstream of the LHCb bending magnet.

LHCb operates at $\mathcal{L}_{\max} = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ since 2022 with an upgraded detector. It will take data at $1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ during Runs 5 & 6, about $\times 7.5$ times higher than Runs 3 & 4 (Fig. 2). The current UT cannot cope with the **data rate** and the **high occupancy** (up to $\sim 10\%$).

The upgrade II UT (U2UT) detector will use **CMOS Monolithic Active Pixel Sensors (MAPS) technology**. We present the proposed design, performance studies, and R&D plan.

Luminosity Simulation

Performance studies are based on simulation samples generated in Upgrade II conditions using the available Run 3 UT material & design in Geant4 and Run 5 luminosity.

The two relevant occupancy related quantities for the future UT design are the **mean and maximum hit density per bunch crossing**, respectively.

Figure 3 shows the average hit densities per bunch crossings in p-p and Pb-Pb collisions.

- In p-p running conditions, the average density is **5.9 hits/cm²/BX** in colliding bunch crossings, or 4.0 hits/cm²/BX in all bunch crossings, while it is **2.9 hits/cm²/BX** for colliding Pb-Pb bunch crossings

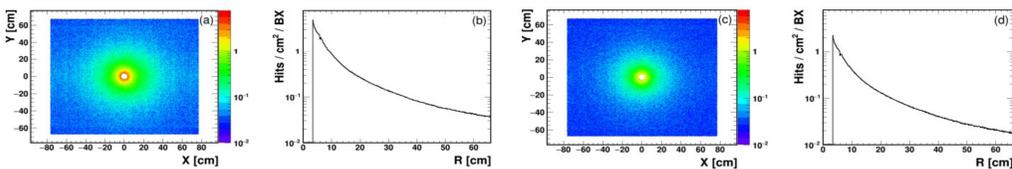


Fig. 3: The mean UT hit density per BX at the first plane per beam-beam colliding bunch in (a and b) the p-p programme, and (c and d) the Pb-Pb programme

Detector Design and Layout

A potential detector layout is illustrated in Fig.4. A plane consists of 12 staves, which in turn, is composed of multi-MAPS modules per staff.

- **Fourteen chips in a 7×2 array** are interconnected to a flex circuit to form a module.
- The common HL-LHC radiation tolerant ASIC for data, timing, trigger and control, known as the IpGBT, will be utilized for data acquisition.
- **A total of 36 modules** are mounted alternately on both sides of a supporting bare staff, **in total 12 staves per plane**.

A four-plane detector based on HVCMOS is proposed. Layout using other MAPS technology like LVCMOS is similar.

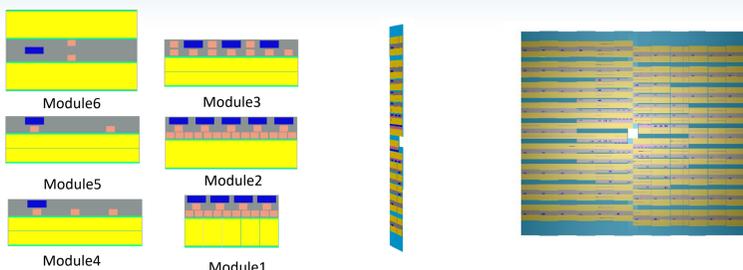


Fig. 4: Geometry construction using DD4hep

CMOS Sensor Options

The ongoing R&D studies indicate that monolithic active pixel sensors can be considered as very strong candidates for UT.

To achieve substantial depletion in the sensing volume and improve the speed and radiation tolerance of the detector, DMAPS implementations follow two different approaches, namely large fill-factor or high-voltage (**HVCMOS**) and low fill-factor or low-voltage (**LVCMOS**) with small electrode.

More details in Zhiyu's poster "Test of CMOS chip using 55nm process".

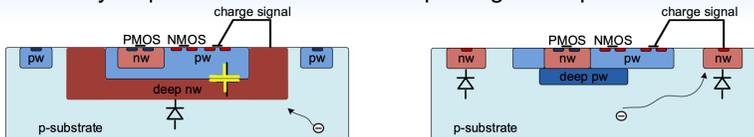


Fig. 5: The schematic of HV-CMOS (left) and LV-CMOS (right)

Reference and links:

[1] "Framework TDR for the LHCb Upgrade II Opportunities in flavour physics, and beyond, in the HL-LHC era", CERN, Geneva, LHCb Collaboration, CERN (Meyrin)

Software Development

Detector description has been developed both in DetDesc and DD4hep framework. "Fake digitization" study was based on MCTruth level. The **material budget** scan was performed in two frameworks with consistent results.

Figure 6 shows the radiation length of the first layer of U2UT plane in x/y and η/ϕ view. The last plot shows the projection map on the η axis.

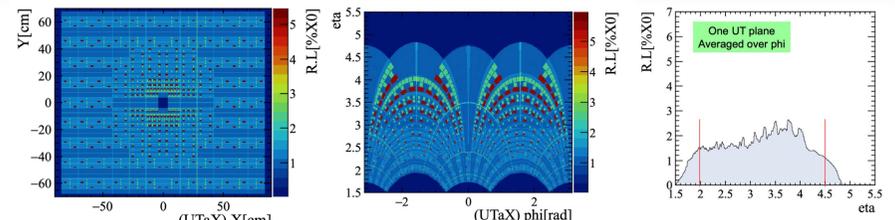


Fig. 6: Radiation length in DD4hep

Full Simulation Framework

The LHCb simulation framework consists of several software packages and tools that work together to simulate the entire data flow process, from the initial generation of events to the final reconstruction and analysis of the simulated data.

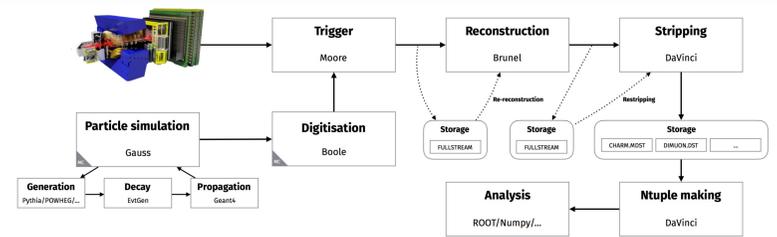


Fig. 7: The LHCb data flow and the associated applications

Related studies are accomplished at Boole level:

- **The hottest pixel occupancy** (0.256%) was estimated based on 1.2K miniBias MC events, consistent with estimation in FTDR.
- **Particle response efficiency** was treated as a function of particle momentum per layer compared with the current UT, both with efficiencies around 95%.

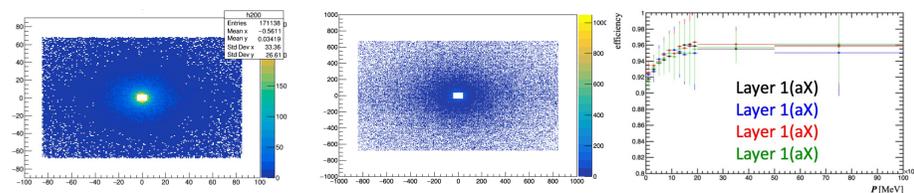


Fig. 8: 100 MCHits distribution in Gauss of first layer (left) and corresponding 100 MCDeposits in Boole (middle); particle response efficiency (right)

Comparison of UTDigits and MCHits:

- By decoding from MCDeposits to UTDigit, we get the **ChannelID** and **ADC value**. Decoded hits are consistent with MC inputs.
- Position of each ChannelID of trajectory is obtained.
- The decoded UTDigits are used for subsequent **track reconstruction**.

The track reconstruction framework added in Moore is ongoing.

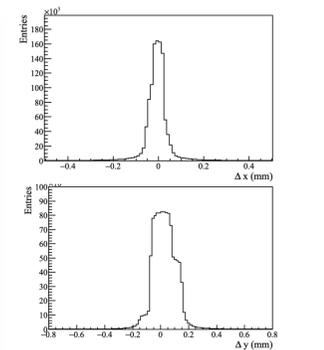
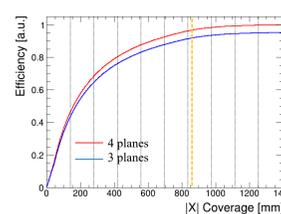
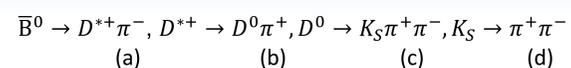


Fig. 9: Difference of UTDigits and MCHits in x(Up) and y direction (Down)

Track Efficiency

In order to study alternative scenarios aiming to **enhance the detector performance** for U2UT, the performance of 3- or 4-layer detectors were evaluated. We found that the performance is significantly compromised with **3-plane solution**.

Tracking efficiency of pions was studied for U2UT coverage optimisation using $\bar{B}^0 \rightarrow D^{*+}\pi^-, D^{*+} \rightarrow D^0\pi^+, D^0 \rightarrow K_S\pi^+\pi^-, K_S \rightarrow \pi^+\pi^-$ process, as shown in Fig.10. The impact on the reconstruction efficiency was assessed by increasing the horizontal coverage. And more decays will be studied afterwards.



Single Track With 3 UT Hits, $ x < 836.2 \text{ mm}$				
Requirement	(a)	(b)	(c)	(d)
Total 4 planes	0.962	0.971	0.962	0.960
Total 3 planes	0.913	0.925	0.913	0.914

Fig. 10: Efficiency vs X Coverage and Number of Planes

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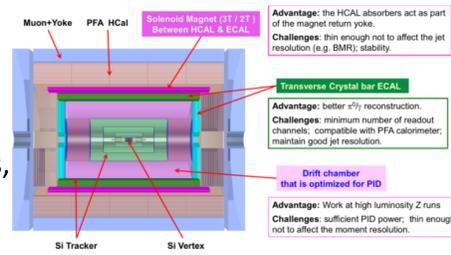
The 2023 International Workshop on the High Energy Circular Electron Positron Collider
October 23-27, 2023, Nanjing

1. CEPC Vertex Detector

The Circular Electron Positron Collider (CEPC)^[1] is a large international scientific facility proposed to explore the aforementioned physics program.

The Vertex Detector is an important sub-detector of CEPC, and its main purpose is to measure position and angles of charged particle tracks to sufficient precision.

The CEPC Vertex Detector has three layers, with detector units on both sides of each layer.



2. Digitization

The simulation path of the HEP experiments includes Event Generation, Detector Simulation, Signal Simulation, Reconstruction and Analysis.

Signal Simulation, which can also be called as Digitization, is the process of converting from analog to digital form.

The main purpose of this project is to develop a ML-based Digitization program for CEPC vertex detector.

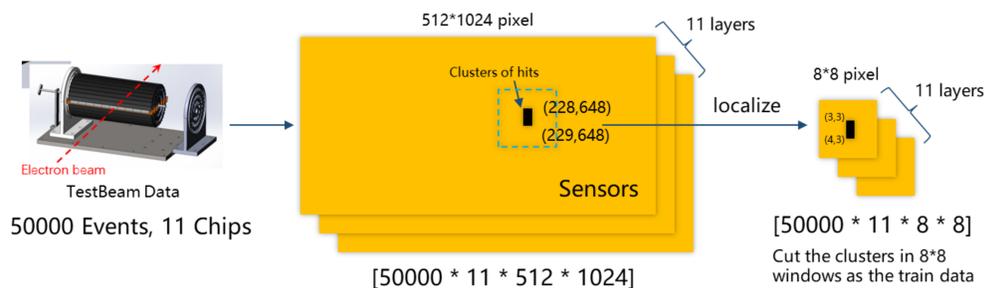


3. Methods

(1) Dataset

To meet the specific requirements of CEPC vertex detector, the MOST2 project was launched to develop a fully functional pixel sensor.

The sensor was characterized at the DESY test beam facility on Dec. 2022 and Apr. 2023. A beam telescope composed of 11 CMOS-based sensor chips (TaichuPix-3) was tested by 4Gev electron beam in these experiments.^[2]

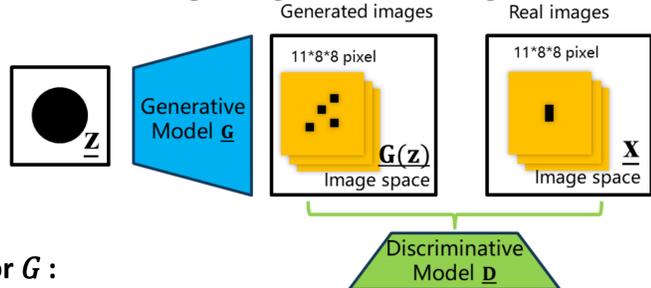


- The sensor size is 12.8mm*25.6mm, the pixel size of which is 25 μ m*25 μ m.
- Localization: Collect the clusters of hits using a 8*8 pixels window, which is used as the training dataset in the following NN model training.

(2) Model & Training

We developed a generative adversarial network (GAN) capable of digitization for CEPC vertex detector.

In a GAN, two neural networks contest with each other in the form of a zero-sum game, where one agent's gain is another agent's loss.^[3]



Generator G :

Input Z : randomly sampled from the latent space

Goal: try to make output resemble real samples (train data) as much as possible.

Discriminator D :

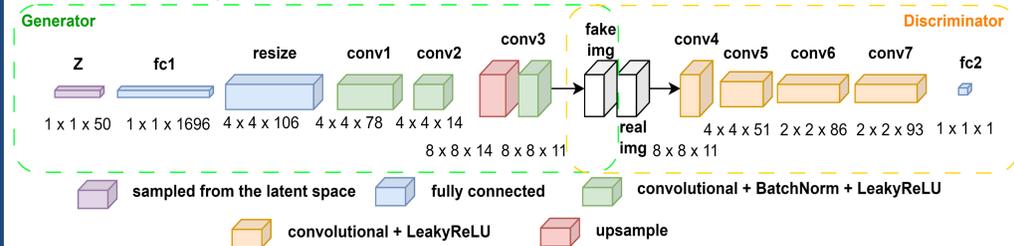
Input: real sample or the output of G

Output: the possibility that input is a real sample

- For every 10 times the discriminator is trained, the generator is trained once.
- Loss Function: Wasserstein Distance
- Metric: relative entropy of real and generated samples

(3) Optimization

- Generator\discriminator with different network models (fully connected neural network, CNN ...)
- Optimize the model with automatic hyperparameter optimization software framework **Optuna**.



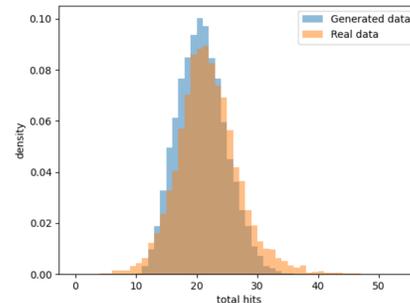
Optimized network architectures for the best performance is shown above.

The relative entropy of real and generated samples is considered as the metric of the performance, which of the different models is shown below.

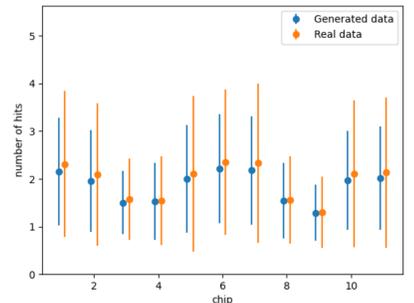
Model	NN	NN_Optuna	CNN	CNN_Optuna
Metric(relative entropy)	2.7548	2.1639	0.2393	0.0497

4. Evaluation

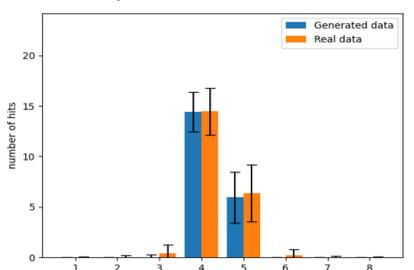
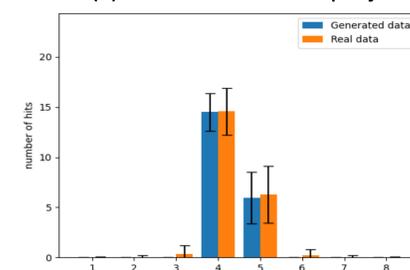
(a) Distribution of total clusters size per event



(b) Mean cluster size for each chip



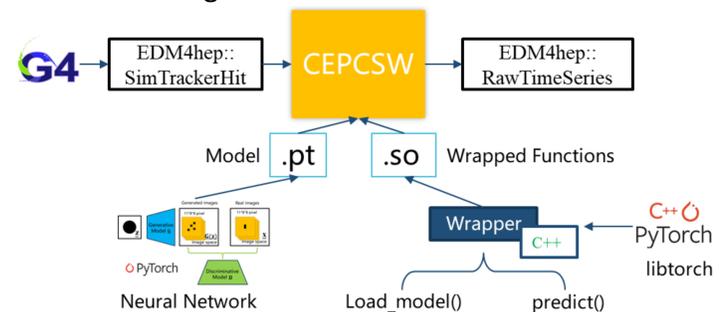
(c) Mean cluster size projected on X-direction/Y-direction



The distribution of digitization generated by the current model is generally as expected.

5. Application

The model has been integrated in CEPCSW.



The simulation path for CEPC vertex detector:

- GEANT4 generates simulate track hit.
- Digitization Algorithm use trained ML model to generates clusters of hits and stores them in EDM4hep::RawTimeSeries format.

We wrapped some features of libtorch in a .so file due to the conflict between ROOT and libtorch. The wrapped function can load the trained generator model and generates clusters.

6. Code

https://github.com/stch-zhangyzh/VDX_digitization

7. Reference

- CEPC Study Group. "CEPC Conceptual Design Report: Volume 2-Physics & Detector." arXiv preprint arXiv:1811.10545 (2018).
- Wang, Wei, et al. "Characterization of a CMOS Pixel Sensor prototype for the CEPC vertex detector." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 1056 (2023).
- Schlegl T, Seeböck P, Waldstein S M, et al. f-anogan: Fast unsupervised anomaly detection with generative adversarial networks[J]. Medical image analysis, 2019, 54: 30-44.



Design progress of CEPC electromagnetic calorimeter

Chang Shu , Quan Ji

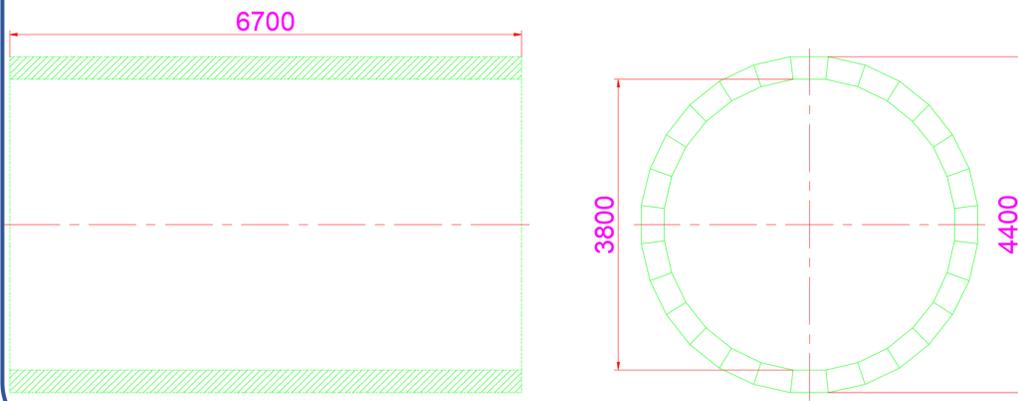
Institute of High Energy Physics, Chinese Academy of Sciences

Abstract

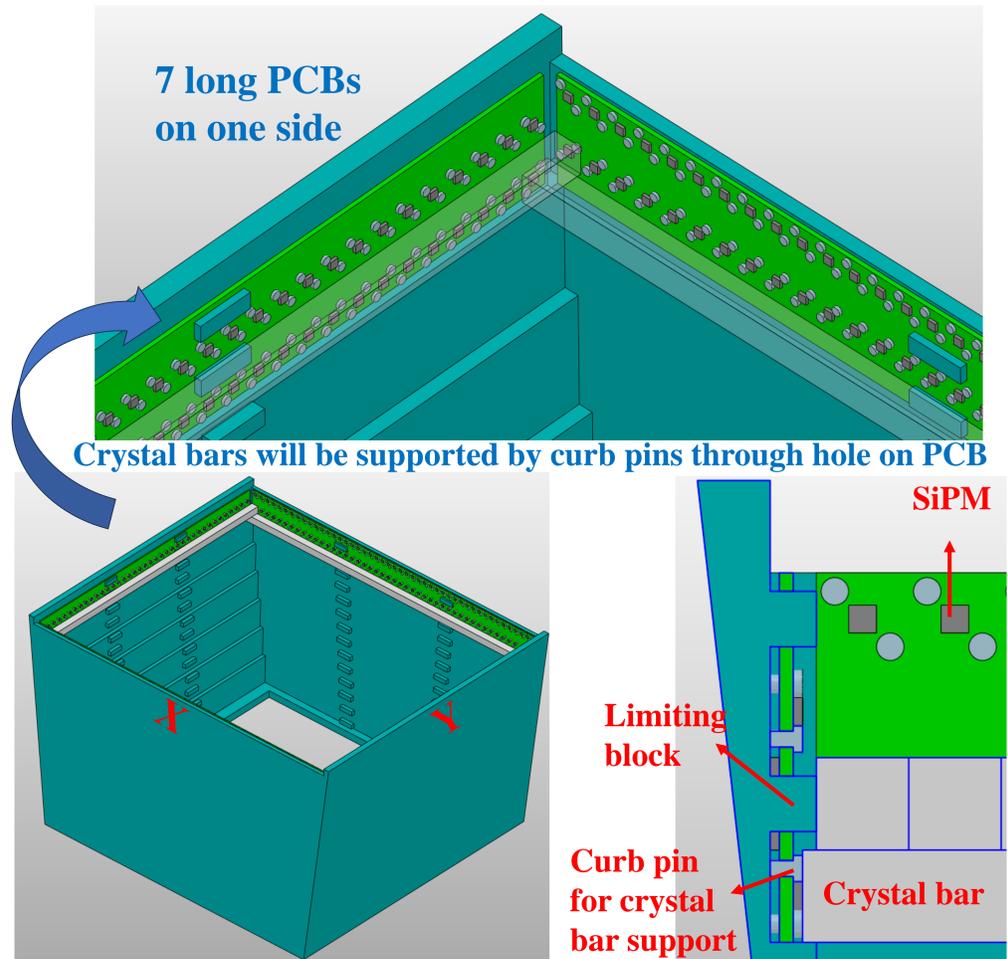
CEPC electromagnetic calorimeter is mainly composed of three parts, including an external honeycomb frame, an internal BGO crystal module and a BGO crystal readout unit. The main update of this design includes the optimization of the size of the honeycomb frame, the optimization of the size and arrangement of the internal crystal bars, and the discussion of different installation methods.

Detailed Structure

The reference dimensions of ECAL are shown in the following figure. The reference length is 6700mm, the outer diameter is 4400mm, and the inner diameter is 3800mm.



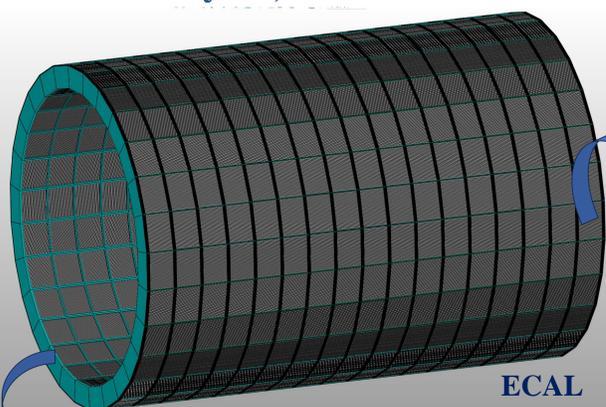
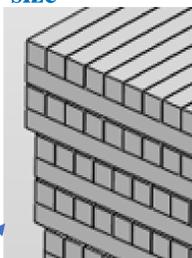
Detailed assembly of PCB and crystal bars



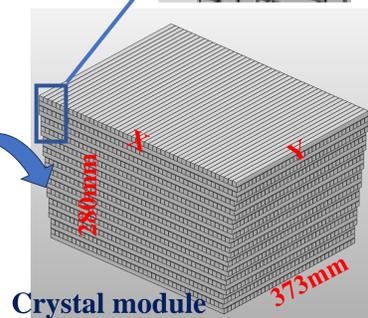
Barrel ECAL geometry design

Barrel ECAL is composed of 17 rings along the beam direction, with each ring containing 28 crystal modules weighing about 344kg; Each crystal module is divided into 7 groups, with different sizes of crystal bars in the X direction. The size decreases from the center to the outer edge. Each module contains 1134 crystal bars, which are arranged orthogonally between layers, readout from two ends.

4 layers per group with the same Y direction size

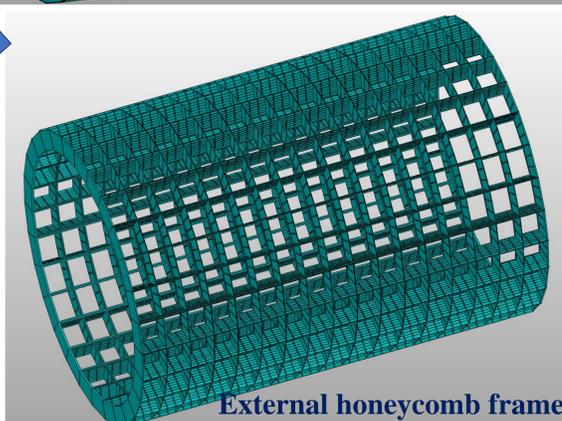


ECAL



Crystal module

The length of the external honeycomb frame is 6660mm, The weight is approximately 2.8 tons with carbon fiber material, and approximately 4.1 tons with aluminum material.



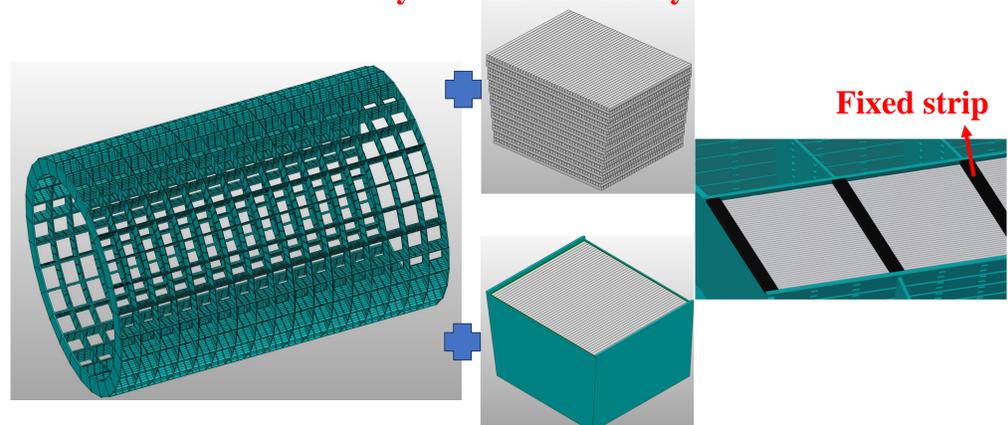
External honeycomb frame

The crystal bars in the X direction are supported by steps every four layers, while the crystal bars in the Y direction are supported by the crystal bars in the X direction; The two ends of the crystal bars are fixed by two curb pins, while the sides are fixed by two limiting blocks.

Question : Assembly under honeycomb structure

- Assembly of a single crystal bar

Key issue: Inefficiency



- Assembly of unit module

Key issue: Large amount of substance



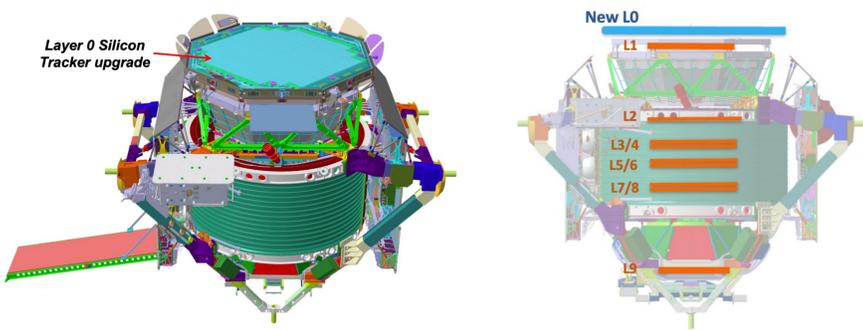
AMS-02 L0 Ladder Assembly Using a Robotic Gantry



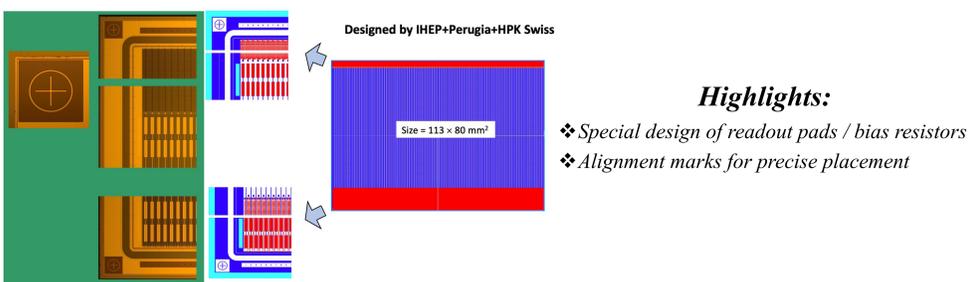
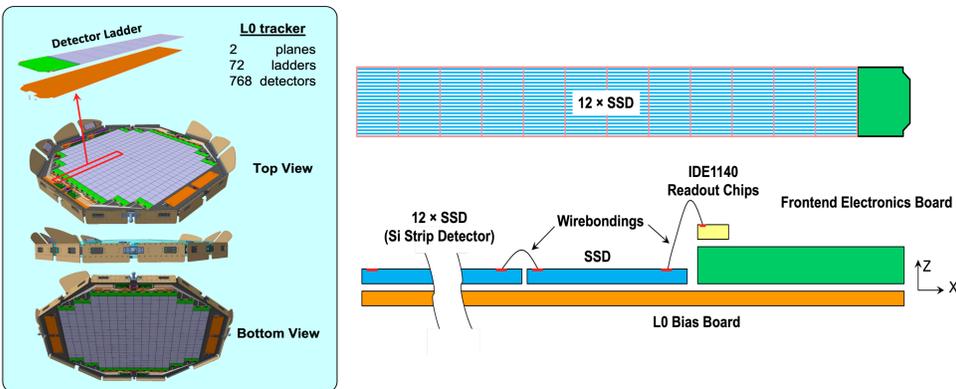
Baasansuren Batsukh¹ on behalf of the AMS-02 upgrade team
Institute of High Energy Physics¹, CAS

AMS-02 and L0 upgrade

AMS is a multipurpose particle physics detector that was installed onboard the International Space Station (ISS) in 2011. The objective of the experiment include indirect searches for dark matter, the primordial anti-matter, and the origin and propagation of the cosmic ray. The AMS-02 detector has a large acceptance of $0.5 \text{ m}^2 \text{ sr}$ and designed to carry out precise measurements of charged cosmic rays. The detector includes: a silicon tracker, the four planes of time-of-flight scintillation counter; transition radiation detector TRD, a ring imaging Cherenkov detector; an electromagnetic calorimeter, and the permanent magnet.



The L0 layer consists of two planes. Each plane is made up of 36 ladders and there are three types of ladders (with 8, 10 and 12 SSDs). The main responsibility of the Chinese team is to build ladders with silicon strip detectors (SSDs) using robotic gantry. Alignment precision is to be $5 \mu\text{m}$. Each SSD bears four fiducial marks and with a pattern recognition, alignment accuracy can be controlled. SSDs are glued on top of L0 Bias Board (LBB from now on) using conductive and structural glues. With this upgrade, the acceptance of the current detector will increase by 300% and the heavy ion identification will improve to the nickel.



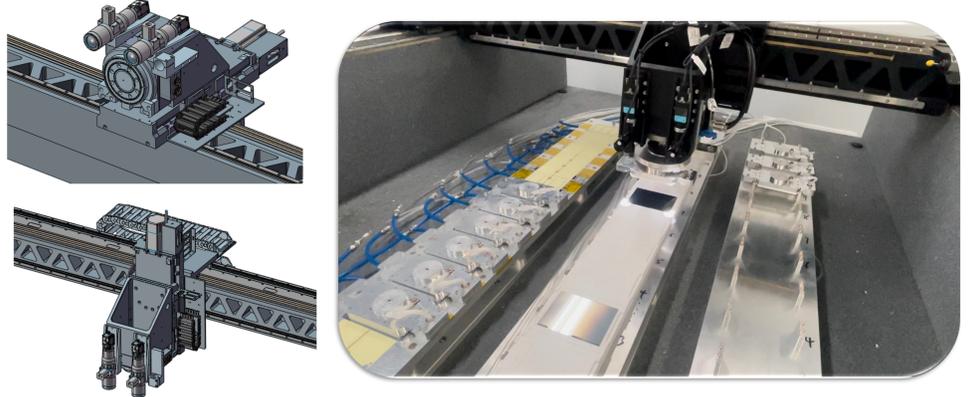
Characterization and Quality Assurance of SSD

To select good SSDs for ladder production: visual inspection, IV, CV measurements are required.

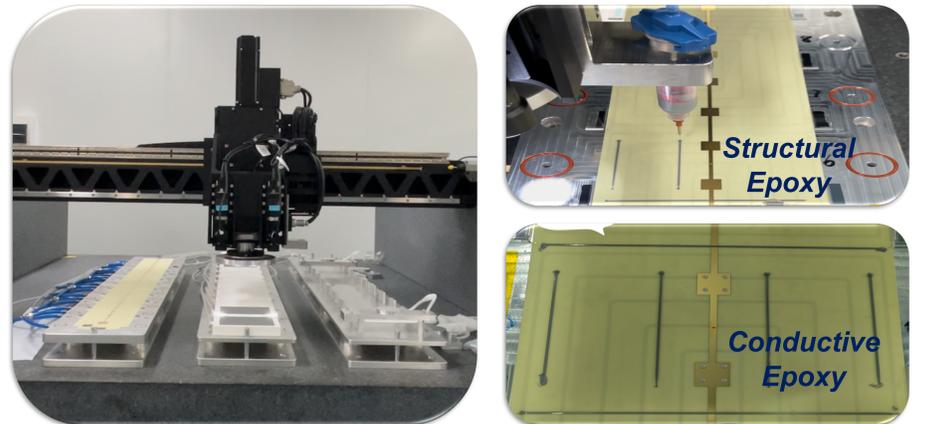


L0 Ladders and Assembly Procedure

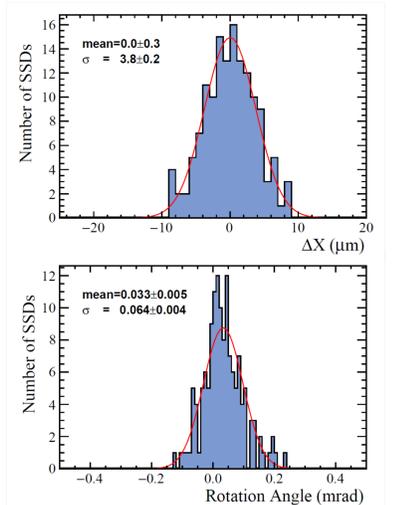
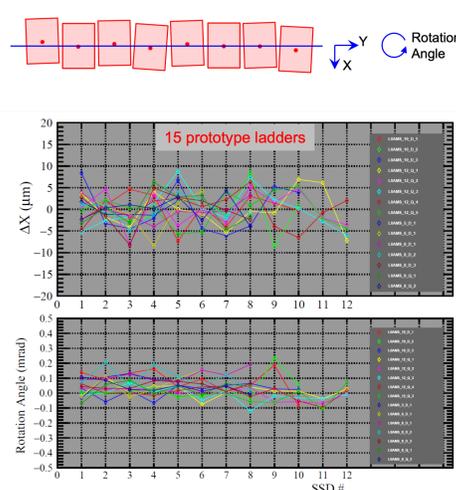
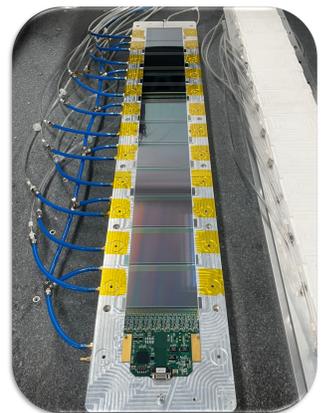
Robotic gantry consists of two cameras and can move in x , y , z and θ . Two camera will recognize two fiducial marks at the same time. This will provide the real-time coordinate information of SSD position that will be used for alignment.



Specific vacuum pick-up tools are made by a company. These tools will be picked up by the gantry head using vacuum pump. After this, vacuum pick-up tool will suck the SSD and bring it to the desirable location on top of LBB. Before these procedures, glues will be dispensed.



Once the ladder is assembled, alignment precision is assessed using an optical metrology system. The coordinates of all four fiducial marks on the SSDs are measured, and these measurements determine the alignment. We fit the X and Y coordinates to assess deviations along the vertical axis, as well as the vertical distances between two SSDs. The optimal vertical gap between two SSDs should be around $150 \mu\text{m}$. Thus far, we have achieved our goal of $5 \mu\text{m}$ precision along the horizontal axis.



Tracker optimization for the Fourth Detector Concept of CEPC



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on behalf of the CEPC tracker optimization team

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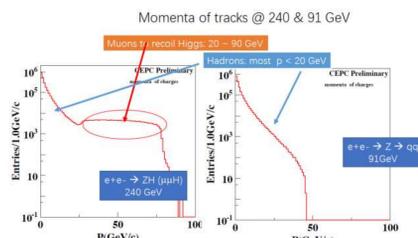
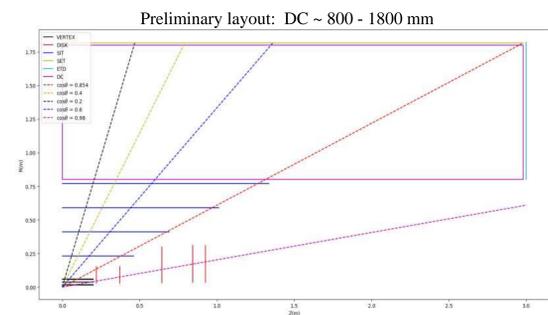
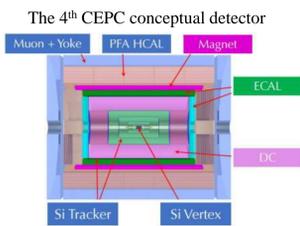
1. Abstract

The tracking system of the fourth conceptual detector at CEPC consists of a silicon pixel vertex detector, a silicon tracker of HV-CMOS, and a drift chamber (DC). In addition to tracking, the DC plays an important role in particle identification which is essential for flavour physics programme. The layout design will be a trade-off between optimal tracking and PID performance. Large DC volume will benefit identification of various hadrons, but should not cost deterioration of momentum resolution of tracks. The study of **tracking performance** as function of CEPC **DC volume** is necessary, using two fast-simulation tool and two full-simulation tools validating each other.

2. Introduction

Tracking system consists with a silicon pixel vertex detector(VXD), a silicon tracker (SIT and SET) of HV-CMOS, and a drift chamber (DC)

- Particle ID with a drift chamber is a key feature for the 4th conceptual detector
- Most hadrons (K/pi) of CEPC are below 20 GeV/c
- The tracker must have sufficient good momentum resolution for tracks < 20 GeV/c (flavor and jet study)
- VXD has already been optimized by others



Tools used for calculation & simulation

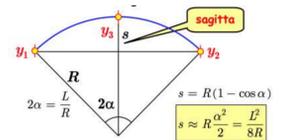
- Two fast tools
 - Analytic calculation based on python developed by Gang Li et al
 - LDT: a matlab fast simulation package developed by Wiener group
- Full simulation implemented in CEPCSW, CKF (Combined Kalman Filter) is used to track finding, reconstructed by
 - GenFit: developed by Yao Zhang et al
 - MarlinTrk: ILCSoft tracking maintained by Chengdong Fu

3. Momentum Uncertainty

Momentum error -Sagitta measurement without multiple scattering

$$\frac{\delta p}{p} = \frac{8p\sigma_{r\phi}}{0.3BL^2}$$

$$R = \frac{p}{0.3B} \quad \frac{\delta p}{p} = \frac{\delta R}{R}$$



Important features:

- the percentage error is proportional to the p itself
- the error is inversely proportional to B
- the error is inversely proportional to 1/L²
- the error is proportional to spatial resolution

$$s = R(1 - \cos \alpha)$$

$$s \approx R \frac{\alpha^2}{2} = \frac{L^2}{8R}$$

$$s = y_3 - \frac{y_1 + y_2}{2}$$

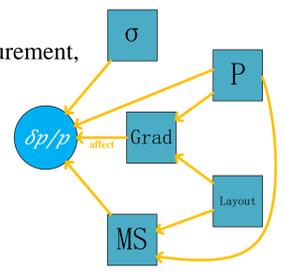
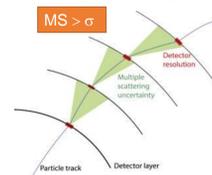
$$\delta s = \delta y_3 - \frac{1}{2} \delta y_1 - \frac{1}{2} \delta y_2$$

The error on the radius is related to the sagitta error → momentum error, and it's easy to get the relationship between sagitta and the 3 measurements:

- Necessary to have more measurements at the middle for better resolution
- The optimal allocation of measurements is 1:2:1

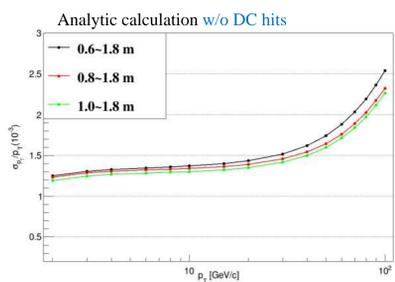
Momentum error with multiple scattering (MS)

- It is found to be complicated, when considering more factors on the momentum measurement.
- The left figures indicate that the MS affect the tracks, and the MS was influenced by the amount of materials, layout, momentum, and so on
- There are quite a few factors affect the momentum measurement, the relationships among them are shown in the right



4. Preliminary Results

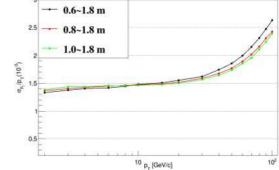
Without DC hits



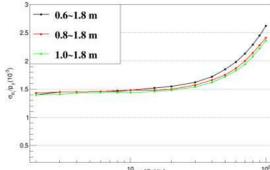
Analytic calculation comparison w/o DC hits

- The three lines has a small difference without DC hits but with DC materials
- SIT's location has a small effect on momentum measurement
- DC inner radius at 1.0m is better than 0.6 or 0.8m

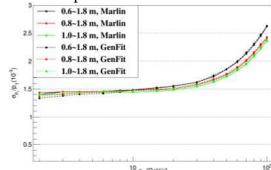
GenFit w/o DC Hits:



Marlin w/o DC Hits:



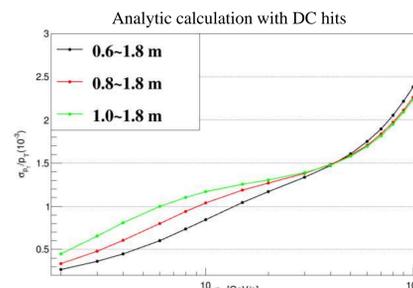
Comparison w/o DC Hits:



Validation: GenFit and MarlinTrk, w/o DC Hits

- The results are very similar when we don't use the DC hits,
- There are a little differences between these two, especially at low momentum

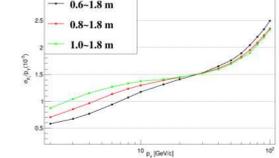
With DC hits



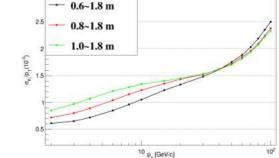
Analytic calculation with DC hits

- The difference becomes more significant when DC Hits are used, in particular at low momentum
- DC inner radius at 0.6m is better for tracks < 40 GeV/c

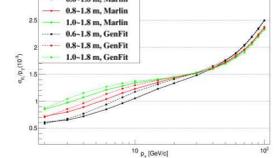
GenFit with DC Hits:



Marlin with DC Hits:



Comparison with DC Hits:

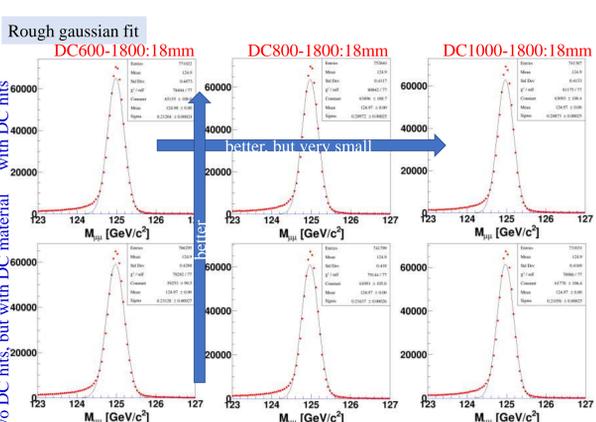


Validation: GenFit and MarlinTrk, with DC Hits

- The difference becomes more significant when DC Hits are used, in particular at low momentum
- The results of other simulations are consistent with the analytic calculation

5. Physics Performance

Resolution of Higgs Mass (H → μμ)



The sigmas of Higgs Mass (H → μμ)

DC volume	0.6-1.8(m)	0.8-1.8(m)	1.0-1.8(m)
w/ DCHits(GeV)	0.212	0.210	0.209
w/o DCHits(GeV)	0.231	0.216	0.211

- For Higgs physics(at high momentum), the DC volume has little effect on momentum measurement
- Using DC will significantly improve higgs momentum measurement

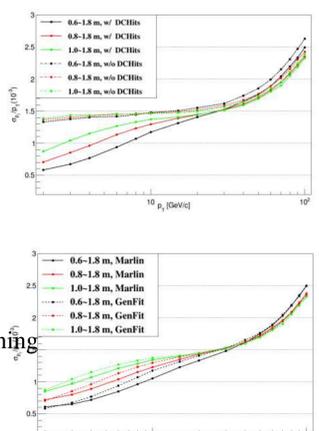
6. Conclusion & Discussion

Comments on tools

- Good agreement between AnaCalc & LDT
- Good agreement between GenFit and MarlinTrk w/o DC
- Rough agreement between GenFit and MarlinTrks w/ DC
- All trends of different tools are consistent

Preliminary conclusion

- DC useful for momentum measurement
 - Shapes and trends are constantly consistent for all results
 - More consistent results of different methods need more tuning
- Larger DC favored by low momentum (<20 GeV) tracks
- Larger DC also benefits PID





Institute Of High Energy Physics,
Chinese Academy of Sciences

Test of CMOS chip using 55nm process

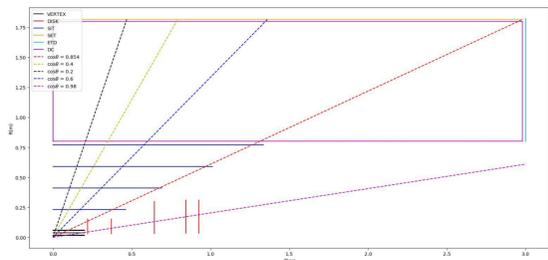
Yiming Li [♣] Dexing Miao [♣] Jianchun Wang [♣] Zhiyu Xiang [♣] Zijun Xu [♣] Xiaoyu Zhu [♡]
[♣]Institute of High Energy Physics, CAS [♡]Central China Normal University



CEPC workshop 2023, 23-27
October, Nanjing

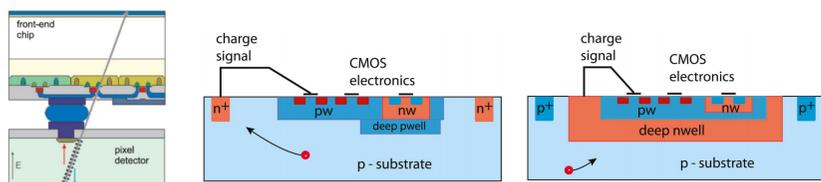
1 Introduction

CEPC plans to utilize a large-area, fine-pitch, low-material, fast-readout and economic silicon-based tracker system to achieve exceptional spatial resolution.



An alternative tracing system conceptual design.

CMOS technology presents an appealing solution due to its high performance and cost-effectiveness. Compared to hybrid silicon pixel sensors, the CMOS process allows for a smaller size while guaranteeing a lower amount of material budget. It is also a potential candidate for future upgrades to other experiments, i.e., the LHCb Upstream Tracker. Unlike many CMOS processes that require modifications and enhancements to generate sufficient signal, the commercially available high resistance wafer based High Voltage CMOS (HVC MOS) is intrinsically radiation hard and has large capacitance for signal acquisition. The potentially lifting noise and power consumption of HVC MOS, compared to the small-electrode CMOS, are tolerable for large area tracker. Moreover, the HVC MOS production process has further developed in domestic foundry recently, could be customized commercially.



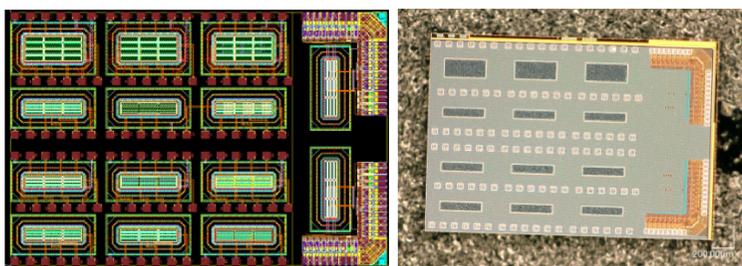
Hybrid silicon pixel sensor

small-electrode CMOS

high-voltage CMOS basic structure

2 MPW submission

The 1st design was submitted in October 2022 for MPW with 55nm low leakage process. 12 layout designs integrated on a chip with an area of $3 \times 2 \text{ mm}^2$. Each array contains 12 pixels, which minimum size is $25 \times 150 \mu\text{m}^2$ or $50 \times 150 \mu\text{m}^2$, varying with or without P stop between them. Simple charge sensitive amplifier structure was also added. Though the high resistance substrate was not yet available, a similar deep N well separating the transistors and the sensor part. The 2nd design has also been submitted in August 2023, which will be the real validation of the sensor with high resistance wafer. The updated analog amplifier, switch circuit and variant diode structures were added in this version.



The 1st layout design of CMOS chip and its production sample.

3 Lab test set up

The preliminary test, mainly IV and CV test, is based on production sample from the 1st design. In order to stably measure reliable sensor characteristics

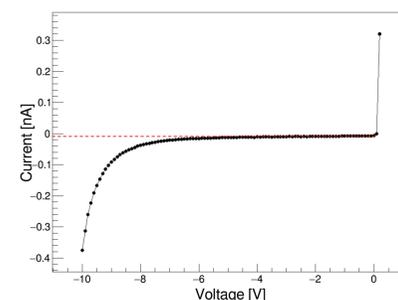
for different pixel array to prove the behavior whether is good diode like or not. The chip was tested by connected to probes in a thermostatic and magnetic shielded probe station. The Keithley 2470 source-meter was used as a bias source meantime could measuring current with a stable accuracy of 1 pA, and the capacitance of pixel array was measured by E4980A LCR instrument with an accuracy of several tenth fF approximately. The accuracy is sufficient for a single small diode of $0.1 \sim 0.2 \text{ pF}$ and a leakage current of 10 pA in estimation.



The IV and CV test probe station.

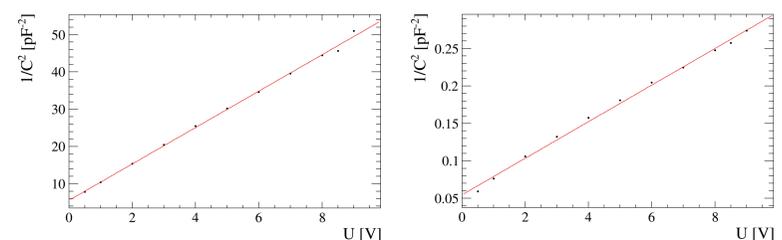
4 IV/CV results || Discussion

The IV test results show very good diode behavior with low leakage $\sim 10 \text{ pA}$ for all diode design, as expected. It is obvious that there is clear positive conduction, and gradually reverse breakdown begins as voltage increases to $-9\text{V} \sim -10\text{V}$. Significant improvement in reverse breakdown voltage is expected with the use of high resistivity substrate and high voltage process.



A typical IV test result, the leakage as low as $\sim 10 \text{ pA}$.

The CV test results are comparable for different diode design. The capacitance tends to stabilize as the diode is depleted and is proportional to the number of pixels in parallel. After subtracting the external capacitance of the testing system, around 0.5 pF , a good linear relationship between pixel array capacitance in inverse square and voltage can be obtained. For single small pixel, the calculated capacitance is compatible with predictions $0.1 \sim 0.2 \text{ pF}$.



An example of CV test result, where the left plot shows a single pixel and the right for the result of ten pixels in parallel. Note that the external capacitance of $\sim 0.5 \text{ pF}$ has been subtracted.

As a conclusion, first test results from CMOS chip show that the technology of 55 nm process with low leakage is promising. The preparation for test the HVC MOS in the near future is ongoing:

- IV/CV test under different conditions.
- Prepared laser system to verify pixel size and spatial resolution.
- Using nucleon beam in SNC, DESY or CERN to investigate real response of the HVC MOS chip to the MIP, and also study the radiation resistance.

The Luminosity Measurement of the CEPC and ATLAS with the LGAD

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介绍

未来高亮度大型强子对撞机 (HL-LHC) 升级后, 亮度测量的不确定性需要控制在1%以内。run2使用的金刚石探测器辐照后性能下降, 不能完成亮度准确测量。高能所设计的一款低增益雪崩探测器 (LGAD) 可在大剂量 ($2.5 \times 15 \text{ Neq/cm}^2$) 辐照后仍保持良好的信噪比, 因此被ATLAS选中, 代替金刚石探头进行亮度测量。目前LGAD技术也尝试应用于未来正负电子对撞机的快速束流监测上, 以保证其亮度测量的准确及物理潜力的实现。

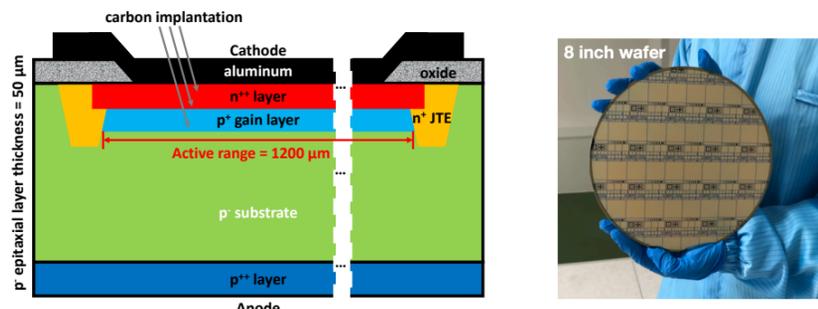


Figure 1: (left) Sketch of the LGAD structure (not to scale), (right) IHEP-IME LGAD sensor which could survive after $2.5 \times 15 \text{ Neq/cm}^2$ irradiation.

ATLAS 亮度测试新系统BMA安装及实验

ATLAS的亮度测试采用多套系统互相校正的策略, 以保证最终亮度测试的不确定性小、线性度好及稳定性高。其中一套为HL-LHC run4 特别设计的亮度探测系统叫做ATLAS束流监测探测器 (Beam Monitor for ATLAS, BMA), 安装于2022年。主要是为了应对HL-LHC升级后亮度升级带来更多的一次对撞事例数 ($\mu 60 \rightarrow 200$) 带来的亮度测量挑战。BMA安装在ATLAS实验前端屏蔽体JFC3处, 探头采用了两个IHEP-IME LGAD 传感器 (1.7mm^2)。具有易于每年更换和不需要额外散热设备的优点。BMA在run3 取数过程中进行了性能测试。

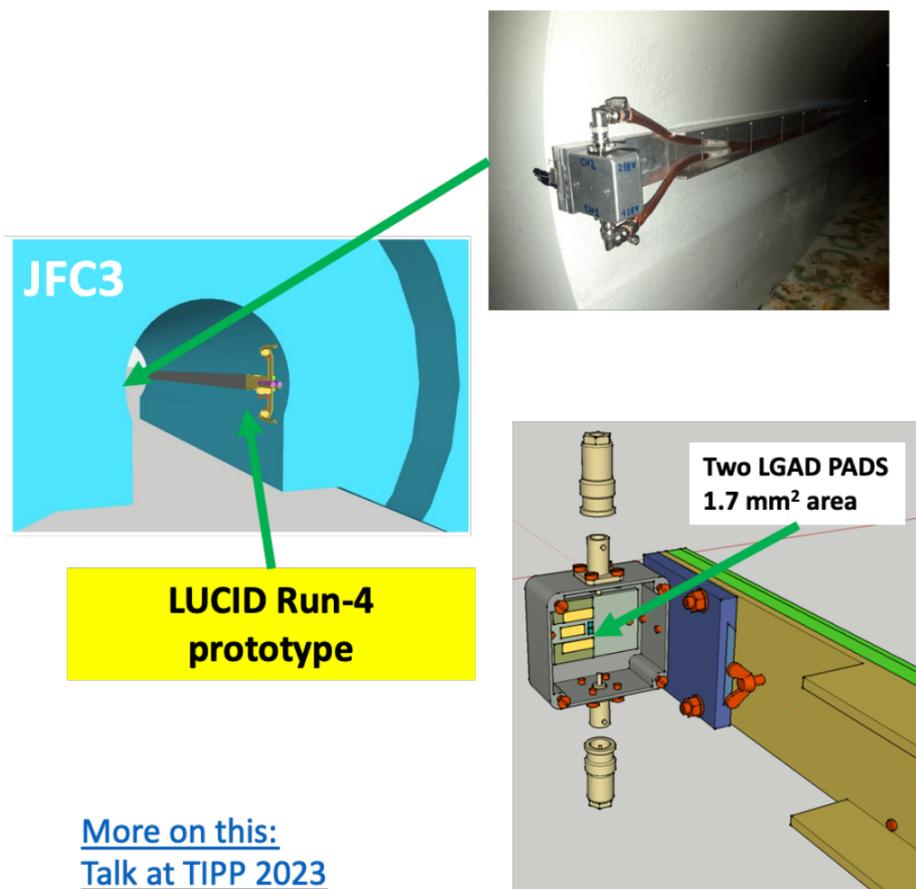


Figure 2: ATLAS 亮度测试探测器BMA安装示意图。

CEPC 快速亮度探测器设计

CEPC的亮度测试需要快速的给出亮度的信息以便快速判断束流对撞质量及给出调整信息。根据模拟知道CEPC亮度的主要信号来自Barbar反应, 为GeV的电子, 在束流管两侧分布不对称, 且在10m位置处, 会与束流方向以1mrad夹脚穿出束流管道。且信号强度高于背景电子两个数量级以上。因此, 为了进行亮度的快速监测, 计划将LGAD安装在束流管10m处, 与束流方向为1mrd 夹脚, 且两侧对称放置, 如图5所示。采用LGAD超快皮秒独处的特性, 实时快速束流密度, 即采用超快电子学测量信号电子数量, 给出超快束流亮度信息。

BMA亮度测试性能试验结果

如图3和4, 在2022年和2023年的束流实验后, BMA具有优良的线性度及稳定性。经过增益下降修正后, 使用了IHEP-IME LGAD的BMA的稳定性良好, 较ATLAS的主亮度探测器之一LUCID2%以内, 且不具有mu的依赖性。在未来进一步增益退化修正后具有更高精度测量亮度的潜能。

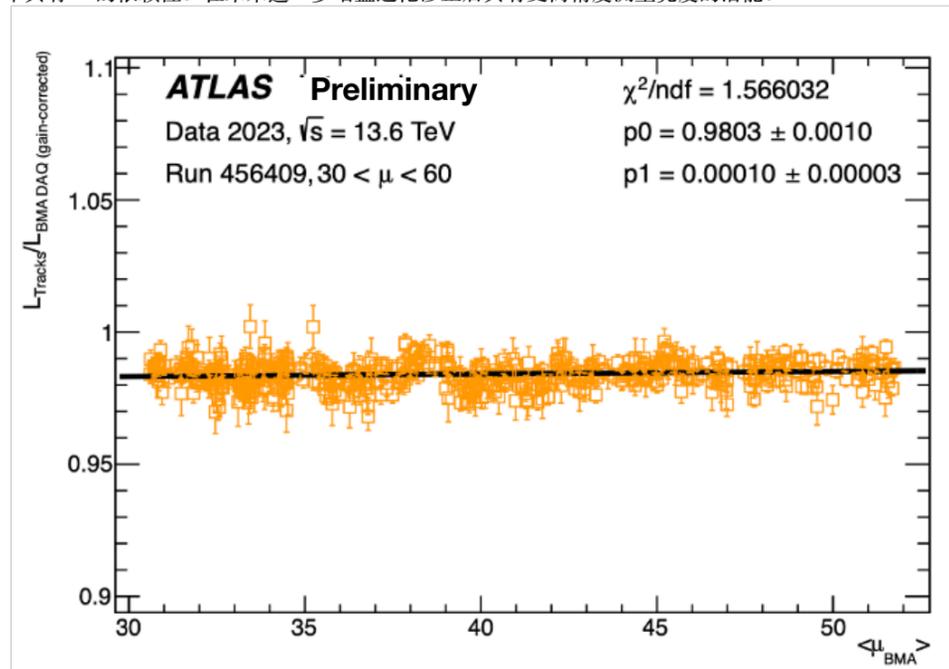


Figure 3: Mu dependence of BMA

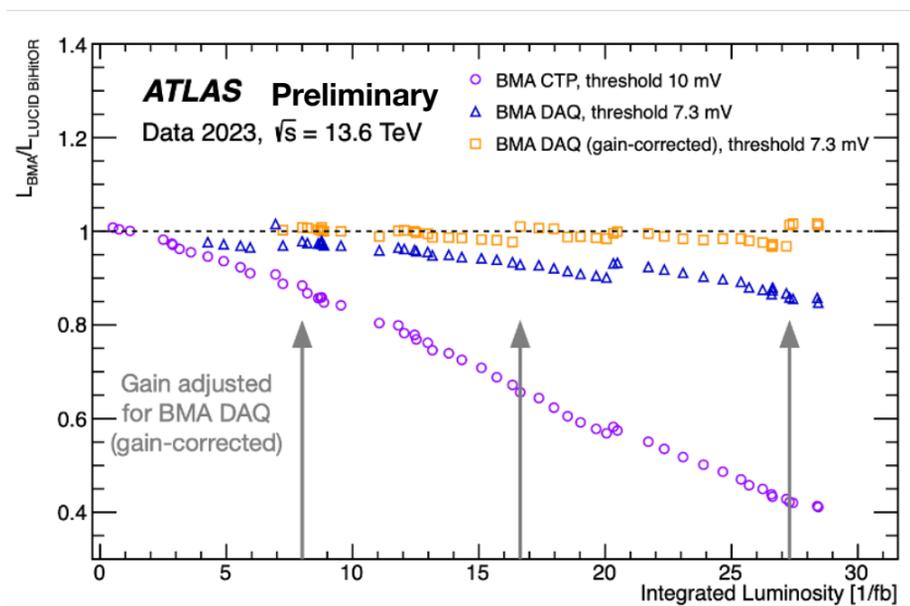


Figure 4: Ratio of the run-integrated-luminosity of BMA wrt to LUCID

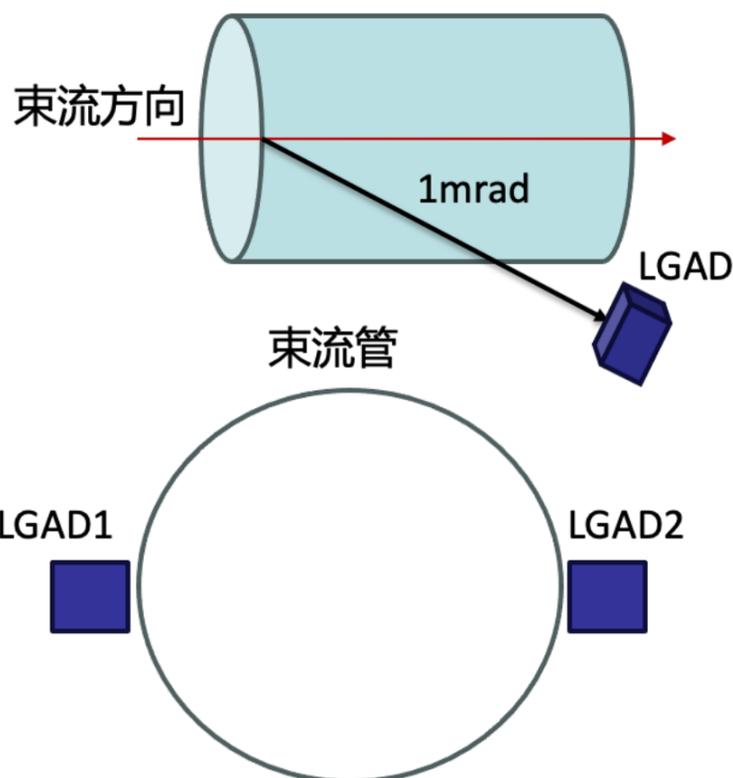
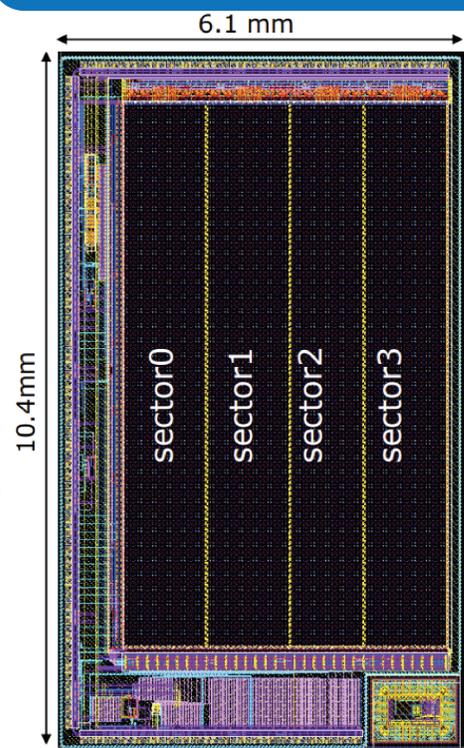


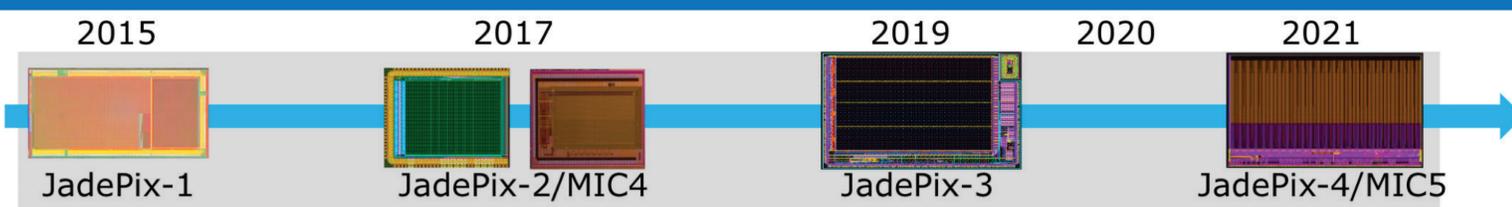
Figure 5: LGAD亮度探测器放置示意图, (up) LGAD位于CEPC束流方向1mrad处 (down) 两个LGAD对称放置于束流管切面两侧

Abstract: JadePix-3, one of the prototype designs for the CEPC vertex detector, prioritizes the investigation of two crucial performance metrics: spatial resolution and power consumption. Developed using the TowerJazz CIS 180nm process, JadePix-3 is a fully functional, large-scale detector chip. It achieves a remarkable spatial resolution of less than 5 μ m and an integration time of under 100 μ s, while maintaining a power consumption of approximately 50 mW/cm². These parameters have surpassed international standards, positioning JadePix-3 as an ideal candidate for beam telescope design due to its low noise level and high resolution capabilities. By utilizing the beam telescope, further advancements can be made in exploring the potential of CMOS silicon pixel detectors with enhanced precision, based on the foundation of JadePix-3.

THE JADEPIX-3



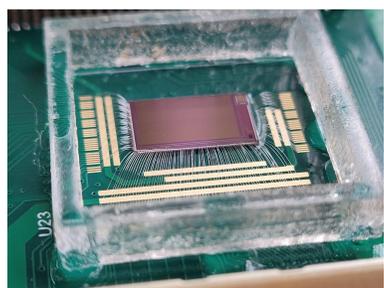
Layout of JadePix-3



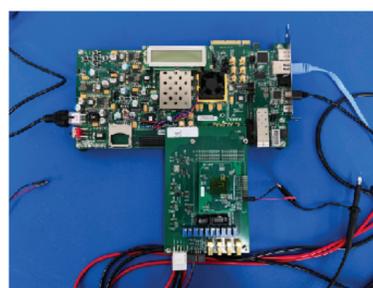
Key parameters:

1. Pixel array: 512 rows and 192 columns
2. Minimal pixel size: 16 x 23.11 μ m
3. Rolling shutter readout: 512 rows x 192ns/row = 98.3 μ s/frame
4. Four parallel sectors, scalable in z direction

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μ m	FE_V0	DGT_V0	16 x 26 μ m ²
1	2 + 2 μ m	FE_V0	DGT_V1	16 x 26 μ m ²
2	2 + 2 μ m	FE_V0	DGT_V2	16 x 23.11 μ m ²
3	2 + 2 μ m	FE_V1	DGT_V0	16 x 26 μ m ²



Chip bonding



Characterization and evaluation platform

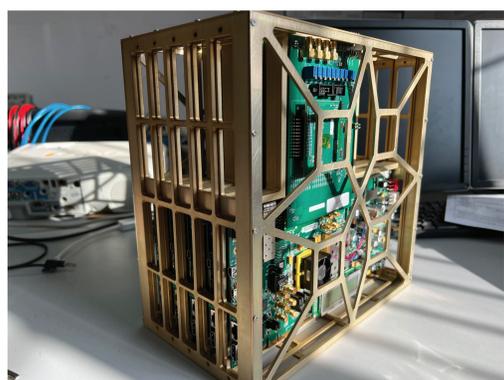
Characterisation Results :

1. Minimum threshold: 90e⁻ to 140e⁻
2. Noise: below 1x10⁻¹⁰/frame/pixel
3. Power consumption: 127 mW
4. Spatial resolution: 3 μ m (tested by infrared laser beam)

Publications:

1. The DAQ and control system for JadePix3
2. Design and Characterization of the JadePix-3 CMOS pixel sensor

TELESCOPE DESIGN

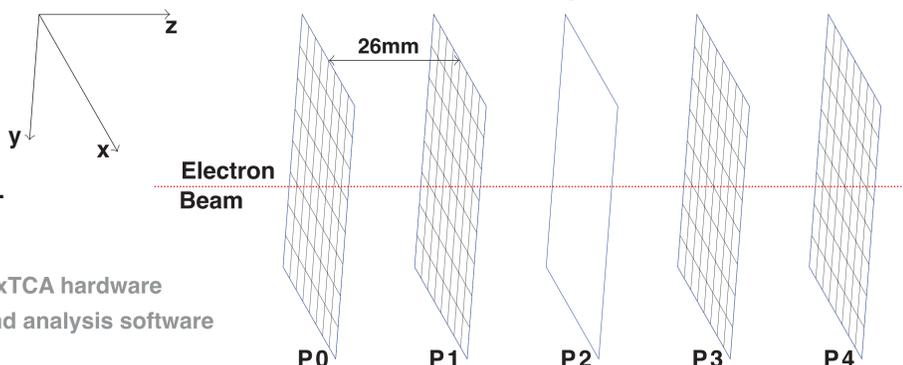


JadePix-3 telescope framework

Beam Telescope Design:

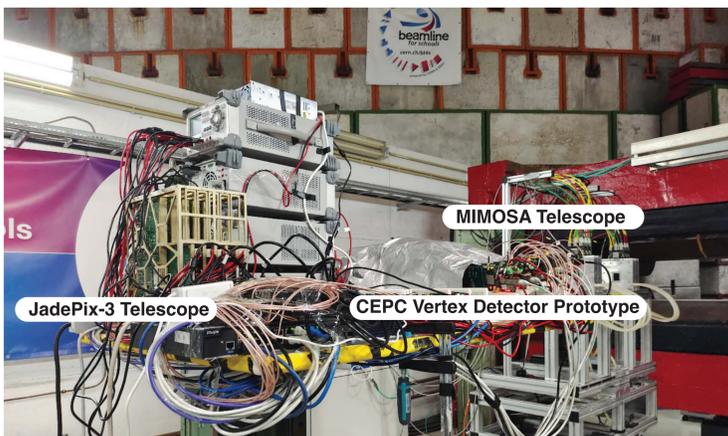
1. Synchronized clock fanout system
2. IPbus¹ based distributed readout and control system
3. Corryvreckan² integrated for offline data analysis

¹ IPbus: a flexible Ethernet-based control system for xTCA hardware
² Corryvreckan: a modular 4D track reconstruction and analysis software for test beam data

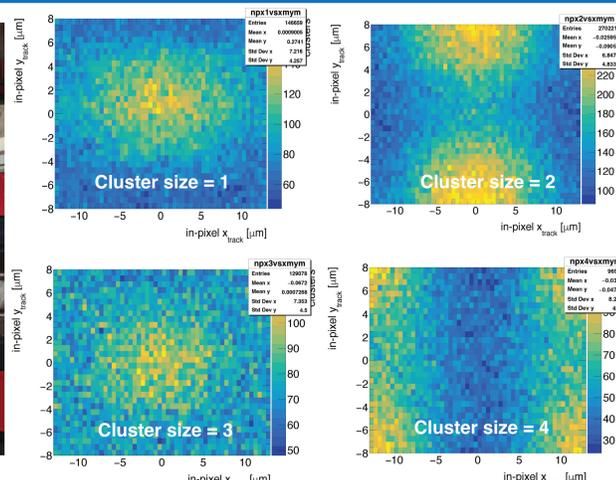


JadePix-3 telescope layout

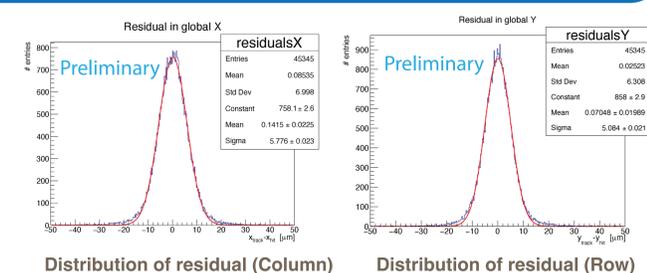
BEAM TEST AND PRELIMINARY ANALYSIS RESULTS



Beam test setup 2023 @DESY TB21



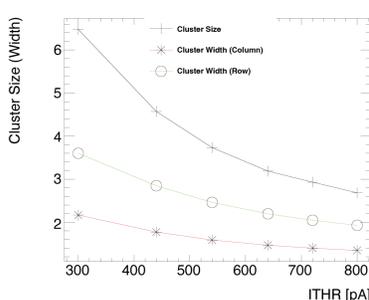
Location of different cluster size event



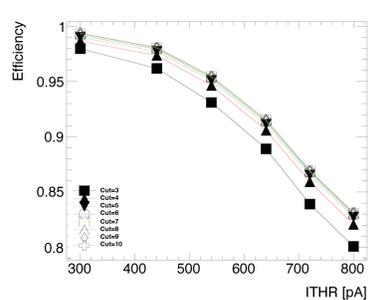
Distribution of residual (Column) Distribution of residual (Row)

Beam Telescope Performance (Preliminary):

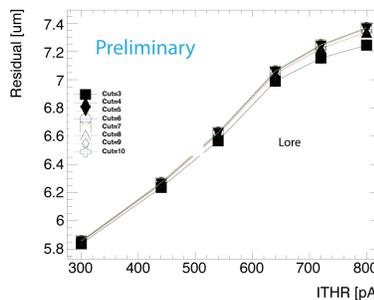
1. Best efficiency: 99.3%
2. Best resolutions in the row and column directions of JadePix-3: 5.2 μ m, 4.5 μ m
3. Best resolutions in the row and column directions of JadePix-3 telescope: 2.6 μ m, 2.3 μ m



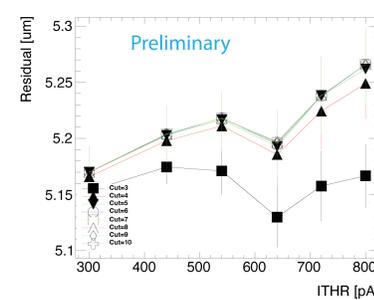
Cluster size vs current threshold



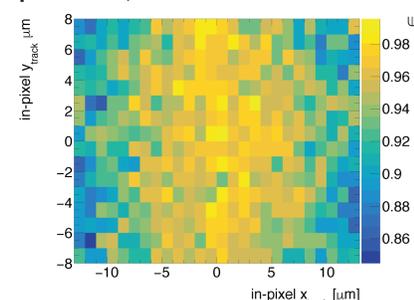
Efficiency vs current threshold



Residual (column) vs current threshold



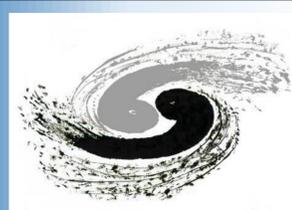
Residual (row) vs current threshold



Efficiency distribution in pixel

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Keywords: HVCMOS, Pixel sensor, Readout, UVM

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² Karlsruhe Institute of Technology (KIT)

³ Zhejiang University (ZJU)

1. Introduction

Monolithic Active Pixel Sensor (MAPS) in high-voltage CMOS (HVCMOS) technology is one of the most advanced detectors for high-energy particle detection. It is a high performance and cost effective choice for particle tracking in CEPC. In order to make research on new circuit structures and test their performance on a more advanced process node, an HVCMOS pixel sensor prototype is designed by a collaborative team from KIT and IHEP for Multi Project Wafer (MPW) running using the 55 nm process.

In this analog-digital mixed prototype, a 26×26 pixel matrix and related digital readout circuits are integrated. The digital module receives hit pulses from the pixel matrix and it is responsible for the timestamp measurements and data uploading. A readout structure based on quad pixel units together with joint transmission of address and hit pulse is developed. Additionally, a more standardized design process using Universal Verification Methodology (UVM) is utilized within this design. This poster provides an introduction to the digital design of this pixel sensor prototype.

2. Design of digital module

The digital module of the CEPC HVCMOS pixel is responsible for receiving hit pulses from the front-end pixel array via the address bus and performing time-to-digital conversion. The left-most two columns of pixels are dedicated to digital readout, while other pixels produce analog hit outputs. As a result, multi-readout strategies are aimed to be verified in this prototype. In this 26×2 pixels on digital readout, a 2×2 pixel array is divided as a quad pixel unit (QPU), resulting in a total of 13 QPUs. Each QPU is assigned a unique address, numbered from 1 to 13, with address 0 reserved to indicate no hit on the pixels. Pixels within the same corner direction across all QPUs share a common address bus, resulting in a total of four address buses as inputs to the digital module. When a pixel is hit, it drives out its 4-bit address on its address bus and this achieves a mixed transfer of hit pulse and address.

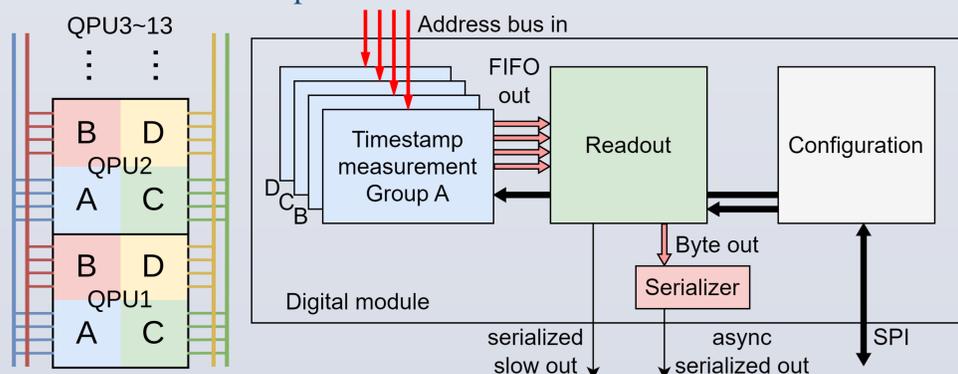


Fig. 1. QPU and address bus (left), and diagram of digital module (right)

The digital logic comprises four timestamp measurement modules, a data readout state machine, an asynchronous serializer, and a configuration block. An internal counter operates under the timestamp clock and produces timestamp values in gray code. The hit pulse from the address bus is operated with an OR logic in the timestamp measurement state machine to capture the leading and trailing edges. As the address bus is wired-OR driven, it could happen that multiple pixels generate overlapping hit pulses simultaneously. To address this, two check position parameters are set for a double check on the hit address, issuing an error bit in case of a mismatch. Additionally, to control the data rate and shield the noise spurs, a maximum detect length parameter is set. When a hit pulse is detected, the state machine locks for a specified clock period by this length, even if a trailing edge has already been detected. In the event of an exceptionally long hit pulse, potentially due to overlapping on the address bus, the state machine will terminate the current detection after reaching this maximum length. The measurement results are pushed into four parallel FIFOs and sent to the readout module. All of these parameters can be configured via the SPI configuration module.

The readout module performs polling check among the four FIFOs and generates a 48-bit data package for each hit. When a FIFO is enabled for reading, the readout state machine locks its number, captures the data package and waits for the byte shifter from the output interface to load the data package. Once this is complete, the readout state machine returns to the polling check state for the next data package.

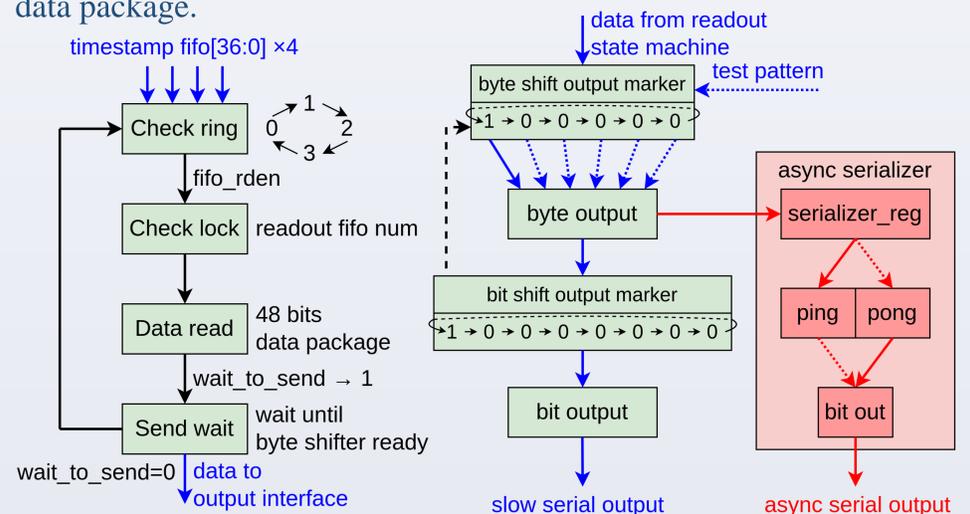


Fig. 2. Diagram of readout module and data interface

Two mutually exclusive readout interfaces are implemented for readout logic test, which can be selected active by configuration. In the slow serial output interface, the data package is transmitted on a single bit under the readout state machine's clock domain. In the asynchronous readout interface, the data package is sent on byte set to the serializer. The serializer locks the byte data with a ping-pong register, ensuring a sufficient setup time when crossing the clock domain. With this structure, the data can be readout on bit under an asynchronous clock whose frequency is eight times faster than that of the state machine.

3. Functional Verification by UVM

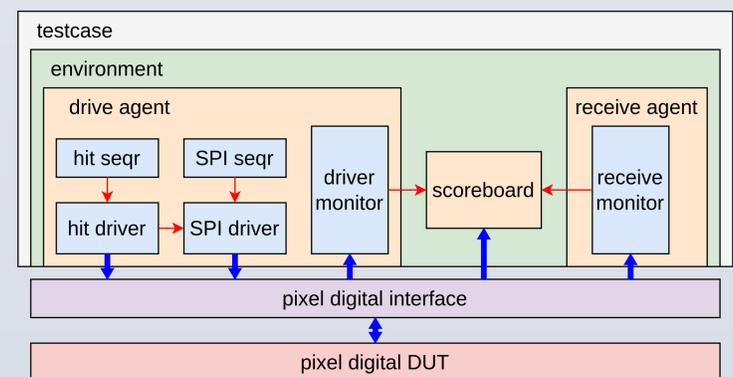


Fig. 3. UVM verification platform

For functional verification of the digital module, a UVM platform is established, as shown in Fig. 3. This testbench mainly focuses on two functions: configuration and readout. Two sequence classes are defined for generating SPI transactions and hit transactions separately. Correspondingly, two drivers control the start of these sequencers. The SPI driver starts the SPI sequence, randomizing a certain number of transactions and drives them to the DUT interface as random data/address configuration operations. It can also control the generation of abnormal short/long configuration operations to verify that the configuration module doesn't crash during incorrect operations.

The hit driver starts the hit sequence to generate a series of hit pulses on the address bus. This includes random, super long, spurs and overlapped pulses under different test cases when simulating various hit conditions. It also declares parameter settings to the SPI driver via a put-port. The driver monitor collects the hit pulse information and calculates expected output data packages, and in parallel, the receive monitor deserializes the output of the logic module into received data packages. Transactions from both monitors are sent to the scoreboard via tlm-analysis-fifo for matching and the scoreboard gives out the final verification result.

Exploration of a 55nm HV-CMOS process for the CEPC silicon tracker

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ABSTRACT

To explore process for next generation HV-CMOS pixel sensors, a prototype was designed and submitted in August 2023 using a 55nm HV-CMOS technology with a $1\text{k}\Omega\cdot\text{cm}$ substrate. This prototype includes a guard ring with a width of $170\mu\text{m}$, a 32×20 pixel-matrix, and 5 diode arrays. The pixel matrix comprises 6 flavor charge sensing diodes with a constant pixel size of $40\mu\text{m}\times 80\mu\text{m}$. Charge sensing amplifier and discriminator are integrated in pixels. The peripheral block includes row/column selection, bias DACs, a bandgap reference, and readout buffers.

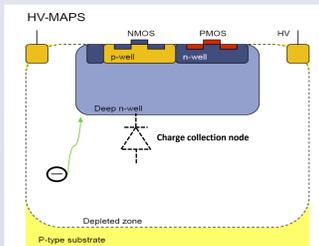
INTRODUCTION

Monolithic Active Pixel Sensors (MAPS) utilizing a specialized High-Voltage CMOS technology (HV-CMOS) have proven to be a promising choice for the CEPC silicon tracker. By applying a high reverse bias voltage ($> -50\text{V}$) to a highly resistive substrate ($> \text{a few hundreds of } \Omega\cdot\text{cm}$), it becomes possible to create a depletion depth of a few tens of microns. This results in superior time resolution and enhanced radiation hardness compared to standard CMOS processes.

Over the past decade, the development of HV-CMOS MAPS has primarily focused on the 180/150 nm processes. Transitioning to a smaller technology node not only enhances the current design's performance (power dissipation, readout speed, TID, etc.) but also opens up new possibilities. With a smaller technology node, more transistors and functionalities can be integrated into each pixel.

PROCESS SPECIFICS

- ❑ 55nm High-Voltage CMOS process;
- ❑ $1\text{k}\Omega\cdot\text{cm}$ p-type substrate;
- ❑ Custom designed IO;
- ❑ Core power: 1.2V;
- ❑ Triple-well process: n/p/deep n-well;
- ❑ Deep n-well/p-substrate breakdown Voltage $> 50\text{V}$;
- ❑ 10-metal layers is possible for fine pitch routing, including 2 thick metal layers for power;



Layout of the submission

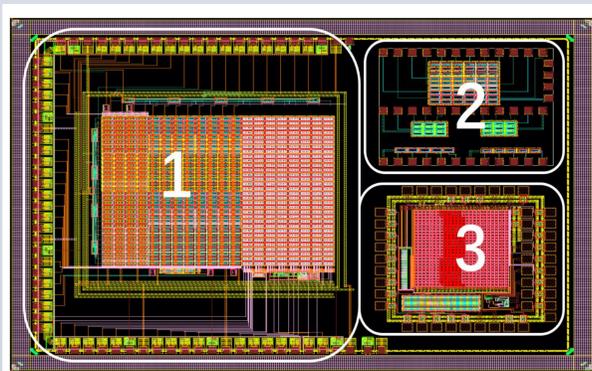


Figure: layout of the first submission on the 55nm HV-CMOS process. 3 independent sections are included for different purpose. The whole chip size is $4\text{mm}\times 3\text{mm}$.

- ❑ 1st section: a 32×20 pixel matrix comprises various diodes and in-pixel amplifier and discriminator design for process validation;
- ❑ 2nd section: 5 diode array for charge sensing diodes I-V/ C-V study;
- ❑ 3rd section: a 26×26 pixel matrix with relative digital readout periphery for new electronics structure study; (Hui Zhang's talk & Ruoshi Dong' poster)

Guard ring & pixels

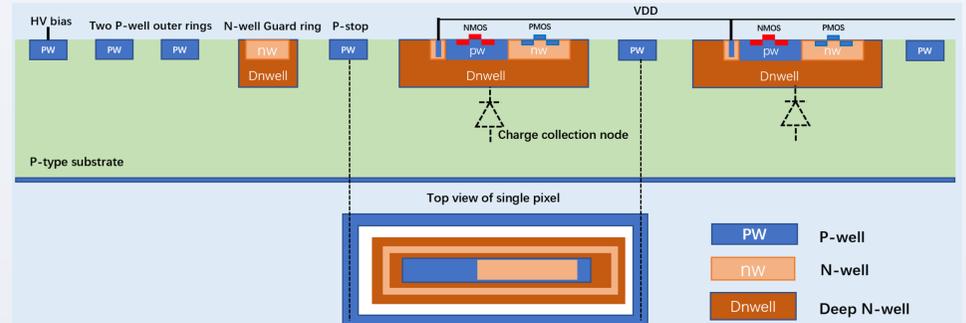


Figure: Cross-section and top view of the guard ring and pixel design.

Table: 6 flavor charge sensing diodes comprised in the section 1&2.

Diodes flavor	Specifications
Pix_D10core	Single DNW size: $30\mu\text{m}\times 70\mu\text{m}$, With P stop
Pix_D10core_wps	distance between two diodes $10\mu\text{m}$ Without P stop
Pix_D15core	Single DNW size: $25\mu\text{m}\times 65\mu\text{m}$, With P stop
Pix_D15core_wps	distance between two diodes $15\mu\text{m}$ Without P stop
Pix_D20core	Single DNW size: $20\mu\text{m}\times 60\mu\text{m}$, With P stop
Pix_D20core_wps	distance between two diodes $20\mu\text{m}$ Without P stop

Charge Sensing Amplifier & Discriminators

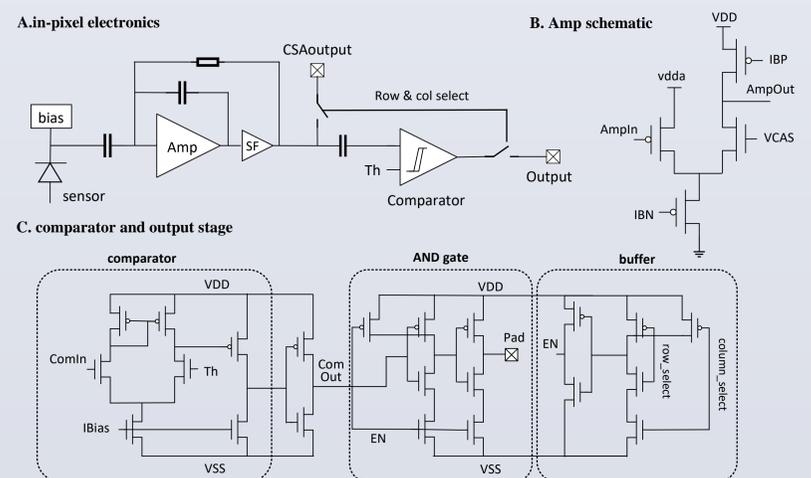


Figure: One version in-pixel electronics in the 1st section (two different versions in total). Both the analogue and digital signals are output.

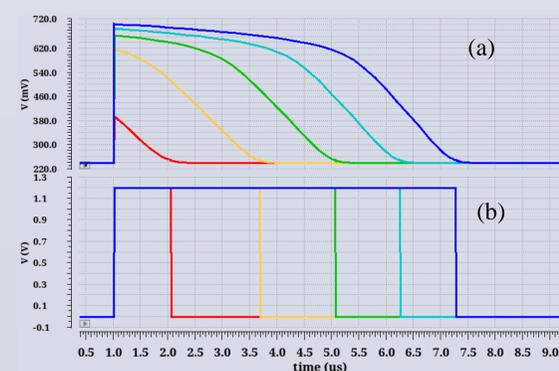
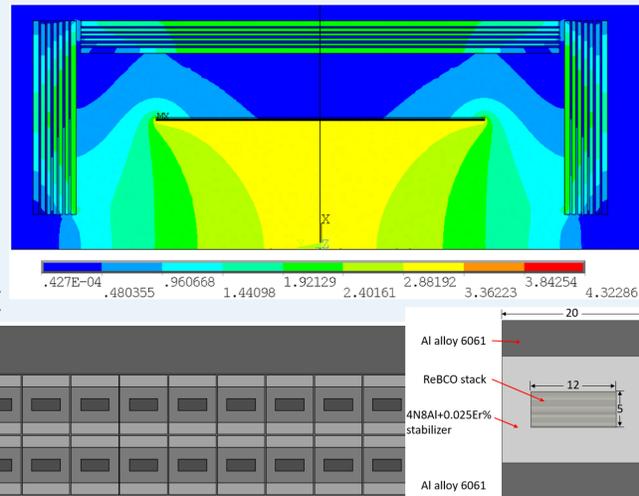
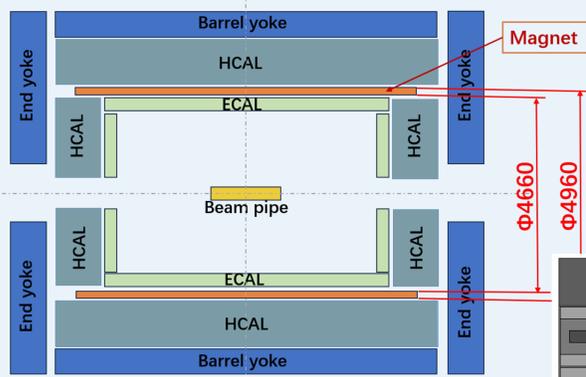


Figure: Output transients voltage of the output of (a) CSA, (b) the discriminator for different charge varied linearly between 2ke^- and 18ke^- in 4ke^- steps (simulation results, $C_{\text{input}} = 150\text{fF}$)

CONCLUSION AND PERSPECTIVES

The initial submission utilizing the 55nm HV-CMOS process was completed in August 2023. It incorporated various versions of charge sensing diodes, in-pixel electronics, and readout structures. Currently, efforts are underway for preparation of design validation. The forthcoming test results are anticipated to offer vital insights, serving as essential benchmarks for the future advancement of HV-CMOS pixel sensors for the CEPC tracker.

CEPC Detector Magnet HTS version

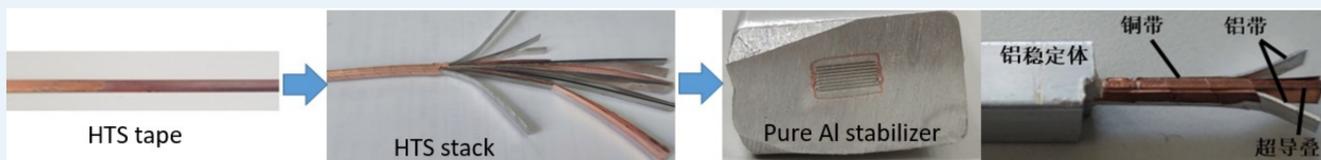


Magnet parameters:

Magnetic field	3 T	Current	28000 A
Inner diameter	4660 mm	Inductance	1.27 H
Outer diameter	4960 mm	Stored energy	500 MJ
Magnet thickness	150 mm	Cold mass	27 ton
Length	8 m	HTS cable length	10.7 km
Total weight	48 ton	ASTC weight	16.6 ton

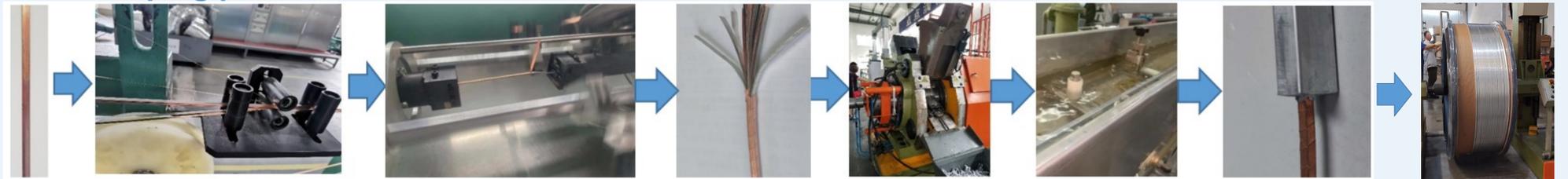
Al stabilized Stacked HTS Tape Conductor (ASTC) development

Superconducting cables are the key to detector magnets. In 2017, IHEP proposed a high temperature superconducting (HTS) scheme for detector magnet and innovatively designed an aluminum stabilized HTS stacked conductor, then began the development of small-scale sample cable.



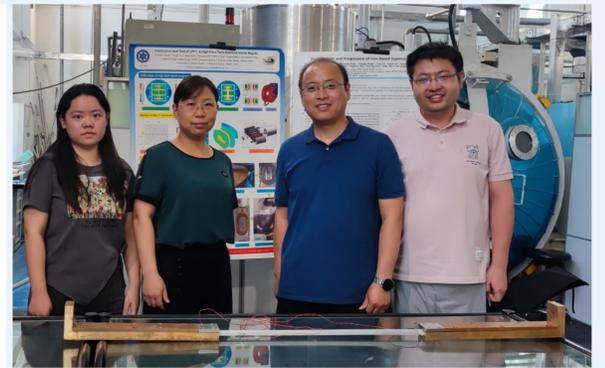
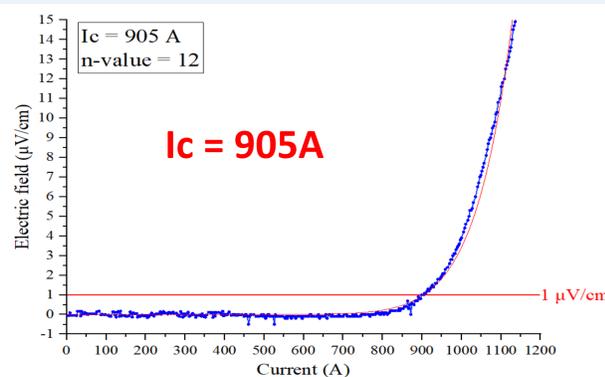
Small-scale sample cable

Developing process of ASTC:

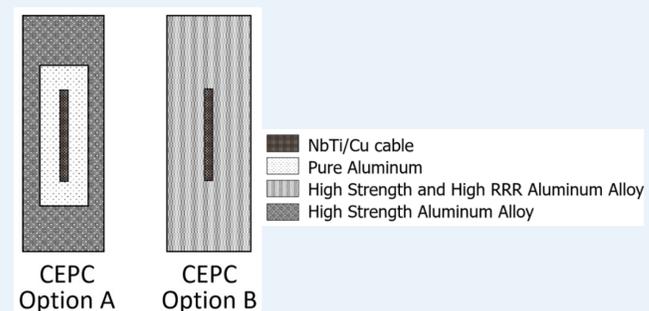
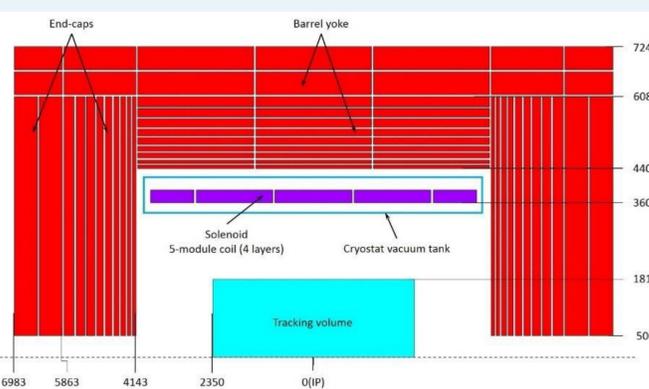


Object: single tape core $I_c > 100 \text{ A}@77\text{K}$; considering the self-field effect, The critical current of a 14-core cable is larger than $830 \text{ A}@77\text{K}$, self-field.

After three years of research and development, the performance of the cable has met the expected requirements.



CEPC Detector Magnet LTS version



Development of Aluminium stabilized superconductor

Aluminium stabilized superconductor:

- Dimension: 4.7mm*15mm
- Diameter of Strands: 1.2mm
- Number of Strands: 16
- The residual resistivity ratio (RRR): >800
- Yield strength of superconductor: >150 MPa.
- Shear strength between the aluminum and the Rutherford cable: >20 MPa.
- Critical current of a single strand:
 - Before coextrusion: 1501A@5.5T, 4.2K
 - After coextrusion > 1,350 A@5.5 T, 4.2 K.

fig4. micro view of bonding surface

Dimensions: 15*4.7mm²
Number of strands: 14
Material: COPPER+Al(99.99% purity)
Complete time: 2011.8
Shear strength (COPPER & Al): >35MPa

Progress of Box configuration superconductor

Box configuration superconductor is obtained through a secondary co-extrusion process on the outside of aluminum-stabilized superconducting cable.

dummy cable 56*22mm
Aluminum alloy+ copper 4.7mm*15 mm cable

Box superconductor 56*22mm
Electrical grade Aluminum + 4.7*15mm cable

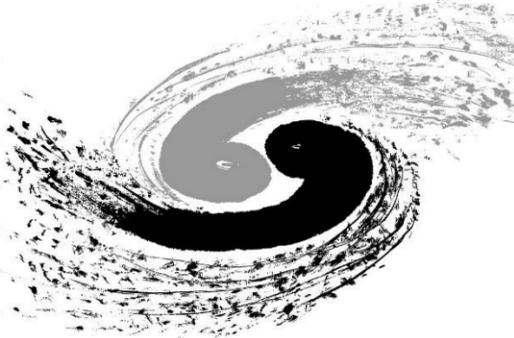
By experimenting with different alloy aluminum materials and preheating temperatures of the forming molds, finally we achieved the box configuration superconductor from the electrical grade aluminum and 4.7mm*15mm cable by a second coextrusion process.

- Rutherford cable: 20.5*2.15mm, 32 strands of NbTi, pitch: 129mm, fill factor: 86%, Ic decay after stranding: <5%
- First extrusion: 10mm*33mm
- Second extrusion: 22mm*56mm

Rutherford cable 32 strands

first co-extrusion pure Aluminum + Rutherford cable

second co-extrusion Electrical grade aluminum+cable from last step



The status of SiPM developed by IHEP

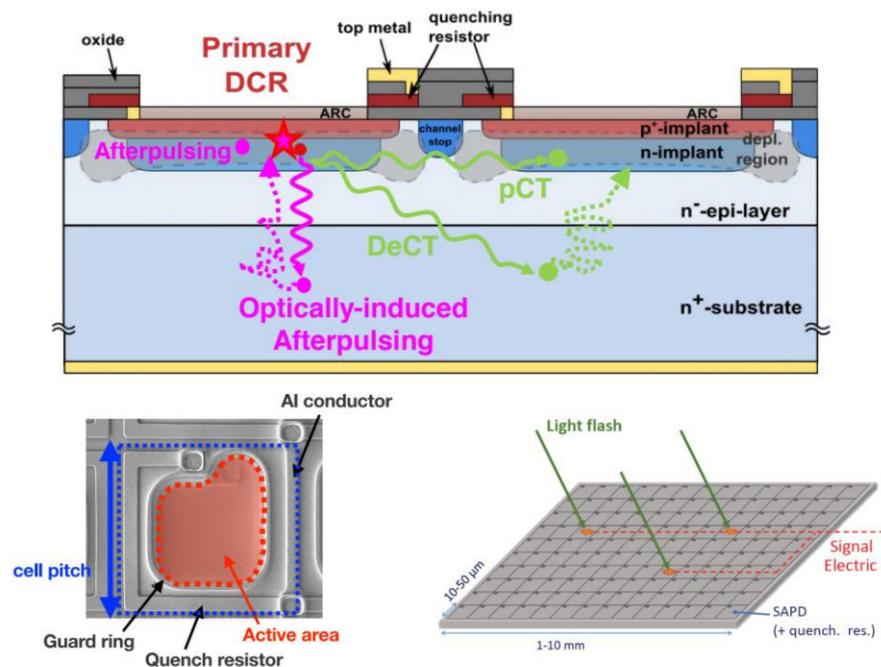
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Silicon Photomultipliers (SiPM) has advantages such as low operating voltage, high gain, high photon detection efficiency, and resistance to magnetic field interference, making it a high-performance device for photon counting. SiPM is also a key component in major scientific projects such as CEPC, LACT, and HERD. Self-developed SiPM can reduce the construction cost of the detectors, conduct personalized customization, and will have high yield, high consistency, and sufficient production capacity. Preliminary structural and technological design of radiation resistant SiPM based on the existing domestic radiation resistant LGAD design. At present, preliminary performance testing has been completed for SiPM sample produced along with radiation resistant LGAD, and its structural design and some technologies have been verified.

Introduction to SiPM Structure



IHEP SiPM v1 design

Electric field distribution

Total current density distribution

I-V

QE vs. Wavelength

Mask design

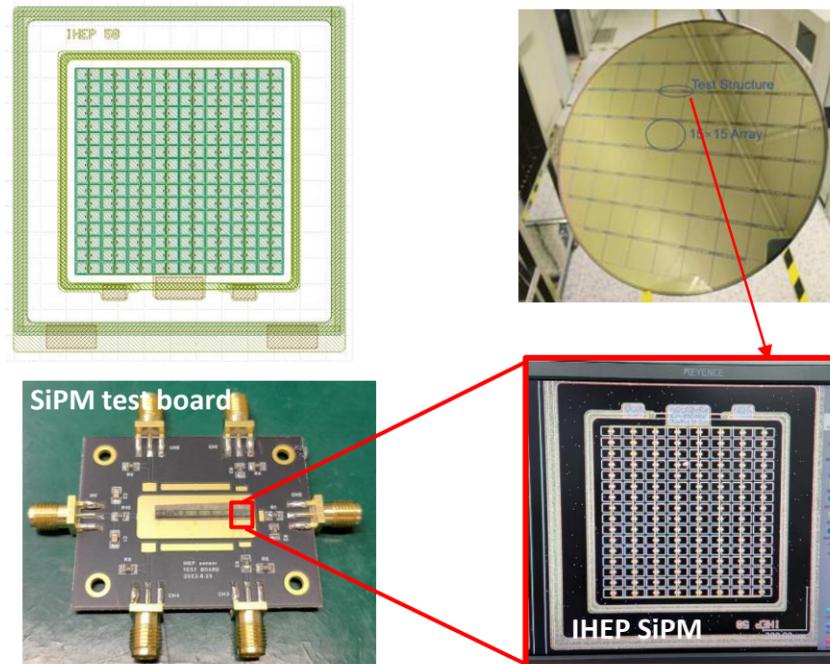
Electrode distribution

- SiPM size:**
- 7.6mm×7.6mm
 - 3.0mm×3.0mm
 - 1.5mm×1.5mm
 - 152 x 152 pixels
- Pixel size:**
- 100um、 50um、
 - 20um、 10um

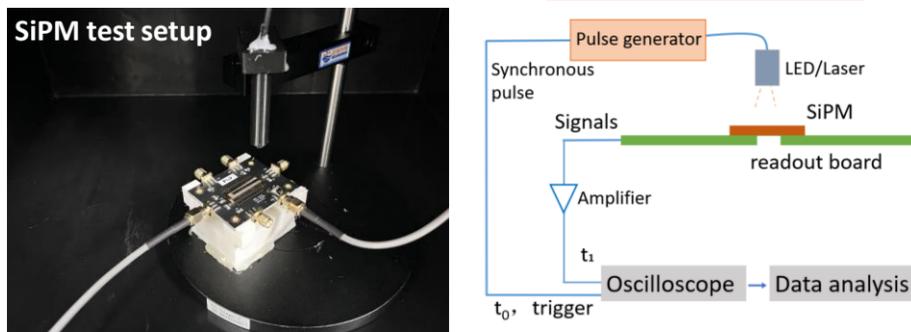
Formal tape-out plan:

- **Submit design layout at the end of October**
- **Complete the first version of tape-out by the end of the year**
- **January to February 2024: Testing**
- **March to April 2024: Optimize the design and submit the second version of the tape-out**

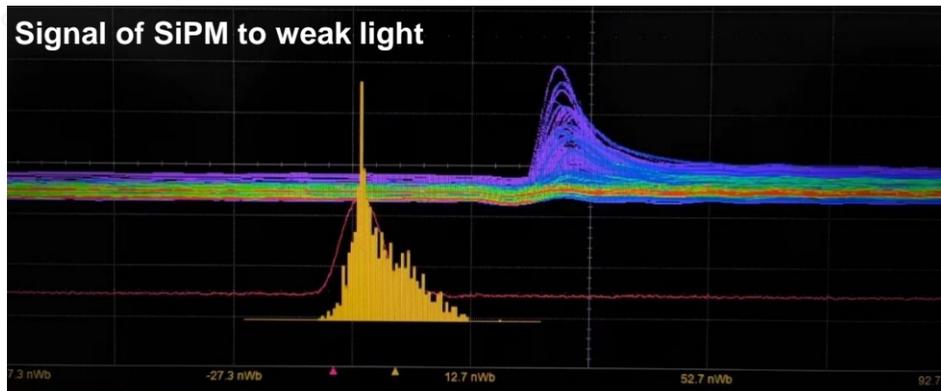
SiPM sample produced along with LGAD pre-production (IHEP SiPM v0)



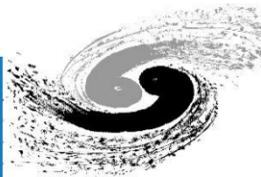
SiPM test setup



Signal of SiPM to weak light



IHEP's self-developed radiation resistant SiPM based on LGAD's existing excellent technologies and structural design will be used for collider experiments and space experiments. At present, we have produced SiPM samples, and after preliminary testing, the energy resolution and leakage current need to be optimized. The official wafer layout has been designed and SiPM wafers are planned to be completed by the end of this year for further testing and optimization to develop SiPM with radiation resistance and large dynamic range.



Offline analysis for the beam test of CEPC vertex detector prototype

Shuqi Li (IHEP, shuqi.li@cern.ch)

The 2023 International Workshop on the High Energy Circular Electron Positron Collider



Introduction

CEPC ?

- **Circular Electron Positron Collider**^[1] proposed by Chinese particle physics community
- Double-ring collider with **electron and positron** beams circulated in opposite directions in separate beam pipes
- Precise measurement of properties of **Higgs, W and Z bosons**

Vertex detector ?

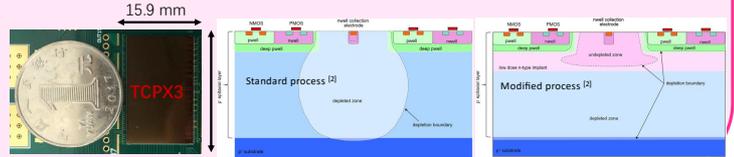
- H → bb precise **vertex reconstruction**
- H → uu precise **momentum measurement**

High spatial resolution (3~5 μm)
Radiation hard (> 1 Mrad)

CMOS pixel sensor prototypes?

- **TaiChuPix3 pixel sensor developed for the vertex detector**
1024 x 512 Pixel array
25μm x 25 μm per pixel → high spatial resolution
- **Process: CIS 180nm process**
Standard process (baseline option)
Modified process^[2] (an extra low dose n-type layer)

**modified process:
faster charge collection**

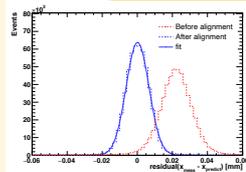


Beam test @ DESY

DESY TB21 beam line ^[3]

- 4 ~ 6 GeV electron beam

Offline data analysis flow



- **Clustering:** geometric center of the gravity of the neighboring fired pixels
- **Alignment:** Millipede^[4]
- **Track fitting:** Straight line fit and General broken line fit^[5]



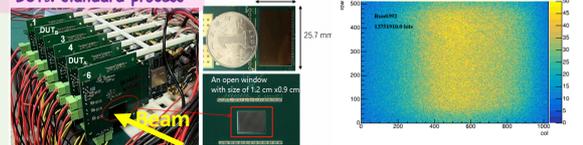
Test beam on pixel sensor prototype

Setup

- 6 equally spaced (4cm) detector module with TaichuPix3

DUTs: modified process
DUTs: standard process

Hitmap of one DUT



Spatial resolution

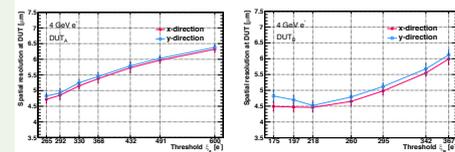
- **Estimation of intrinsic resolution**^[6]

$$pull_b \equiv p_b = \frac{r_b}{\sqrt{\sigma_{int}^2 - \sigma_{t,b}^2}}$$

r_b : biased residual
 σ_{int} : intrinsic resolution
 $\sigma_{t,b}$: biased track uncertainty

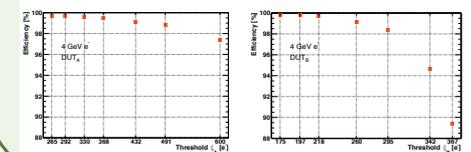
- $pull_b \sim N(0, 1)$, if accurate estimate of the intrinsic resolution and scattering angle
- The standard deviation of $pull_b$ iteratively used to update the estimate σ_{int}

Resolution vs. Threshold



Higher threshold → less cluster size → less charge sharing effects → worse spatial resolution

Detection efficiency

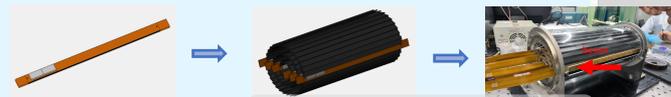


The detection efficiency for both process can reach 99% at the lowest threshold

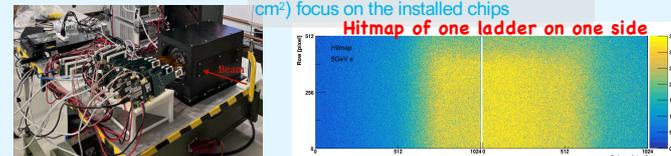
Test beam on vertex detector prototype

Mechanical prototype assembly

- Doubled ladder with **2 TaichuPix3 chips on each side**
- **6 ladders** mounted on the mechanical prototype



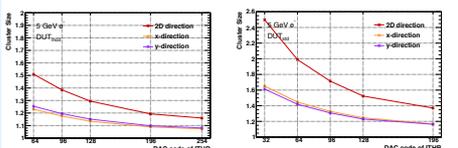
Beam test setup



Biggest collimator available (2.5 x 2.5 cm²) focus on the installed chips

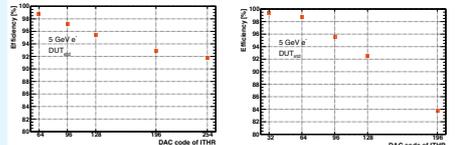
Hitmap of one ladder on one side

Cluster size



The DUT with the standard process shows more charge-sharing effects

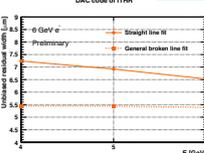
Detector efficiency



The detection efficiency also can reach 99% for the vertex detector prototype at the lowest setting threshold

Unbiased residual width

The unbiased residual width before and after correction for multiple scattering



Conclusions

- The spatial resolution of TaichuPix3 sensors can be < 5 μm for both processes
- The detection efficiency is larger than 99% for both processes of TaichuPix3 sensors.
- The vertex detector beam test results show nearly identical results to the sensor beam test.

References

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Introduction

TPC (Time Projection Chamber) is a promising candidate for track resolution and time resolution as the baseline track detector concept design in CEPC (Circular Electron Positron Collider), TPC can easily meet the spatial resolution demand at the Higgs mode, just there are massive electrons and ions in gas chamber when running Z pole, which led to the distortion of track. The massive electrons or ions in the gaseous detector chamber is a critical issue affecting the spatial resolution that need to study. Aimed to simulate this situation and accorded to the interaction mechanism and research of UV light and the materials, UV light triggers mainly two reaction in a TPC prototype. Photoelectric effect occurs on the surface of metal materials (placed inside the chamber), and two-photon ionization occurs in the interaction between the UV light and gas molecules in the chamber. These two effects can be used in simulating the space charge effect and particle tracks inside TPC respectively. The feasibility of such simulations is promised in this experiments.

Generating mimic space charge with deuterium lamp

- In our experiment, Aluminum plates with different LPI is placed inside the TPC prototype and radiated by UV deuterium lamp. The electrons generated by photoelectric effect are expected to mimic the space charge in the working environment of TPC.

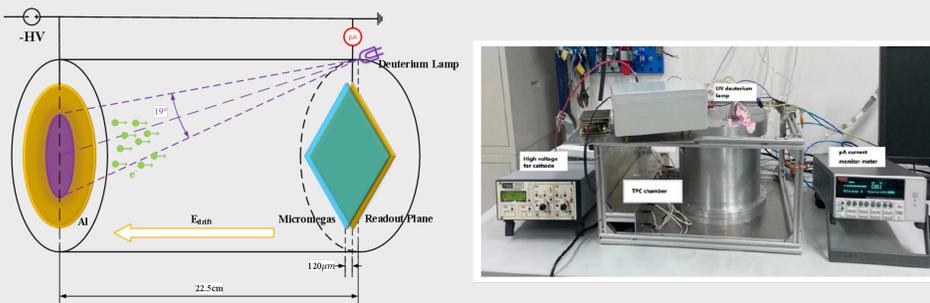


Figure 1: A sketch and the installation of our experiment generating and testing the mimic space charge with UV deuterium lamp.

Result of the UV deuterium lamp created the massive electrons by photoelectric effect

- The photocurrent is measured with different LPI Aluminum surfaces and electric field.

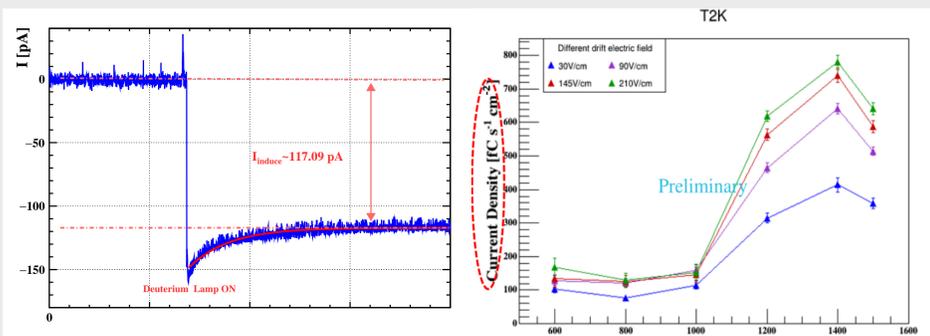


Figure 2: The result of the massive electrons current created by photoelectric effect with UV deuterium lamp, showing a stable output.

Photocurrent amplification

- Massive electrons caused by UV deuterium lamp are amplified by Micromegas in different working gas ($Ar/iC_4H_{10} = 95/5$, T2K, CF_4)

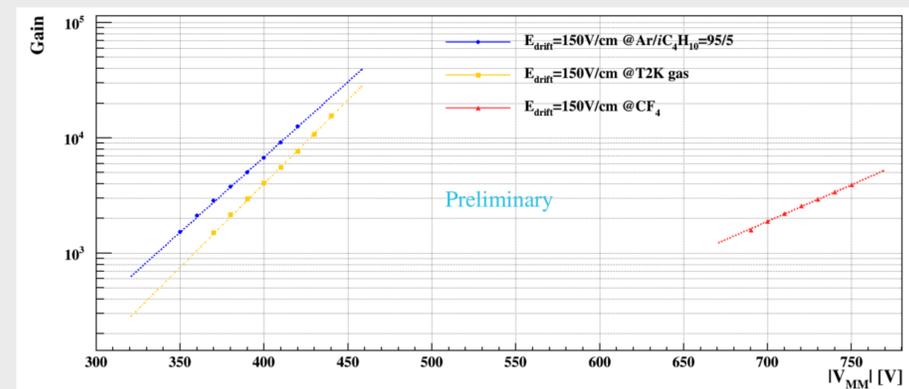


Figure 3: The measure of amplified current shows a ideal gain curve in different kinds of working gas.

Acknowledgment

This study was supported by National Key Programme for S&T Research and Development (Grant NO.: 2016YFA0400400), the National Natural Science Foundation of China (Grant NO.: 11975256), the National Natural Science Foundation of China (Grant NO.: 11535007), the National Natural Science Foundation of China (Grant NO.: 11775242), and the National Natural Science Foundation of China (Grant No.: 11675197).

TPC prototype integrated with UV laser beams

- The TPC detector with a drift length of 500 mm and a diameter of 380 mm, supported by four brackets is enveloped by a UV laser calibration system.
- UV laser system can generate 6 straight laser beams simultaneously at predefined positions along the TPC drift volume.

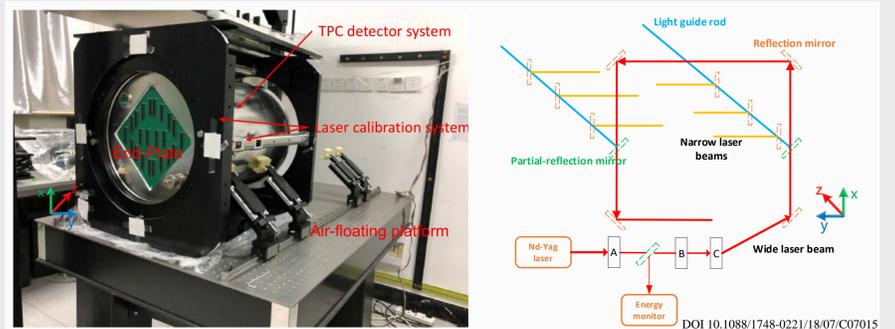


Figure 4: Picture of the TPC prototype integrated with UV laser beams (Left) and Principle of generating multiple laser tracks in the TPC prototype (Right).

Laser Track Reconstruction

- The middle four laser tracks, which are at $z=50$ mm, 160 mm, 270 mm, and 380 mm, are reconstructed successfully after event selection.

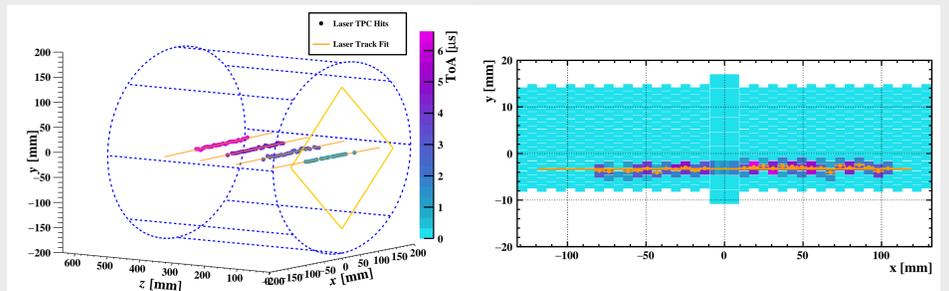


Figure 5: An event display of the reconstructed laser tracks. 3-D track fit for the middle four laser tracks (Left) and the projection in the x-y plane of the first laser track (Right).

Spatial Resolution & dE/dx resolution

- The spatial resolution can be less than $100 \mu m$ (@50 mm drift length) and the N_{eff} is (43.6 ± 6.2) without magnetic field.
- dE/dx resolution is determined to be $(8.9 \pm 0.4)\%$ for a single laser track (38hits). Extrapolation to CEPC TPC 220 hits, dE/dx resolution determined to be $(3.4 \pm 0.3\%)$.

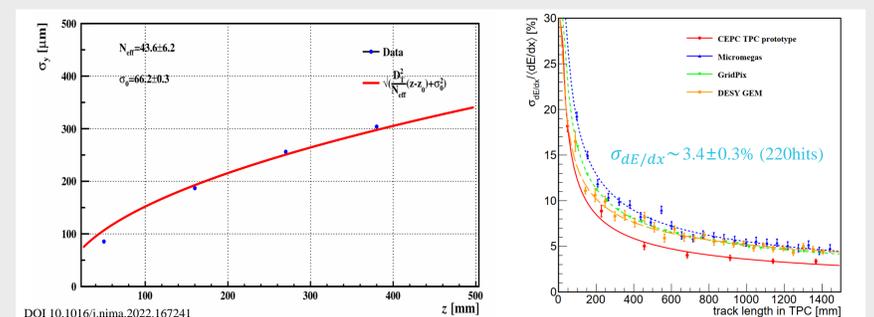


Figure 6: The spatial resolution as a function of drift distance (Left). The dE/dx resolution versus the track length in a pseudo-track of various lengths (Right).

Surface defect detection of silicon sensors



Shengbo Cao(曹圣博)¹, Changcheng Liu(刘长城)², Hanbing Liu(刘涵兵)³, Xuhao Yuan(袁煦昊)⁴, Lusen Zhang(张鲁森)⁴

1,3. Jilin University 2. Shandong University 4. Institute of High Energy 5. Hunan University

Introduction

The AMS experiment is a dark matter and antimatter searching experiment mounted on the International Space Station. AMS experiment will be upgraded in 2024 with a new layer of silicon detector layer (LO detector) which contains ~ **1000** silicon micro-strip sensors. The CMS experiment is a general purpose particle detector at LHC, CMS experiment will be upgraded with a new end-cap high granularity calorimeter (HGCAL), which contains ~ **27,000** silicon sensors and will be installed in the next long shut-down of LHC. Silicon sensors in both detectors need to be checked before installation. These large-scale applications bring about a challenge during the construction process of semiconductor detectors: **surface quality inspection**.

Why is surface quality inspection necessary?

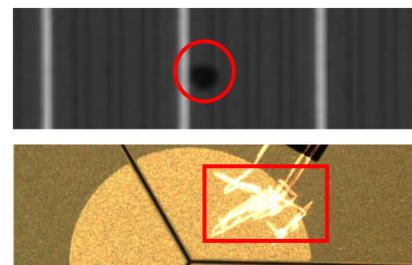
Surface damage → inadequate detector performance.

Why is surface quality inspection a problem in large-scale production processes?

The need to visually inspect the damage → a large number of images to be analyzed.

How to solve this problem?

Automatically identifying defects on sensors through machine vision methods.

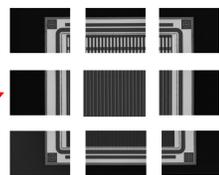
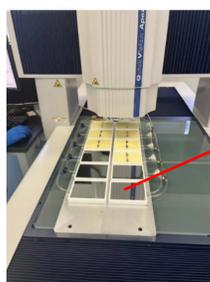


Methodology and Approach

AMS LO detector:

The First Step: Taking photos

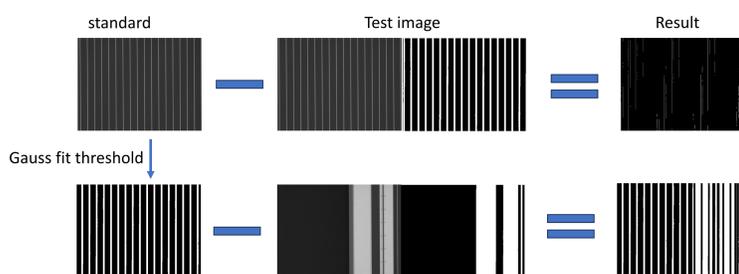
Automated capturing of SSD surface photos is performed on the Mitutoyo QV-X606 device. Each SSD scan takes ~ 1 hour (>4k photos) and is automatically completed overnight.



Each SSD photo will be divided into 9 categories, and a more detailed defect detection will be performed on each category.

The Second Step: Classification(**standard mapping method**)

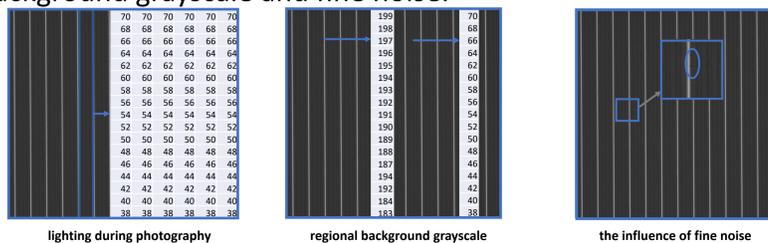
Select one image as the standard image for each category and subtract it from the image to be processed for classification.



The Third Step: Defect detection

The original OpenCV functions have low accuracy in defect recognition, so we propose a highly accurate "**strip-by-strip recognition method**".

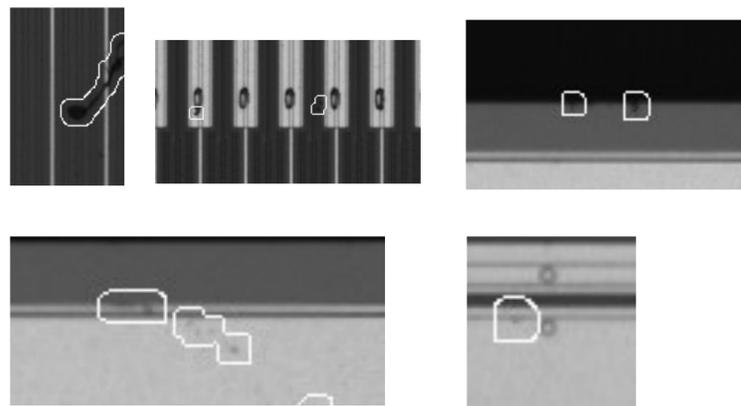
But high-precision recognition also represents more influencing factors, such as the influence of lighting during photography, regional background grayscale and fine noise.



The above influencing factors can all lead to inaccurate threshold results.

Using different methods for different situations can yield good results.

What is the **final result** obtained?



CMS HGCAL:

What is the new problem?

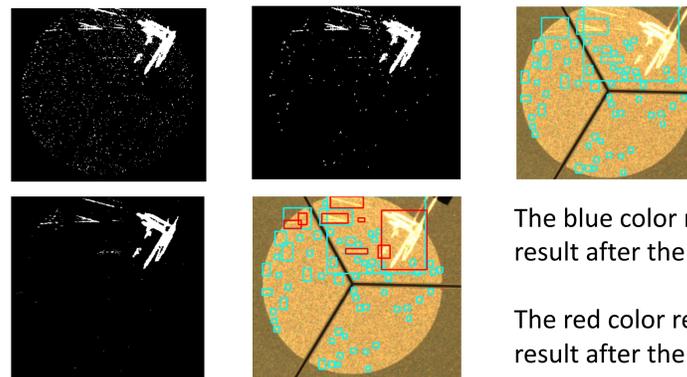
Noise handling. Due to severe noise and shallow traces, traditional methods of noise processing have become ineffective.

	color	gray	binary
scratches			
noise points			

How to solve the problem?

The "**two-step screening**" method is used. The first judgment is performed to eliminate some noise and determine the region for the second judgment. The second judgment employs multiple criteria to differentiate between noise and traces.

What is the **final result** obtained?



The blue color represents the result after the first screening.

The red color represents the result after the second screening.

Summary and Prospect

• Summary:

Our work aims to achieve recognition of surface defects on detectors through machine vision, in order to free up previous human investment in this area. Through the development of machine vision programs, it is now possible to achieve defect detection for AMS and CMS, and it also has good applicability for defect identification on other detectors(such as CEPE).

• Prospect:

In the future, machine learning will be introduced to achieve more intelligent and versatile visual detection, while also incorporating detection of more complex areas (containing characters or irregular graphic areas) that cannot be recognized at present. We will also try to develop a fault monitoring program for detector processing and operation in the future.

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Prospect of $t\bar{t}$ Analysis at CEPC

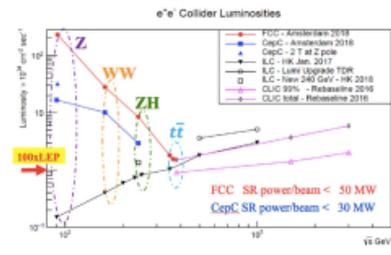
Mustapha Biyabi, Siya Feng, Jiabao Gong, Shudong Wang, Xiaoxu Zhang, Yaquan Fang, Gang Li, Hongbo Liao, Lei Zhang

Introduction

The versatility and capabilities of CEPC make it an exciting prospect for advancing our understanding of particle physics.

CEPC provides an ideal environment for studying $t\bar{t}$ processes at $\sim 360\text{GeV}$. By precisely measuring the properties of $t\bar{t}$ system, valuable insights into the top electroweak couplings can be gained.

Moreover, it is of significant importance for Higgs complementary measurements and BSM searches.



Top Electroweak Couplings

The importance of studying top electroweak couplings:

- Setting constraints on new physics scale
- High sensitivity to BSM physics
- Test of composite Higgs models

At the CEPC, the $t\bar{t}(V=V, Z)$ couplings could be probed directly through the top pair production process.

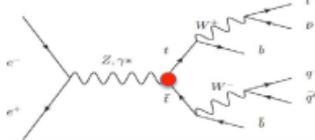
The most general Lorentz-invariant vertex function describing the interaction of a neutral vector boson V with two on-shell top quarks can be written:

$$\Gamma_{t\bar{t}V}^{\mu} = \frac{i}{2} \left\{ (A_V + \delta A_V) \gamma^{\mu} - \gamma^{\mu} (B_V + \delta B_V) \right\} + \frac{(p_1 - p_2)^{\mu}}{2m_t} (\delta C_V - \delta D_V \gamma_5)$$

The energy and angular distributions of the decay products, in particular, the charged lepton and the b-quark, are powerful tools to disentangle and access different components of the $t\bar{t}$ and $t\gamma$.

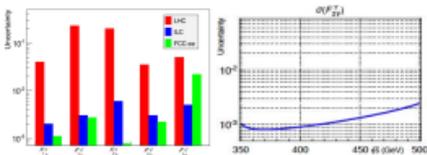
For the interaction between top quarks and neutral vector bosons, there are two observables can be measured:

- Cross-section: to measure the strength of the interaction.
- FB asymmetry: can be calculated by measuring the angular distribution of the charged leptons, providing insights into the interaction.



The present LHC precision in measuring top electroweak couplings is not very constraining. However, similar to the FCC-ee scenario, CEPC could reduce the statistical uncertainties by orders of magnitude.

With conservative assumptions on lepton identification, b-tagging efficiencies, and lepton angular and momentum resolutions, the estimated precisions at FCC-ee are at the order of 10^{-2} to 10^{-3} at the energy of 365 GeV.



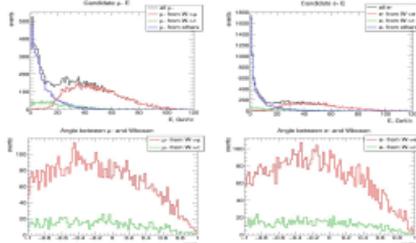
Analysis at CEPC

Detailed studies about selecting and reconstructing $t\bar{t}$ events at CEPC are in progress.

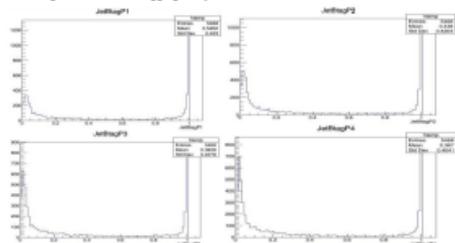
The top EW coupling can be measured by studying the energy-angle distribution of the lepton from the semileptonic decay:

$$e^+e^- \rightarrow t\bar{t} \rightarrow b\bar{b}q\ell^+\ell^-(\ell = e, \mu)$$

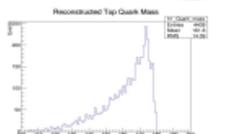
The figures show energy and angle distribution of lepton(muon and electron) in this decay:



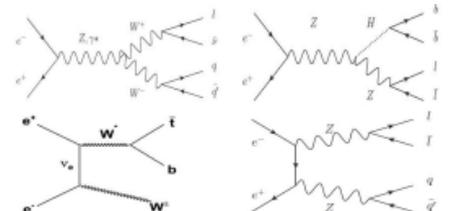
And these figures show the Blagging of 4 jets:



Reconstruction of top quark mass is tried but there is still a long tail:



And background samples (diboson and single top) are in production:



To tag the semileptonic $t\bar{t}$ events, background rejection is performed by using discriminating variables, and muons and electrons originating from tau decays are excluded.

Summary and Future Perspectives

Studying the top EW couplings is highly significant due to its sensitivity to new physics. This measurement can be performed at CEPC, and it is expected to achieve satisfactory precision.

Regarding the future perspectives of $t\bar{t}$ analysis:

- Optimize event selection and reconstruction to improve the analysis.
- Improve the analysis including fully leptonic final states.
- Improve the analysis including b quark energy-angle distribution