国家重点研发计划

高能环形正负电子对撞机关键技术研发和验证

课题2：硅径迹探测器关键技术验证

报告人：　　梁志均
项目负责人：　João Guimarães da Costa
项目承担单位：中国科学院 高能物理研究所

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

南京大学

国家重点研发计划

R&D and Verification of Key Technologies for a High Energy Circular Electron-Positron Collider

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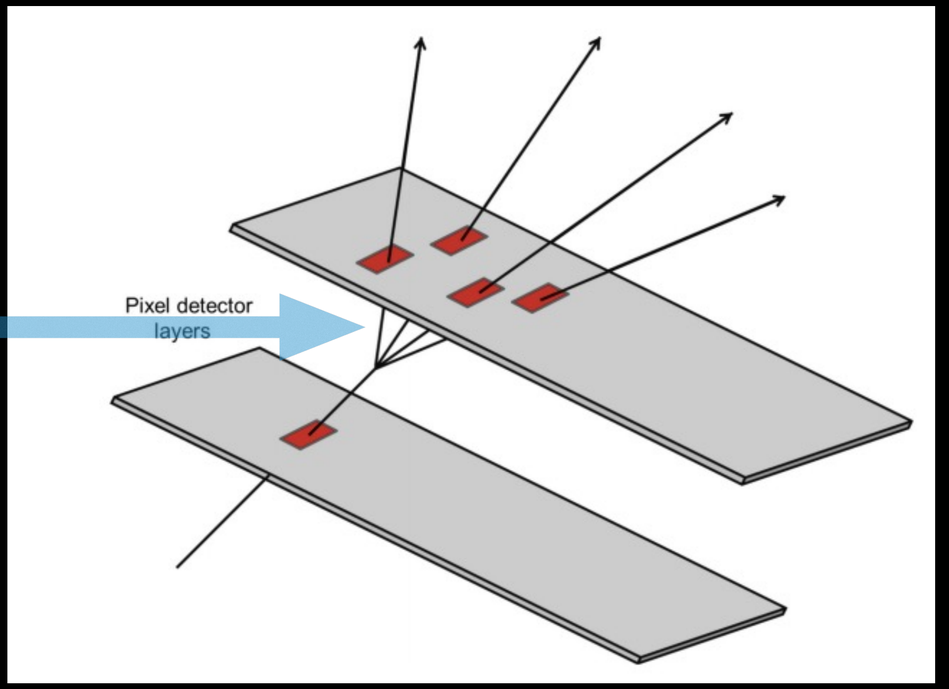
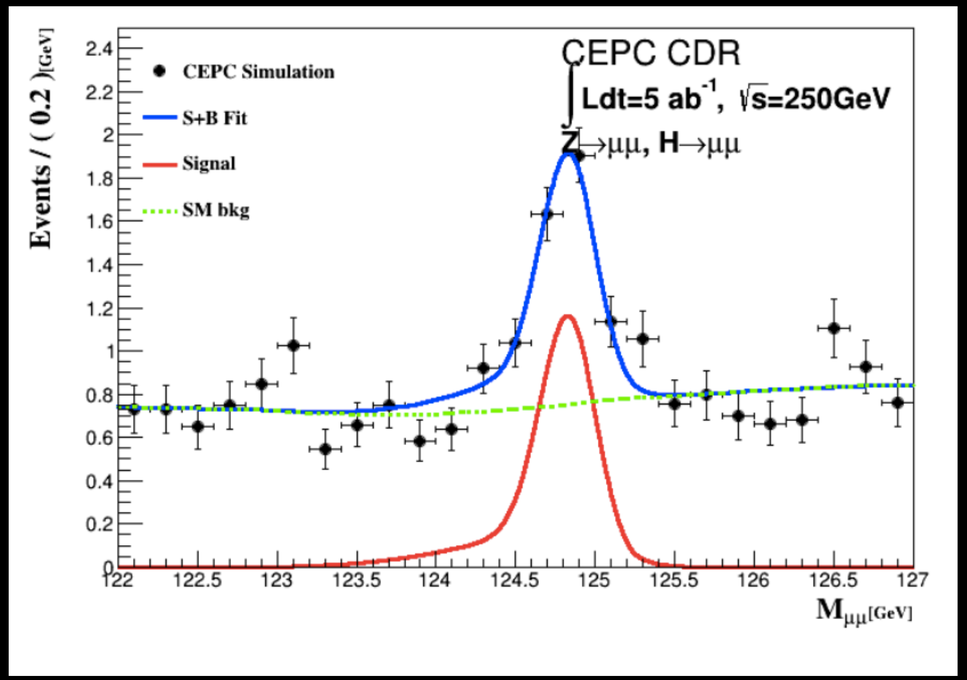
Vertex detector: Physics goal

- Higgs precision measurement
  - H → bb precise vertex reconstruction
  - H → μμ (precise momentum measurement)

Need tracking detector with high spatial resolution



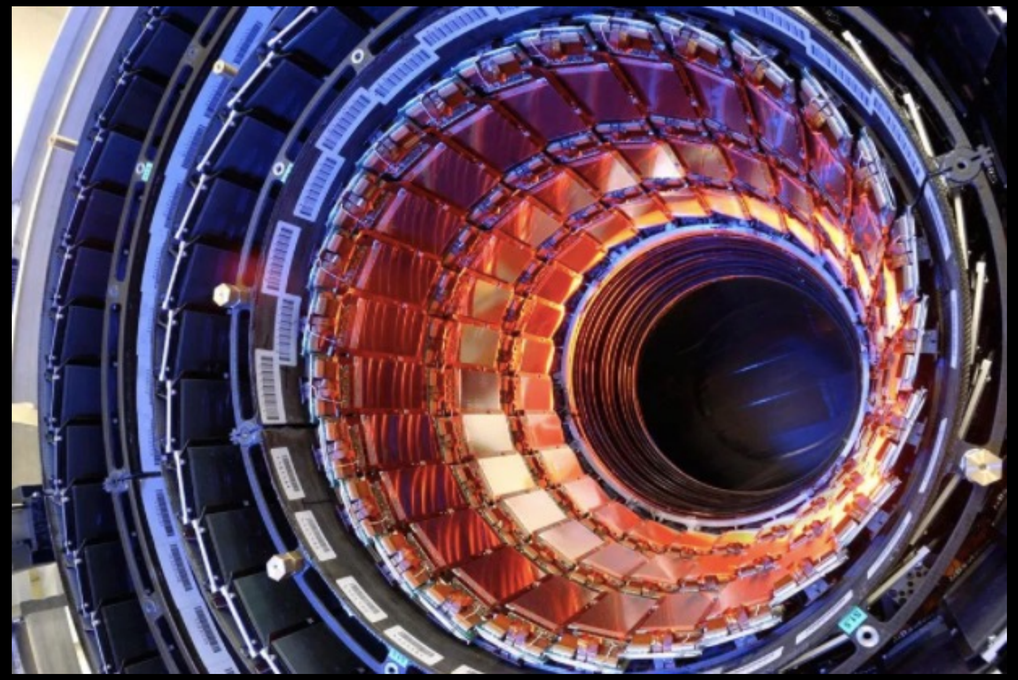
- Main technology
  - High spatial resolution technology → pixel detector
  - Radiation resistance technology



MOST2 vertex detector R & D: Research Goal

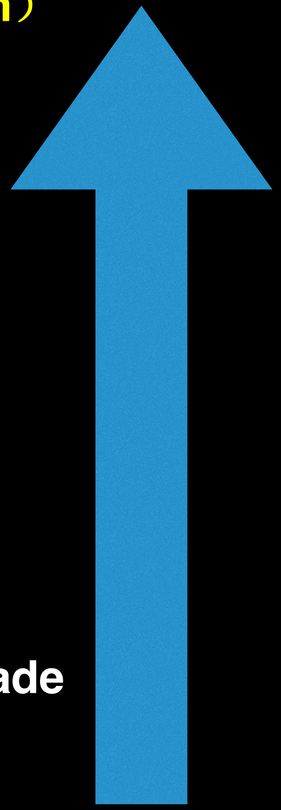
- Produce a world-class vertex detector prototype
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (>1 MRad)
- Key goal
  - Develop the know-how in China to be such advanced detectors

Typical cost of pixel detectors: 350-700 M RMB



Key ingredient:

Full size sensor/ASIC (2-4 cm²)



Achievement Presentation and Assessment Methods

Silicon Detector

考核指标[2]				
指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	考核方式(方法)及评价手段[4]
硅径迹探测器原型机的空间分辨率	无	研制出小型传感器芯片，像素单元尺寸小于或等于25微米 ×25微米。	3-5微米	同行专家评审。(通过束流实验，离线分析数据获得空间分辨率。该测试结果写入原型机设计与测试报告，以供同行专家评审)
所设计的抗辐照硅传感器能承受的总剂量	无	完成传感器的初步设计，通过仿真初步验证其抗辐照性能	1 MRad	同行专家评审 (提供传感器的设计与测试报告供专家评审)

Assessment index

Spatial resolution

- Final : **3-5 μm** resolution in **Beam test**

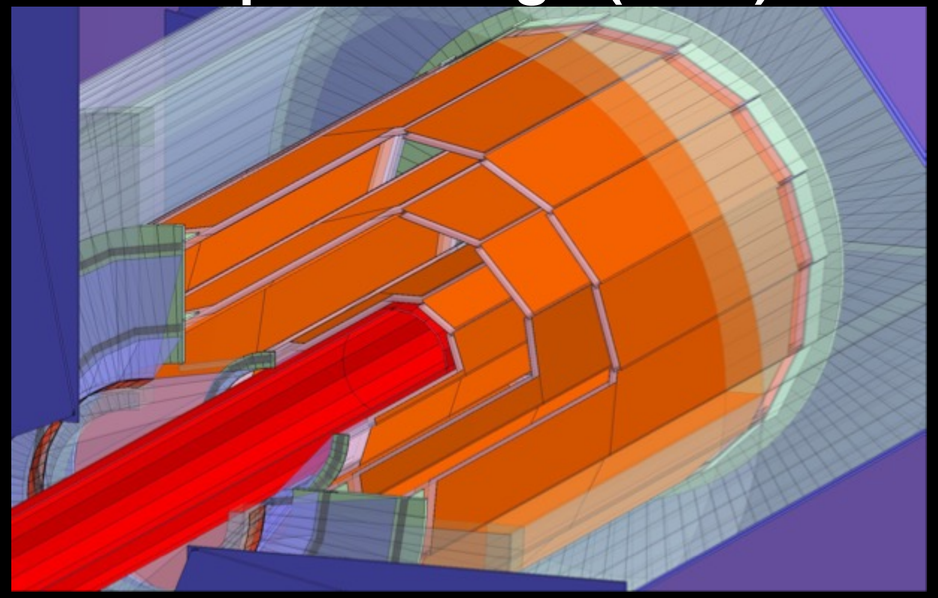
Radiation hardness

- Final : Total ionization dose **>1 Mrad**

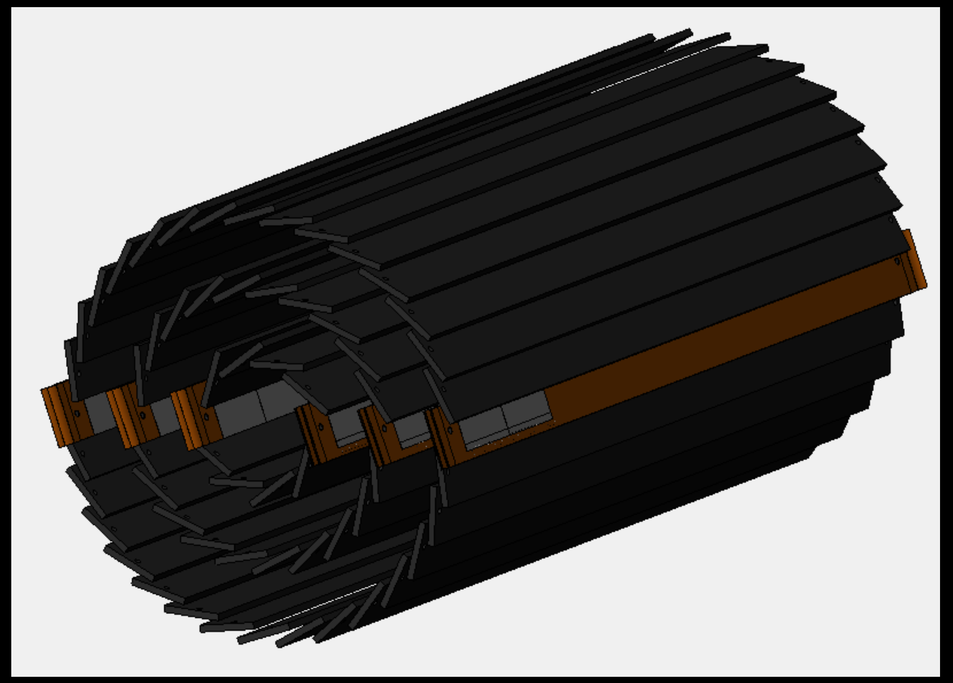
Vertex detector prototype structure optimization

- Based on CEPC vertex detector conceptual design → Three double-layer barrel detector
  - This project plan to prototype the important part of vertex detector (CDR design)
  - The cost for the full vertex detector is high (eg: ~50 M CHF for ATLAS ITk pixel detector)
    → not necessary for technology R & D
- Optimize the geometry based on real ASIC and electronics dimension
  - Optimize geometry based on its physics performance from simulation
  - Engineering design of prototype structure

CEPC Vertex detector
Conceptual design (2016)

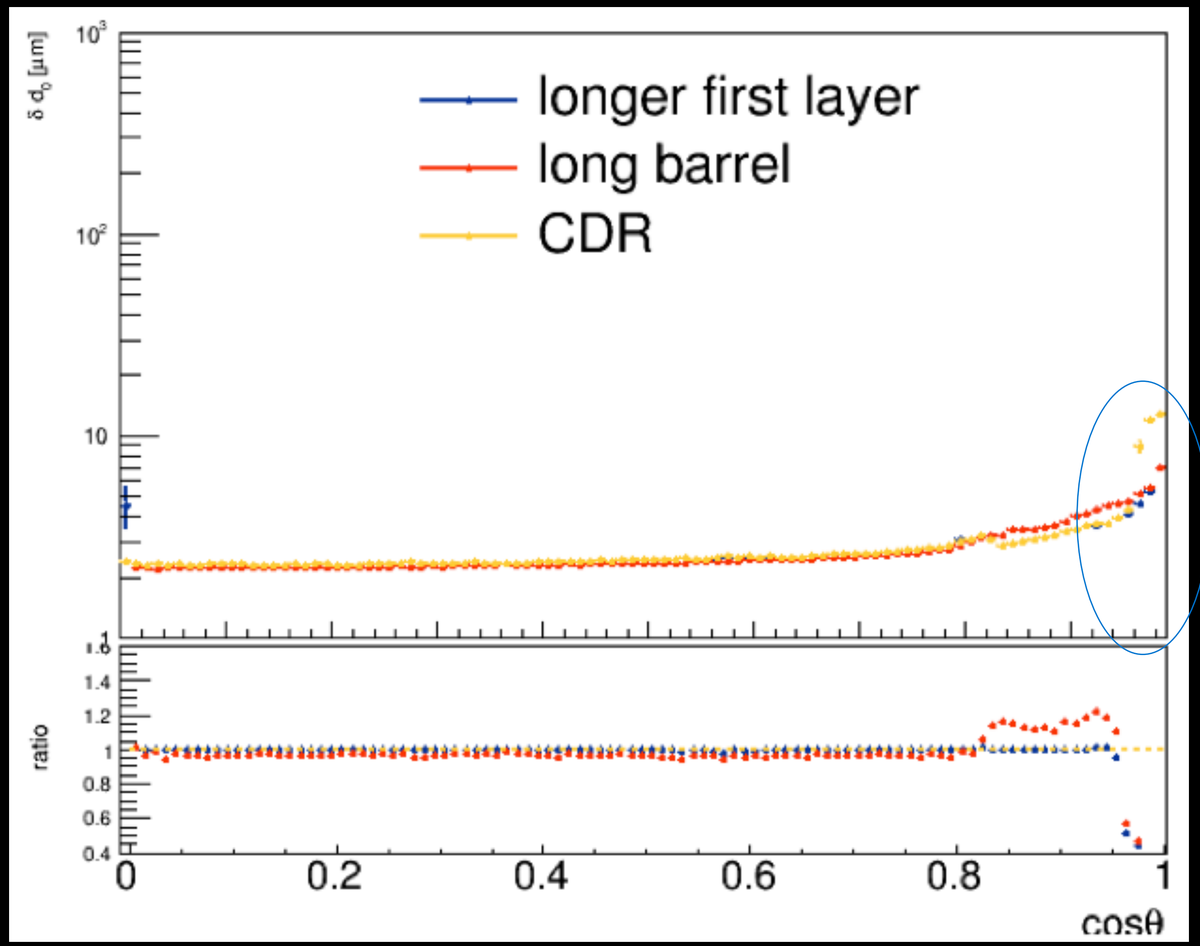


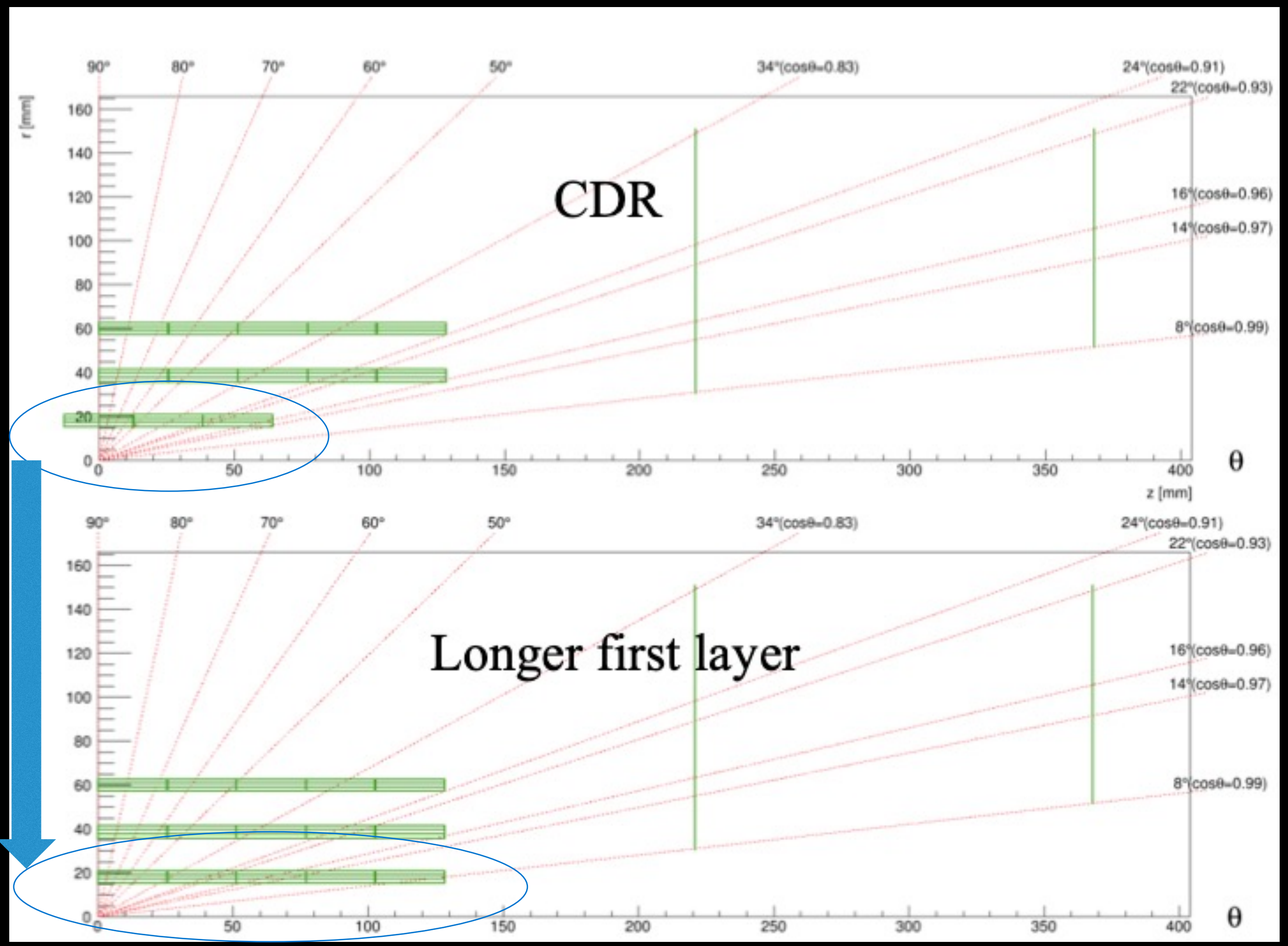
This project
Vertex detector prototype design



Vertex detector prototype structure optimization

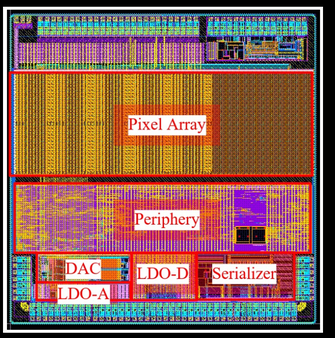
- One example of detector geometry optimization based on simulation :
  - Increase the length of the inner layer of the detector
  - To improve the impact parameter resolution for forward tracks

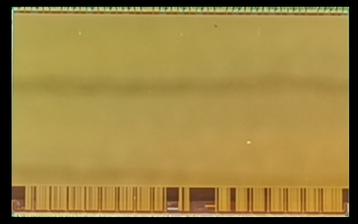




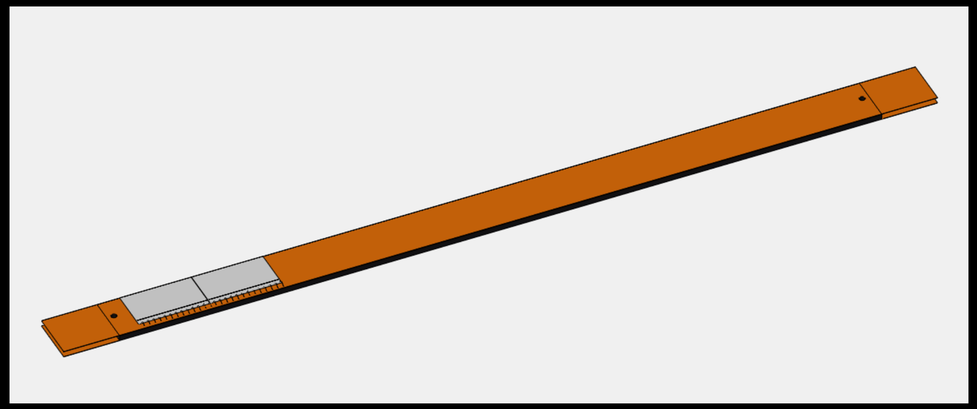
Overview of MOST2 vertex detector R & D

CMOS imaging sensor prototyping

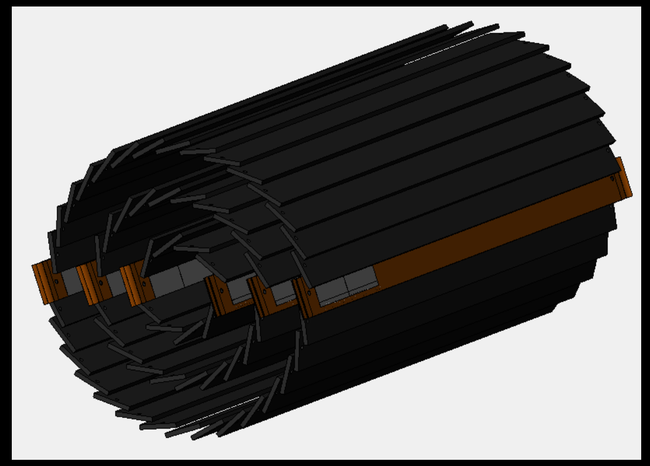


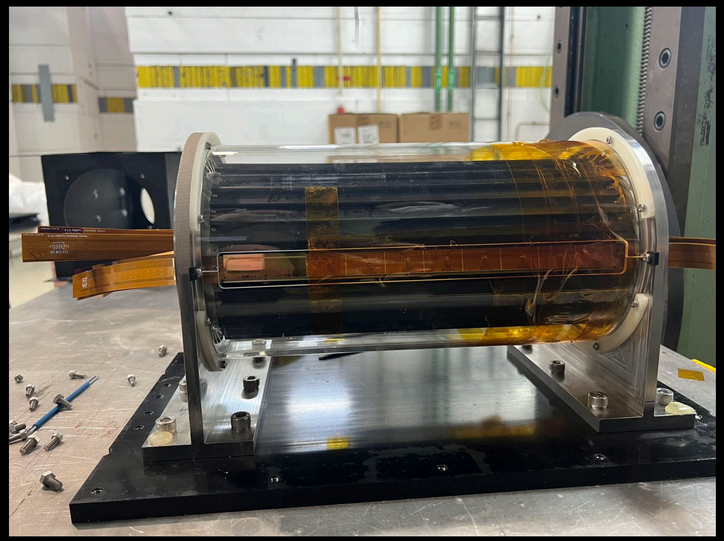


Detector module (ladder) Prototyping



Vertex detector Prototype for beam test





- Design CMOS imaging sensor chip
- Detector Module prototyping
- Vertex Detector assembly and testbeam

Research Team in MOST2 silicon project

4 institutes

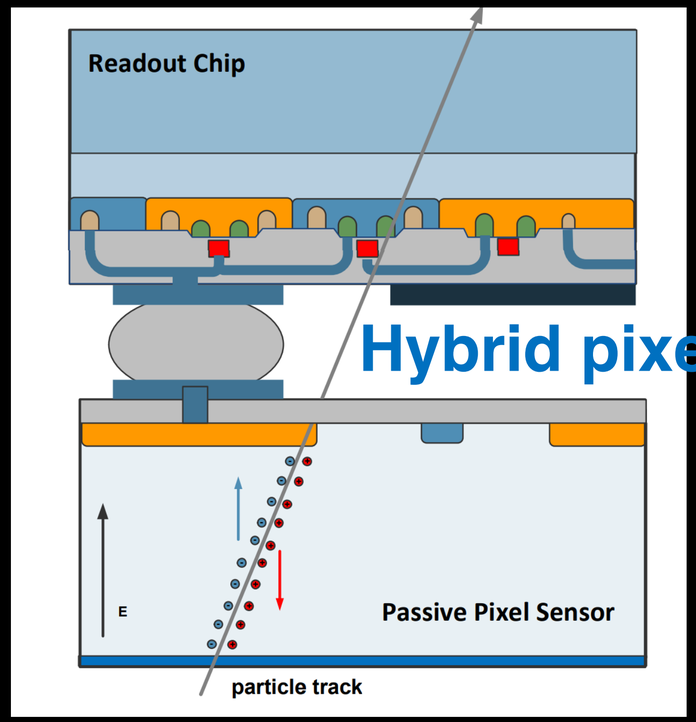
课题2：**IHEP -** 中国科学院高能物理研究所
SDU - 山东大学
NJU - 南京大学
NWU - 西北工业大学

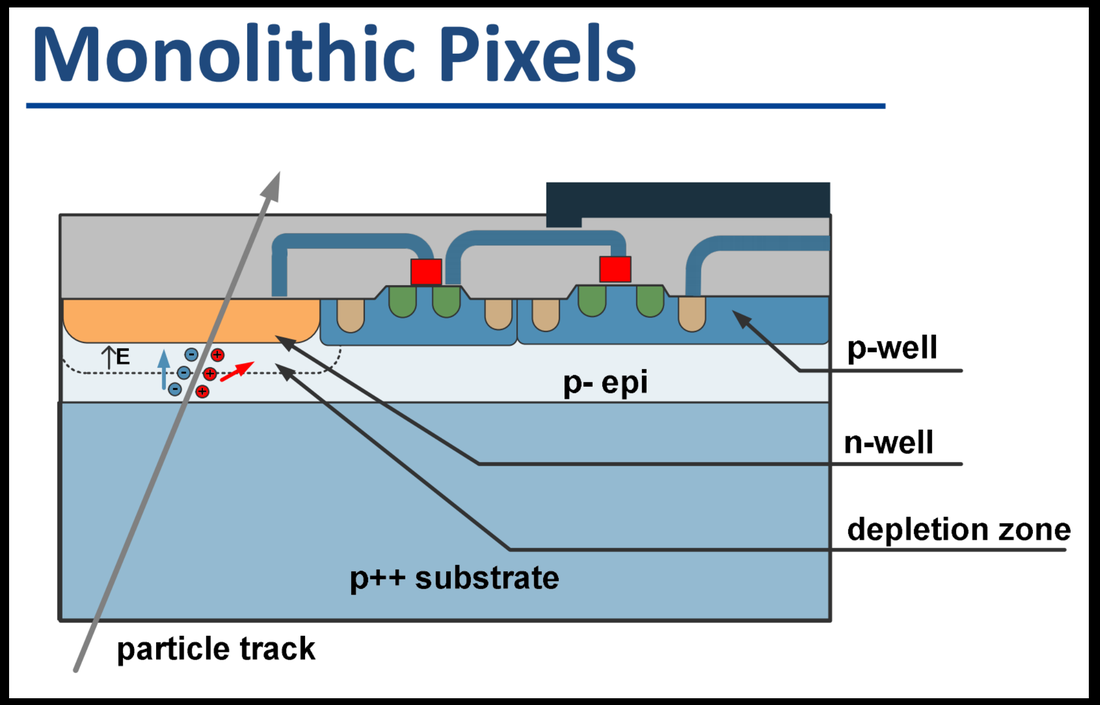
Fund: 1200万

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning
CCNU/IFAE	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
SDU	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
NJU	Irradiation, test beam organization

CMOS Monolithic pixel sensor

- Conventional Hybrid pixel technology at Large Hadron Collider
  - Need to bump bonding with readout ASIC
  - Typical pixel size >=50μm, much more difficult for bump bonding with smaller pixels
- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - Sensor and ASIC high integrated in one chip, easier for detector assembly
  - Can have compact structure in pixel array design.
    - Pixel size can be reduced to 25um → can achieve better spatial resolution





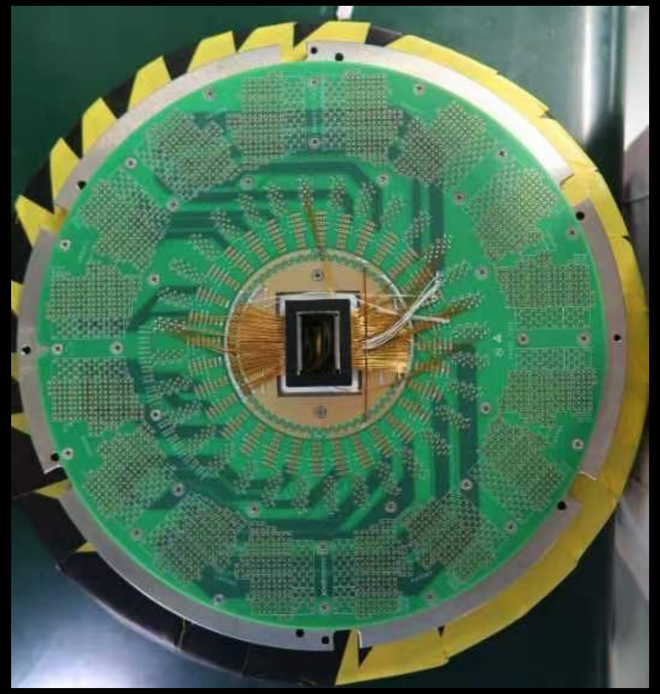
CMOS Sensor chip R & D

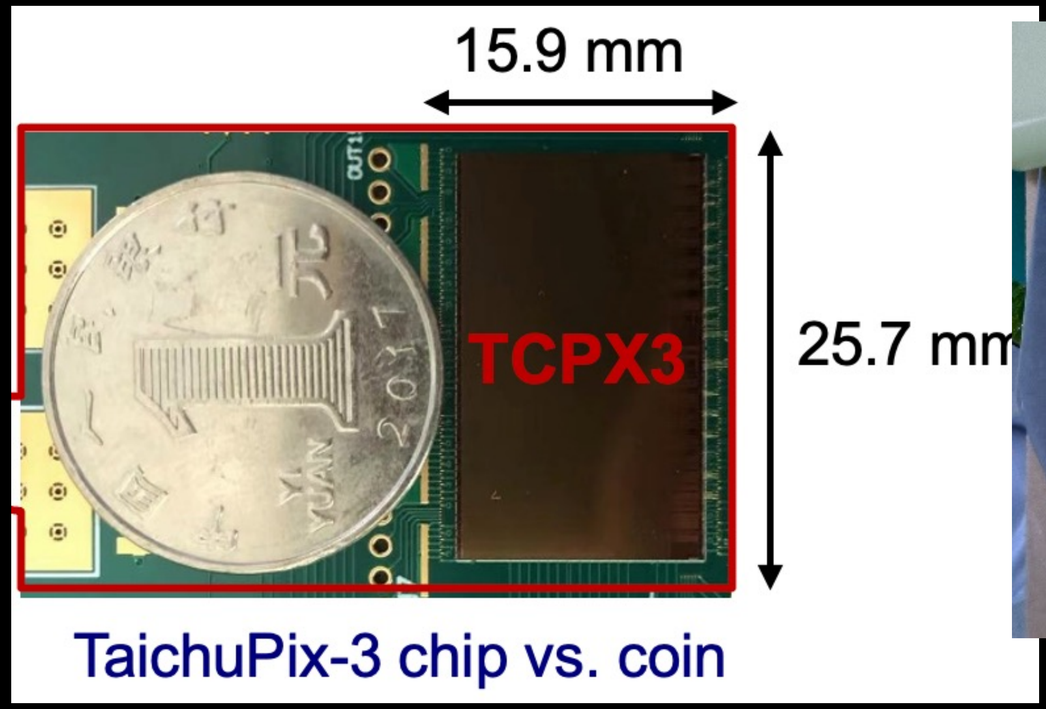
- The existing CMOS monolithic pixel sensors can't fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - Radiation tolerance **(per year): >**1 Mrad
  - High readout speed -> for high luminosity CEPC Z pole running

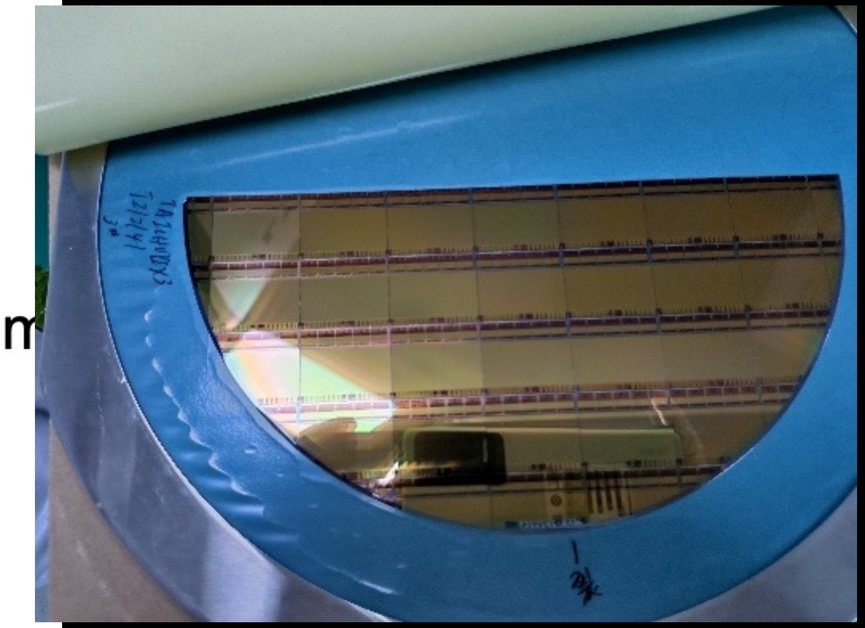
	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

Full-size TaichuPix3 prototyping (engineering run)

- **Developed the first full-size CMOS pixel sensor for particle detector in China**
  - **Full size 1024×512 Pixel array, Chip Size：15.9×25.7mm**
    - **25μm×25μm pixel size → high spatial resolution**
    - **Process: Towerjazz 180nm**
  - **Fast Periphery digital readout , high-speed data interface**

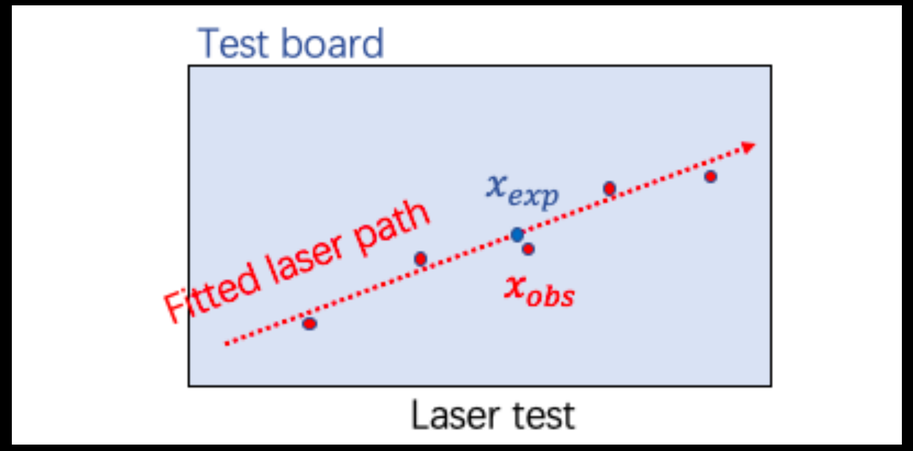




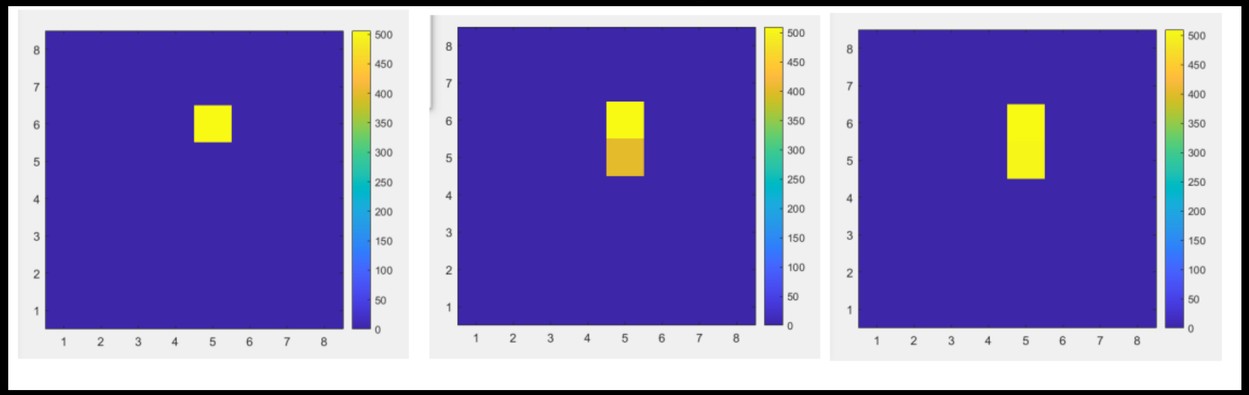


Spatial resolution measured by Laser tests

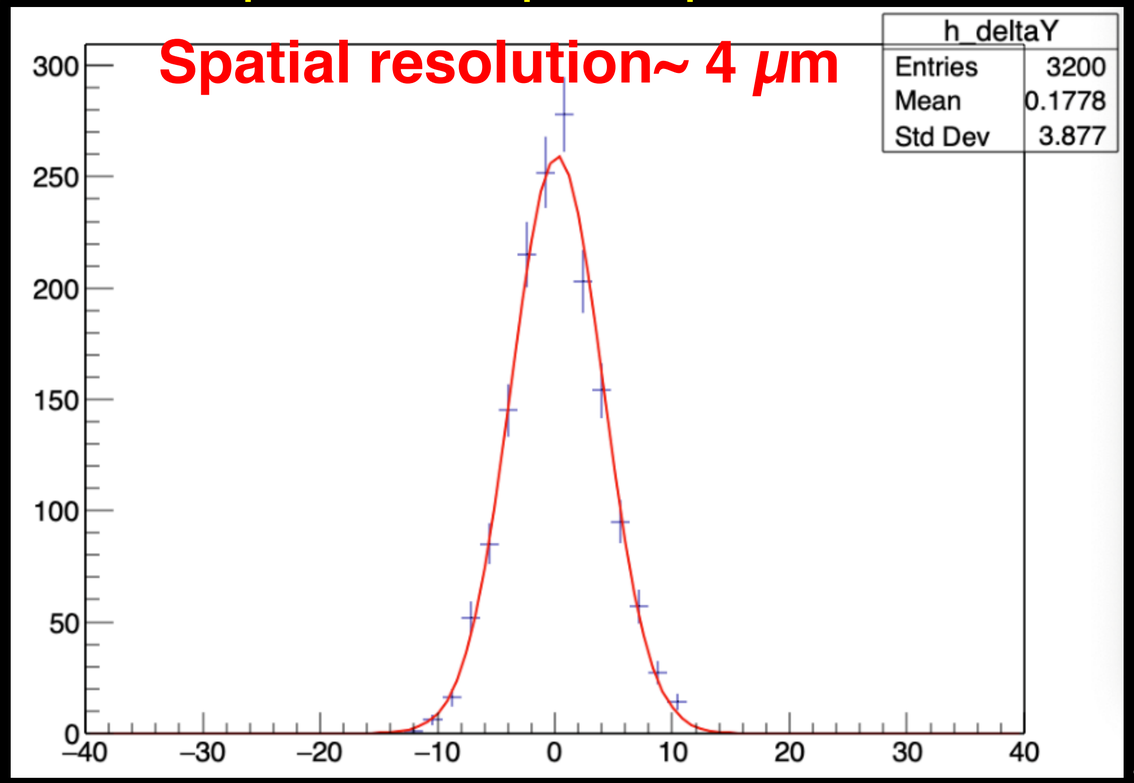
- Spatial resolution of Taichu2 can reach ~4 μm in laser tests
  - Use high precision 2D movable station in laser scan
  - Laser was scanning with a step of 1 μm



Laser beam spot during scan



Residual distribution
(measured position – expected position from station)

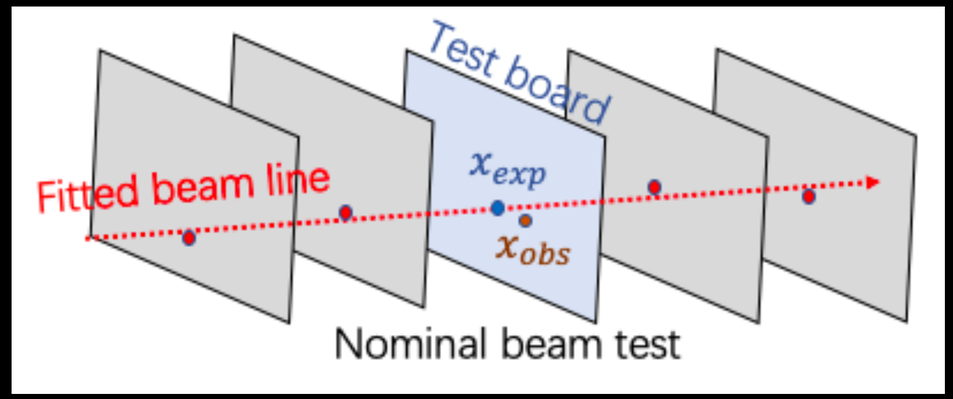


Spatial Resolution in X and Y direction

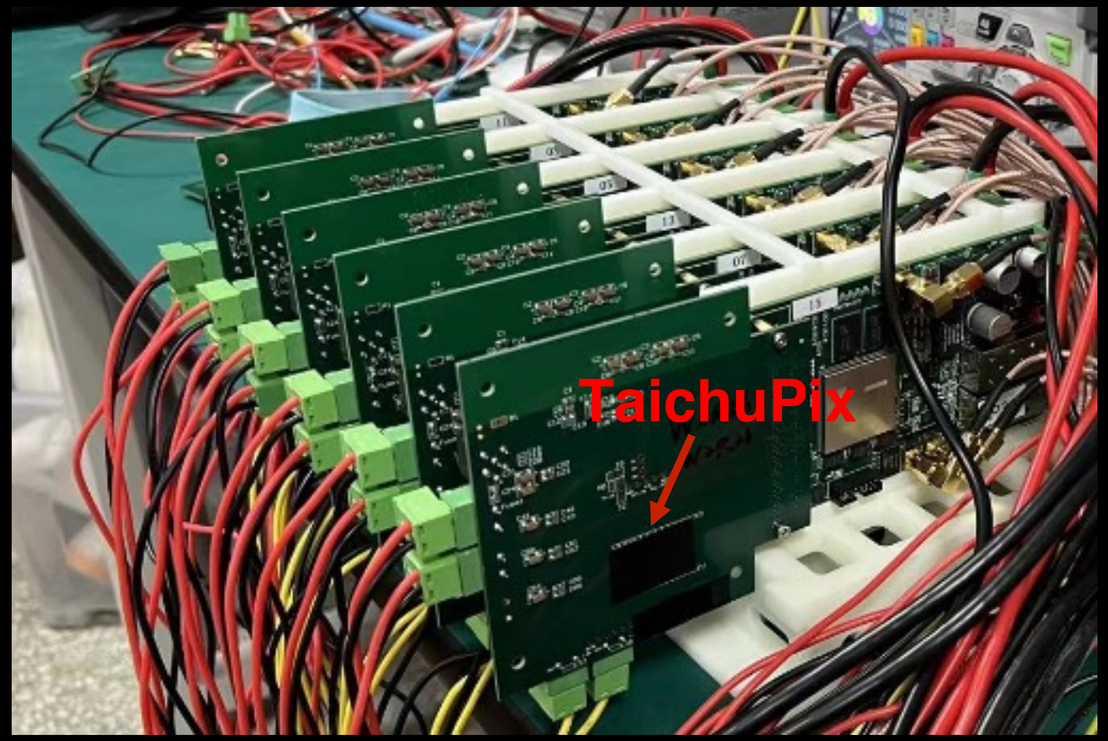
	Resolution (μm)	Overall error (μm)
X	3.98	±0.23
Y	4.12	±0.25

Spatial resolution measured by testbeam

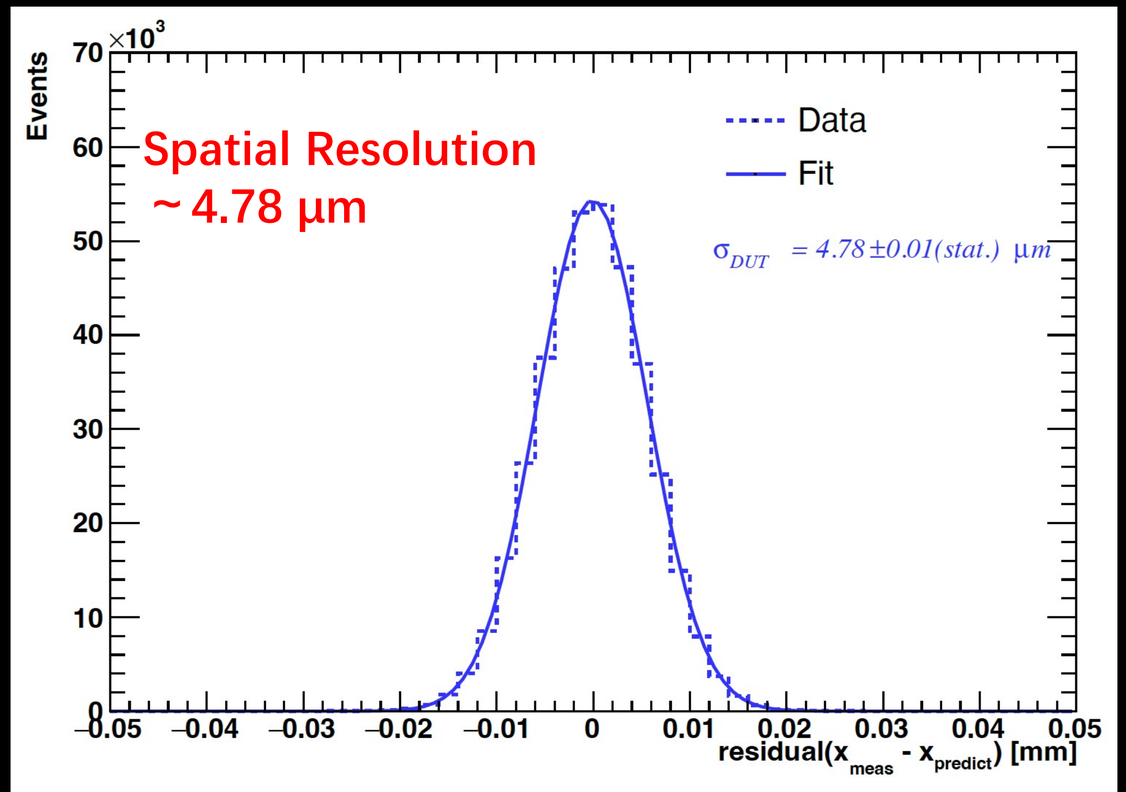
- The 6-layer of TaichuPix-3 telescope built
  - Tested at DESY with 4-5 GeV electron beam, 1kHz rate
  - One layer of TaichuPix used as Detector-Under-Test (DUT)
  - Other five layers as beam telescope used for track fitting
  - Spatial resolution of TaichuPix reach 4.78 μm
    - Reach the goal of the project (3-5 μm)



Setup for Taichupix beam telescope



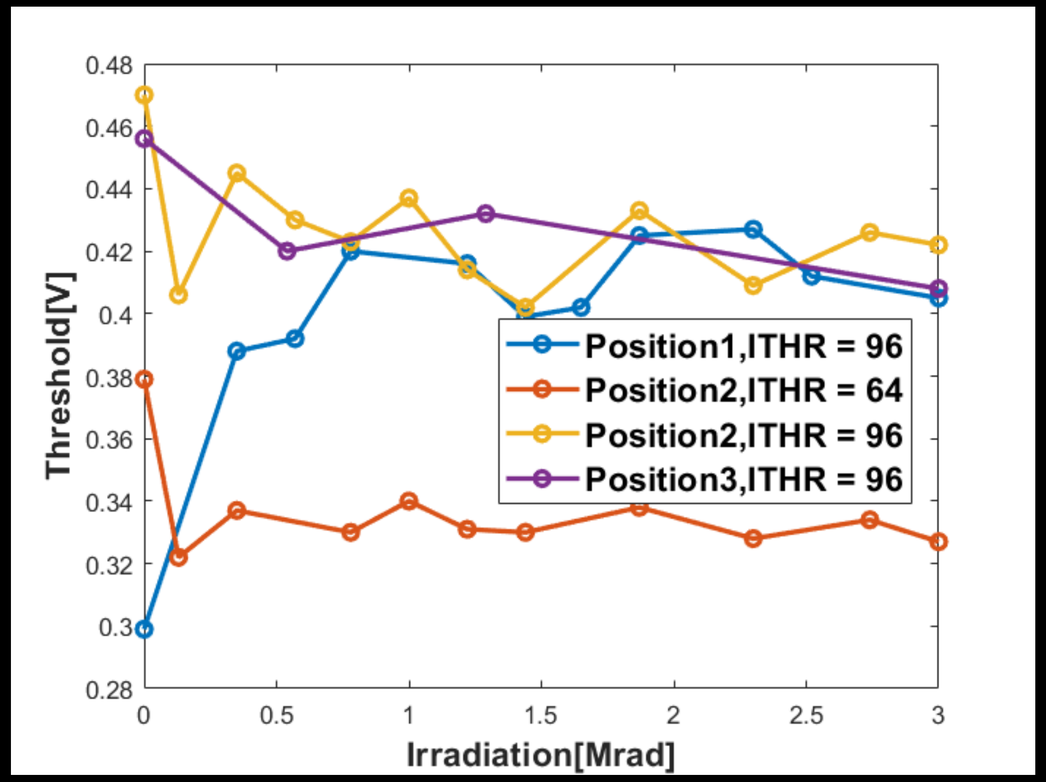
Residual distribution
DUT measured position – expected position from track



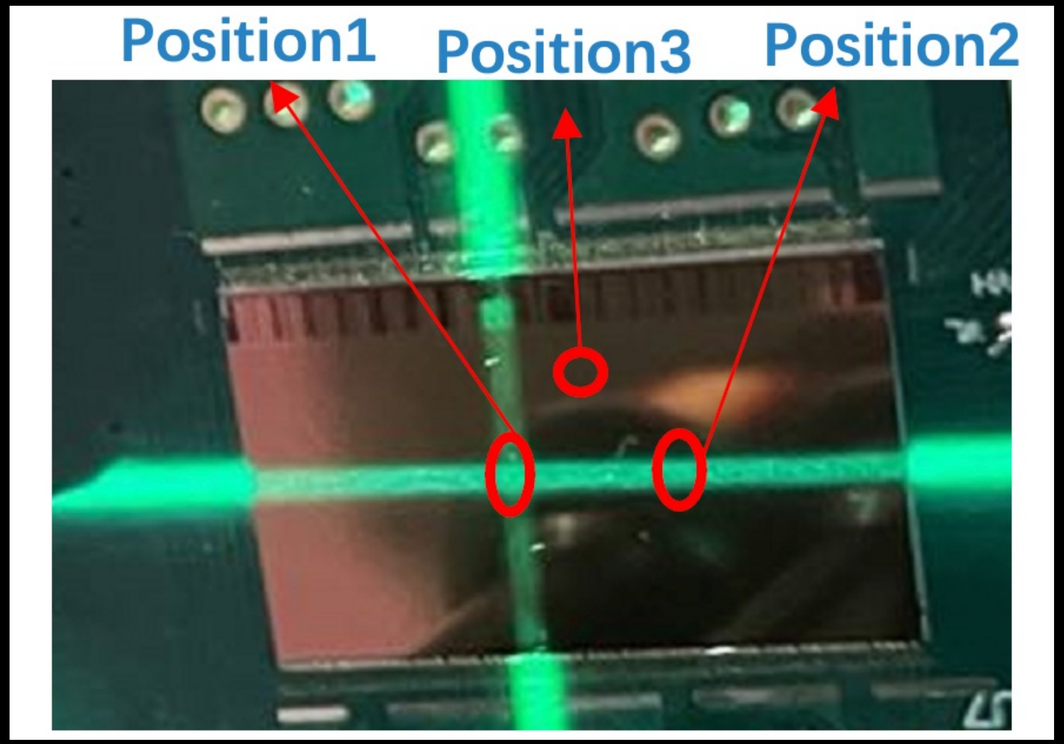
Radiation tests

- Taichupix3 was irradiated in-situ tested up to 3 Mrad
  - Normal chip functionality and reasonable noise performance
  - Reach the goal of the project: radiation hardness on total ionization does >1 Mrad

Taichupix3 irradiation test
Pixel threshold vs. TID



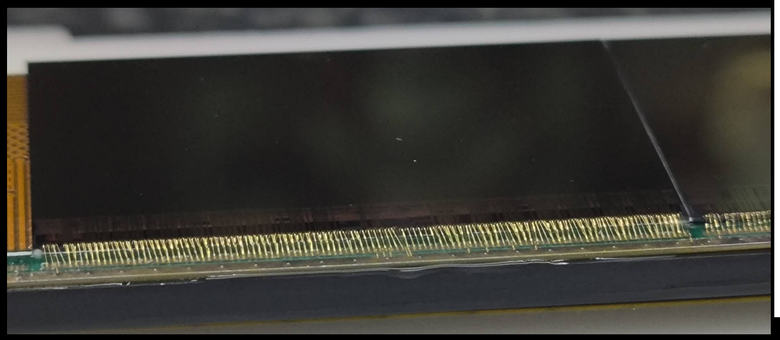
TaichuPix-3 irradiated at Synchrotron radiation beamline (12 keV X-ray)



Detector module (ladder) R & D

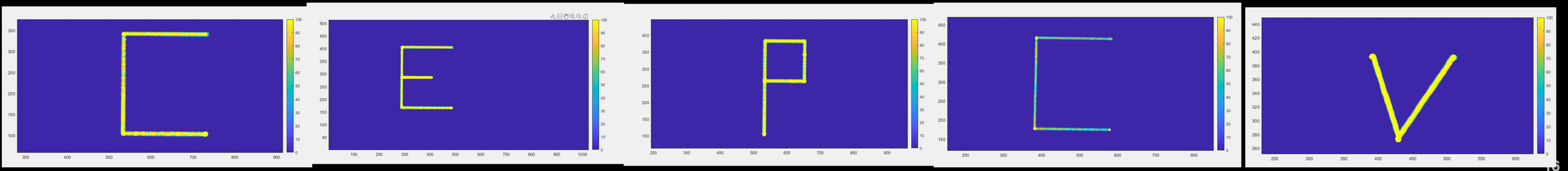
- Detector module (ladder)= sensors + support structure+ flexible PCB+ control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control , power, ground will be handled by control board through flexible PCB

Taichupix chip wire bonded on FlexPCB



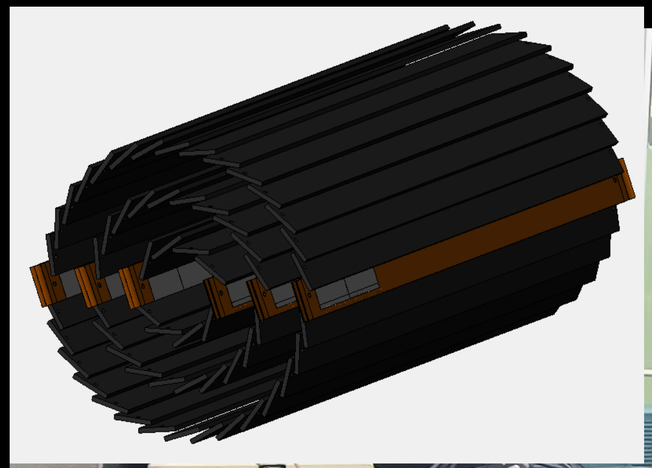
Full ladder test setup

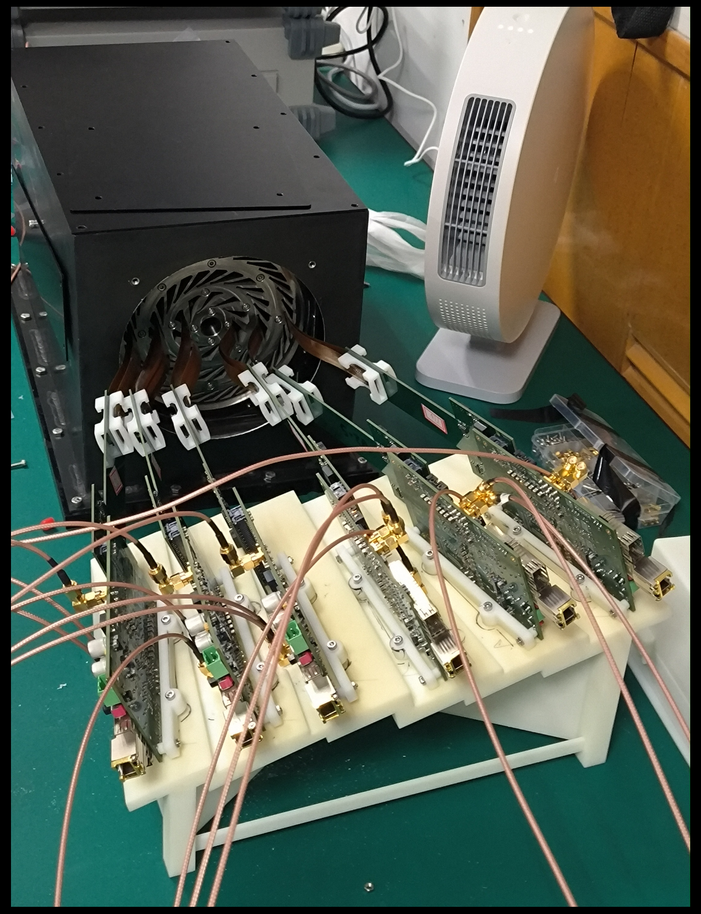
Laser tests on Taichupix chip on full ladder
（"CEPCV" pattern by scanning laser on different chips on ladder）



Vertex detector Prototype assembly

- Six double-side ladders installed on the vertex detector prototype
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype

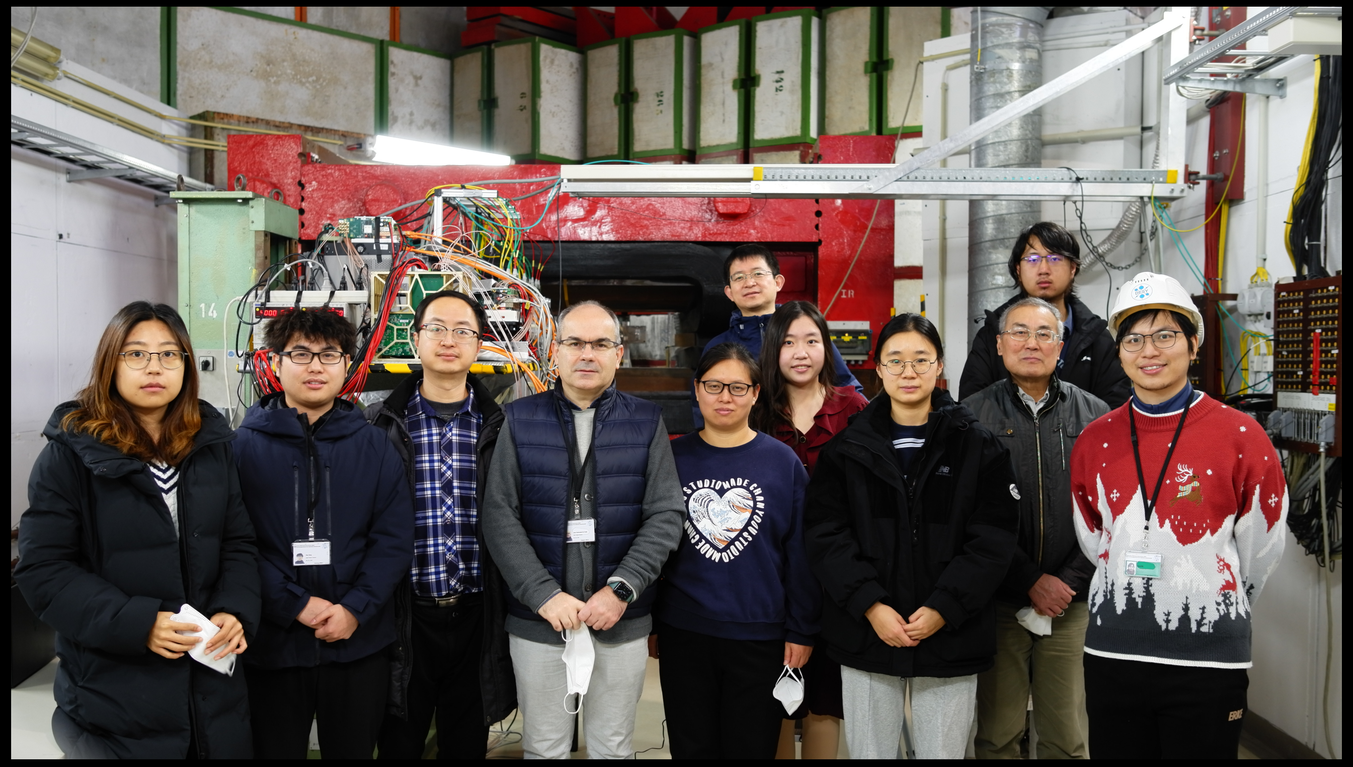




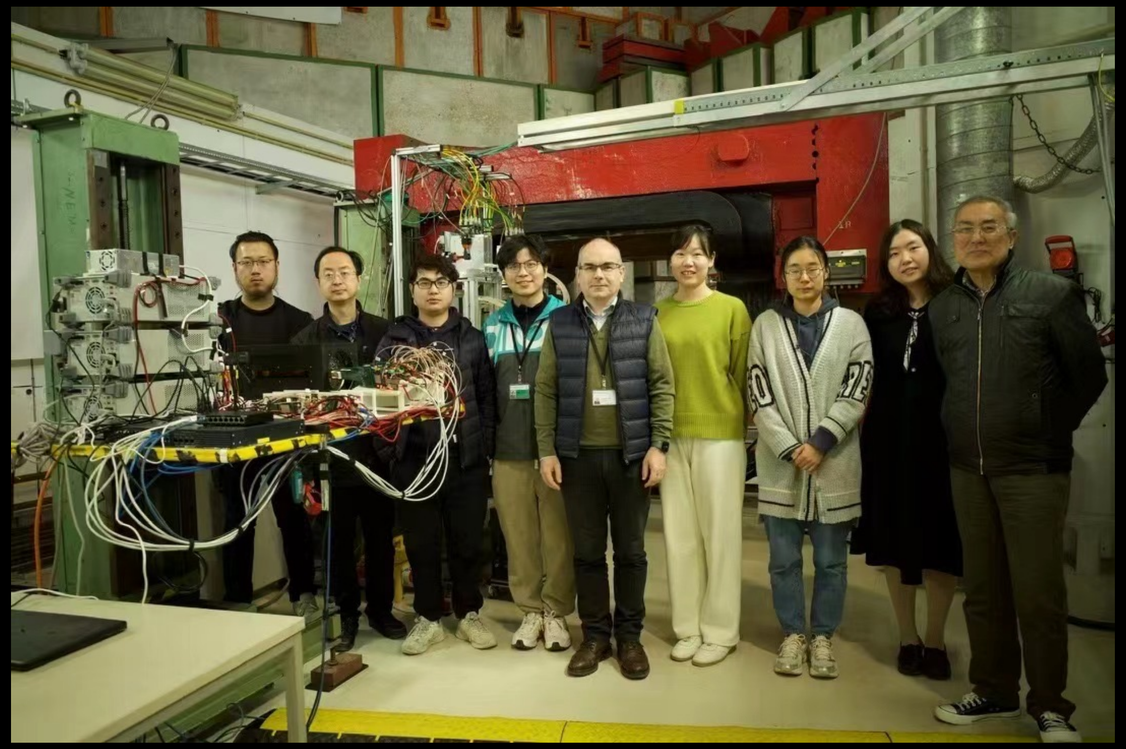
Test beam @ DESY

- 2nd testbeam: April 11-23 2023 DESY test beam in Germany (4-6GeV electron)
  - Vertex detector prototype testbeam
- 1st testbeam: Dec 12-22 2022 DESY test beam in Germany (4-6GeV electron)
  - TaichuPix Beam Telescope testbeam

2022 DESY test beam



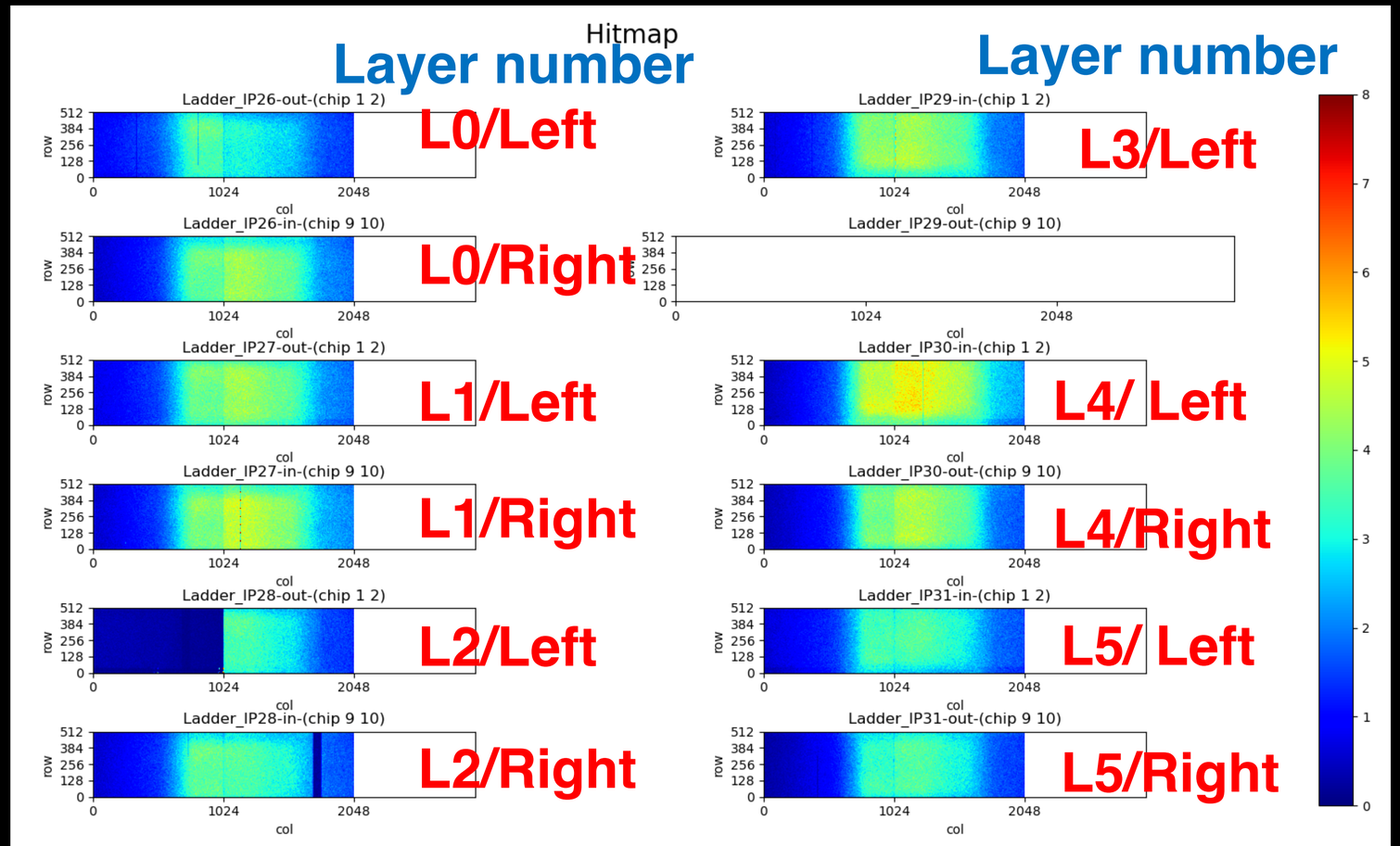
2023 DESY test beam



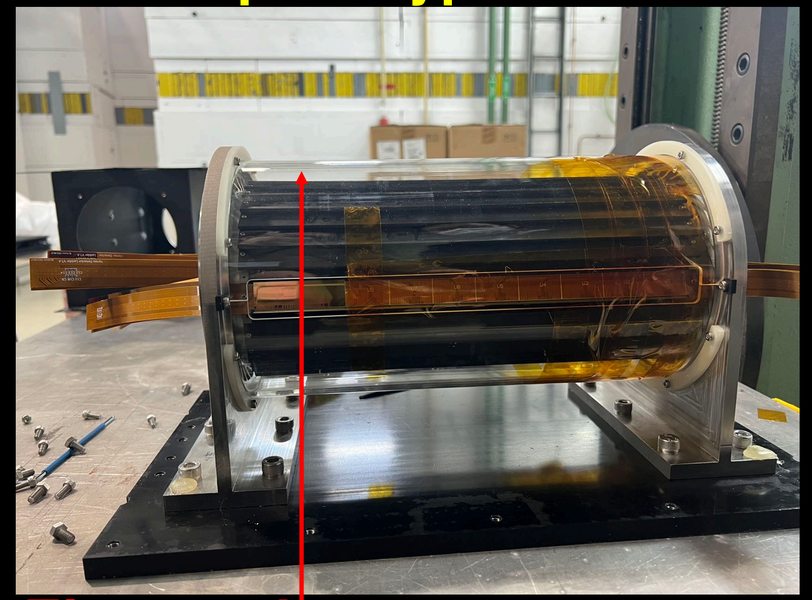
Test beam @ DESY for detector prototype

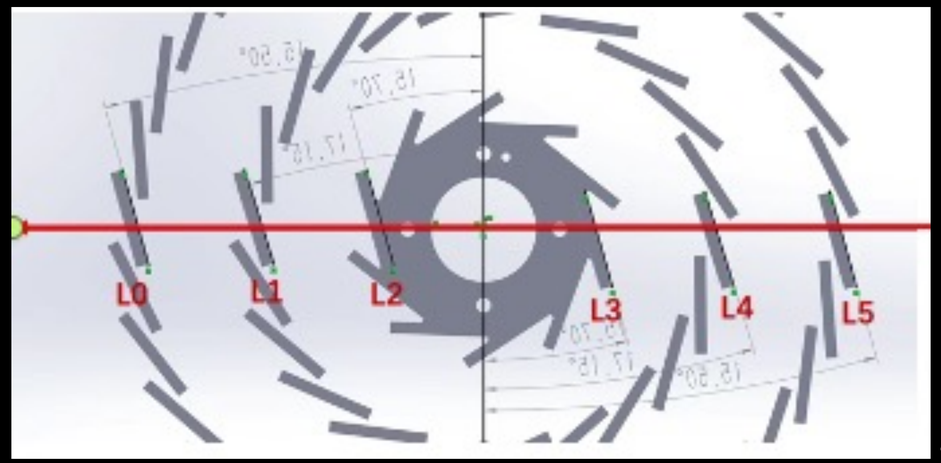
- Six double-side ladders installed on the vertex detector prototype for DESY testbeam
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype
  - Beam spot (~2×2cm) is visible on detector hit map
  - Record about one billion tracks in two weeks

Hit maps of all layers taichupix on prototype



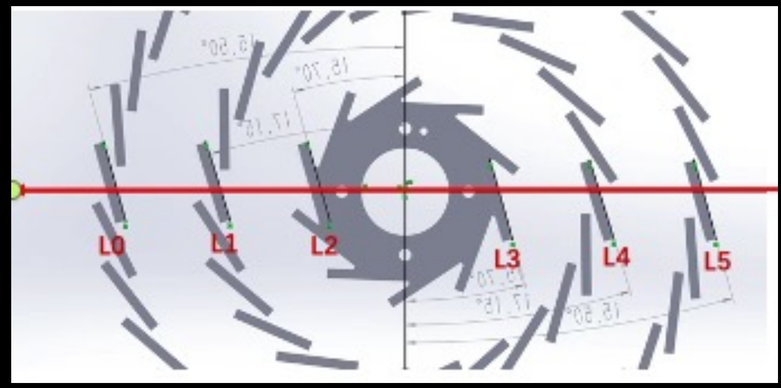
Detector prototype in testbeam





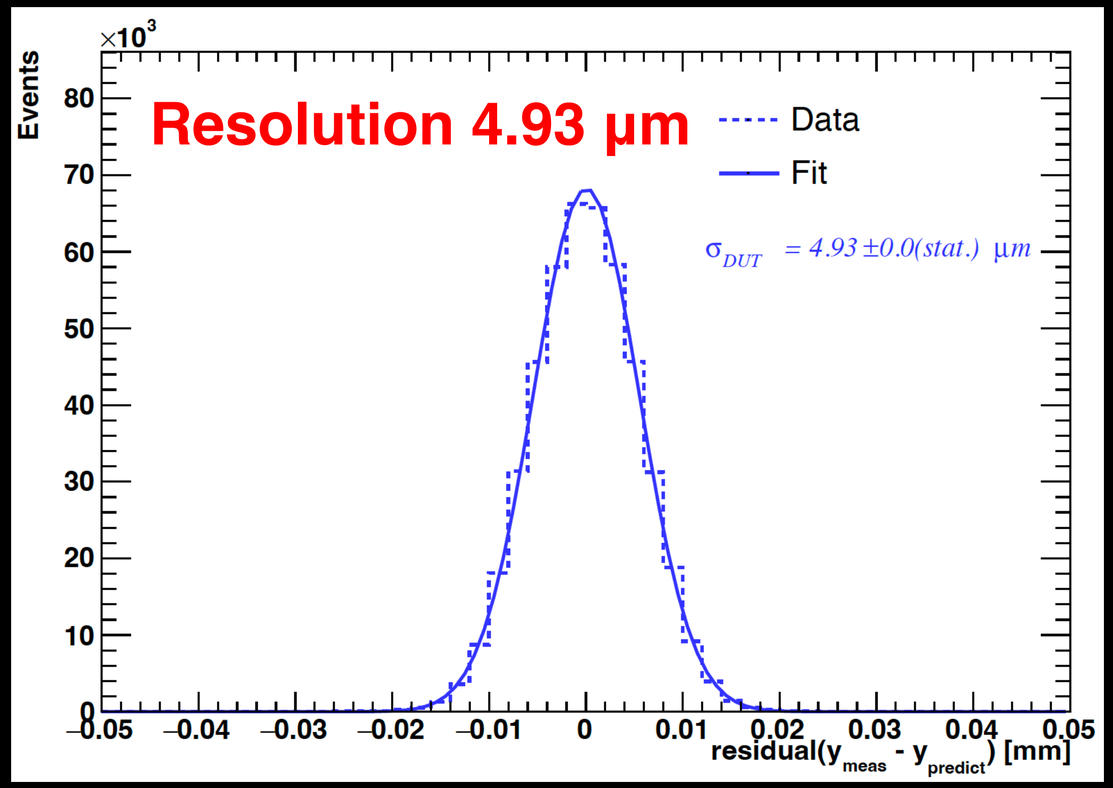
Test beam results (April 2023)

- Extract Spatial resolution from detector prototype testbeam data
  - One layer (L1) of TaichuPix used as Detector-Under-Test (DUT)
  - Other layers of vertex detector prototype used for track fitting
  - Spatial resolution reached 4.93μm the goal of the project
    - Spatial Resolution met the requirement (3-5μm)

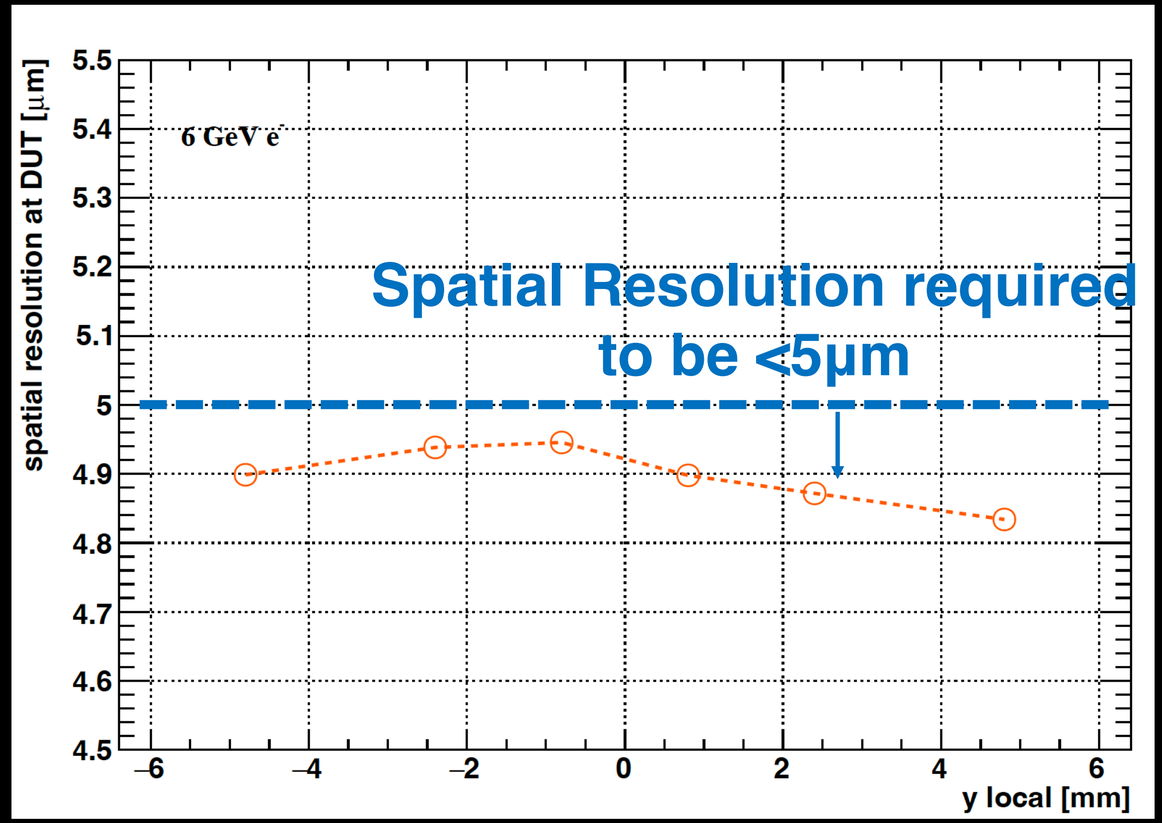


Residual distribution

DUT measured position – expected position from track



Spatial resolution vs hit positions



Publications and students education

- 文章

- T. Wu et al, The TaichuPix1: a monolithic active pixel sensor with fast in-pixel readout electronics for the CEPC vertex detector, 2021 JINST 16 P09020
- Wei, X.; Wei, W.; Wu, T.; Zhang, Y. et al. High data-rate readout logic design of a 512 × 1024 pixel array dedicated for CEPC vertex detector, Journal of Instrumentation, Volume 14, Issue 12, pp. C12012 (2019)
- Ying Zhang et al, Development of a CMOS pixel sensor prototype for the high hit rate CEPC vertex detector，Nucl.Instrum.Meth.A 1042 (2022) 167442
- Jinyu Fu et al, Mechanical design of an ultra-light vertex detector prototype for CEPC，Rad.Det.Tech.Meth. 6 (2022) 2, 159-169
- Tianya Wu, Weiguo Lu, et al.“A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector”, 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)

- 人才培养
  - 博士后(postdoc)： 2人
  - 博士(Ph.D)： 8人
  - 硕士(Master)： 23人

Patent（专利）(1)

- 1. 付金煜, 祝翱·吉马雷斯·达·科斯塔, 梁志均, 屈化民. 一种超轻梁的振幅测量装置. CN: CN113432699A, 2021-09-24.
- 2. 付金煜, 祝翱.吉马雷斯.达.科斯塔, 梁志均, 屈化民. 一种探测器气冷测试装置. CN: CN113311473A, 2021-08-27.
- 3. 魏晓敏, 张浩楠,王佳,薛菲菲,郑然,胡永才. 一种树状组织的缓存结构及其应用. CN: 2021.11130545.6，2021-11-5
- 4. 魏晓敏, 张浩楠, 王佳, 郑然, 薛菲菲, 蔡耀, 胡永才. 一种粒子图像的数据压缩电路和数据压缩方法, CN202210632037.0，2022-06-07
- 5. 王佳, 杨聚鑫, 郑然, 魏晓敏, 薛菲菲, 胡永才. 一种小面积快速瞬态响应全片上集成LDO电路, CN202111161887.9，2021-9-30
- 6. 郑然, 李志军, 王佳, 魏晓敏, 薛菲菲, 胡永才. 一种静态功耗自动配置的低功耗前端读出电路及设计方法, CN202111087544.2，2021-9-16
- 7. 薛菲菲, 黄雪蕾, 郑晓亮, 魏晓敏, 王佳, 郑然, 胡永才.一种电荷型逐次逼近ADC结构, CN202111089036.8，2021-9-16

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- 8.　张浩楠, 魏晓敏, 王佳, 郑然, 薛菲菲, 蔡耀, 胡永才. 一种拥塞缓解数据读出系统和方法, CN202210631994.1，2022-06-07
- 9.　王佳, 张浩楠, 魏晓敏, 郑然, 薛菲菲, 胡永才. 一种地址快速读出电路及读出方法, CN202111256292.1，2021-10-27
- 10. 郑然, 李佳乐, 王佳, 魏晓敏, 薛菲菲, 胡永才. 以电阻做负载的全差分迟滞比较器温度补偿系统及方法, CN202111182808.2，2021-10-11
- 11. 郑然, 李志军, 王佳, 魏晓敏, 薛菲菲, 胡永才. 电荷灵敏前置放大器结构及设计方法, CN202111087596.X, 2021-9-6
- 12. 郑然, 刘超, 赵子崴, 王佳, 魏晓敏, 薛菲菲, 胡永才. 一种应用于辐射粒子检测芯片的轨对轨单端转差分电路. CN202210440094.9, 2022/4/25

Conference talks (1)

1. Joao Guimaraes Da Costa, CepC phys/detectors, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
2. Xinchou Lou, Future e+e- (CEPC, FCC, ILC, CLIC), XXXIX International conference on high energy physics (ICHEP2018), July 4-11, 2018, Seoul
3. Ying Zhang, Design and Characterization of Prototype CMOS Pixel Sensors for the CEPC Vertex Detector, 2018 IEEE Nuclear Science Symposium and Medical imaging conference ,10-17 November, Sydney,Australia
4. Wei Wei, Full size pixel chip for high-rate CEPC Vertex Detector，Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
5. Xiaomin Wei, High data-rate readout logic design for 1024*512 CMOS pixel array dedicated for CEPC experiment, International workshop on radiation imaging detectors, International workshop on radiation imaging detectors, July 2019 Crete, Greece
6. Ying Zhang, Development of CMOS pixel sensor prototypes for the CEPC, International workshop on semiconductor pixel detector for particles and imaging (PIXEL 2018) , 10-14 December, 2018
7. T. Wu , A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector, in proceeding of International Conference on Electronics Circuits and Systems, Nov. 27-29, 2019, Genova, Italy.
8. YunPeng Lu, Development of the Silicon Tracker for CEPC, XXXIX International conference on high energy physics (ICHEP2018), July 4-11,2018, Seoul
9. Chengdong Fu, CepC full silicon option , Workshop on the circular Electron-positron Collider -- EU editon, May 24-26, 2018, Roma, Italy

Conference talks (2)

1. Joao Guimaraes Da Costa, CepC phys/detectors, Workshop on the circular Electron-positron Collider -- EU editon, May 24-26, 2018, Roma, Italy
2. Ying Zhang, Overview of the chip design for the MOST2 CEPC vertex project, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
3. Xin Shi, CepC pixel prototypes , Workshop on the circular Electron-positron Collider -- EU editon, May 24-26, 2018, Roma, Italy
4. Ying Zhang, Fast in-pixel readout for a CMOS pixel sensor prototype developed for the CEPC vertex detector， 12th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors，14-18 December，2019， Hiroshima， Japan
5. Y. Zhang et al, "Development of CMOS Pixel Sensor prototype for the high-rate CEPC vertex detector", 12th International conference on Position sensitive detectors, 英国伯明翰，2021年9月15日
6. Zhijun Liang, Status of CEPC vertex detector prototype, CEPC workshop for 4th detector concept , YangZhou， 2021年4月13日
7. Wei Wei, Status of the TaichuPix chip for the high-rate CEPC Vertex Detector, CEPC workshop for 4th detector concept, YangZhou, 2021年4月13日
8. Weiwei, Status of the CEPC vertex and tracking detector R&D, The 2022 International Workshop on the High Energy Circular Electron Positron Collider, Beijing, Oct 24-28 , 2022
9. Zhijun Liang, CEPC vertex detector R & D global overview, Joint Workshop of the CEPC Physics, Software and New Detector Concept in 2022, Beijing ,May 23 – 25, 2022

Summary of CMOS Sensor chip R & D

- **Developed the first full-size CMOS pixel sensor for particle detector in China**
  - **High spatial resolution and radiation hard**
- **Developed three double-layer vertex detector prototype**
  - **Readout electronics and data acquisition for detector prototype was developed**
- **Completed beam tests for the sensor prototype and the detector prototype at DESY**
  - **The Assessment indicators of the project have been achieved**

	Requirement	Result	
Spatial resolution	3-5 μm	Laser test: ~ 4 μm Chip-level Beam Test : 4.8 μm ✓ Prototype level Beam Test: 4.9μm	World leading
Radiation hardness (total ionization dose, TID)	>1 Mrad	>3 Mrad ✓	First in China

backup

International collaboration

- **Very close collaboration with IFAE (spain) in sensor chip design.**
- **We have one engineer visited Oxford and Liverpool for 4 weeks in 2019**

☐ **Planning to collaborate with UK groups on module and detector structure**

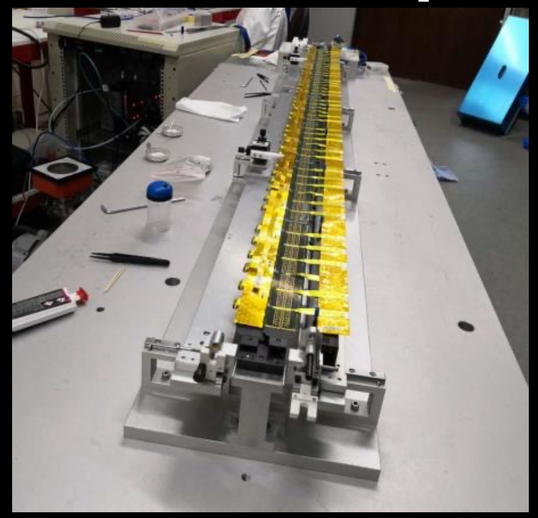
☐ **Unfortunately, Collaboration in UK groups didn't continue due to CovID**

- **IFAE(Spain): very active in CMOS Sensor design and testing**
- Liverpool (UK): Tracker mechanical design,
- Oxford(UK): CMOS sensor design validation, thermal design

Mu3e ladder, Atlas barrel strip stave prototype.

Lab visit in Oxford

Labs visit in Liverpool



Module of Alice's OB tracker, Advance material Lab

CEPC vertex detector R & D

- Three on-going R & D programs on vertex detector
  - Previous update in CEPC day (June 15th) https://indico.ihep.ac.cn/event/11875/
- This talk focuses on MOST2 project
  - MOST2 aims to build full-size vertex detector prototype

Funding agency	Process	International collaborators	Objectives of the project	schedule
CEPC MOST1	CMOS	Strasburg IPHC	Small pixel size design with in-pixel digitization and low power frontend	2016.6-2021.5
MOST2	CMOS	IFAE/Oxford/ Livepool …	vertex detector prototyping (Full-size sensor support structure, module …)	2018.5-2023.4
NSFC	SOI	KEK/SOIPIX collaboration	Verification of SOI process with small pixel size and low noise design	2016-

Publications, patent and International talks

High data-rate readout logic design of a 512 × 1024 pixel array dedicated for CEPC vertex detector

X. Wei,[a,1] W. Wei,[b] T. Wu,[c,d] Y. Zhang,[b] X. Li,[b] L. Zhang,[e] W. Lu,[b] Z. Liang,[b] J. Dong,[e] L. Li,[e] J. Wang,[a] R. Zheng,[a] R. Casanova,[d] S. Grinstein,[d] Y. Hu[f] and J. Guimaraes da Costa[b]

Development of a CMOS pixel sensor prototype for the high hit rate CEPC vertex detector

Ying Zhang [a,b], Wei Wei [a,b,*], Xiaoting Li [a,b], Zhijun Liang [a,b], Tianya Wu [a,b], Raimon Casanova [c], Xiaomin Wei [d], Liang Zhang [e], Jianing Dong [e], Jia Wang [d], Weiguo Lu [a,b], Ran Zheng [d], Long Li [e], Sebastian Grinstein [c,f], Joao Guimaraes da Costa [a]

Mechanical design of an ultra-light vertex detector prototype for CEPC

Jinyu Fu[1,2,3] · Zhijun Liang[1,2] · Hao Zeng[1,3] · Gang Li[1] · Mingyi Dong[1,2,3] · Huamin Qu[1] · Joao Guimaraes da Costa[1]

A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector

Tianya Wu[1,2], Raimon Casanova[2], Wei Wei[3], Xiaomin Wei[4], Ying Zhang[3], Liang Zhang[5], Xiaoting Li[3], Zhijun Liang[3], Joao Guimaraes da Costa[3], Weiguo Lu[3], Jianing Dong[5], Long Li[5], Wang Jia[4], Ran Zheng[4], Ping Yang[1], Guangming Huang[1] and Sebastian Grinstein[2]

➢ Publication:

JINST 14 (2019) C12012

Nucl.Instrum.Meth.A 1042 (2022) 167442

Rad.Det.Tech.Meth. 6 (2022) 2, 159-169

IEEE ICECS
(doi: 10.1109/ICECS46596.2019.8965105.)

➢ Patent

【1】付金煜, 祝翱·吉马雷斯·达·科斯塔, 梁志均, 屈化民. 一种超轻梁的振幅测量装置. CN: CN113432699A, 2021-09-24
【2】付金煜, 祝翱.吉马雷斯.达.科斯塔, 梁志均, 屈化民. 一种探测器气冷测试装置. CN: CN113311473A, 2021-08-27.

➢ Selected Six International conference talks:

- Joao Guimaraes Da Costa, CepC phys/detectors, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
- T. Wu , A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector, in proceeding of International Conference on Electronics Circuits and Systems, Nov. 27-29, 2019, Genova, Italy.
- Xiaomin Wei, High data-rate readout logic design for 1024*512 CMOS pixel array dedicated for CEPC experiment, International workshop on radiation imaging detectors, International workshop on radiation imaging detectors, July 2019, Crete, Greece
- Ying Zhang, Overview of the chip design for the MOST2 CEPC vertex project, Workshop on the CEPC,EU Edition, April 15 - 17, 2019, Oxford, UK
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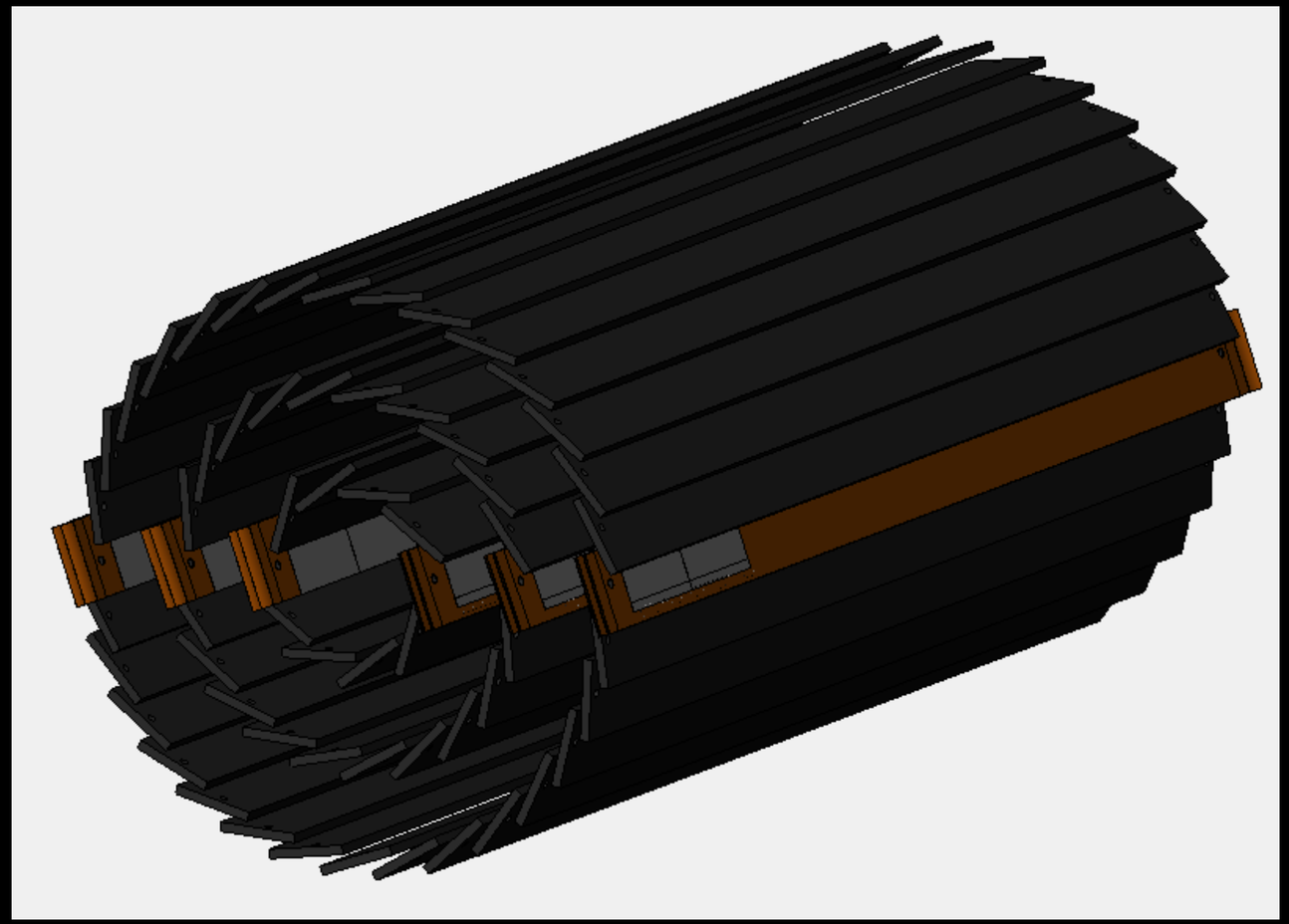
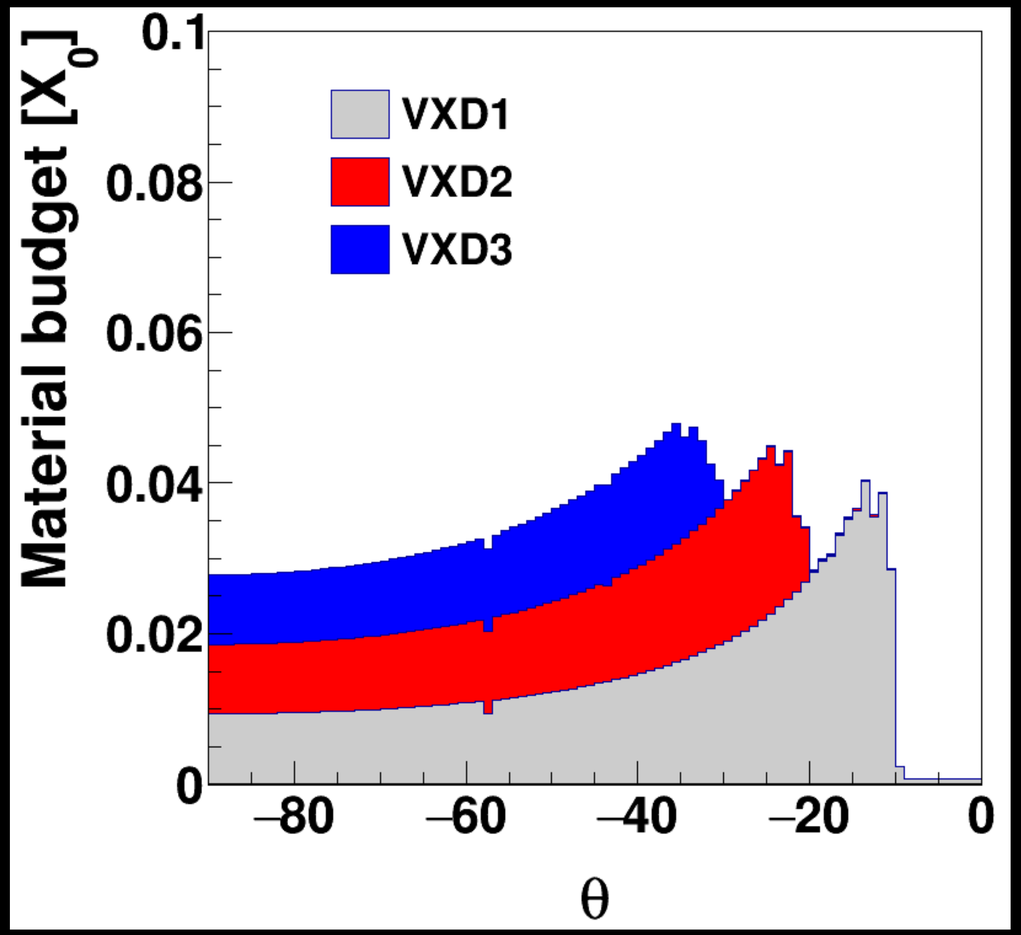
Estimated Material budget for vertex detector prototype

- Estimated material budget 0.026 X0 for three double ladders vertex detector (6 layers)
  - Copper in flexible PCB are major contributions
  - Plan to replace copper into Aluminum in final CEPC vertex detector



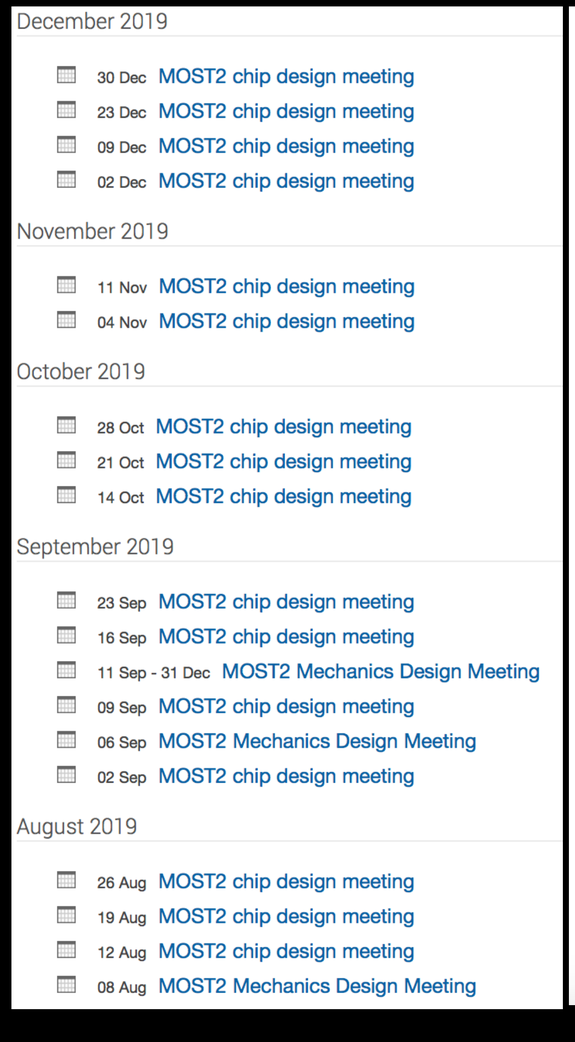


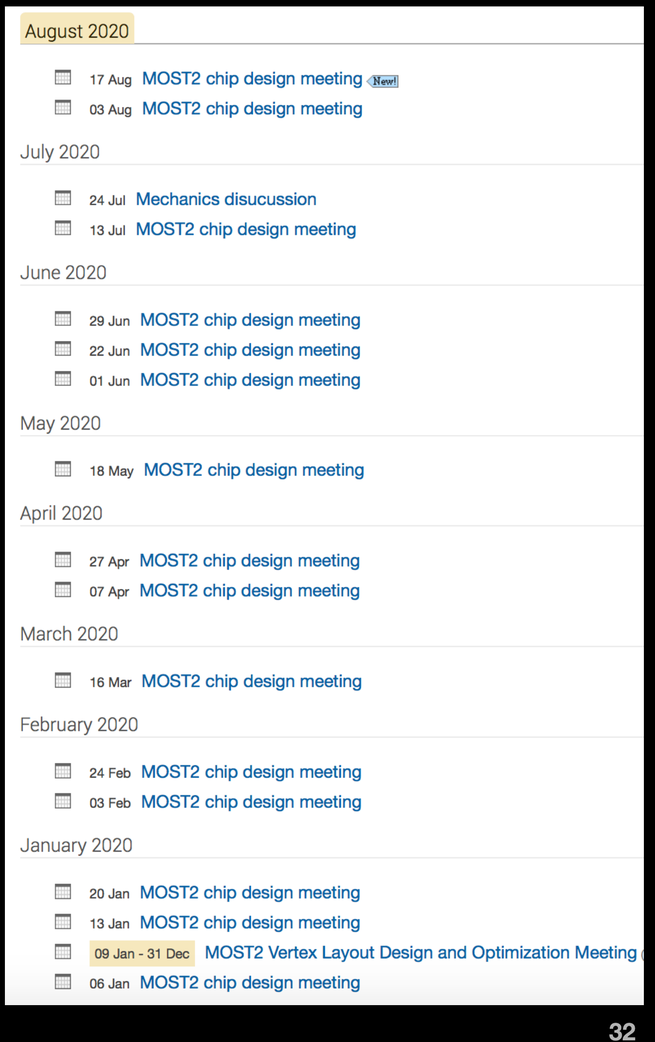
Internal organization

Task 2 meetings

- CMOS sensors chip design meeting (weekly)
- Vertex detector overall design meeting (weekly)
- Full-day internal review meeting (every 3 months)
- Institutes worked closely
- Project leader followed closely the progress

Task 2 meetings

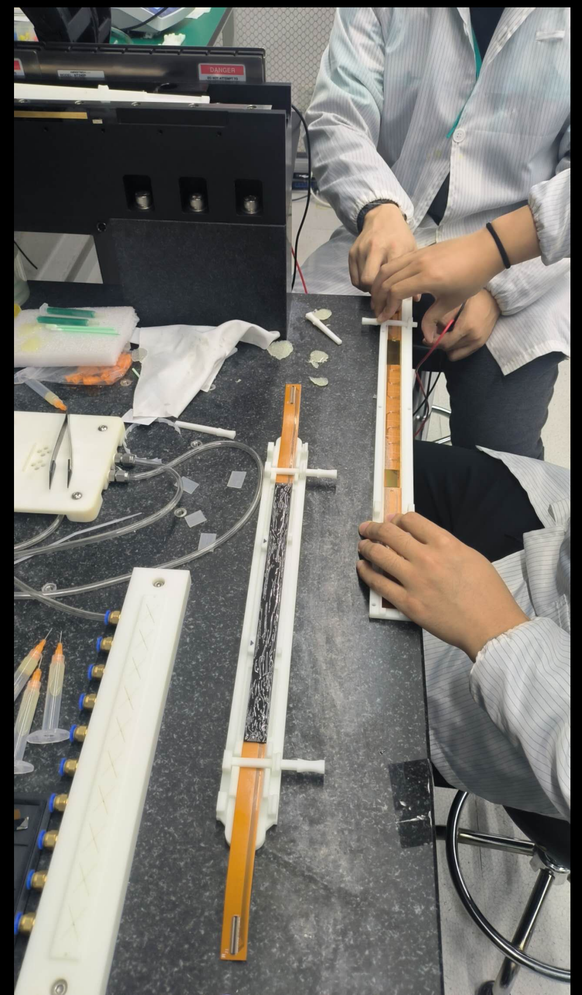




Support structure of the ladder

- Fabricated support structure prototype of the ladder (IHEP designed)
- Both side of ladder has wire-bonding on chip → Challenging
  - Dedicated tooling for double-side ladder assembly

Double-Side ladder assembly



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	Project indicators	Test results
Spatial resolution	3-5 μm	3.98/4.12 μm for X/Y dir. (laser test)
		4.78 μm (beam test)
TID	> 1Mrad	> 3 Mrad