环形正负电子对撞机
Circular Electron Positron Collider

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# 传感器芯片设计与测试

# Sensor chip design and testing

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On behalf of the CEPC MOST2 Vertex detector design team

2023-6-19

# Main specifications of the full-scale chip

- **A full-scale pixel chip should be design to build the first vertex detector prototype**
  - No full-scale CMOS pixel sensor for particle detector exists in China before this project
- **Project assessment index (考核指标)**
  - Spatial resolution: 3-5 μm
  - Total ionization dose (TID) > 1 Mrad

| 考核指标[2] | | | | 考核方式（方法）及评价手段[4] |
|---|---|---|---|---|
| 指标名称 | 立项时已有指标值/状态 | 中期指标值/状态[3] | 完成时指标值/状态 | |
| 硅径迹探测器原型机的空间分辨率 | 无 | 研制出小型传感器芯片，像素单元尺寸小于或等于 25 微米 ×25 微米。 | 3-5 微米 | 同行专家评审。(通过束流实验，离线分析数据获得空间分辨率。该测试结果写入原型机设计与测试报告，以供同行专家评审) |
| 所设计的抗辐照硅传感器能承受的总剂量 | 无 | 完成传感器的初步设计，通过仿真初步验证其抗辐照性能 | 1 MRad | 同行专家评审（提供传感器的设计与测试报告供专家评审） |

# Additional specifications on the full-scale chip

- **Additional specifications considered besides the main goals of project**
  - Assembled on ladder → **large sensitivity area**
  - Low material → **low power density**
  - High detection efficiency → **small dead time**
  - Bunch spacing: Higgs: 680 ns; W: 210 ns; Z: 25 ns

    Hit density: 2.5 hits/bunch/cm$^2$ for Higgs/W; 0.2 hits/bunch/cm$^2$ for Z → **high hit rate**

**TaichuPix design goals**

| Specs | Parameter |
|---|---|
| Hit rate | 120 MHz/chip |
| Data rate | 3.84 Gbps (triggerless)<br>~110 Mbps (trigger) |
| Dead time | < 500 ns |
| Pixel array | 512 row × 1024 col |
| Chip size | ~1.4 × 2.56 cm$^2$ |
| Power Density | < 200 mW/cm$^2$<br>(air cooling) |

**JadePix design goals**

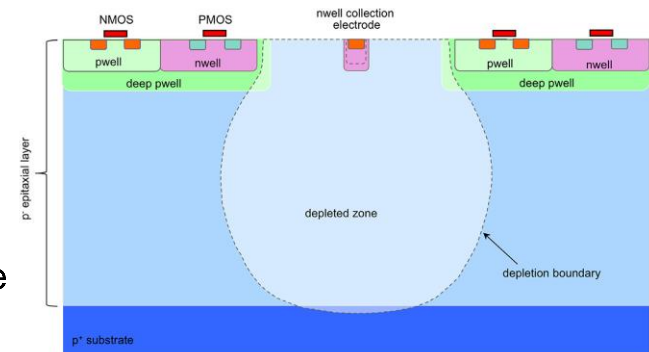
| Specs | Parameter |
|---|---|
| Spatial resolution | $\leq 5$ μm |
| Integration time | $\leq 100$ μs |
| Power Density | < 100 mW/cm$^2$ |
| Chip size | no requirement |

**Major innovation of TaichuPix: High data-rate processing maintaining good spatial resolution**

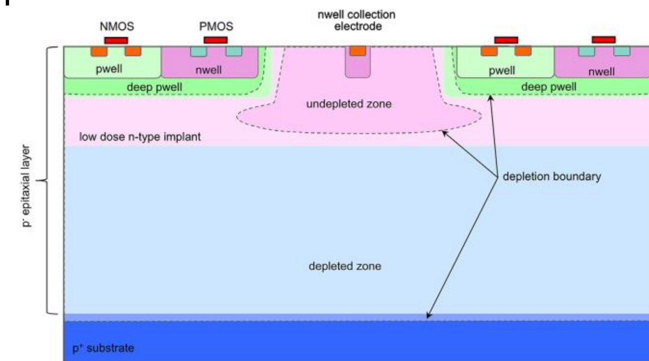
# Structure and process of sensor

- **Technology：CMOS Monolithic pixel sensor**
  - N-well/P-epitaxial diodes employed collection elements
  - Readout electronics integrated on the same Si-substrate
  - ➔ Low material budget, low pixel capacitor, easy to assemble

- **Process : TowerJazz CIS 180 nm process**
  - Process splits:
    - **Standard process**
      - Baseline option, the only choice available in the MPW submissions
    - **Modified process***
      - Adding an extra low dose n-type layer based on the standard process, to achieve faster charge collection, thus a better radiation tolerance
      - Very difficult to access, the first time available to a Chinese institute



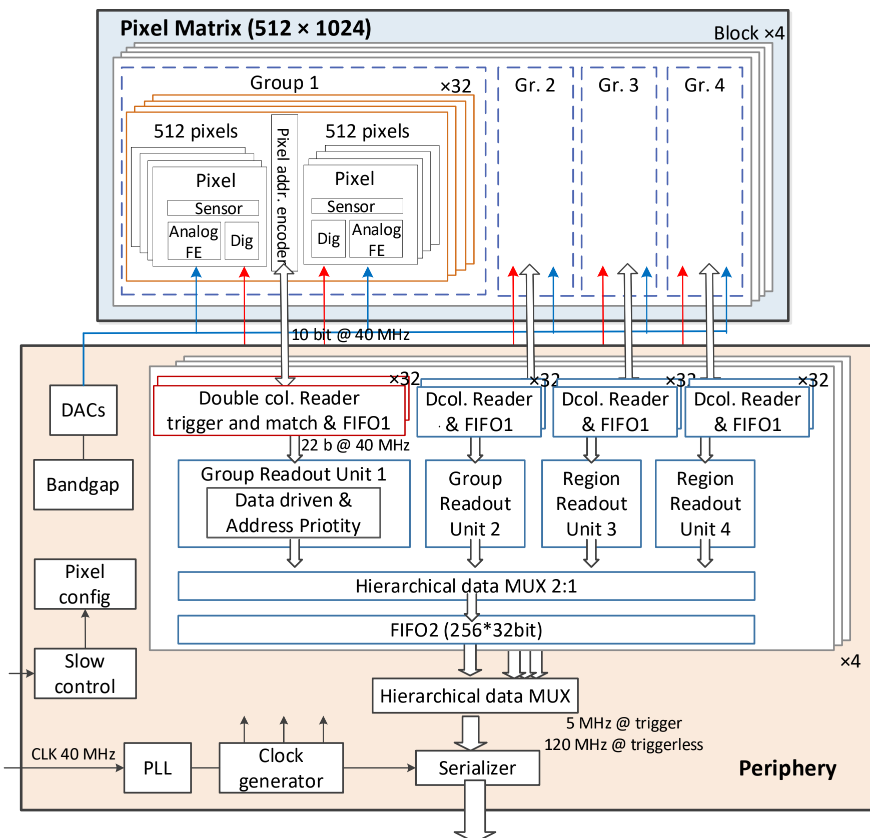

Standard process

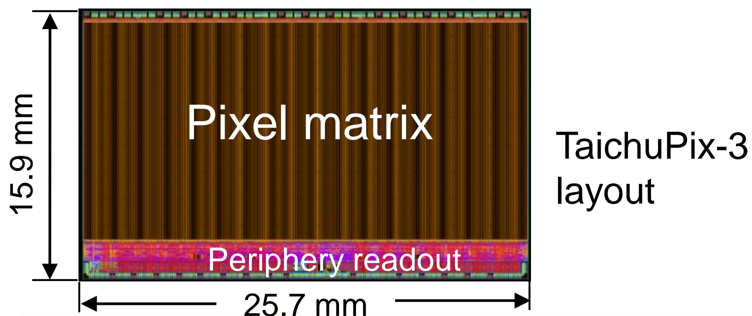



Modified process*

*Reference: NIM, A 871 (2017) 90–96

# TaichuPix sensor architecture




TaichuPix-3 layout

- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge

  Invented a new buffer tree architecture, patented

  专利: CN: 2021.11130545.6

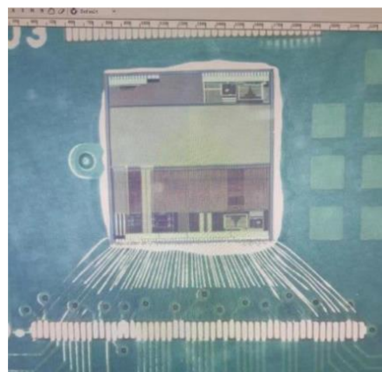
  - L2 FIFO: match the in/out data rate between core and interface

  Proposed a readout scheme for mitigating data congestion

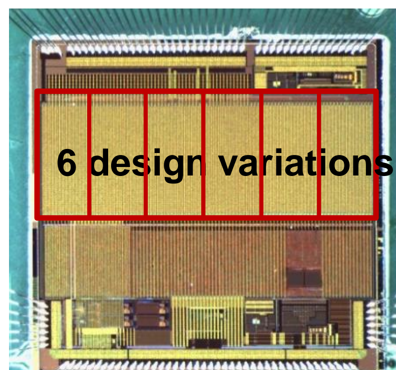
  专利: CN202210631994.1, 2022-06-07
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

# TaichuPix prototypes overview

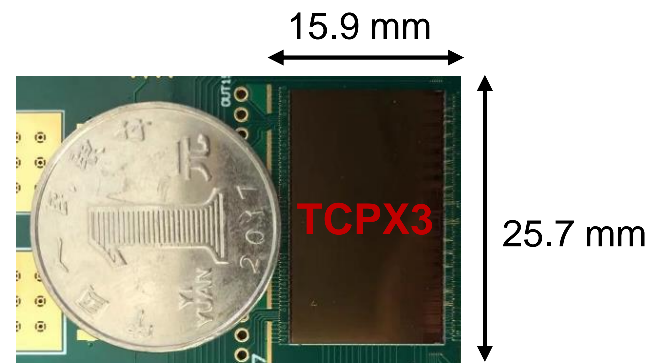
- **Major challenges for the sensor design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz ) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 rounds of sensor prototyping in 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm )
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - **Full-scale chip: TaichuPix-3, received in July 2022 & March 2023**
    - Difficulties encountered in submission: no domestic access, complex and long time procedure from abroad access, very expensive …



**TaichuPix-1**



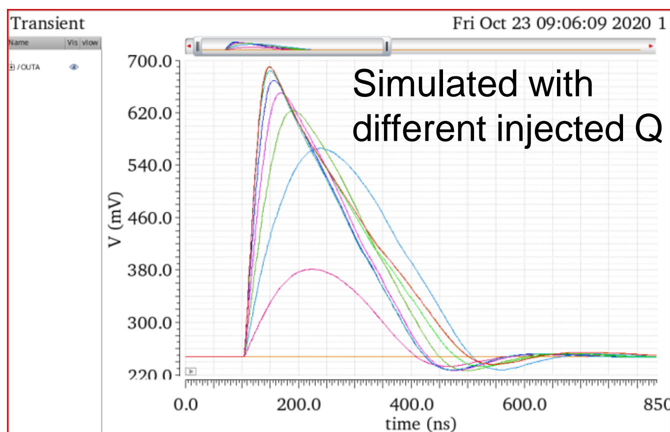

**TaichuPix-2**

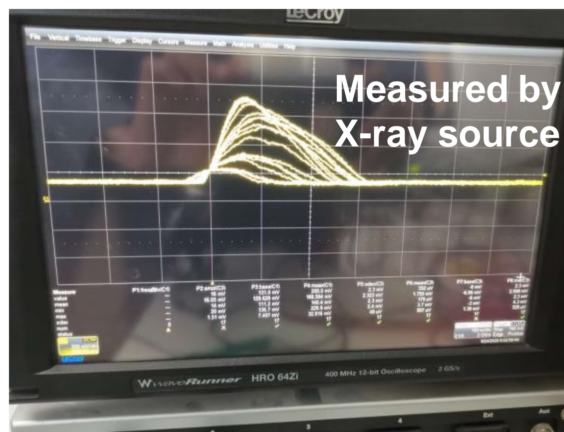



**TaichuPix-3**
**Pixel size：25 μm × 25 μm**

# Functionality of complete signal chain

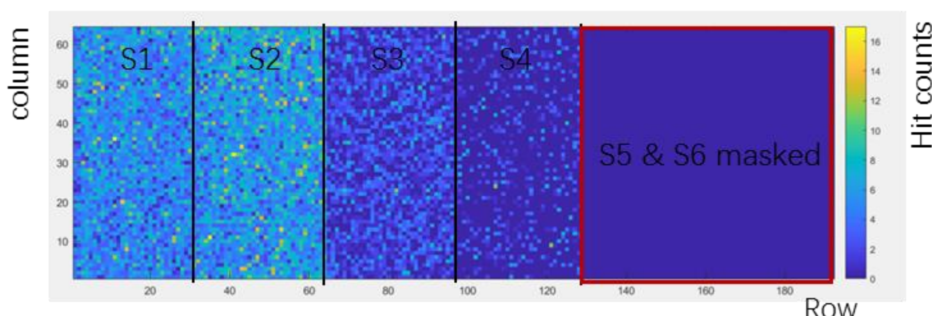
- **Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was firstly proved with X-ray, electron and laser sources.**



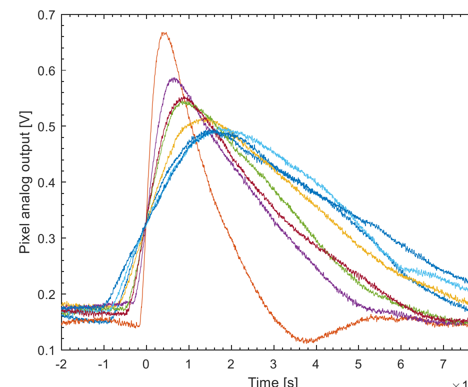




**Measured results consistent with simulations in term of shape, amplitude**

**Pixel analog signals from simulation (left) and measurement (right)**




Hit map of the TaichuPix-2 under X-ray from the X-tube for 5 min.




Analog output of one pixel under $^{90}Sr$ exposure

# TaichuPix-2 test with $^{90}$Sr

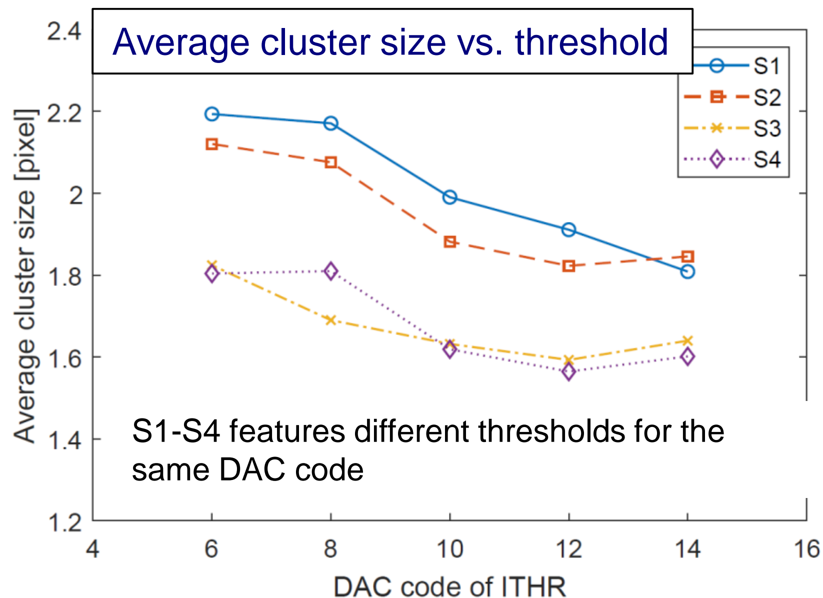
- **Four pixel sectors with different analog front-end variations for design optimization, S1 used in the full-scale chip due to the lowest ENC**

| Sectors | Front-end design features |
|---|---|
| S1 | Reference design, inherited from TaichuPix-1 |
| S2 | PMOS in independent N-wells |
| S3 | One transistor in an enclosed layout |
| S4 | Increased transistor size to reduce the threshold dispersion |

Threshold and noise of different pixel sectors

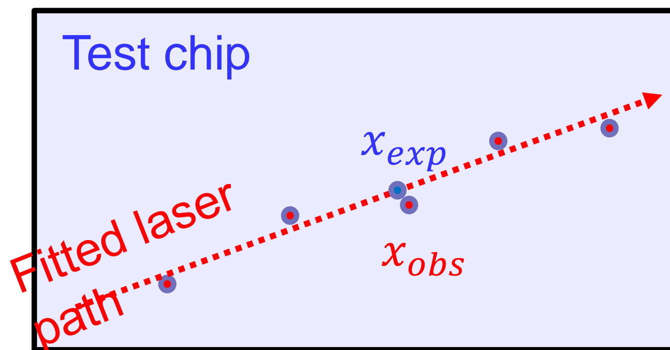
| Sec-tors | Threshold Mean ($e^-$) | Threshold rms ($e^-$) | Temporal noise ($e^-$) | Total equiv. noise ($e^-$) |
|---|---|---|---|---|
| **S1** | **267.0** | **49.8** | **29.3** | **57.8** |
| S2 | 293.4 | 54.5 | 26.9 | 60.8 |
| S3 | 384.9 | 58.4 | 24.4 | 63.3 |
| S4 | 411.9 | 56.6 | 26.5 | 62.5 |

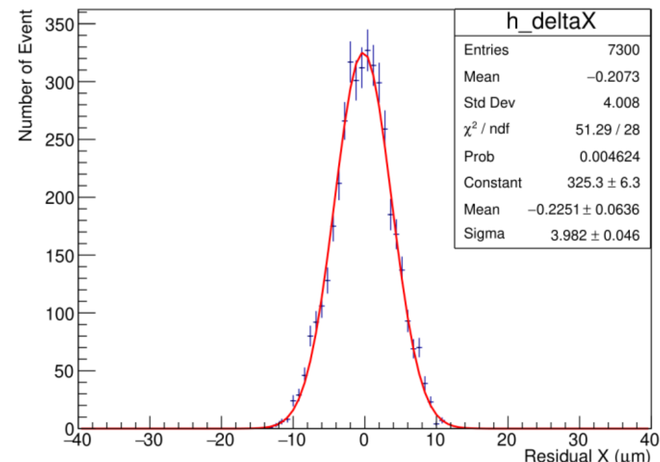
- **TC2 exposure to $^{90}$Sr source**
  - Average cluster size decreases with threshold as expected
  - Average cluster size for S1-S4 larger than 1, → benefits the spatial resolution (better than the binary resolution, $25/\sqrt{12} \approx 7.2\ \mu m$



# Laser test of TaichuPix-2

- **Setup: a 3-D linear translation stage with a 1064 nm laser**
- **Method:**
  - One dimension laser scan on the test chip with a fixed step of 1 μm
  - Take the linear fit of the observed X,Y position as the expected laser position

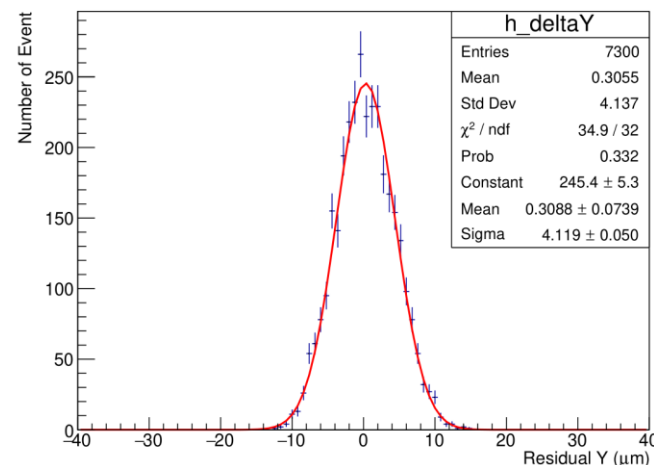



**Distribution of residual X**

**Measured results**

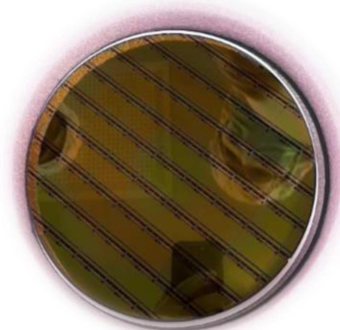
| | Resolution (μm) | Overall error (μm) | Statistical error (μm) | Translation error (μm) |
|---|---|---|---|---|
| X | 3.98 | ±0.23 | ±0.05 | ±0.22 |
| Y | 4.12 | ±0.25 | ±0.05 | ±0.25 |



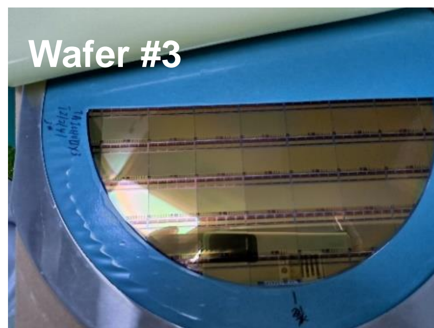

**Distribution of residual Y**

# Large-scale sensor TaichuPix-3

- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafers thinned down to 150 μm and diced**



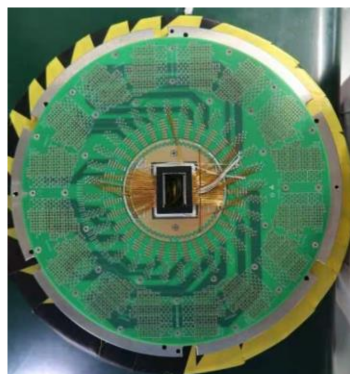
8-inch wafer



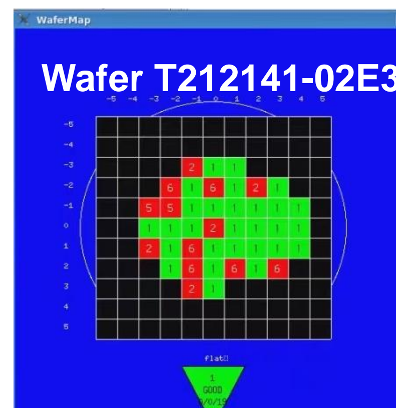

Wafer after thinning and dicing

Thickness after thinning

  - **Wafers tested on probe-station →** chip selecting & yield evaluation



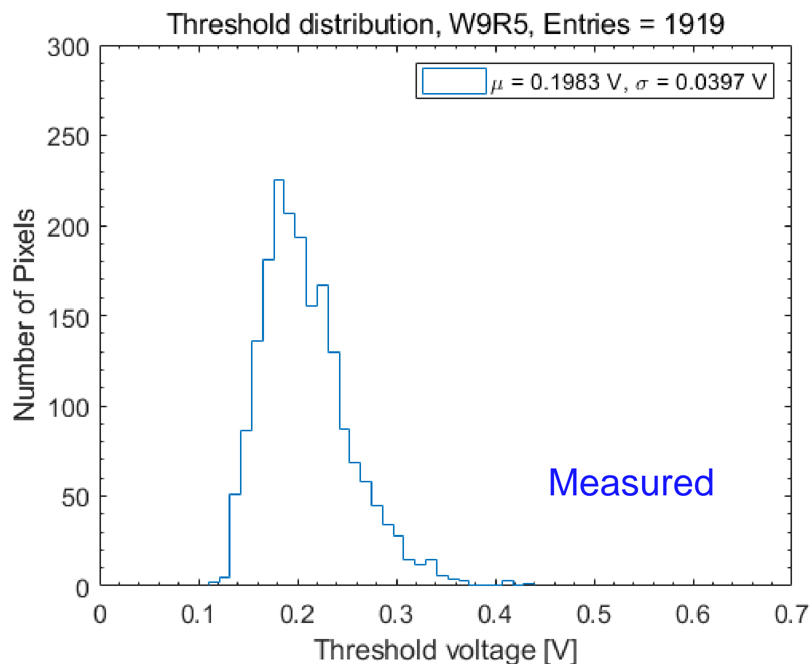
Probe card for wafer test

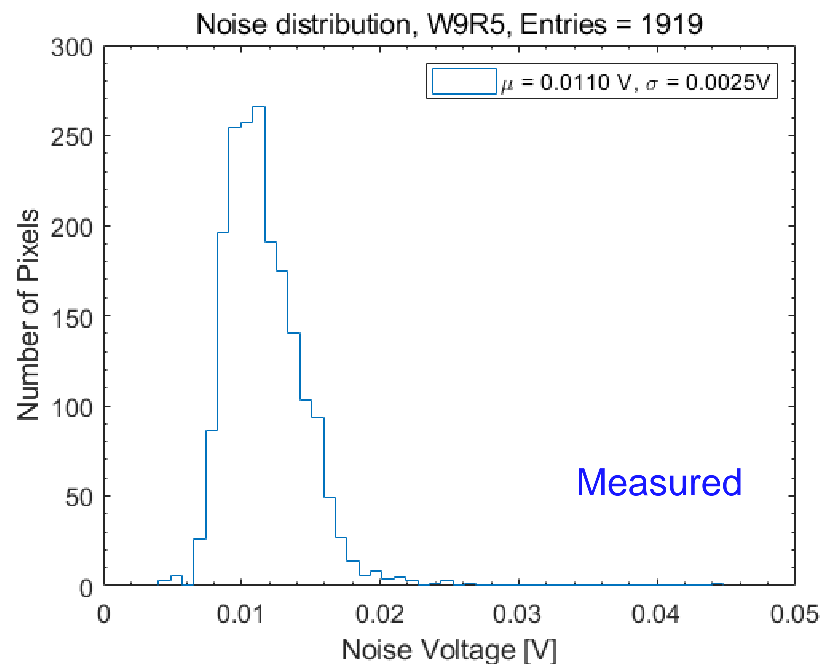



An example of wafer test result

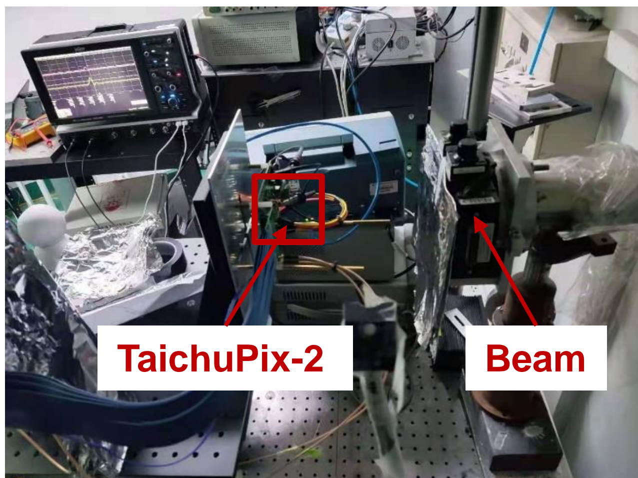
# Threshold and noise of TaichuPix-3

- **Pixel threshold and noise were measured with selected pixels**
  - Average threshold ~215 e$^-$, threshold dispersion ~43 e$^-$, temporal noise ~12 e$^-$ @ nominal bias setting



# TID test setup




TC2 at BSRF 1W2B beamline

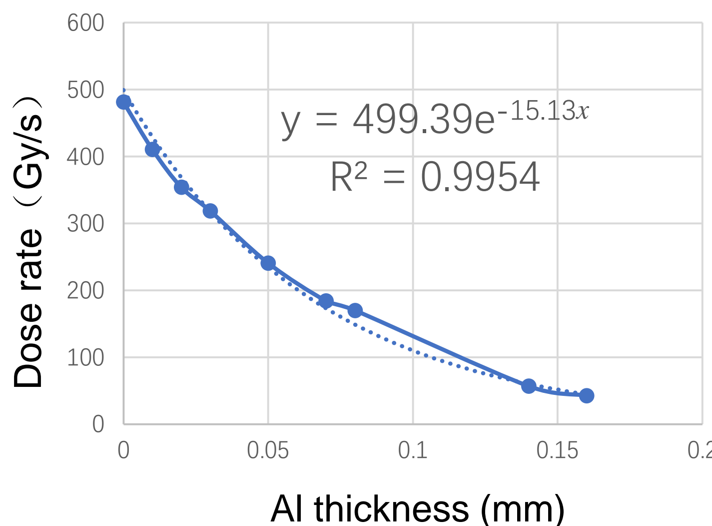
TC3 at BSRF 1W2B beamline

**Beamline Specifications**

| Source | Wiggler |
|---|---|
| Energy Range | 5-18 keV |
| Resolution (ΔE/E) | Over 4 x $10^{-4}$ |
| Flux (photons/sec) | $10^{12}$ |
| Beam Size (HxV) | 1mm x 0.6 mm |

Attenuation of Aluminum (thickness of Al foil is 0.01 mm/layer)

| Aluminum (Al) | Irradiation dose rate |
|---|---|
| 96 layers | 0.02rad/s |
| 64 layers | 3 rad/s |
| 32 layers | 394 rad/s |
| 28 layers | 722 rad/s |
| 24 layers | 1321.6 rad/s |
| 1 layers | 42927 rad/s |

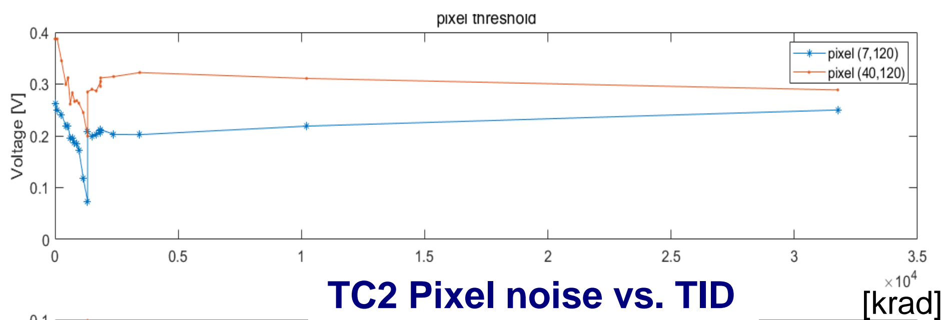



- **Ionization chamber is used to calibrate irradiation dose rate**
- **The irradiation dose is regulated by Al foil**
- **Chip was exposed with full working condition: power, bias, clk, …**

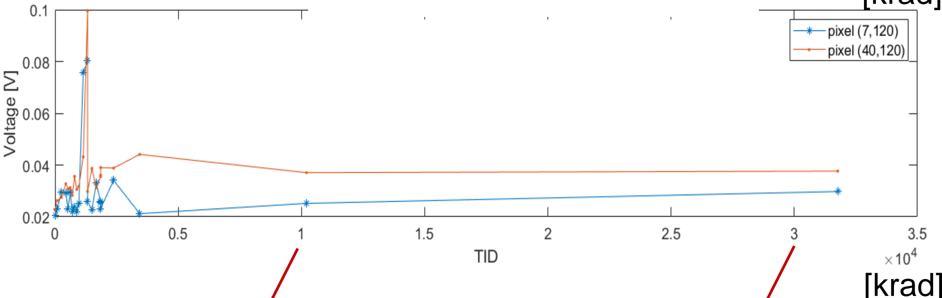
# TID test result

- **Test of TC2**
  - Normal chip functionality and good noise performance proved up to 30 Mrad TID

**TC2 Pixel threshold vs. TID**

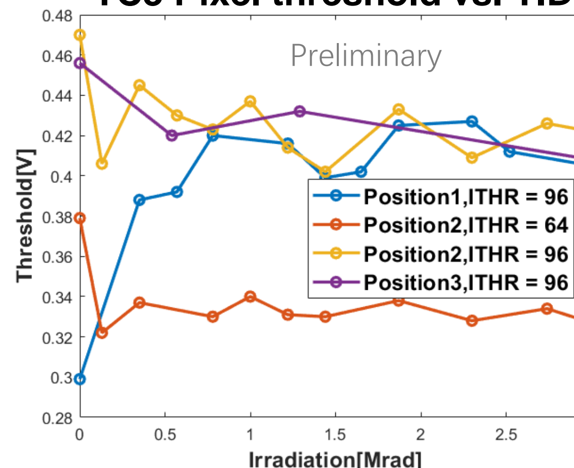



**TC2 Pixel noise vs. TID**

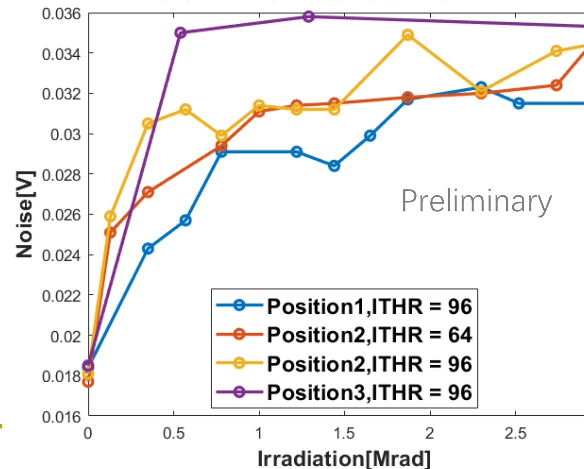



- **Test of TC3**
  - All three irradiation regions indicated a good performance to 3 Mrad TID

**TC3 Pixel threshold vs. TID**

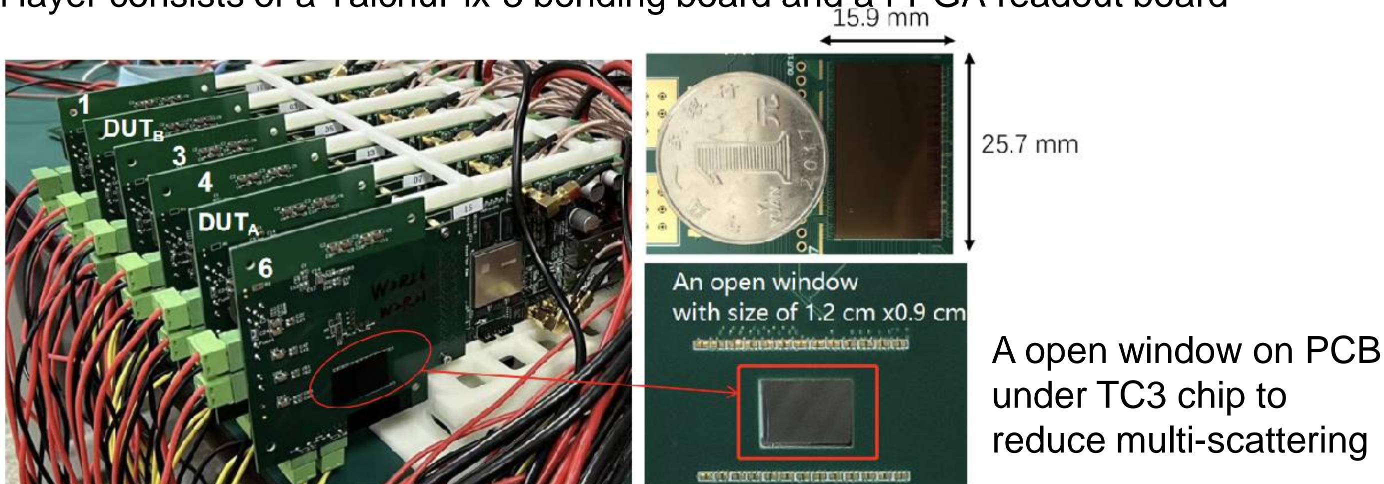



**TC3 Pixel noise vs. TID**



# TaichuPix-3 telescope

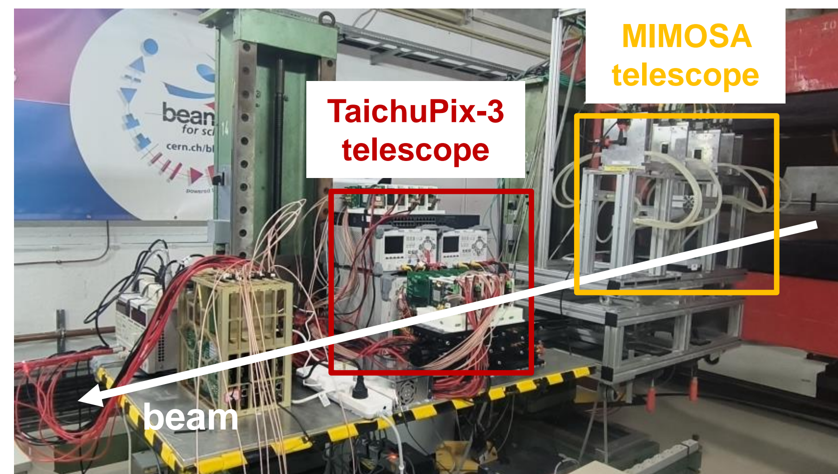
- **The 6-layer of TaichuPix-3 telescope built**
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board




6-layer TaichuPix-3 telescope

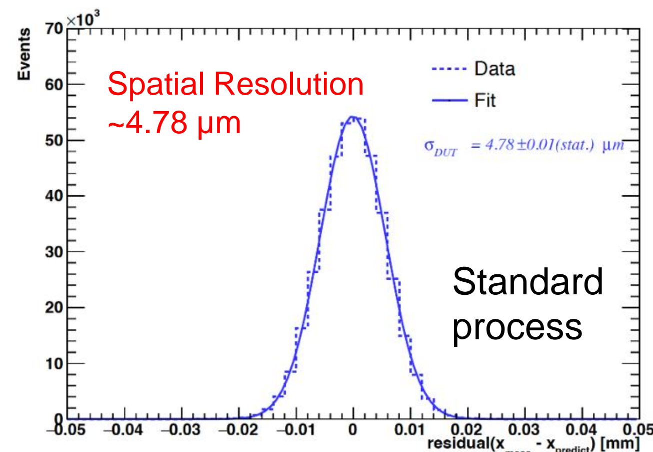
A open window on PCB under TC3 chip to reduce multi-scattering

- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT (Detector Under Test)

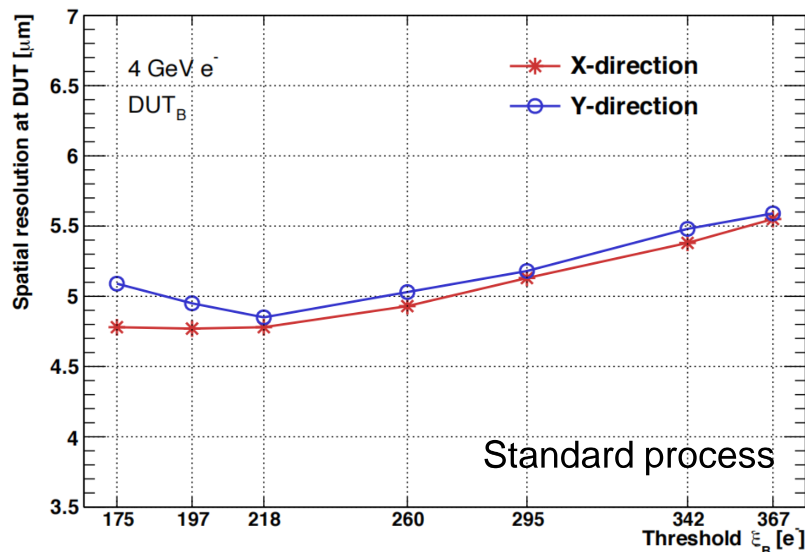


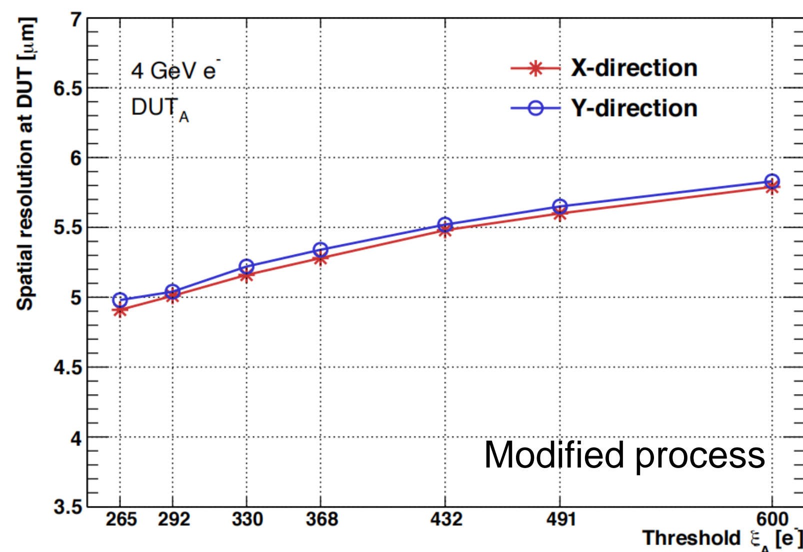
# TaichuPix-3 beam test result

- **2 DUT with different processes tested**
  - $DUT_B$ with the standard process; $DUT_A$ with the modified process
- **Spatial resolution results**
  - The resolution gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved for both processes, best resolution is 4.78 μm




Distribution of residual X

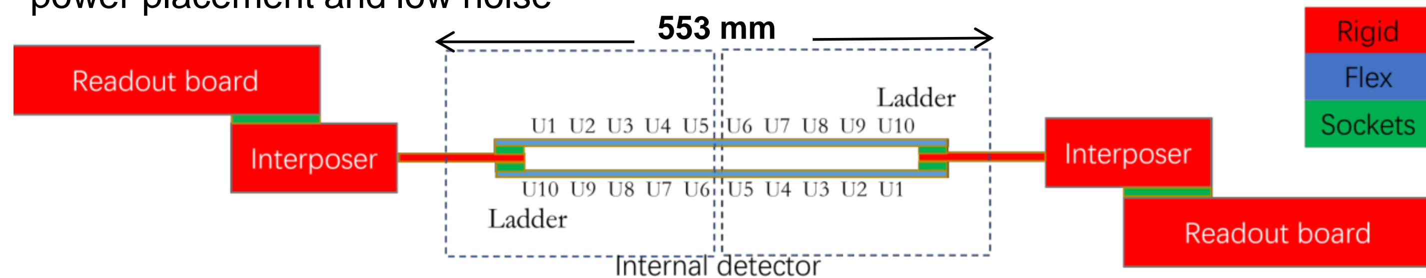



Spatial resolution vs. pixel threshold

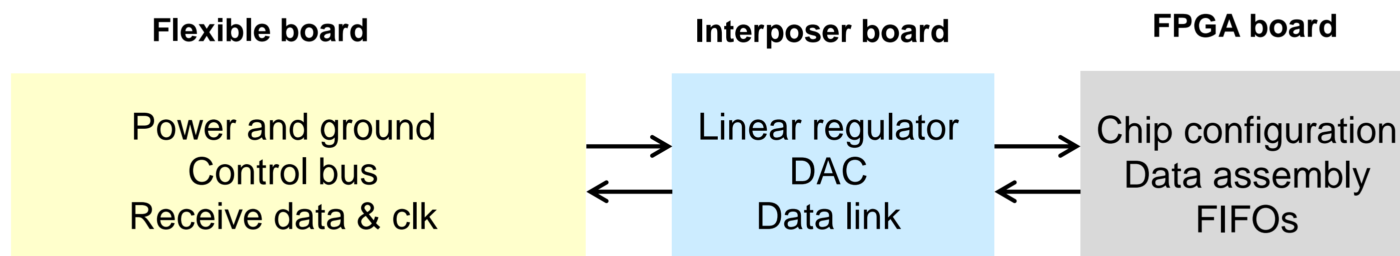
# Ladder readout design

- **Detector module (ladder) = 10 sensors + readout board + support structure + control board**
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Challenges**
  - Long flex cable → hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals
- **Solutions**
  - Read out from both ends, readout system composes of three parts, careful design on power placement and low noise



Ladder readout system

# Ladder readout design

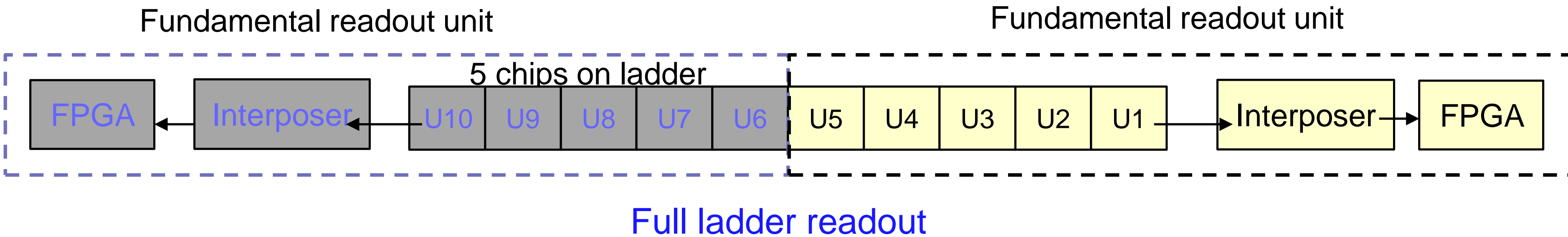



**Functional block diagram of a ladder readout unit**

- **Design key points of the flexible board**
  - Carefully chosen stack-up, minimum the thickness
  - Appropriately sacrifice the slow signals to guarantee the shielding of the major signals and the low impedance path for analog power supply.
  - Very challenging in manufacture because of the extremely long & thin PCB routing

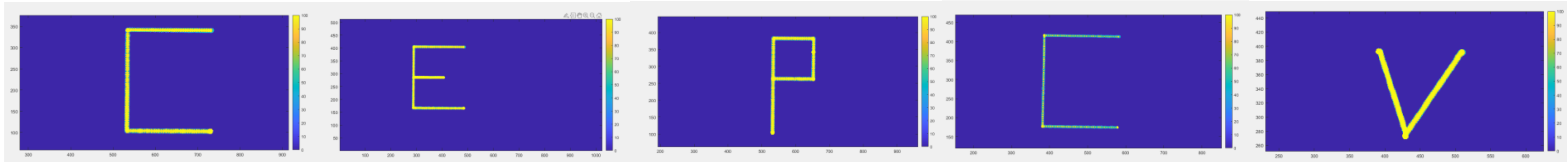
- **Design key points of the interposer board**
  - Ultralow noise power supply to chips, RMS noise ~1 μV
  - Low noise DAC reference: 16 bits, 1 LSB INL
  - Independent power supply and data path for back-to-back ladders

# Laser test result of ladder




Full ladder readout

- **A full ladder includes two identical fundamental readout units**
  - Each contains 5 TaichuPix chips, a interposer board, a FPGA readout board
- **Functionality of a full ladder fundamental readout unit was verified**
  - Configuring 5 chips in the same unit
  - Scanning a laser spot on the different chips with a step of 50 μm, clear and correct letter imaging observed
  - **Demonstrating 5 chips working together → one ladder readout unit working**



Laser tests on 5 Taichupix chip on a full ladder
("CEPCV" pattern by scanning laser on different chips on ladder)

## Summary

- **The full-scale and high granularity pixel prototype, TaichuPix-3, has been designed and tested**
- **The project design indicators were achieved**

| | **Project indicators** | **Test results** |
|---|---|---|
| Spatial resolution | 3-5 μm | 3.98/4.12 μm for X/Y dir. (laser test) |
| | | 4.78/4.85 μm for X/Y dir. (beam test) |
| TID | > 1 Mrad | > 3 Mrad |

- **Readout electronics for the sensor test and the ladder readout were developed**
  - Performed the sensor characterization in the lab successfully
  - Completed beam tests for the pixel sensor prototype and the vertex detector mechanical prototype

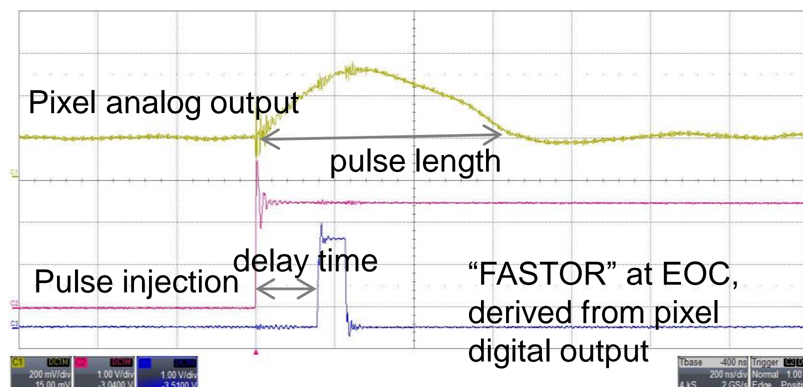
# Backup

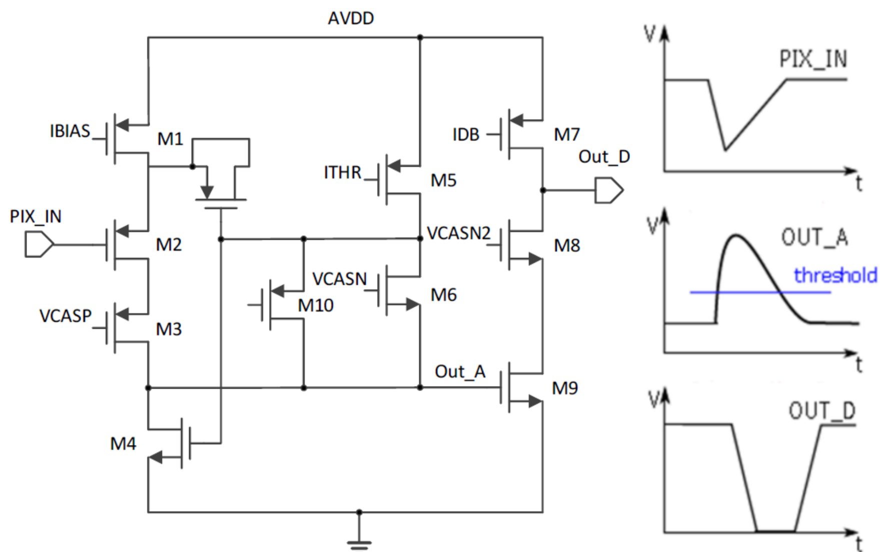
# Patent（专利）

1. 魏晓敏, 张浩楠,王佳,薛菲菲,郑然,胡永才. 一种树状组织的缓存结构及其应用. CN: 2021.11130545.6，2021-11-5
2. 魏晓敏, 张浩楠, 王佳, 郑然, 薛菲菲, 蔡耀, 胡永才. 一种粒子图像的数据压缩电路和数据压缩方法, CN202210632037.0，2022-06-07
3. 王佳, 杨聚鑫, 郑然, 魏晓敏, 薛菲菲, 胡永才. 一种小面积快速瞬态响应全片上集成LDO电路, CN202111161887.9，2021-9-30
4. 郑然, 李志军, 王佳, 魏晓敏, 薛菲菲, 胡永才. 一种静态功耗自动配置的低功耗前端读出电路及设计方法, CN202111087544.2，2021-9-16
5. 薛菲菲, 黄雪蕾, 郑晓亮, 魏晓敏, 王佳, 郑然, 胡永才.一种电荷型逐次逼近ADC结构, CN202111089036.8，2021-9-16

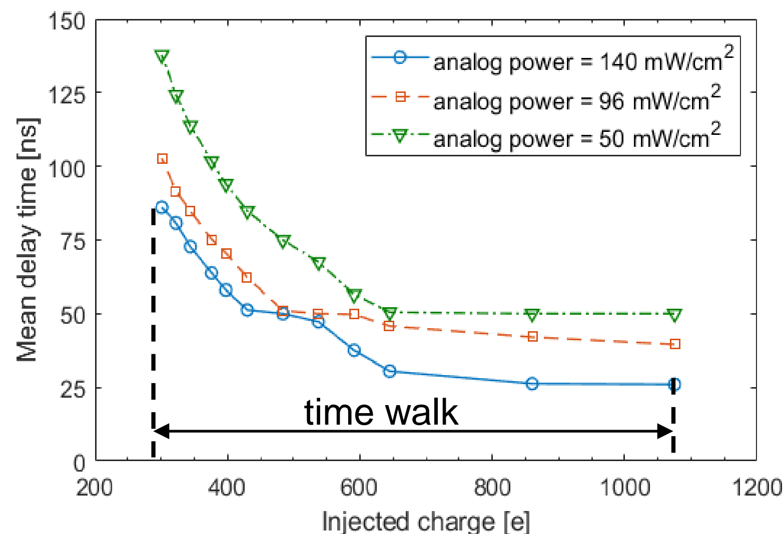
# Pixel analog front-end

- **Based on ALPIDE* front-end scheme**
  - modified for faster response
  - 'FASTOR' signal delivered to the EOC (end of column) when a pixel fired, timestamps of hit recorded at pos. edge of 'FASTOR'



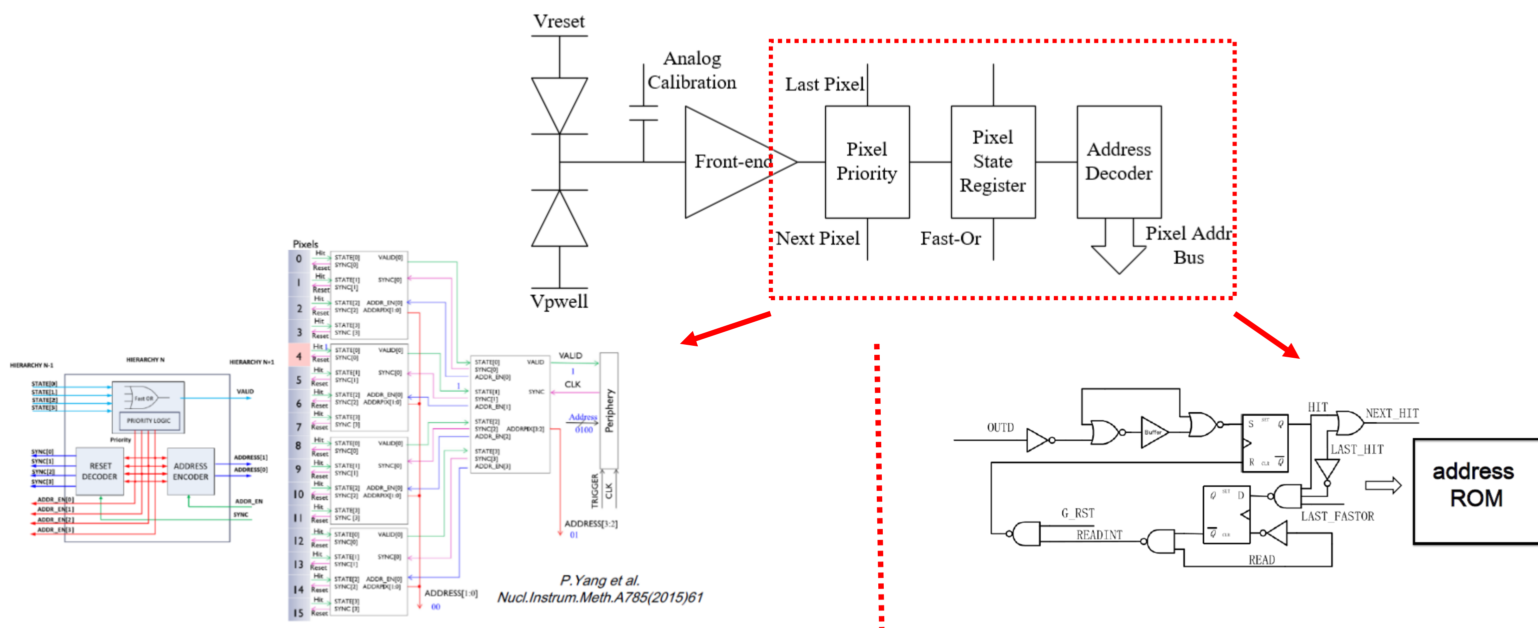

Schematic of pixel front-end




Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

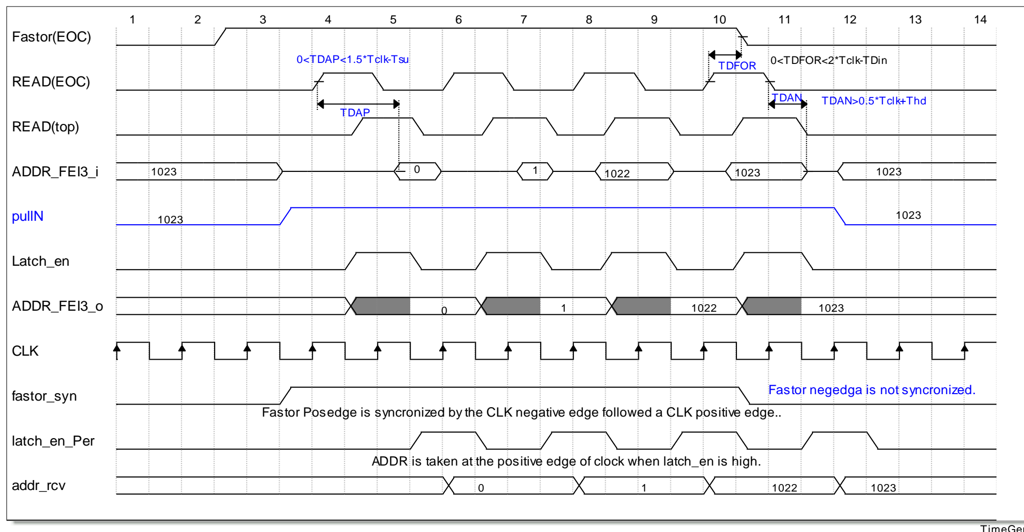
*Ref: D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

# Pixel architecture – parallel digital schemes



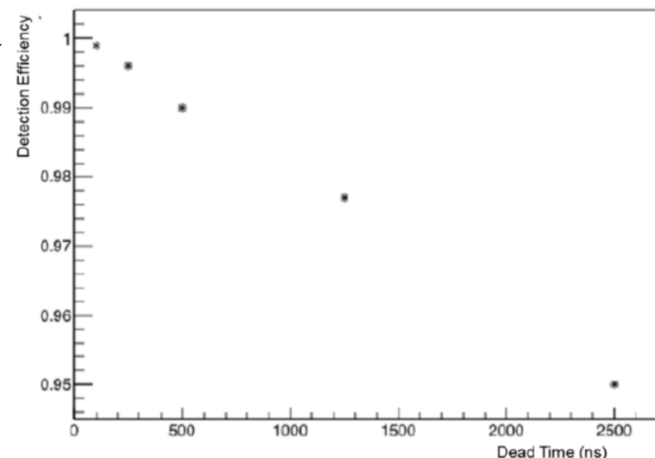

- Simplified column-drain readout:
  - Each double column shares a common Fast-Or bus for hit indication
  - Common time stamp register @40MHz will record the hit arrival time
  - Hit pixels in the same cluster will share a common time stamp as the Trigger ID
- Two parallel digital readout architectures were designed:
  - Scheme 1： ALPIDE-like: benefit from the proved digital readout in small pixel size
    - Readout speed was enhanced for 40MHz BX
  - Scheme 2： FE-I3-like: benefit m the proved fast readout @40MHz BX (ATLAS)
    - Fully customized layout of digital cells and address decoder for smaller area

# Readout & Periphery

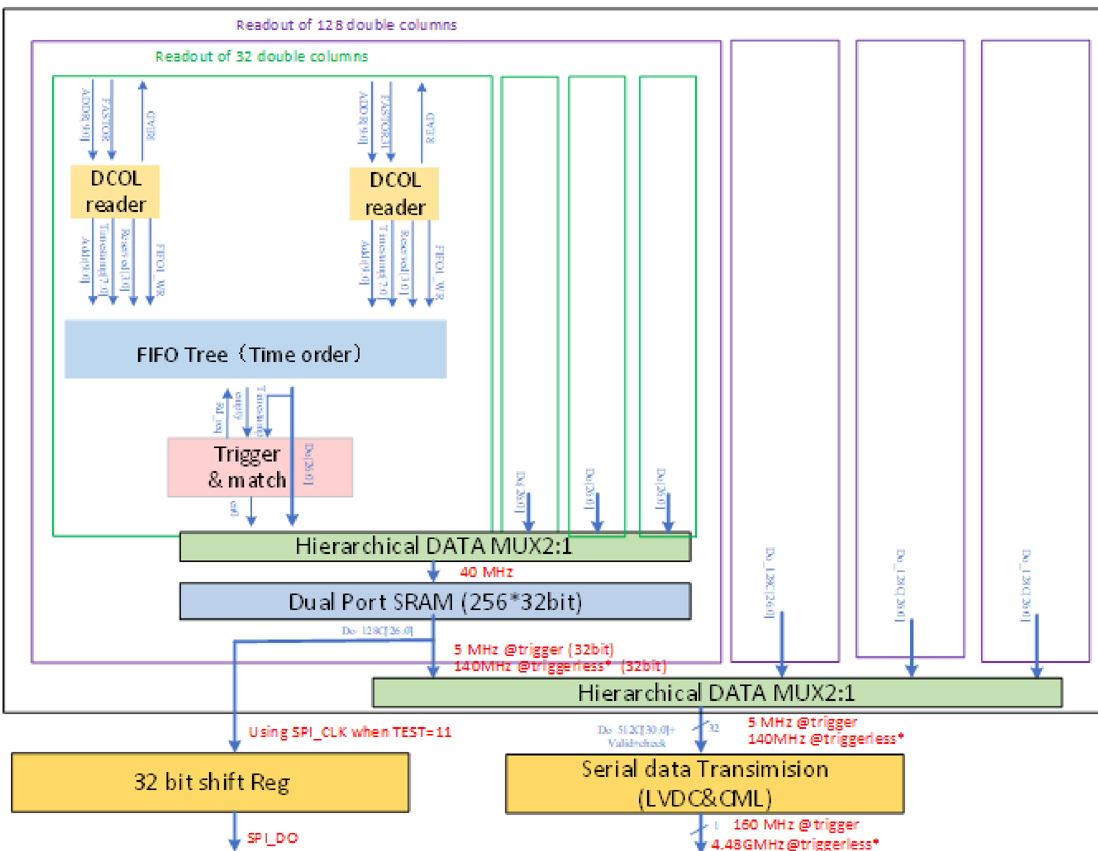



- Time stamp recorded when Fastor is valid
- Each pixel readout by 2 clocks (50ns)
  - Worst delay ~ 25ns
    - Sim by 512 rows (full size)
    - TDA: read sent –addr come
  - Address latch @ 37.5ns
    - @1.5 clock
    - Enough headroom for all corners

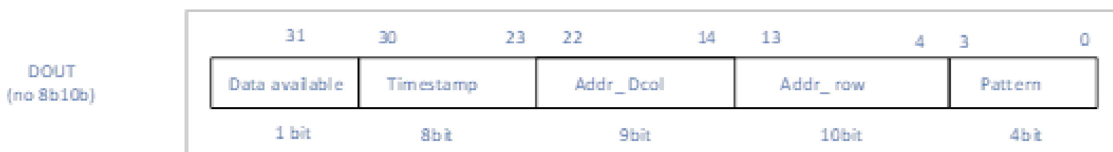
- Designed for low power
  - Only the hit (fastor) info & address are fannout from the pixel array
  - Only the read (acquisition) signal is fanned in to the pixel array
    - Clock & time stamp are localized only in the EOC, different from FE-I3
- Optimized @ CEPC hit rate
  - Common time stamp recorded for a full double column
    - For low power
    - Column is hit every 8.3us / pixel is readout in 2 clocks (50ns) / cluster size 3 pixels
    - Dead time 500ns – 98% trigger efficiency



# Readout & Periphery on 2 level FIFOs

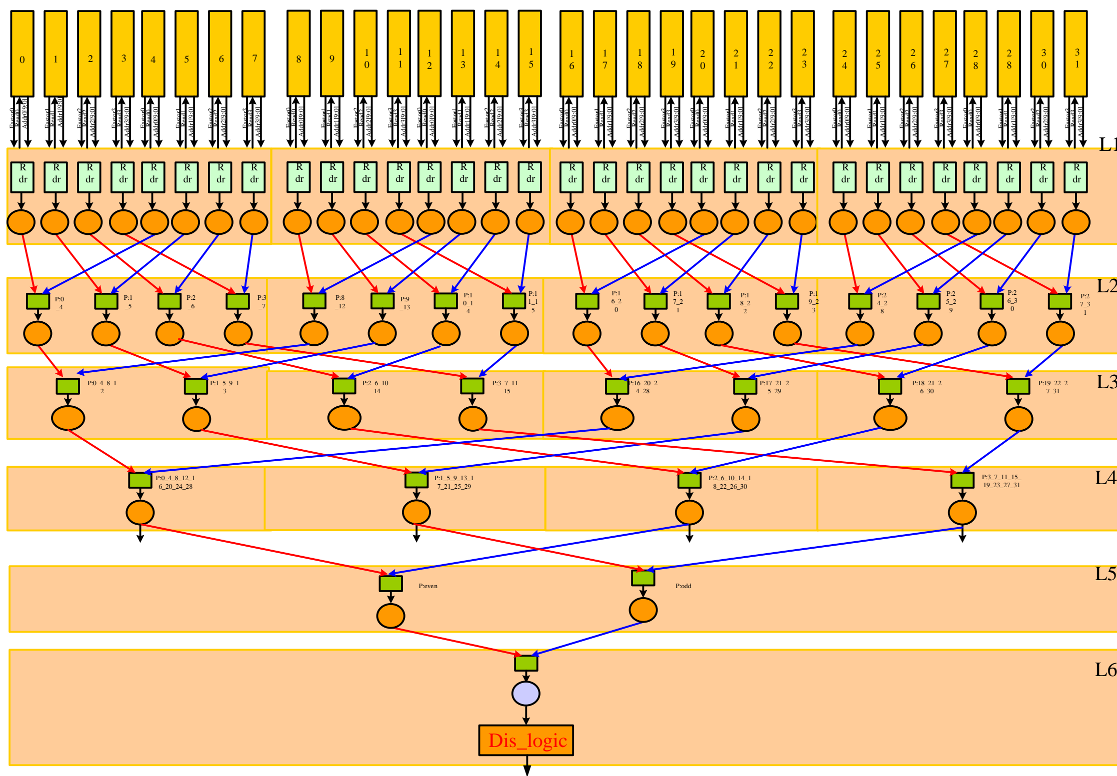


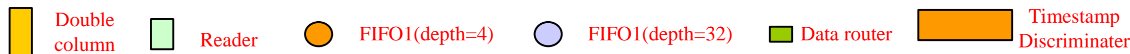

* When 8b10b encoading is enable, valid data bandwidth is 70MHz due to some filling code.




- **FIFO1 group for 32 DCols**
  - Limited by the 25um pitch
  - Depth ≈ 9 *22bits (8+10+4)
  - Row-level priority readout to group interface
- **FIFO2 for 4 FIFO1-Group**
  - Round-robin in 4 groups by data mux
  - DualPort SRAM for each FIFO2
  - Depth 256 * 32bits
- **Serializer interface with PLL & CML/LVDS**
  - Trigger mode @160Mbps LVDS max
  - Triggerless mode @ 4Gbps CML max

# FIFO Tree for 32Dcol



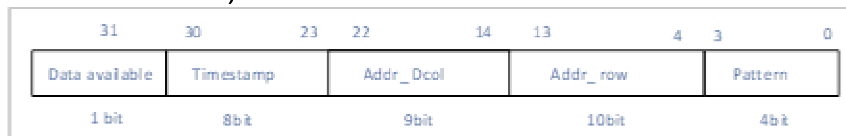




- **Motivation:**
  - **Share the storage volume**
  - **Reduce the area and optimize clock tree**
- **FIFO volumn：288**
  - L1-L5：4
  - L6: 32
- **Router：**
  - Timestamp priority

# Trigger & triggerless readout

- **A window can be set to cover the trigger uncertainty**
  - Time walk, jitter, …
  - By default a ±3LSB(=±75ns) window is set (=7LSBs),
  - Pixel analog's speed is set with the window correspondingly (for low power or high time resolution )

DOUT
(no 8b10b)

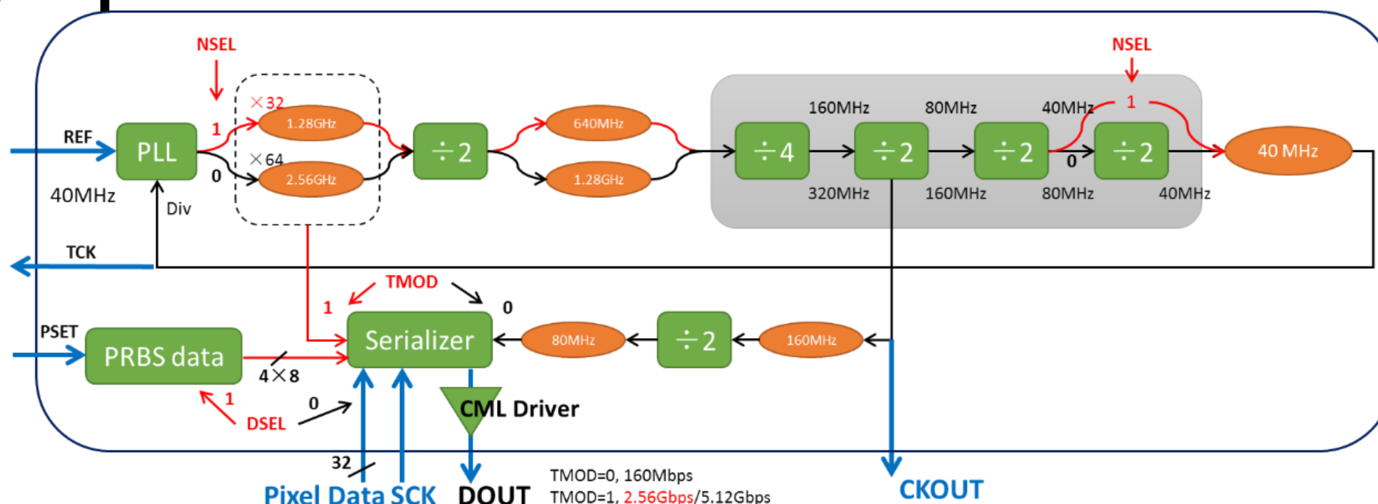


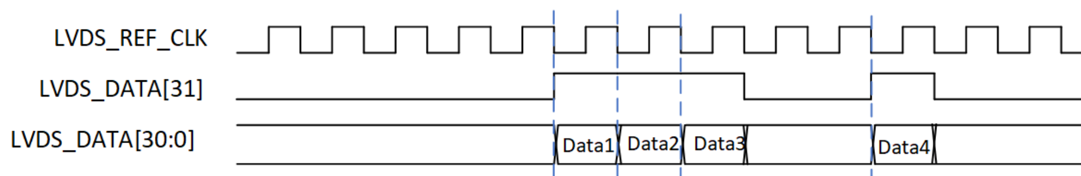

DOUT1
(with 8b10b, first part)

DOUT2
(with 8b10b, second part)

- **8 bit time stamp can cover a range of 6.4us @ 40MHz**
- **Designed for trigger readout by default**
  - Considering the non-overlapped time stamps, estimated trigger latency is ~3us maximum
  - Trigger ID calc. by the trigger's time stamp – latency
  - Only matched event be readout
- **All the raw data can also be readout in triggerless mode**
  - 8b10b encoder added for balanced bitstream at Gbps
    - Limited by the 32bit serializer, a 32-bit data is encoded in two words
      - Discussion in the following part
    - Each with 20bit encoded info and 12bit dummy
    - When data is invalid, k28.5 code will be sent for data alignment

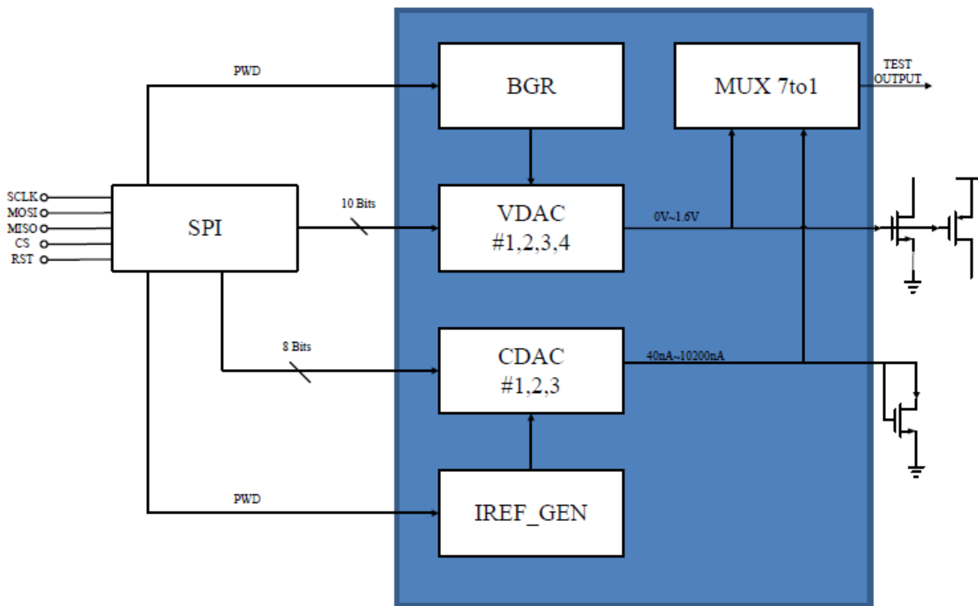
# High speed serial link

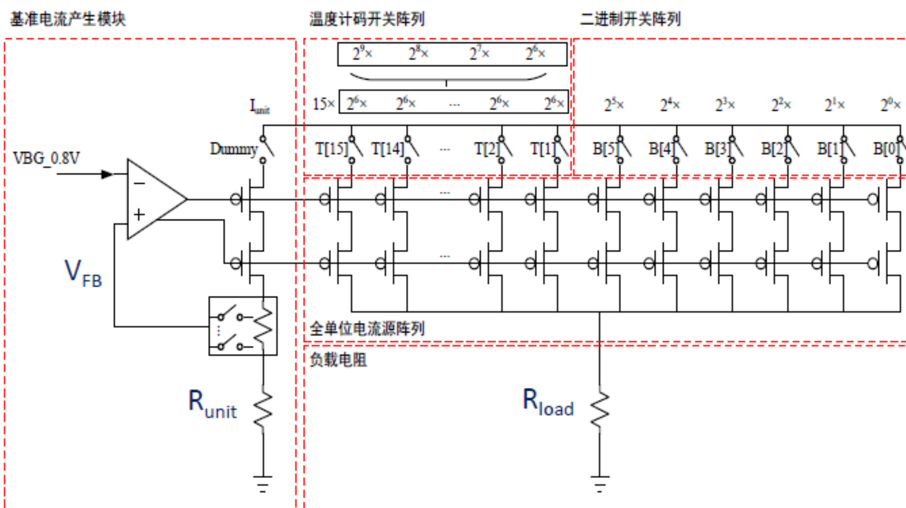


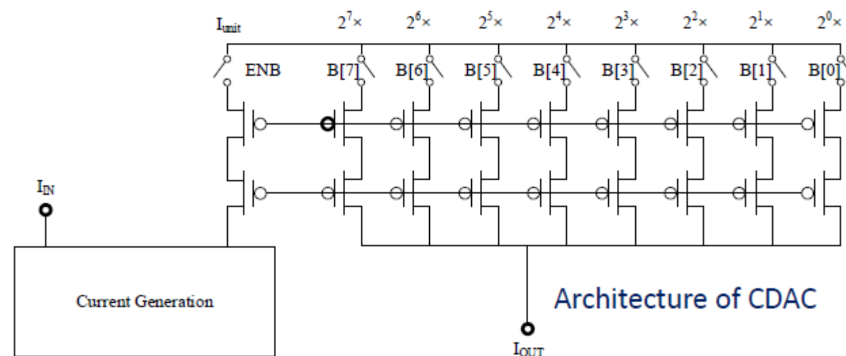

- **High speed clock is generated by the on-chip PLL**
- **Serializer is based on balanced 2：1 Mux architecture**
  - ✔： Benefit for the speed at high clock frequency
  - ✘： Length of the Ser cannot be configured
- **By default, 160Mbps data rate (plain code w/o 8b10b) will be set**
  - MSB D<31> will be used for data synchronization, independently output
  - CML (Gbps) / LVDS (≤160Mbps, in engineering run) optional for optimized power

# Bias generation



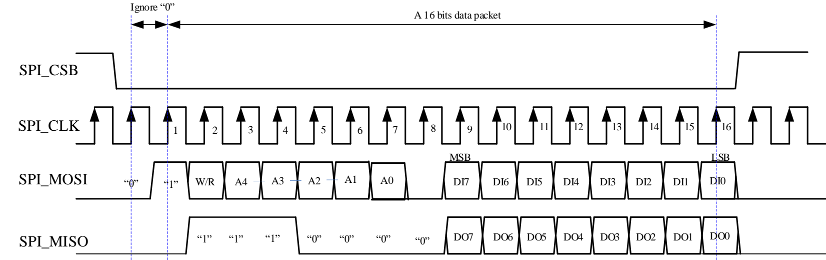




- **Structure of the DAC**
  - Voltage DAC (VDAC)
  - Current DAC (CDAC)
  - Bandgap(BGR)
  - MUX 7 to 1
  - Current bias reference generation
- **Characteristics**
  - Voltage DAC (VDAC)
    - 10 bit
    - LSB:1.56 mV
    - Range:0~1.6 V
  - Current DAC (CDAC)
    - 8 bit
    - LSB:40 nA for common, 0.1nA for ITHR
    - Range:0 nA~10.2 μA




Architecture of CDAC

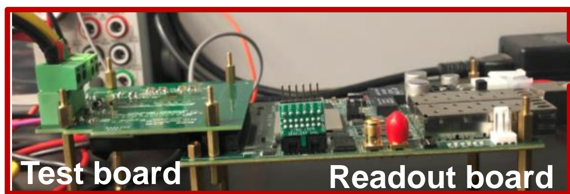
# Chip slow control scheme

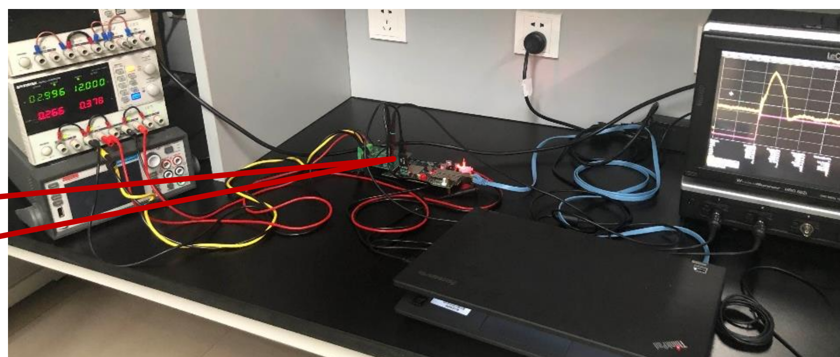


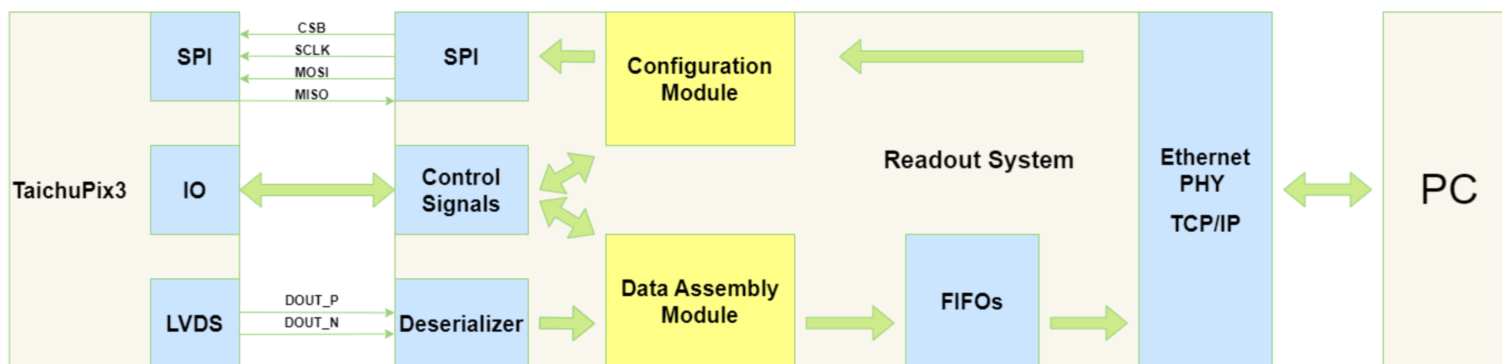

- **All the configuration bits can be loaded by the common SPI interface controlled in the Periphery block**
  - Chip global operation mode
  - DAC bias tuning
  - PLL status
  - Pixel matrix CalEn/Mask bits
- **Standard SPI protocol designed, 8 bits loading each time**
- **Pixel matrix slow control by two steps**
  - Write one row by SPI, 8 cols each time
  - Generate a shift clock by SPI, 1clk each time
  - Send a load pulse, depending on CalEn/Mask configuration
  - Problem left to be solved: matrix configuration speed should be speed up by backend electronics

# Readout system of TaichuPix chips

- **Readout system for single-chip includes**
  - A dedicated test board for chip wire-bonding and power link
  - A readout board loaded with a FPGA to perform chip configuration and data readout
  - A DC power supply
  - A PC



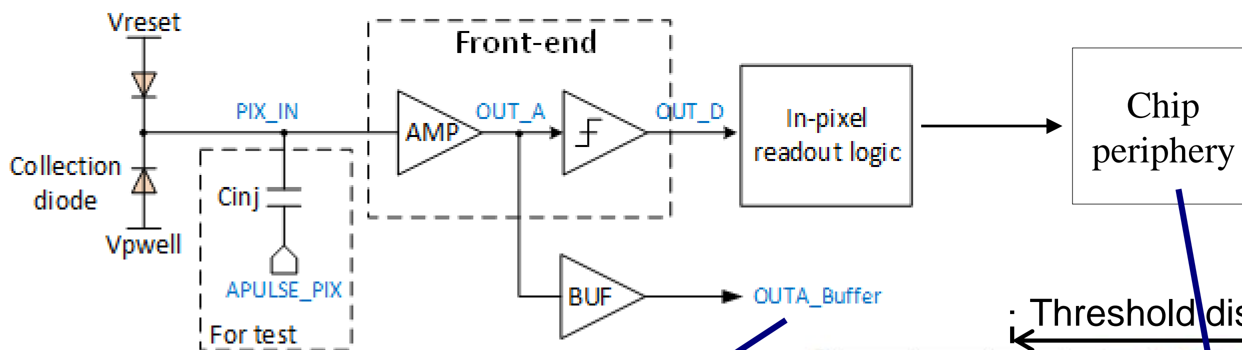



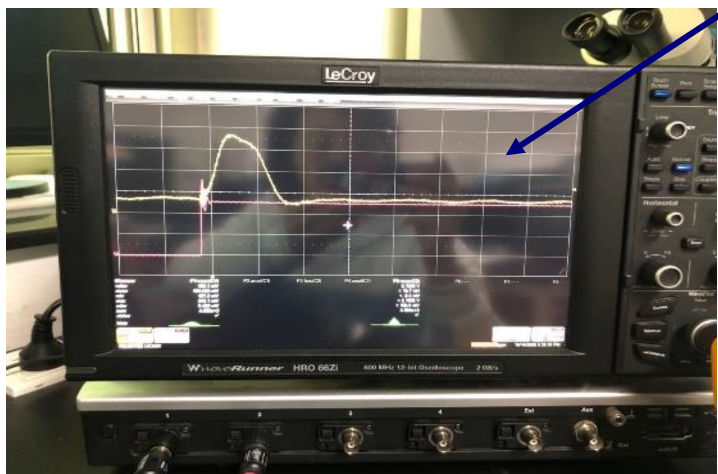



Structure of the readout system

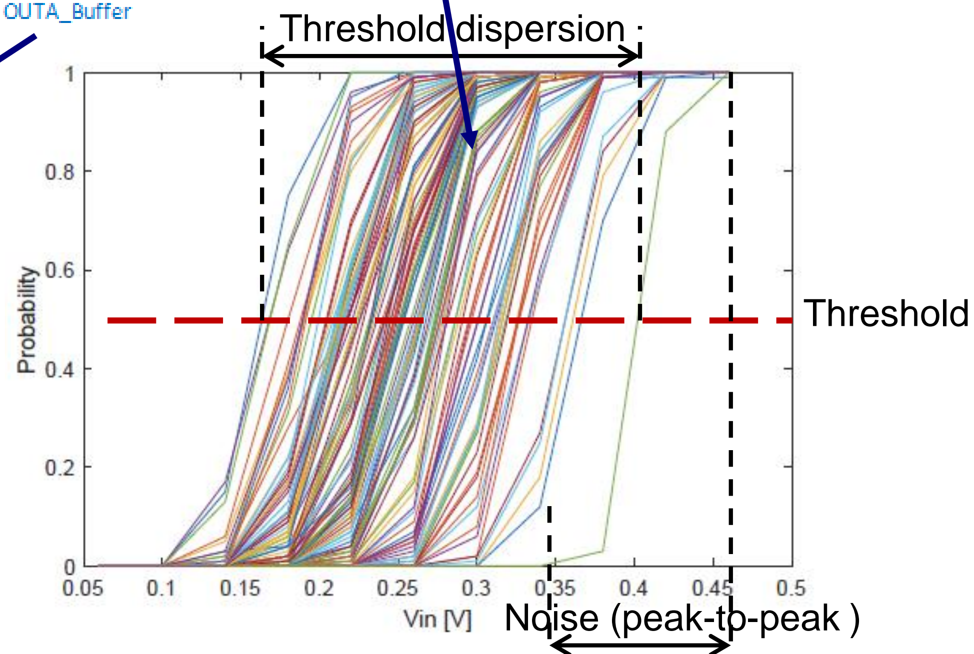
# Electrical test

- **Electrical performance verified by injecting external voltage pulses into pixel front-end**



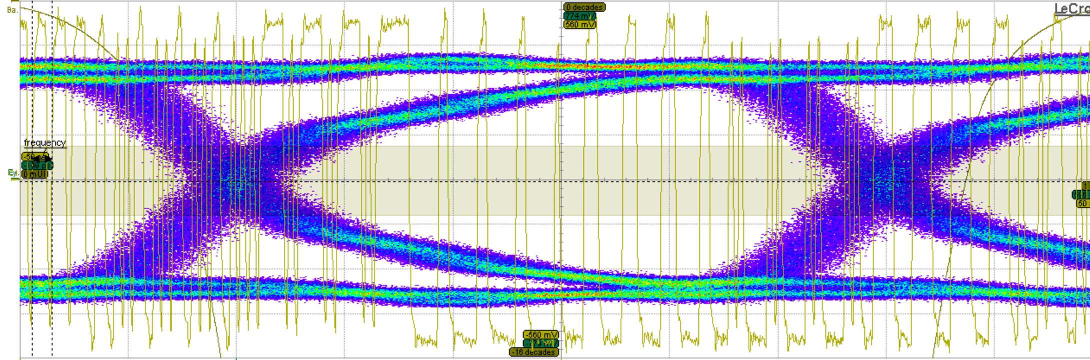




Analog output of a pixel @ Vin = 0.9 V




Measured “S-curve” for 128 pixels

# Test of the data interface (TaichuPix-1)



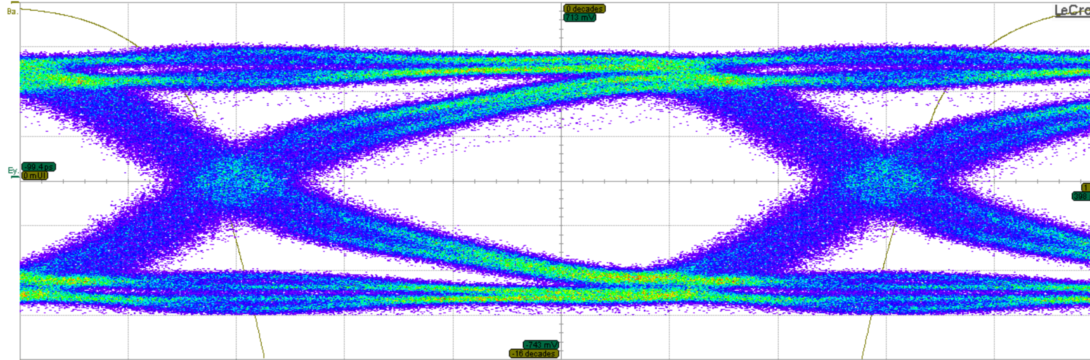
| Measure | P1:freq(C1) | P2:ampl(C1) | P3:base(C1) | P4:top(C1) | P5:ermsj(Eye) | P6:eppj(Eye) | P7:Q(Eye) | P8:pdcd(Eye) | P9:- - - | P10:- - - | P11:- - - | P12:- - - |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 1.12160 GHz | 989.6 mV | -500.4 mV | 489.2 mV | 15.7 ps | 106.3 ps | 8.5436 | 39e-3 | | | | |
| mean | 697.1421 MHz | > 968.105 mV | < -486.665 mV | > 481.440 mV | 15.679 ps | 106.297 ps | 8.543586 | 39.08e-3 | | | | |
| min | 170.92 MHz | > 928.4 mV | < -502.7 mV | > 463.4 mV | 15.7 ps | 106.3 ps | 8.5436 | 39e-3 | | | | |
| max | 1.15117 GHz | > 995.3 mV | < -459.0 mV | > 493.3 mV | 15.7 ps | 106.3 ps | 8.5436 | 39e-3 | | | | |
| sdev | 288.6860 MHz | > 18.188 mV | < 12.536 mV | > 8.534 mV | --- | --- | --- | --- | | | | |
| num | 8.676e+3 | 155 | 155 | 155 | 1 | 1 | 1 | 1 | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ⇕ | ⇕ | ⇕ | ⇕ | | | | |

| SDA Jitter | Tj(1e-12) | Rj(sp) | Dj(sp) | BitRate | Pj | ISI | DCD | DDj | |
|---|---|---|---|---|---|---|---|---|---|
| value | 141.63 ps | 5.39 ps | 64.77 ps | 2.2400 Gbit/sec | 15.80 ps | 45 ps | 3 ps | 48 ps | |
| status | ⇕ | ⇕ | ⇕ | ✓ | ⇕ | ✓ | ✓ | ✓ | |
| **SDA Eye** | EyeHeight | EyeOne | EyeZero | EyeAmpl | EyeWidth | EyeCross | EyeAvgPwr | MaskHits | EyeBER |
| value | 583.5 mV | 441.8 mV | -457.5 mV | 899.3 mV | 352.2 ps | 49.66 % | 2.2 mV | 1.363091e+6 | 6.59283502e-18 |
| status | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ |

C1 DC 140 mV/div 0.0 mV ofst | Eye 194 mV/div 75 ps/div 30.397 k# | BathTub 2.0 decades 100 mUI/div 14.563 k#

Timebase 0.0 ns 10.0 ns/div 2.00 kS 20 GS/s | Trigger C3 DC Stop 640 mV Edge Positive

@2.24Gbps



| Measure | P1:freq(C1) | P2:ampl(C1) | P3:base(C1) | P4:top(C1) | P5:ermsj(Eye) | P6:eppj(Eye) | P7:Q(Eye) | P8:pdcd(Eye) | P9:eppj(Eye) | P10:- - - | P11:- - - | P12:- - - |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 1.1076 GHz | > 889.8 mV | < -460.9 mV | 428.9 mV | 16.2 ps | 115.0 ps | 7.0496 | 18e-3 | | | | |
| mean | 1.036750 GHz | > 903.732 mV | < -466.151 mV | > 437.581 mV | 16.212 ps | 115.034 ps | 7.049625 | 18.14e-3 | | | | |
| min | 255.2 MHz | > 850.4 mV | < -541.6 mV | > 349.8 mV | 16.2 ps | 115.0 ps | 7.0496 | 18e-3 | | | | |
| max | 1.8142 GHz | > 979.1 mV | < -421.1 mV | > 483.3 mV | 16.2 ps | 115.0 ps | 7.0496 | 18e-3 | | | | |
| sdev | 447.550 MHz | > 26.016 mV | < 20.392 mV | > 14.592 mV | --- | --- | --- | --- | | | | |
| num | 14.389e+3 | 173 | 173 | 173 | 1 | 1 | 1 | 1 | | | | |
| status | ⇓ | ⇓ | ⇓ | ⇓ | ⇕ | ⇕ | ⇕ | ⇕ | | | | |

| SDA Jitter | Tj(1e-12) | Rj(sp) | Dj(sp) | BitRate | Pj | ISI | DCD | DDj | |
|---|---|---|---|---|---|---|---|---|---|
| value | 123.27 ps | 4.84 ps | 54.26 ps | 3.3600 Gbit/sec | 7.15 ps | 51 ps | 1 ps | 51 ps | |
| status | ⇕ | ⇕ | ⇕ | ✓ | ⇕ | ⇓ | ⇓ | ⇓ | |
| **SDA Eye** | EyeHeight | EyeOne | EyeZero | EyeAmpl | EyeWidth | EyeCross | EyeAvgPwr | MaskHits | EyeBER |
| value | 479.8 mV | 404.1 mV | -431.1 mV | 835.2 mV | 200.3 ps | 50.01 % | -11.4 mV | 1.524591e+6 | 914.388622e-15 |
| status | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ | ⇕ |

Eye 182 mV/div 49.7 ps/div 51.015 k# | BathTub 2.0 decades 100 mUI/div 24.548 k#

Timebase 0.0 ns 10.0 ns/div 2.00 kS 20 GS/s | Trigger C3 DC Stop 640 mV Edge Positive

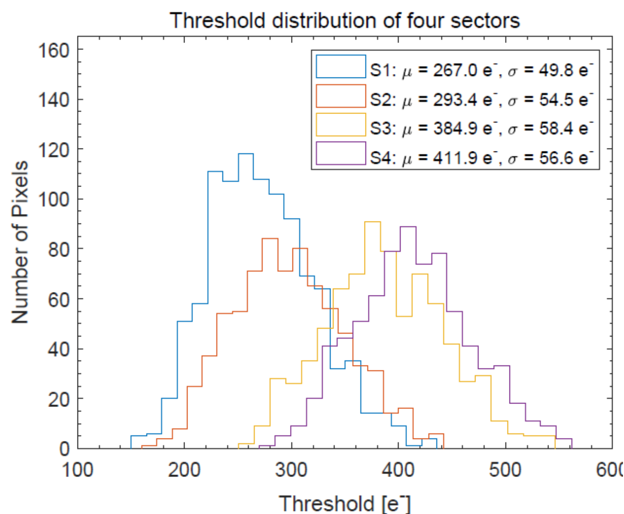
@3.36Gbps

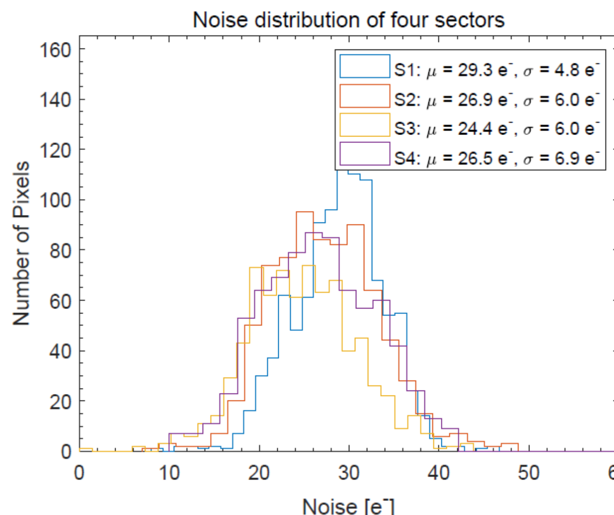
| Bit rate | 2.24Gbps | 3.36Gbps | 4.48Gbps |
|---|---|---|---|
| Clk freq | 1.12GHz | 1.68GHz | 2.24GHz |
| BER | 6.59e-18 | 9.14e-13 | 3.23e-5 |
| Tj@e-12 | 141.63ps | 123.27ps | 147.14ps |
| Rj | 5.39ps | 4.84ps | 5.35ps |
| Dj | 64.77ps | 54.26ps | 70.90ps |

- **Data readout in DDR mode**
- **Data interface was tested by the on-chip PRBS source, a high speed oscilloscope (@16Gsps), and code stream verified in FPGA**
- **BER qualified till 3.36 Gbps, failed at 4.48 Gbps**
- **Concerning the highest data rate for triggerless at 4 Gbps, at least 2 SER interface ports needed**
- **Thus bit rate @2.24 Gbps is safe and power optimized**

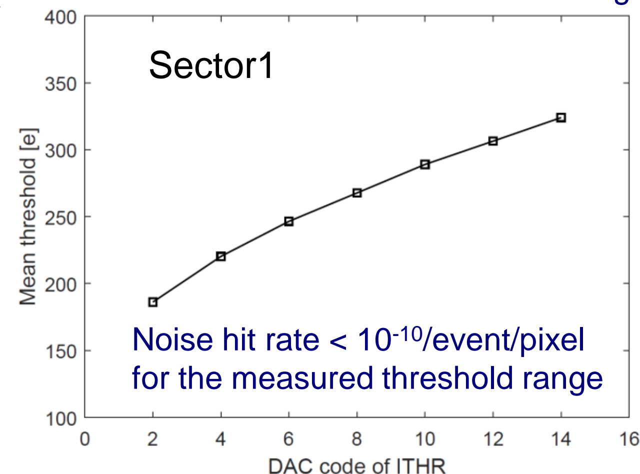
# Performance of threshold and noise of TaichuPix2

- **Pixel array includes 4 sectors with different transistor parameters/layout for analog front-end, S1 chosen for the full-scale design.**
- **Threshold can be tuned by changing 'ITHR' (a global current bias)**



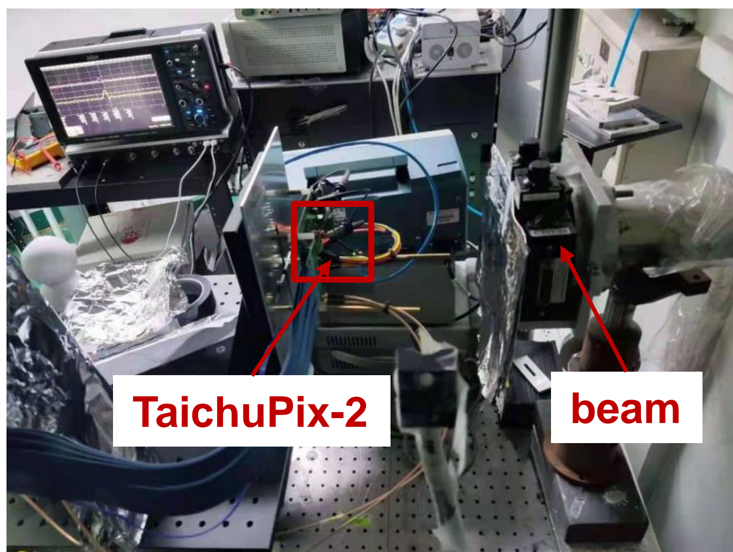

Mean threshold of Sector1 vs. ITHR setting



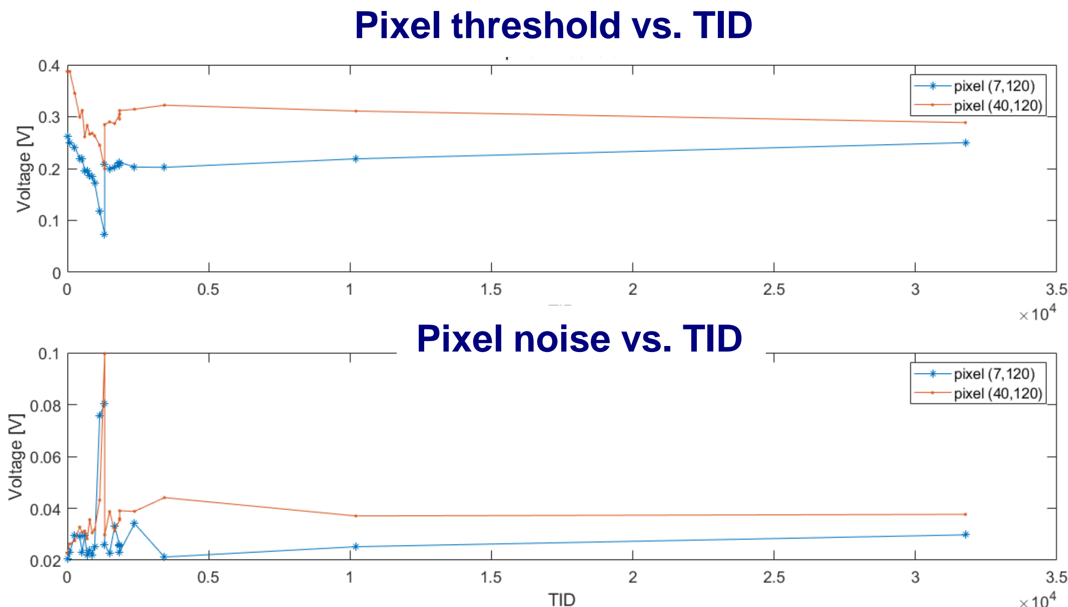

Noise hit rate < $10^{-10}$/event/pixel for the measured threshold range

| Chip4 | Threshold Mean ($e^-$) | Threshold rms ($e^-$) | Temporal noise ($e^-$) | Total equivalent noise ($e^-$) |
|---|---|---|---|---|
| S1 | 267.0 | 49.8 | 29.3 | 57.8 |
| S2 | 293.4 | 54.5 | 26.9 | 60.8 |
| S3 | 384.9 | 58.4 | 24.4 | 63.3 |
| S4 | 411.9 | 56.6 | 26.5 | 62.5 |

# TID test on TaichuPix-2




TaichuPix-2 irradiated at BSRF 1W2B beamline (6 keV X-ray)



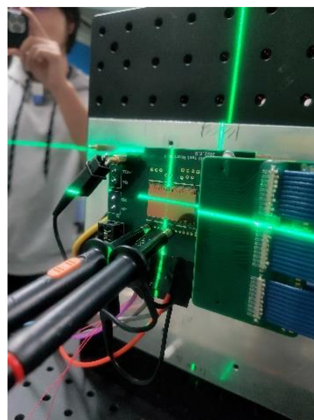

- Chip was exposed with full working condition: power, bias, clk, …
- Dose rate ~17.63 krad/min for the first 2.5 Mrad, then 211.56 krad/min for 51 min, then 1.24 Mrad/min for 15 min
- **Normal chip functionality and good noise performance proved up to 30 Mrad TID**

# TID test on TaichuPix-3

**Beamline Specs**

| Source | Wiggler |
|---|---|
| Energy Range | 5-18 keV |
| Resolution (ΔE/E) | Over $4 \times 10^{-4}$ |
| Flux (photons/sec) | $10^{12}$ |
| Beam Size (HxV) | 1mm x 0.6 mm |

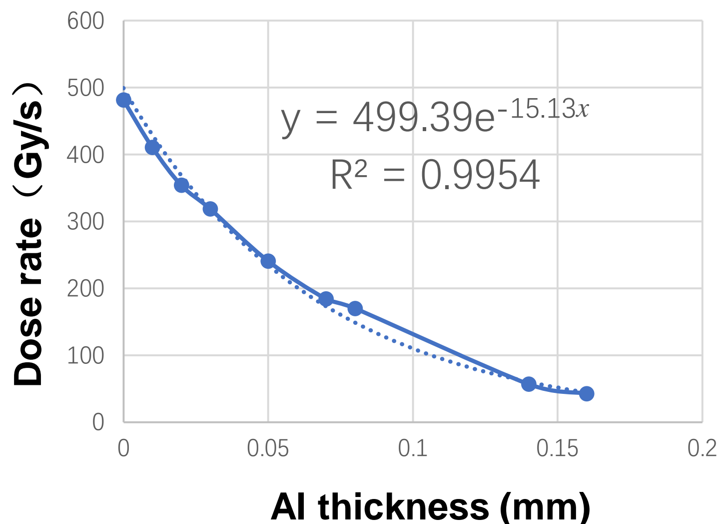
**Beamline Specifications**



**Analog signal of the pixel monitored by the oscilloscope**

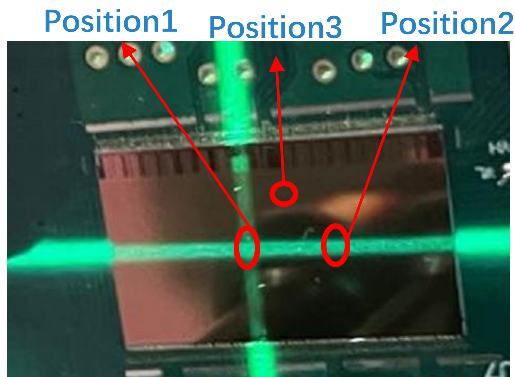
| Aluminum (Al) | Irradiation dose rate |
|---|---|
| 96 layers | 0.02rad/s |
| 64 layers | 3 rad/s |
| 32 layers | 394 rad/s |
| 28 layers | 722 rad/s |
| 24 layers | 1321.6 rad/s |
| 1 layers | 42927 rad/s |

**Attenuation of Aluminum (thickness of Al foil is 0.01 mm/layer)**

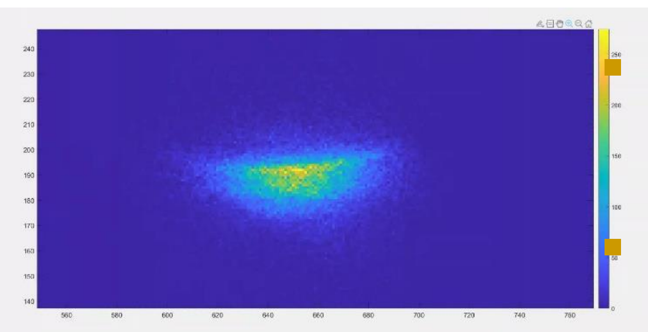



- The energy of X-ray is set to 12 KeV
- Ionization chamber is used to calibrate irradiation dose rate
- The irradiation dose is regulated by aluminum foil

# TID test on TaichuPix-3




TaichuPix-3 irradiated at BSRF 1W2B beamline (12 keV X-ray)



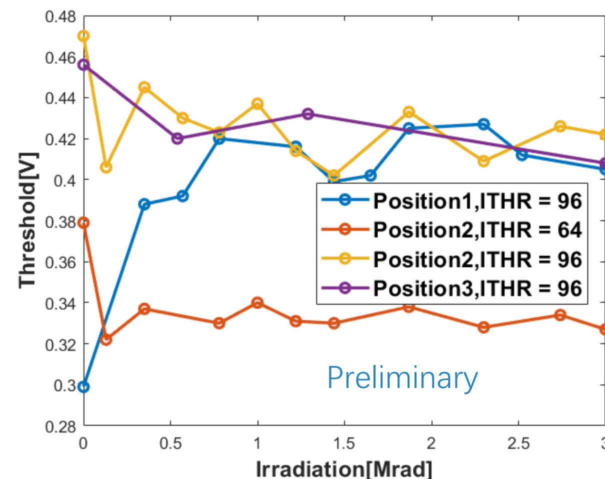
Full image of the X-ray beam spot(position 1)

- **Chip was exposed with full working condition: power, bias, clk, …**
- **Dose rate ~1.2 rad/min for the first 12 min, in order to find the position of beam spot.**
  → The size of beam spot agrees with the expectation of 1 mm × 0.6 mm

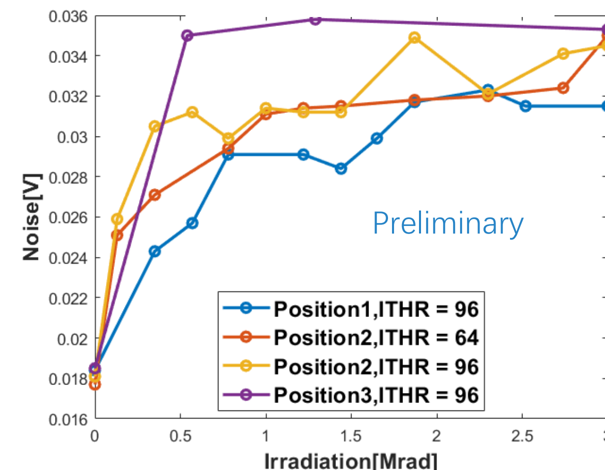
**Dose rate ~43.3 krad/min for 69 min until total dose over 3 Mrad.**

**All three irradiation regions indicated a good performance to 3 Mrad TID**

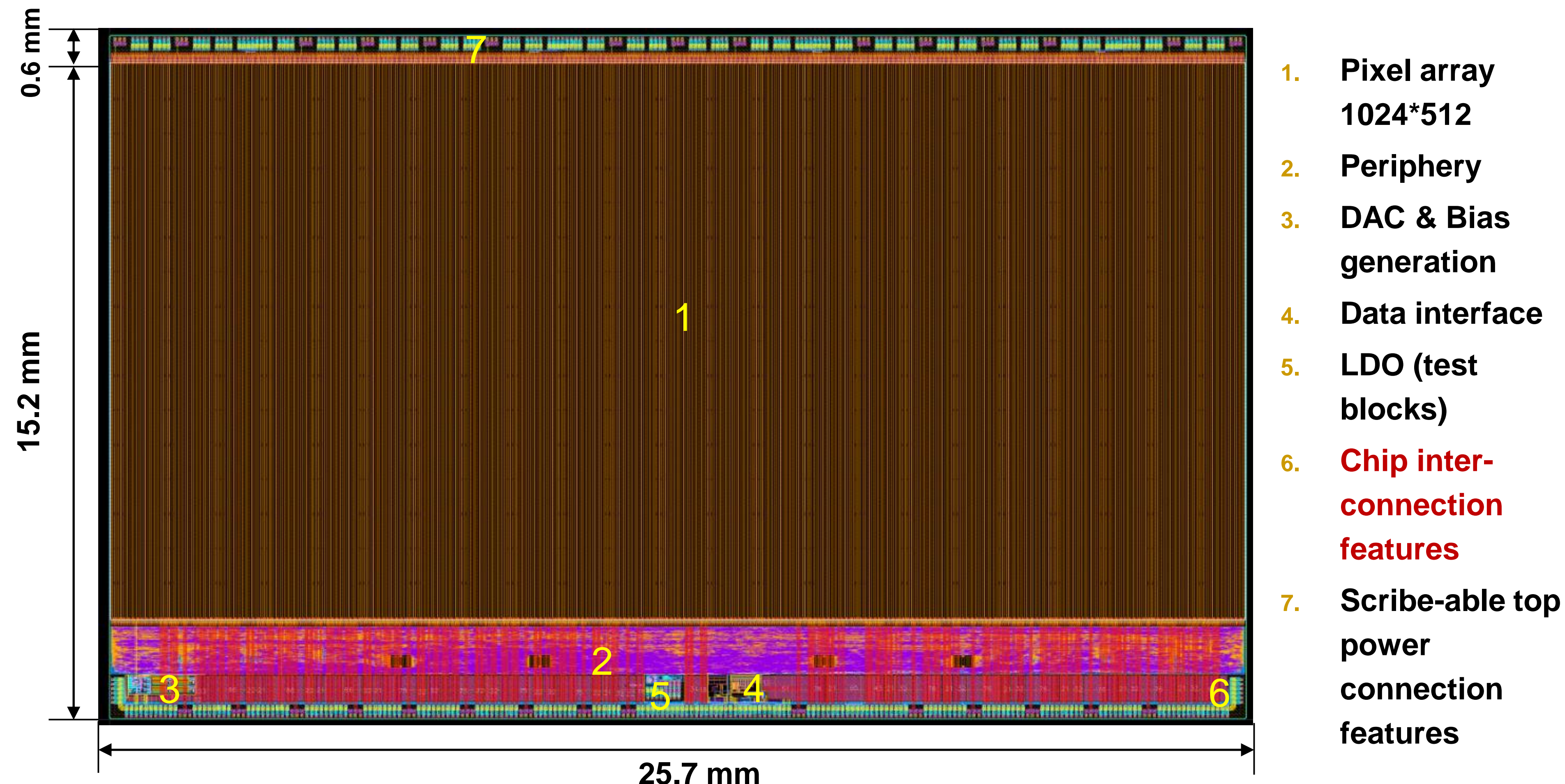
**Pixel threshold vs. TID**




**Pixel noise vs. TID**



# Overview of the full-scale prototype




- **Process: 180 nm CMOS Imaging Sensor process (7 metal layers)**
- **Pixel cell copied exactly from MPW + scaled logic with new layout Periphery + debugged/improved blocks + enhanced power network**

# Yield of TaichuPix-3

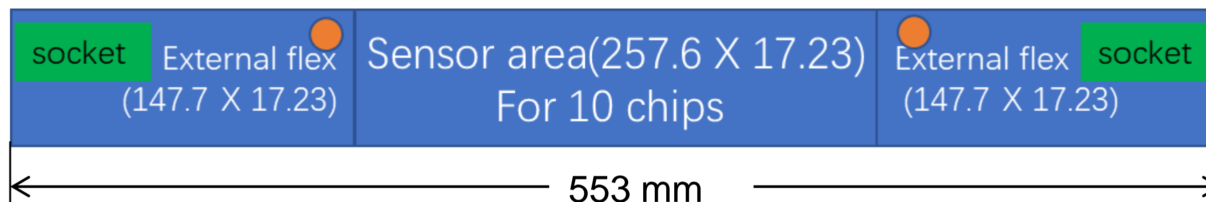
- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafer #1-6 from modified process, 7-12 from standard process**

| Wafer num. | Yield | Wafer num. | Yield |
|---|---|---|---|
| 1 | 0.65 | 4 | 0.475 |
| 2 | 0.725 | 5 | 0.625 |
| 3 | -- | 6 | 0.525 |
| 7 | 0.775 | 10 | 0.675 |
| 8 | 0.725 | 11 | 0.6 |
| 9 | 0.275 | 12 | 0.35 |

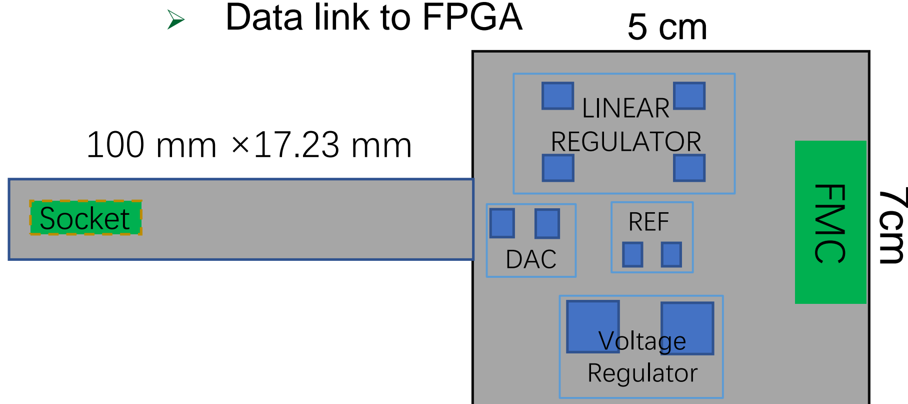
1st round (wafers 1–3, 7–9) — 2nd round (wafers 4–6, 10–12)

# Ladder readout design

- **Flex: for chip bonding and providing power & control bus**
  - Minimize material budget: limited height of flex, minimum set of signals
  - Robust power supply
  - Challenging in manufacture due to long and thin flex




- **Interposer board**
  - Provide power supply
  - DAC, reference, linear regulator
  - Data link to FPGA




- **FPGA board**

  - Communication with chips
  - Data processing and package data
  - Readout to PC via 1Gbps Ethernet
  - Capability of 6 Gbps readout and 2GB internal DDR memory

# Design of the flex board

|  |  |  |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|---|
|  | 12.5 | um | Coverlay | (yellow) |  |  |  |  |  |
|  | 20 | um | Coverlay Adhesive |  |  | Soldmask (green) |  |  |  |
| Layer 1 | 24 | um | ED Base Copper | 12 | um | um + | Plated | 18 | um |
|  | 13 | um | Polyimide (Adhesiveless) |  |  |  |  |  |  |
|  | 12.5 | um | Adhesive |  |  |  |  |  |  |
| Layer 2 | 12 | um | ED Base Copper | 12 | um |  |  |  |  |
|  | 25 | um | Polyimide (Adhesiveless) |  |  |  |  |  |  |
| Layer 3 | 12 | um | ED Base Copper | 12 | um |  |  |  |  |
|  | 12.5 | um | Adhesive |  |  |  |  |  |  |
|  | 13 | um | Polyimide (Adhesiveless) |  |  |  |  |  |  |
| Layer 4 | 24 | um | ED Base Copper | 12 | um | um + | Plated | 18 | um |
|  | 20 | um | Coverlay Adhesive |  |  |  |  |  |  |
|  | 12.5 | um | Coverlay | (yellow) |  |  |  |  |  |
| FPC厚度: | 213 | um | Spec: | 210 | um | +/- | 50 | um |  |

Ladder stack-up

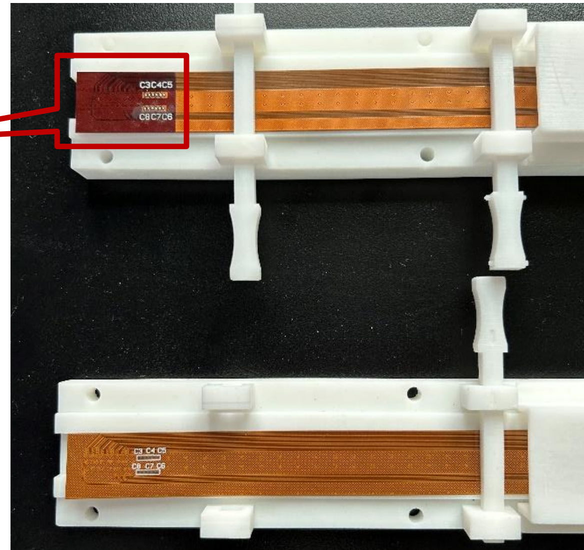
# Production of flex boards

- **Flexible board from FASTPRINT company**
  - Thickness: 0.162 mm (2-layer); 0.273 mm (4-layer);

- **Flexible board from Zsipak company**
  - Thickness: 0.161 mm for 2-layer; 0.213 mm for 4-layer

Old 4-layer
stiffener on
backside of socket

New 4-layer
No stiffener



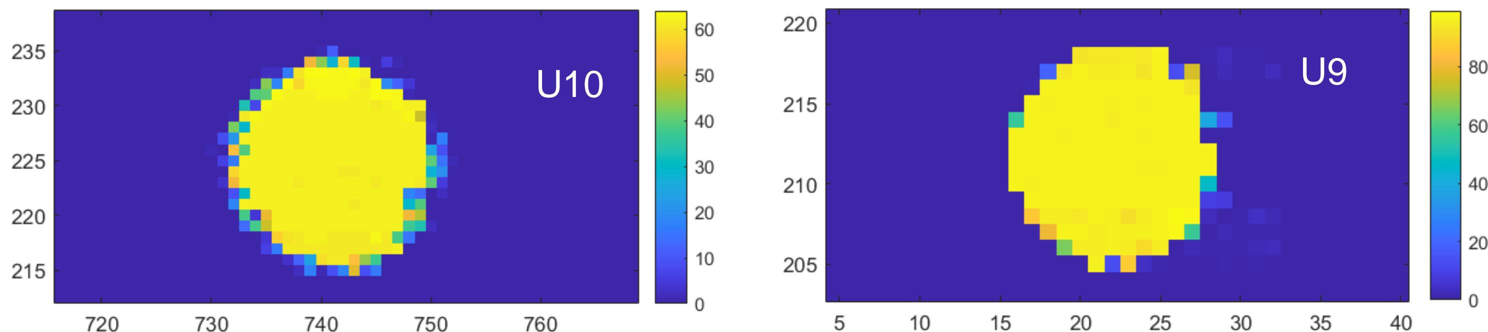
# TaichuPix-3 specification & performance

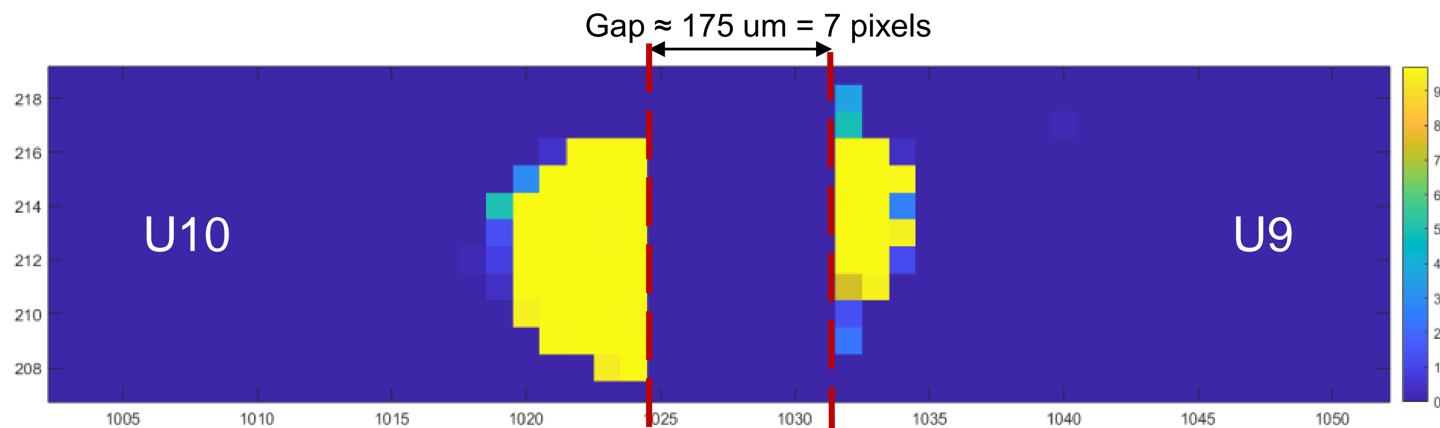
| | Design specs. | Measured |
|---|---|---|
| Spatial resolution* | 3~5 μm | 4.78 μm (best) |
| TID* | > 1 Mrad | > 3 Mrad |
| Pixel pitch | ≤ 25 μm | 25 μm |
| Chip size | ~1.4 × 2.56 $cm^2$ | 1.59 × 2.57 $cm^2$ |
| Dead time | < 500 ns | ~ 300 ns |
| Data rate | 110 Mbps (trigger)<br>3.84 Gbps (triggerless) | Not tested (trigger)<br>Currently 160 Mbps tested (triggerless) |
| Power density | < 200 $mW/cm^2$ | 89 – 164 $mW/cm^2$ @40 MHZ |

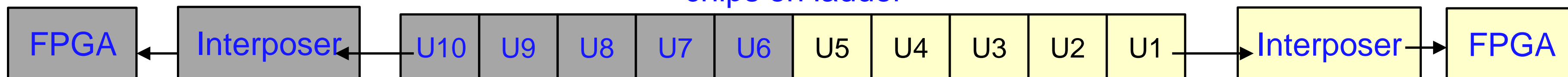
*project indicator

# Laser test result of ladder flex

- **Functionality of flex readout was first verified by two chips bonded**
  - Chips U10 & U9 can work independently
  - Two can work simultaneously, NO error code/cross-talk found



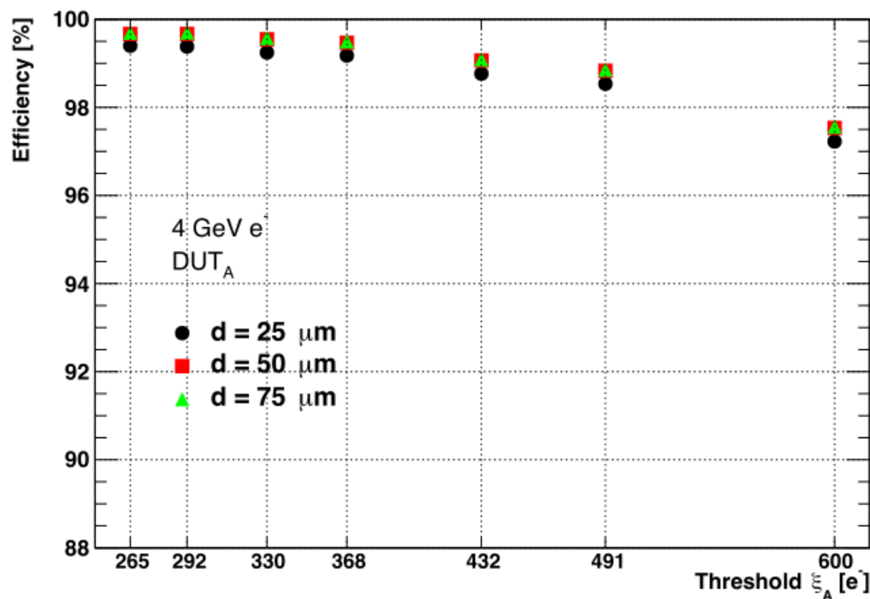



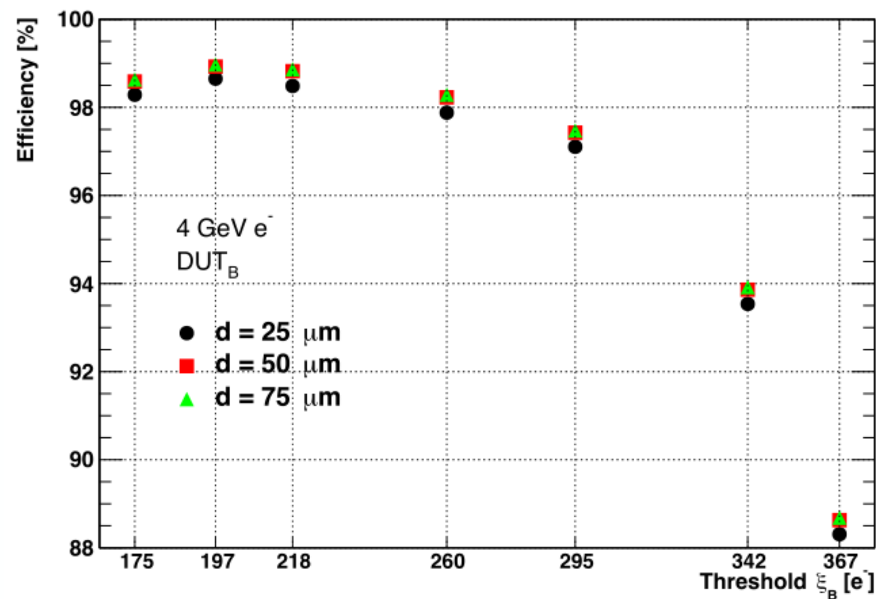
# TC3 beam test results

- **Detection efficiency vs. threshold (4 GeV)**
  - The efficiency decreasing with increasing threshold

$$\epsilon = \frac{N^{matched\ Tracks}_{|x_{meas},y_{meas}-x_{pre},y_{pre}|<d}}{N^{Tracks}_{tel}}$$

- Efficiency is the ratio of tracks that match the hit on the DUT within a distance d around the predicted hit from the telescope to all tracks of the telescope



# Design of DAQ

- **Considering 6 double-sided ladders**