环形正负电子对撞机
Circular Electron Positron Collider

中国科学院高能物理研究所
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Lessons learned and Future Plan (mainly on electronics)

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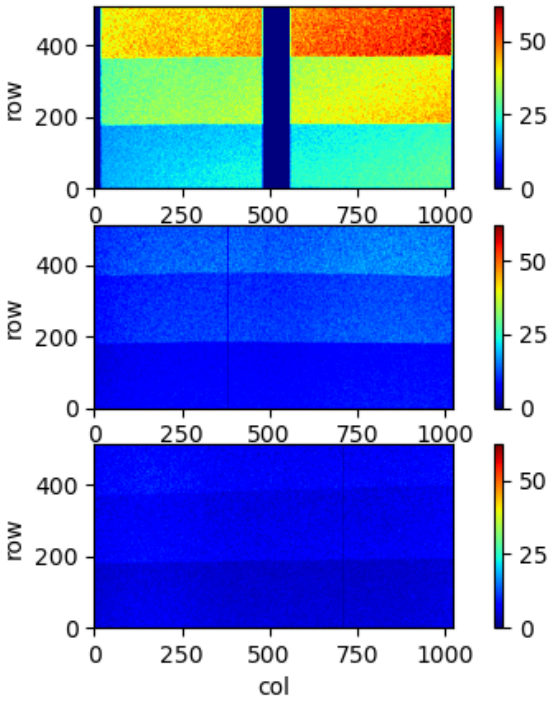
Outline

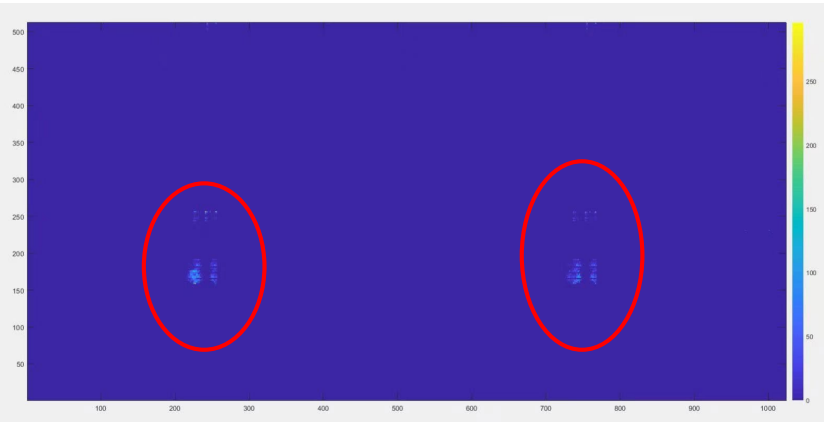
- **Known & to-be-known issues and possible solutions**
- **To do based on what we have**
- **Future plan with current TaichuPix**
- **Towards the next version of TaichuPix**

Known Issue – repeated counts



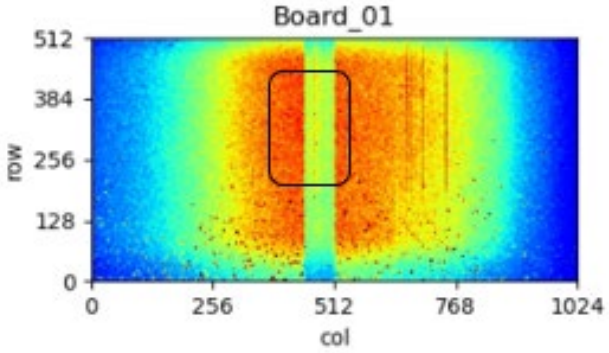
- **Higher rows will give repeated data for a single hit**
  - **The higher number, the more times**
- **The reason was understood**
  - **The fastor-clear(hit flag) is delayed due to the large matrix and long wire, then the periphery sees "multiple hits"**
    - **will only affect the last pixel in one hit-column**
- **Current solution**
  - **Repeated data was monitored in FPGA, redundant information was cancelled**
    - **No effect on resolution, only has impact on hit rate**
- **Solutions for future chip**
  - **Modify the fastor bus**

Known Issue – Ghost data pattern



- **Ghost data pattern can be found with column distance of 512/256/128……**
  - **Will be more serious on ladder**
- **Reasons almost certain**
  - **Imperfect timing constraint during the synthesis of periphery logic**
- **Current solution (imperfect)**
  - **Lower down the system clock from 40MHz -> 20MHz (test board) -> 15.6MHz (ladder), ghost disappeared**
- **Solutions for future chip**
  - **More refined constraint on circuit synthesis**

Known Issue – 32 cols lose during working



- A set of columns(typically 32) will die after a period of working, can only be waken up by re-config.
- Reason still unclear
  - No corresponding structure (based on 32 columns) on chip can explain
- Current solution
  - Rely on data monitoring, reset after problem detection or a regular period
- Next step
  - More experiment needed to understand the issue, make it more predicable
    - Laser, Beta source test
    - Is it related to the hit rate and FIFO, as we suspected?

Known Issue – threshold raised with multi-chips

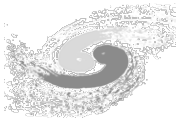
Flex num.	Chip pos.	Chip num.	Status	Min. ITHR
V1p3-L	U1, U2	W2R36, W1R37	Work	U1:128; U2: 128; U1&U2: 192&192
V1p3-M	U9, U10	W1R38, W1R41	Work	U10:96; U9:96; U9&U10: 224&224
V1p3-N	U9, U10	W9R34, W9R33	Work	U10:160; U9:160; U9&U10: 192&192
V1p3-O	U9, U10	W9R31, W9R30	Work	U10:128; U9:128; U9&U10: 224&224

- **Min threshold will raise when multiple chips work together**
- **Due to compound reasons**
  - **No local LDO on chip, chip will see crosstalk from others coming from the power supply**
  - **High ground R from ladder – limited width, limited layer, long routing**
    - **crosstalk on common path**
- **No effect solutions for now**
  - **Multi-layer ladder is proved to be effective, but not good for material**
- **What can we do in future?**
  - **On chip LDO must be involved; Serial powering for multiple chips to be studied**
  - **Wider matrix may help for the ladder design, but big impact on chip timing**

Can be improved – multi-chip synchronization

- **Time stamp 0 for multiple chips are now defined by a test pulse at the initiate stage**
- **Can be improved for a more defined logic on chip**
  - **Better to be considered globally with other detectors**
  - **Also the trigger scheme**

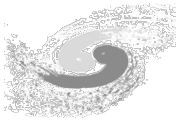
To be studied – behavior of a real full ladder



- **A full ladder with all chips, double sided, for sure is the recent goal**

- **To see how serious the threshold will raise**
- **To see if there is any show stopper(data, power, noise, crosstalk…) for the real full ladder**

To be studied – neg sub, std/mod process

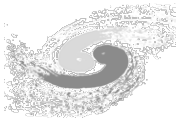


- **It is said, negative substrate voltage can help for the resolution**
  - **Found very risky during the TaichuPix2 test (std process)**
  - **Also heard it is not achievable from other colleagues**
- **It is a chance to make some further study based on different processes**
  - **Behaves differently on std/mod processes?**

- **What is the real benefit/difference between std/mod processes?**
  - **Further test and study with more comparison**

- **To to**
  - **A new PCB/ladder that can support for negative substrate power supply**
    - **New challenge on ladder design**
  - **More beam tests afterwards**

To be studied – advanced chip features



- **Trigger readout mode not considered**
- **No trigger detector considered during the beam test**
  - **What is the time resolution of the prototype with multiple layers?**
- **Side connections for slow controls not verified at the ladder level**
  - **Will help for the ladder design**
  - **Also possibly needed in the real detector**
  - **Worth to try, but new challenges for wire bonding**
- **High speed data link at the ladder level**
  - **Current data speed at 160Mbps for all the test**
  - **Worth to verify high speed data communication at the ladder level**
    - **Is it too sufferred from imperfect data path? Is it too noisy to the chip?**
    - **What is the power consumption for triggerless mode**

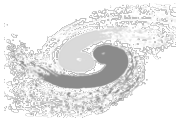
To be studied – low material ladder?

- **The conventional PCB process based on copper involved high material for multi layers**

- **Solutions**
  - **We know at the first day, Al Flex can greatly help**
  - **But we cannot find a vendor in China**

- **Keep finding, or collaborate with abroad?**
- **Local PCB R&D workshop on Al might not be realistic**

Conclusion



- **Key words for current issue**
  - **Timing**
  - **Robustness**
  - **Powering**
- **Very limited which can be done from the ladder design, based on current constraint**
- **Try to collect issues as much as possible before the next chip tapeout**

- **Can we use Towerjazz 65nm someday?**
  - **All specs from CEPC can be satisfied then**

Thank you !