Progress in FPGA-based Detector Array Readout System

Shoulong Lin

Supervised by Xiaomei Li

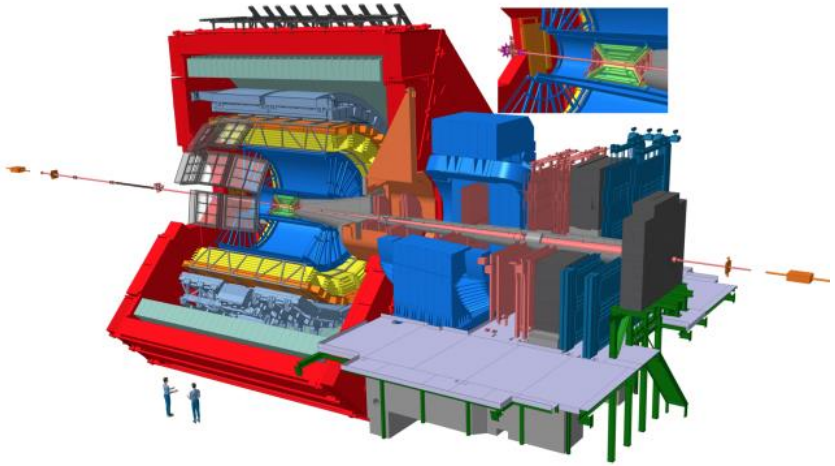
8/18/2023

Outline

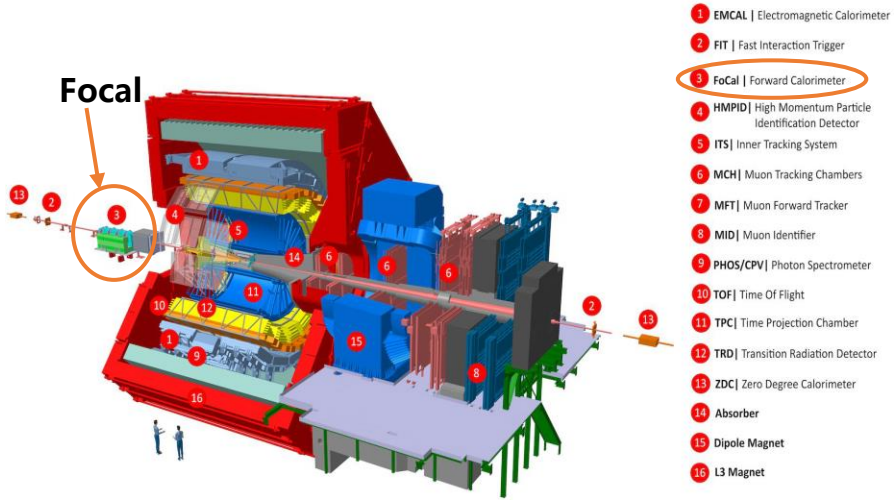
- ALICE Focal Readout system
- FPGA-Based Detector Array Readout
- Summary

ALICE upgrades

A Large Ion Collider Experiment

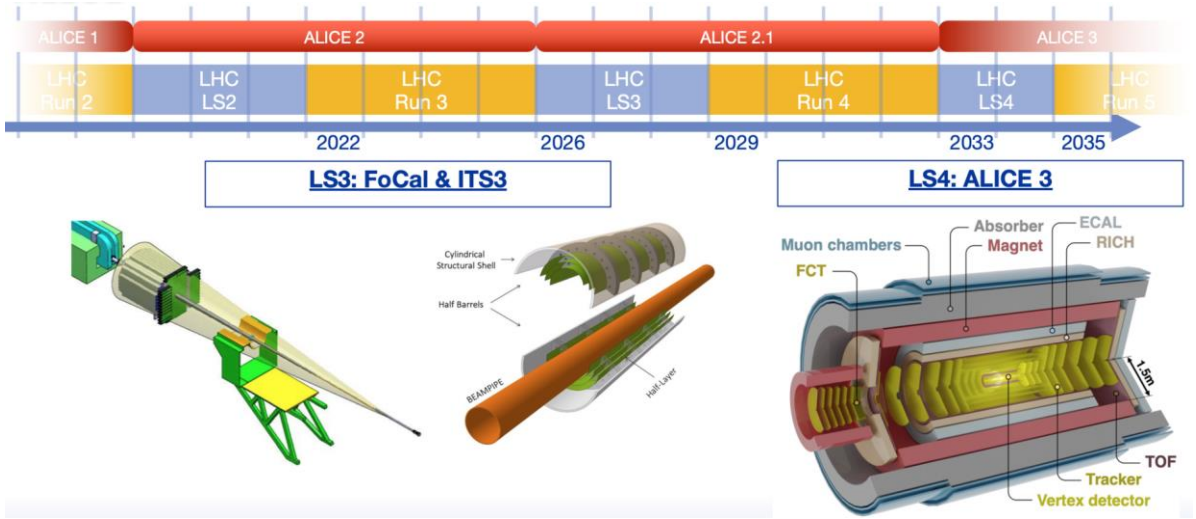


ALICE Schematics as during RUN2



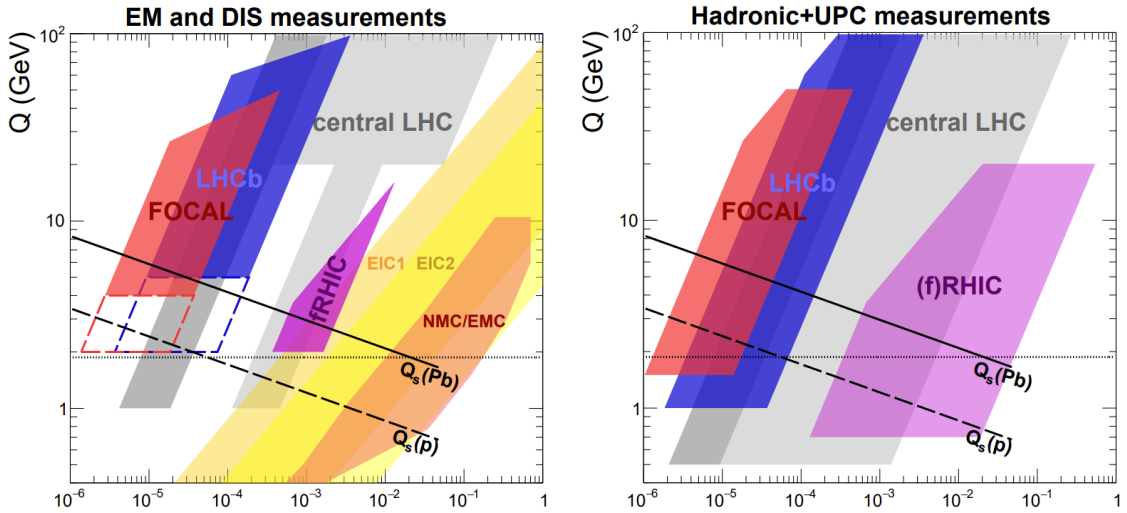
ALICE Detector for RUN4

- Study the properties of quark-gluon plasma (QGP) and its evolution
- Understand the characteristics of quantum chromodynamics (QCD)
- Understand the origin of the universe and its evolution



Timeline of ALICE upgrades

ALICE Focal



Approximate (x, Q) coverage of various experiments

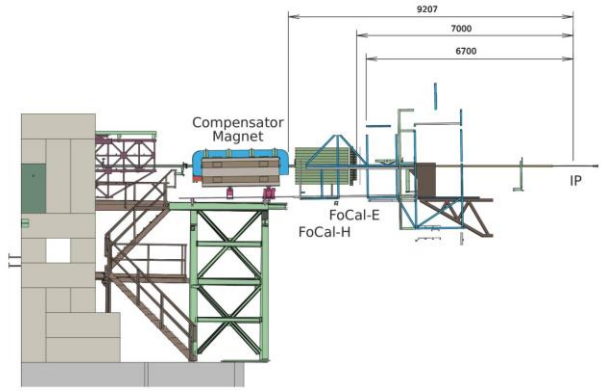
- Covering pseudorapidities of $3.4 < \eta < 5.8$
- Explore the dynamics of hadronic matter at small x down to about 10^(-6)

ALICE-PUBLIC-2019-005

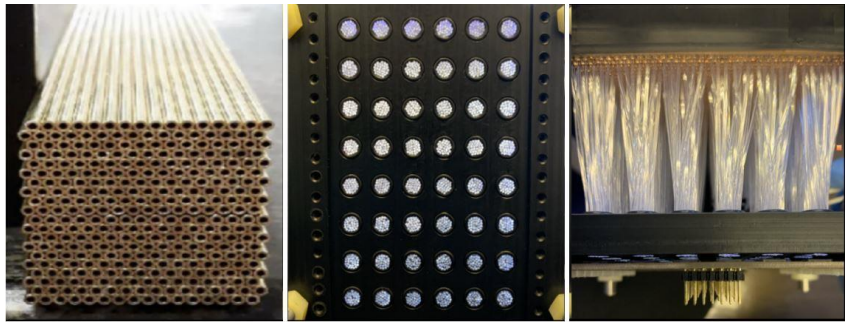
- quantify the nuclear modification of the gluon density in nuclei at small-x and Q^2 by measuring isolated photons in pp and p–Pb collisions
- investigate non-linear QCD evolution by measuring azimuthal π^0–π^0 correlations and isolated γ–π^0 correlations in pp and p–Pb collisions
- investigate the origin of long range flow-like correlations by correlating neutral meson production over large range in rapidity in pp and p–Pb collisions
- quantify parton energy loss at forward rapidity by measuring high-p_T neutral pion production in Pb–Pb collisions

ALICE-PUBLIC-2023-001

Focal Detector

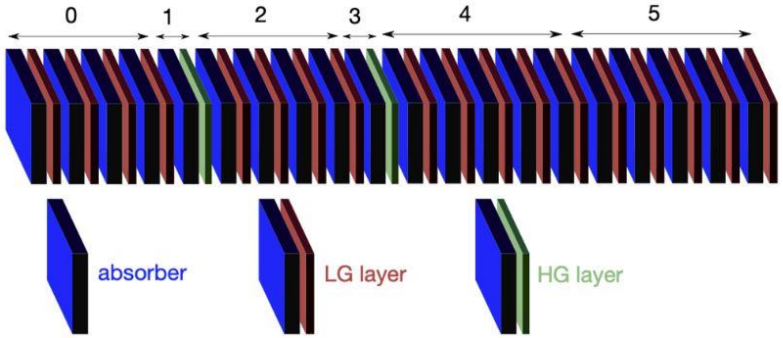


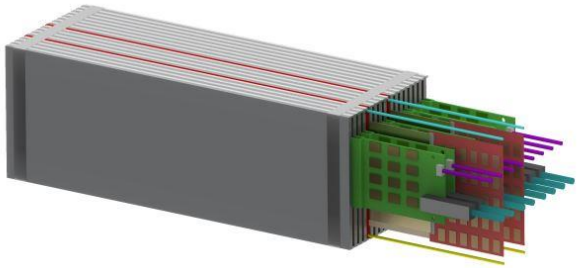
The FoCal is composed of an electromagnetic part (FoCal-E) and hadronic part (FoCal-H)



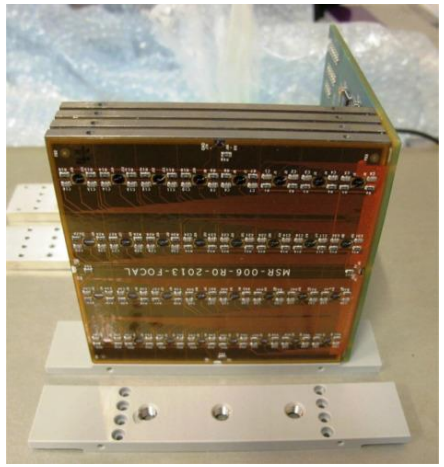
FoCal-H 2021 prototype module with 1440 Cu tubes (left), grouped scintillating fibers at the back of the detector (center) and 16 (out of 48) mounted Onsemi MICROFC-60035-SMT-TR1 SiPMs at the back of the detector (right).

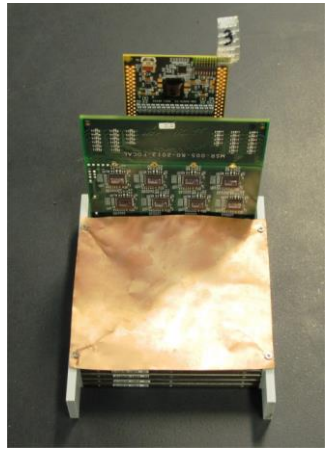
arXiv:2211.14791

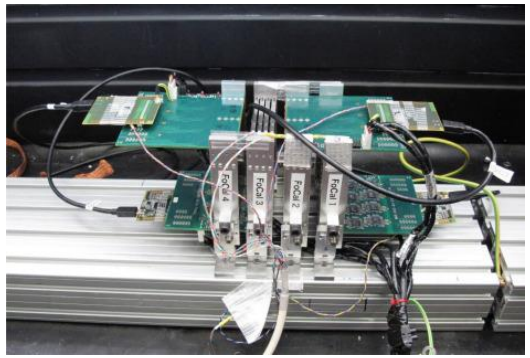




Focal-E containing 20 layers of W converter and Si sensors. 18 of the layers consist of pad sensors, while 2 layers use pixel sensors.





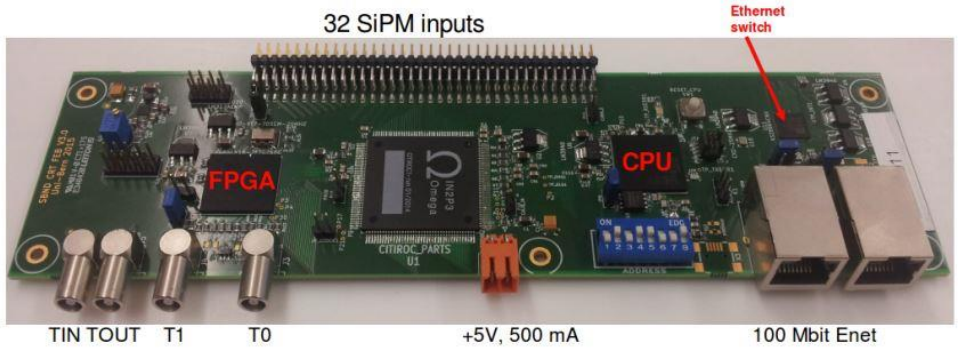


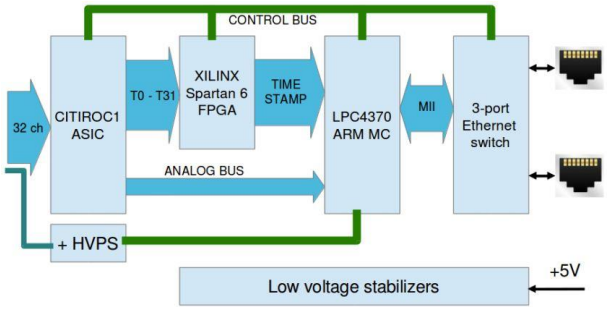
FoCal PAD detector segment and APV25 hybrid front-end card

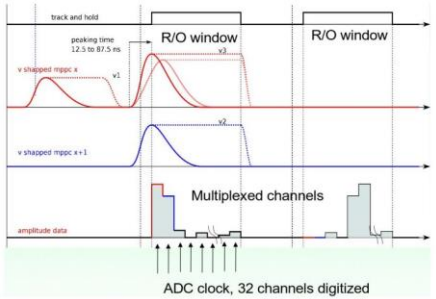
arXiv:1912.11115

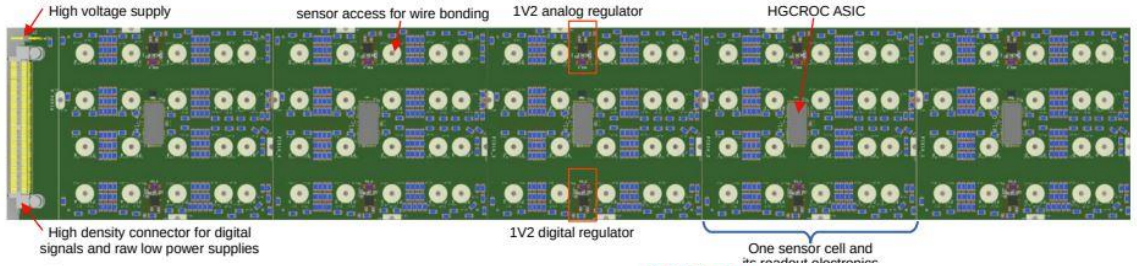
Focal Readout Electronics

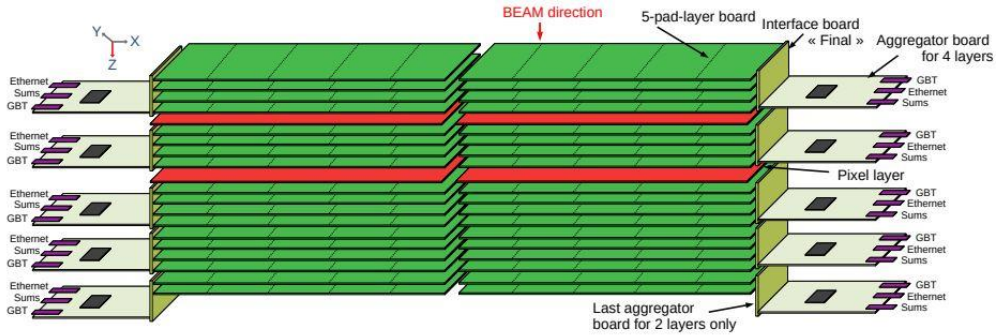
M. Auger et al 2016 JINST 11 P10005



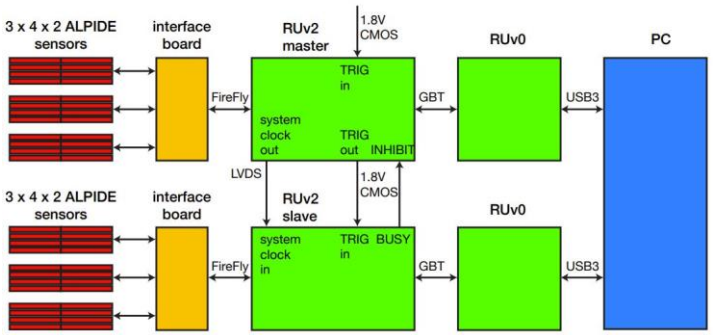






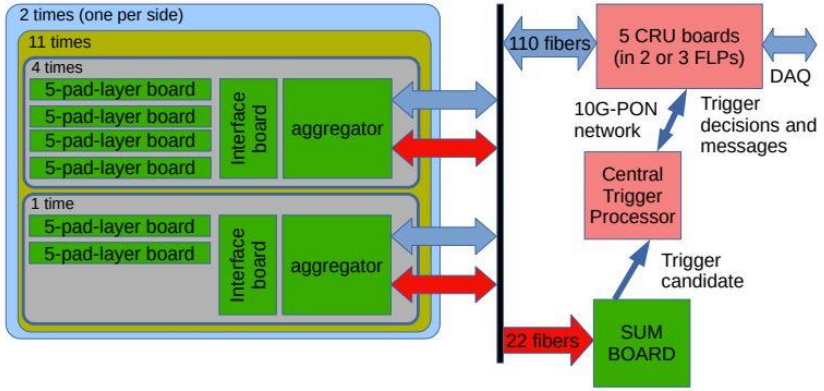


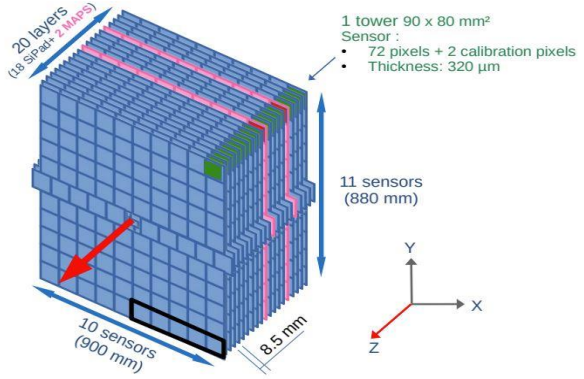
FoCal-H 2021 prototype readout electronics



arXiv:2209.02511

FoCal-E pixel layer prototype EPICAL-2 readout electronics

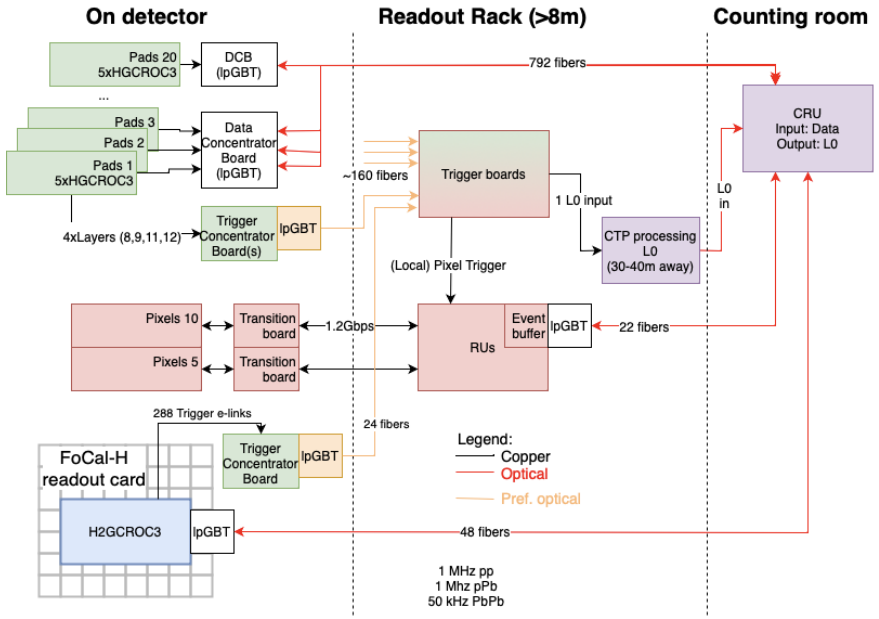




arXiv:2302.13912

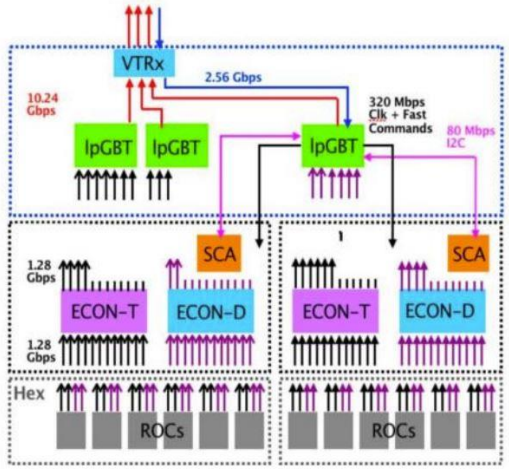
FoCal-E pad layer prototype readout electronics

Focal Readout System

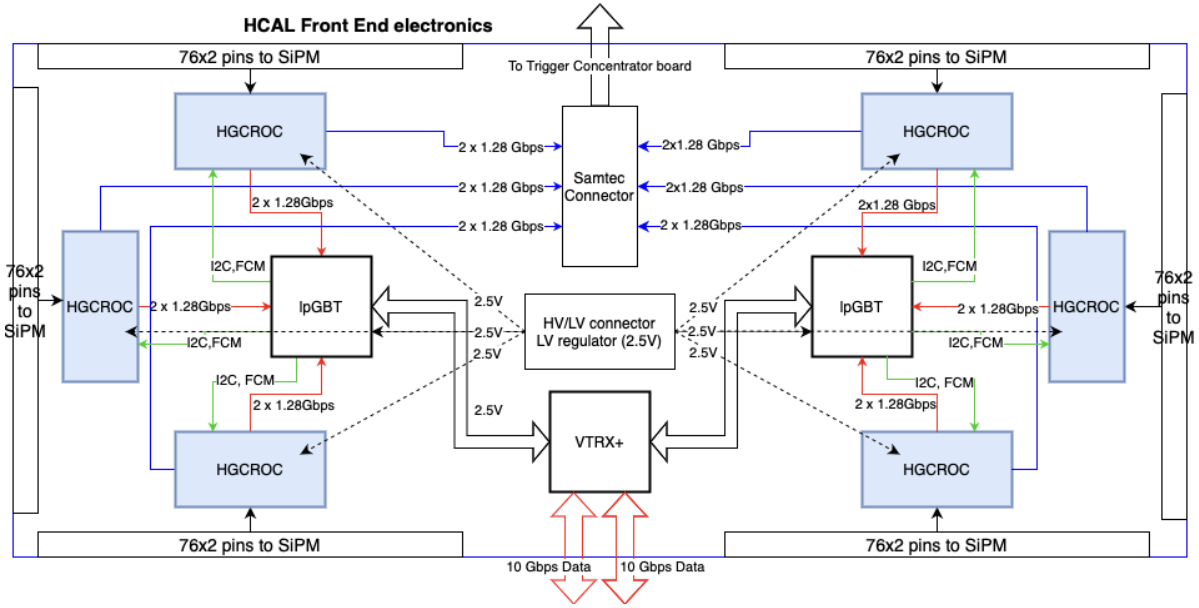


FoCal readout system

- Protect FPGAs with Long Readout Rack
- Use ECON-D and lpGBT readout pixel data
- ALPIDE pixels use continuous trigger mode, or through signals provided by the Pad layer



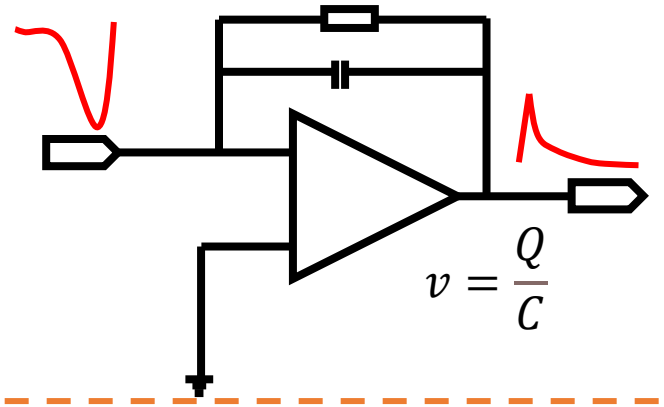
CMS CR -2021/228



FoCal-H readout board

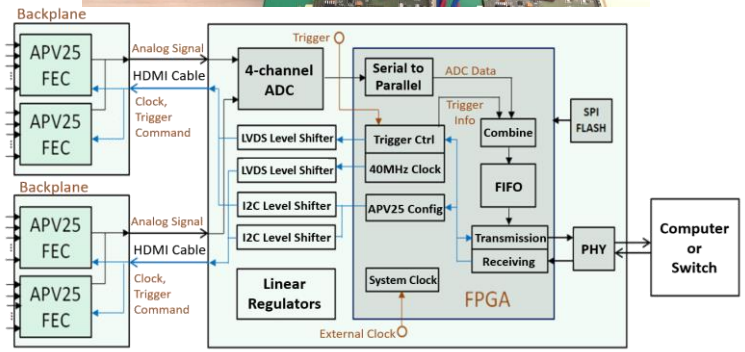
- 6 HGCROC, 2 LpGBT, 1 VTRX+
- 6x72 = 432 channels
- Use ECON-D / ECON-T ASIC compress data

SiPM Charge digitization

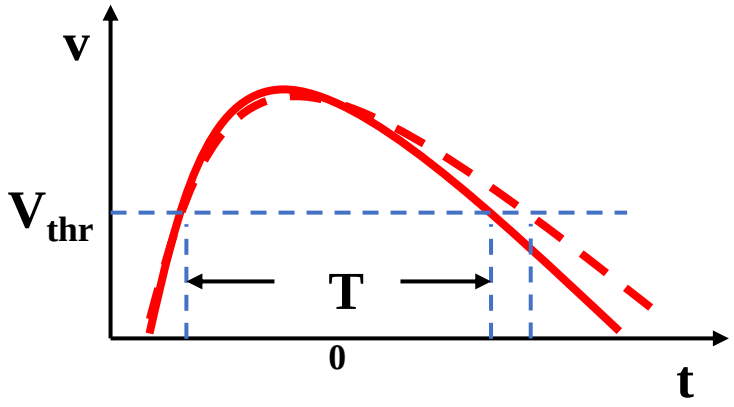


How to measure the voltage?

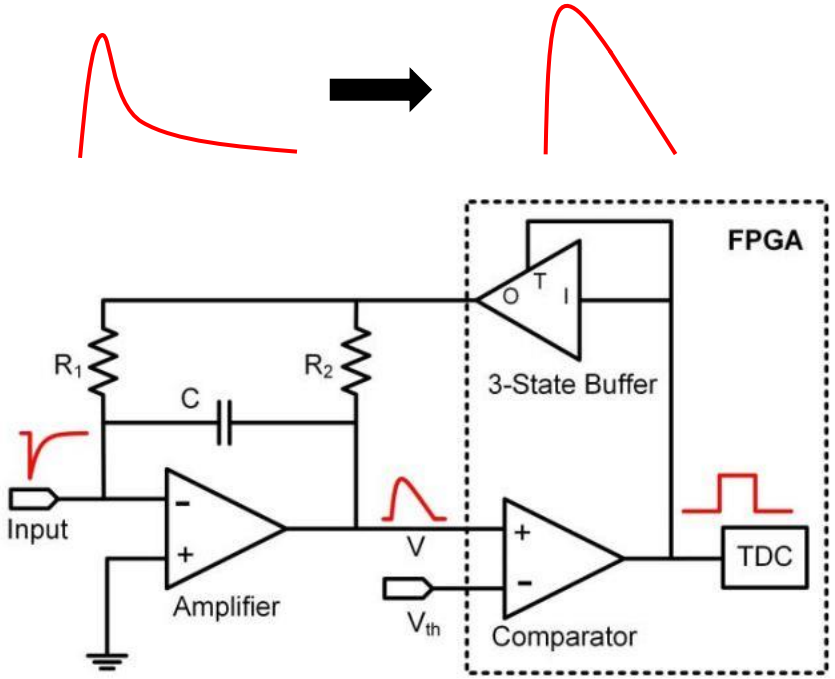
- **ADC**
- **TOT**
- **FPGA-based method**



APV readout system(adc-based)



TOT method



Flexible, low cost, fast speed

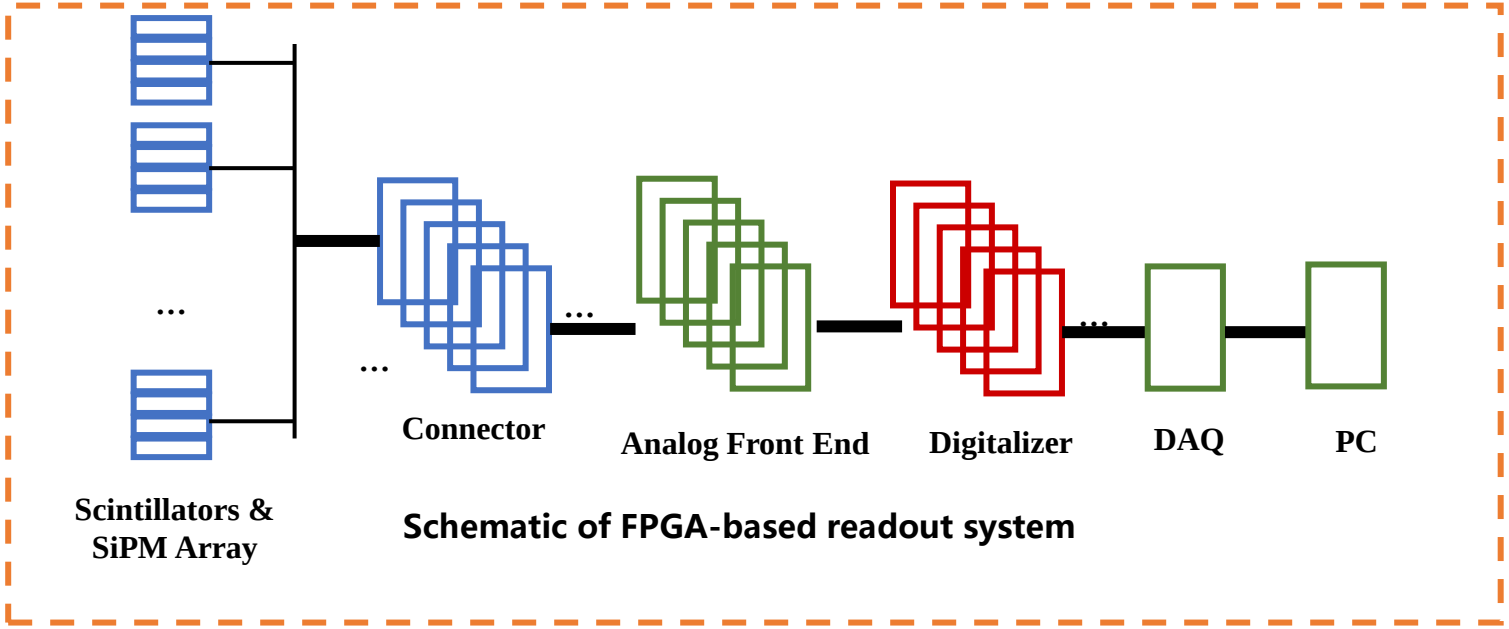
$$\int_0^{T_{start}} \frac{V}{R_1+R_2}dt + \int_{T_{start}}^{T_{end}} \frac{U_0}{R_1}dt + CV_{th} = \int_0^{T_{end}} i(t)dt$$

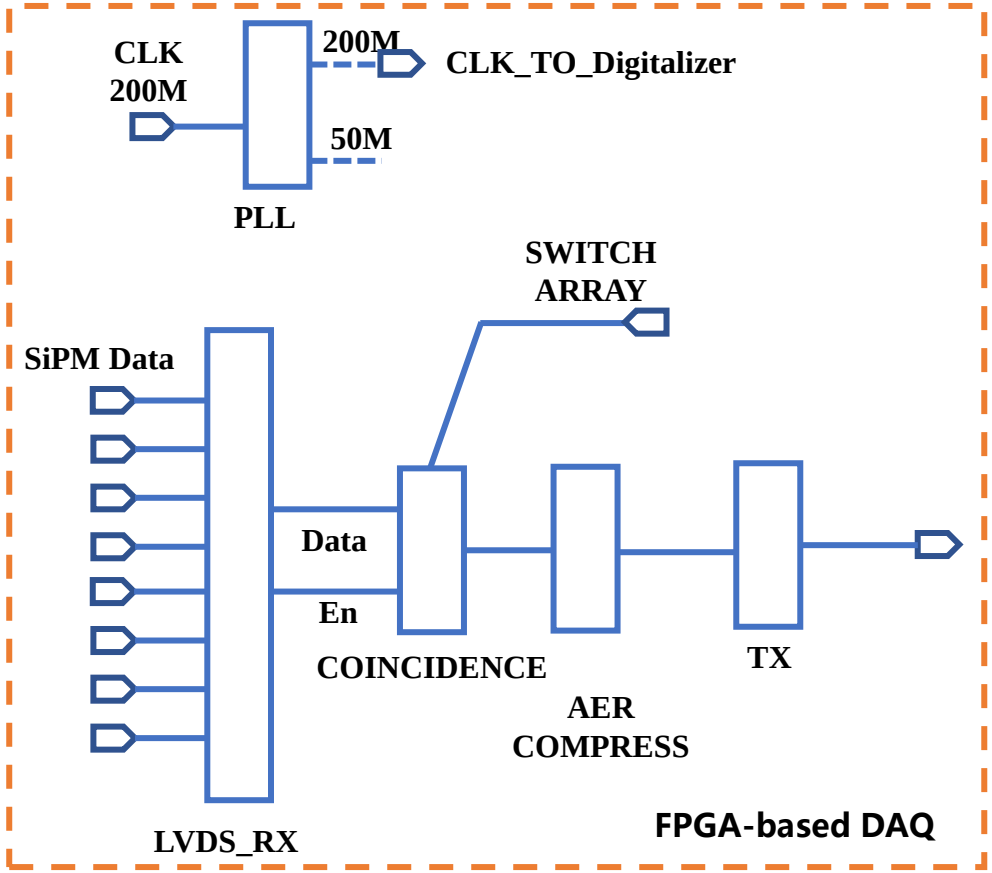
$$\frac{U_0}{R_1}(T_{end} - T_{start}) \approx \int_0^{T_{end}} i(t)dt \approx Q$$

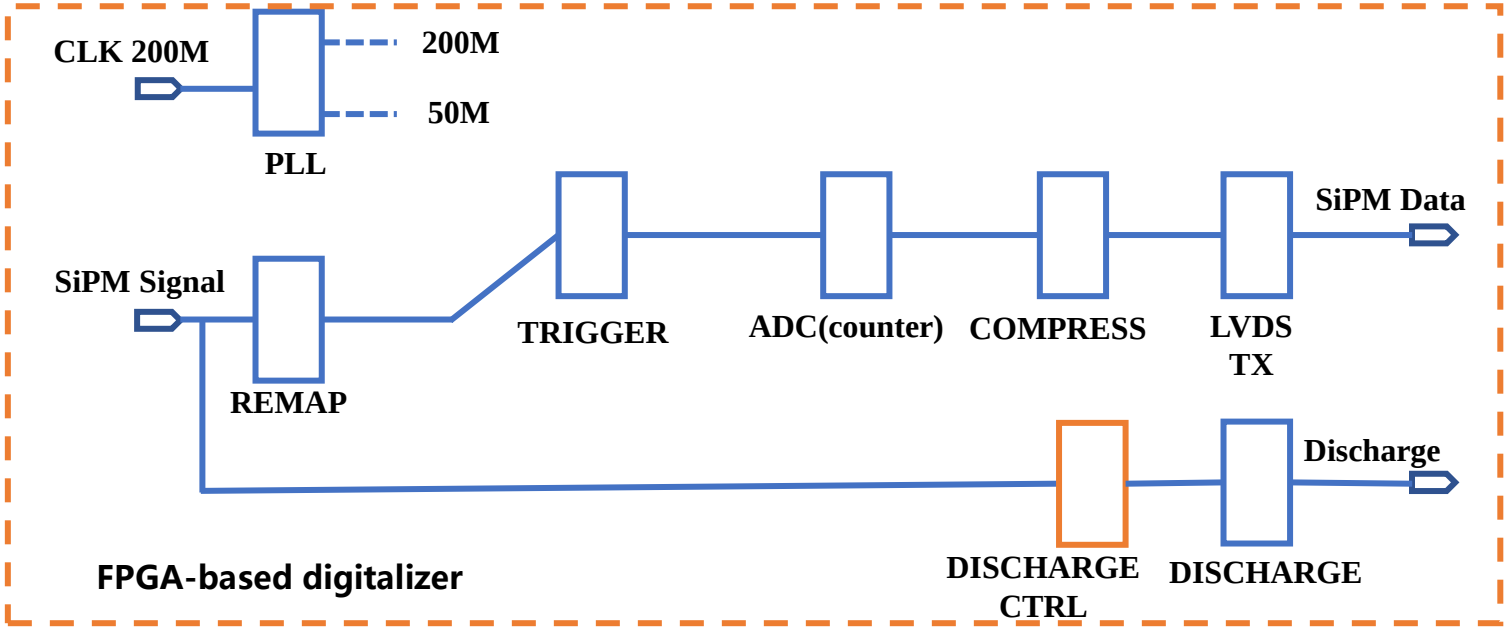
TNS.2017.2648787

Linear discharge readout method (FPGA-based)

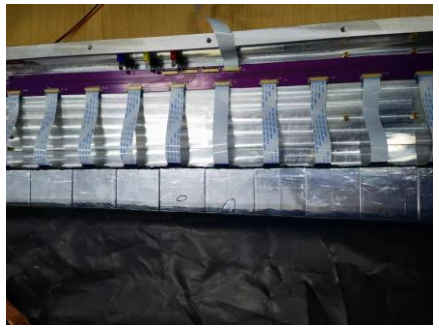
FPGA-based readout system



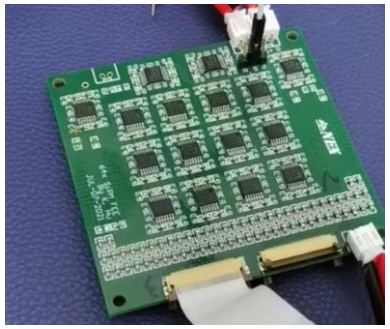




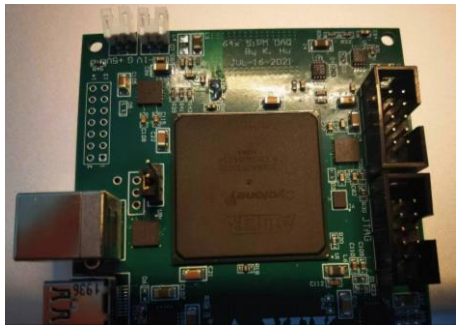
Cosmic ray test



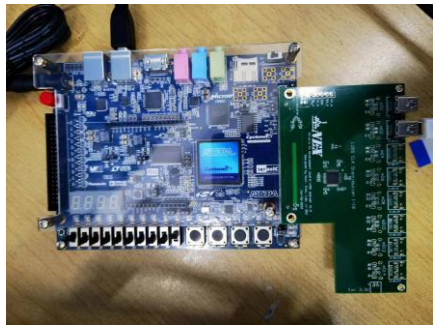
Detector



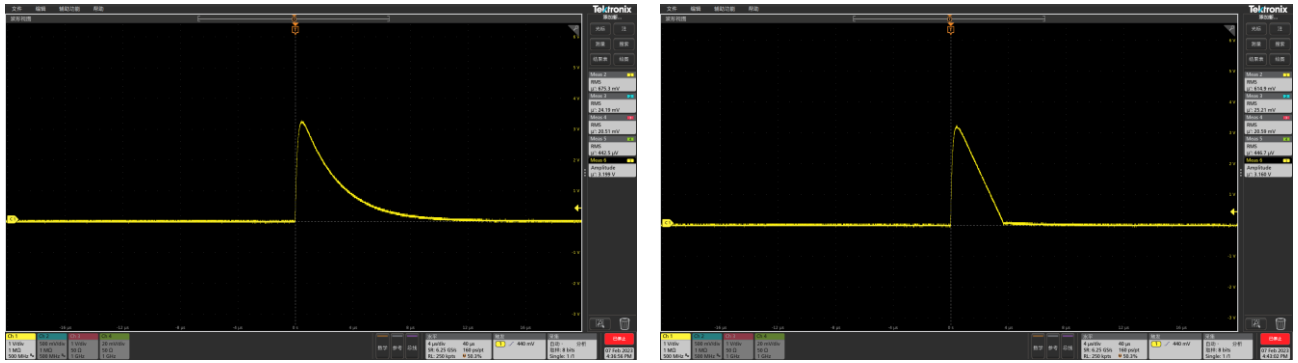
Analog Front End



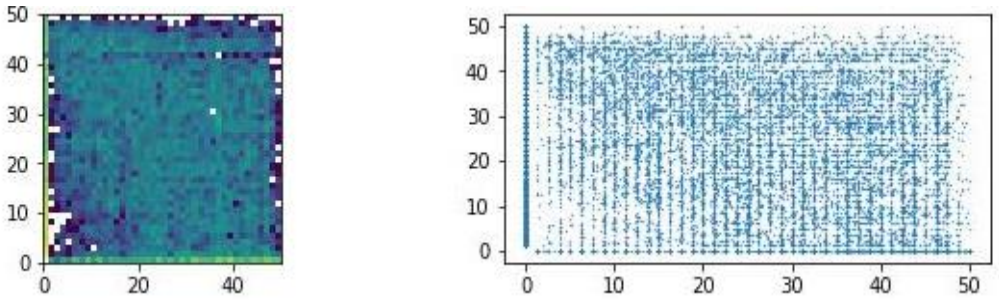
Digitalizer



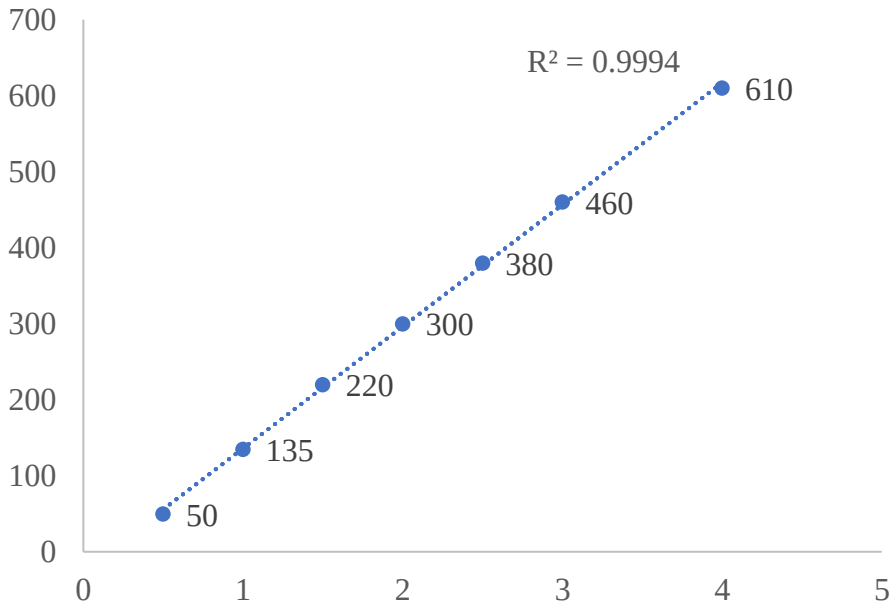
DAQ



Linear discharge test

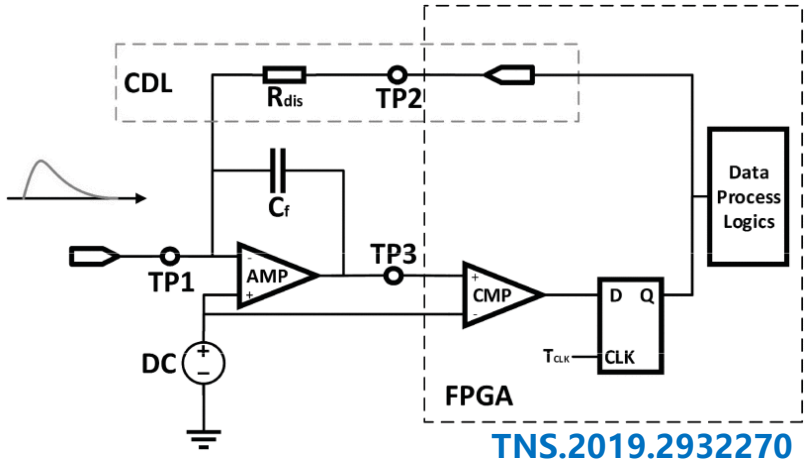


cosmic ray event



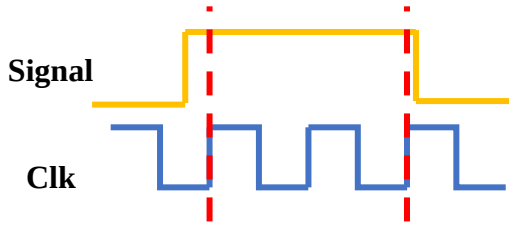
Linearity

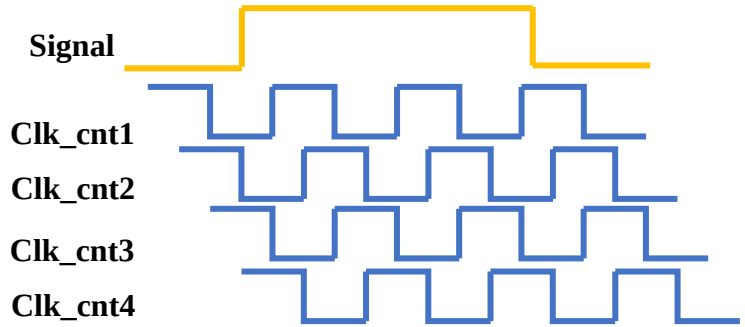
Improvement of FPGA-based readout system



TNS.2019.2932270

Dual-Polarity Readout





TBCAS.2018.2865581

Use Multiphase Counter Increase accuracy

trade-off between resource and precision

Front board

1. **FEE front-end electronics** board (suitable for direct connection detector)
2. **Receiver board** (acquire multiple digital signals)
3. **Clock board**, used as clock distribution, data acquisition

FPGA board

1.Digitalizer
2. Data Aggregation
3. Data Processing

Interface

1.Uart
2.USB3.0
3. Optical communication
4. Data & CLK
5. Ethernet port

PWR JTAG…

- FPGA upgrade for IOs and power consumption
- Versatile electronics baseplate
- Deploy some algorithms on the FPGA, such as noise filters, data compression, coordinate reconstruction

Summary

- FoCal is composed of an electromagnetic part (FoCal-E) and hadronic part (FoCal-H), Many focal prototypes have already been tested.

- Focal electronics prototypes are gradually being established. FPGAs are widely used in communication and control, A high-speed data link is built by HGCROC, lpGBT, VTRX+ …

- An electronic system based on the charge digitization method of FPGA linear discharge was built, and cosmic ray tests were carried out, and the system linearity was good and had the potential to cope with high-frequency events.

- The system is simple and flexible, easy to update and iterate, The upgrade of the system is ongoing.