CEPC vertex detector prototype DESY Testbeam 2023

Zhijun Liang

2023.05.30

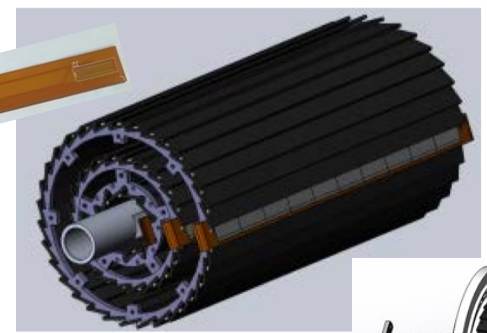# Overview of MOST2 vertex detector R&D

- **Can break down into sub-tasks**

  ➢ CMOS Pixel Sensor chip R&D

  ➢ Detector layout optimization, ladder and vertex detector support structure R&D

  ➢ Detector assembly

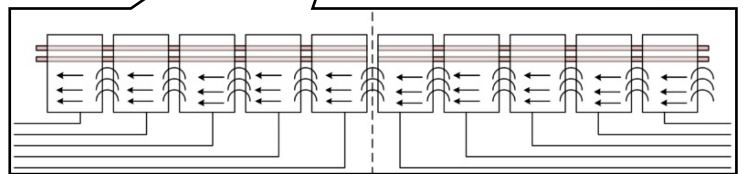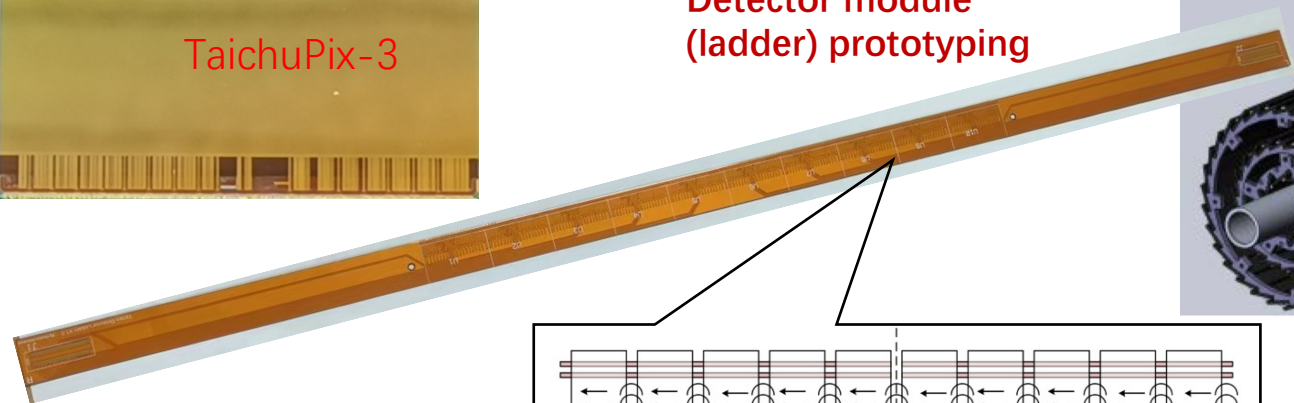 ➢ Data acquisition system R&D

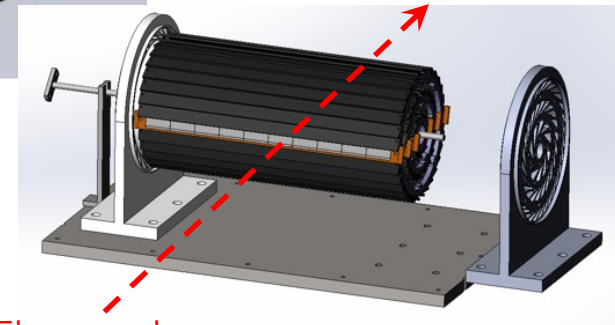CMOS pixel sensor prototyping

TaichuPix-3

Detector module (ladder) prototyping

Full size vertex detector prototype

Beam test to verify its spatial resolution

Double sided ladder
10 sensors/ladder side, read out from both ends

Electron beam

DESY Testbeam Setup

Dec 2022 DESY test beam
Taichu and Jadepix Telescope level

April 2023 DESY test beam
Taichu vertex detector

Jadepix telescope

TaichuPix3 telescope

MIMOSA telescope

Beam

Lifting stage

➤ 3 double layer of Barrel vertex detector
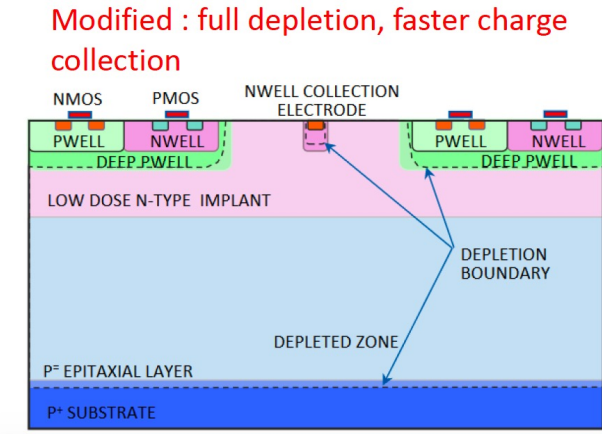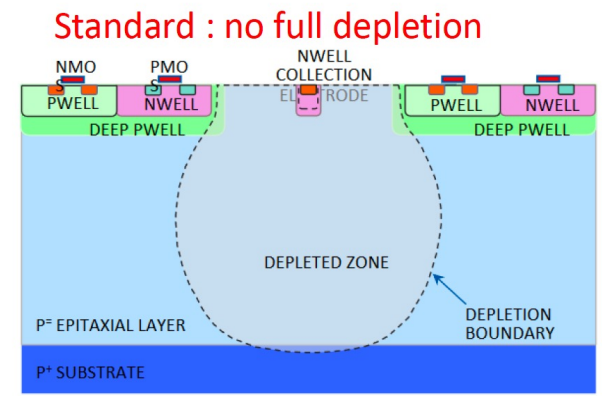➤ 6 ladder assembled
  ➤ 24 Taichu chips operation in testbeam
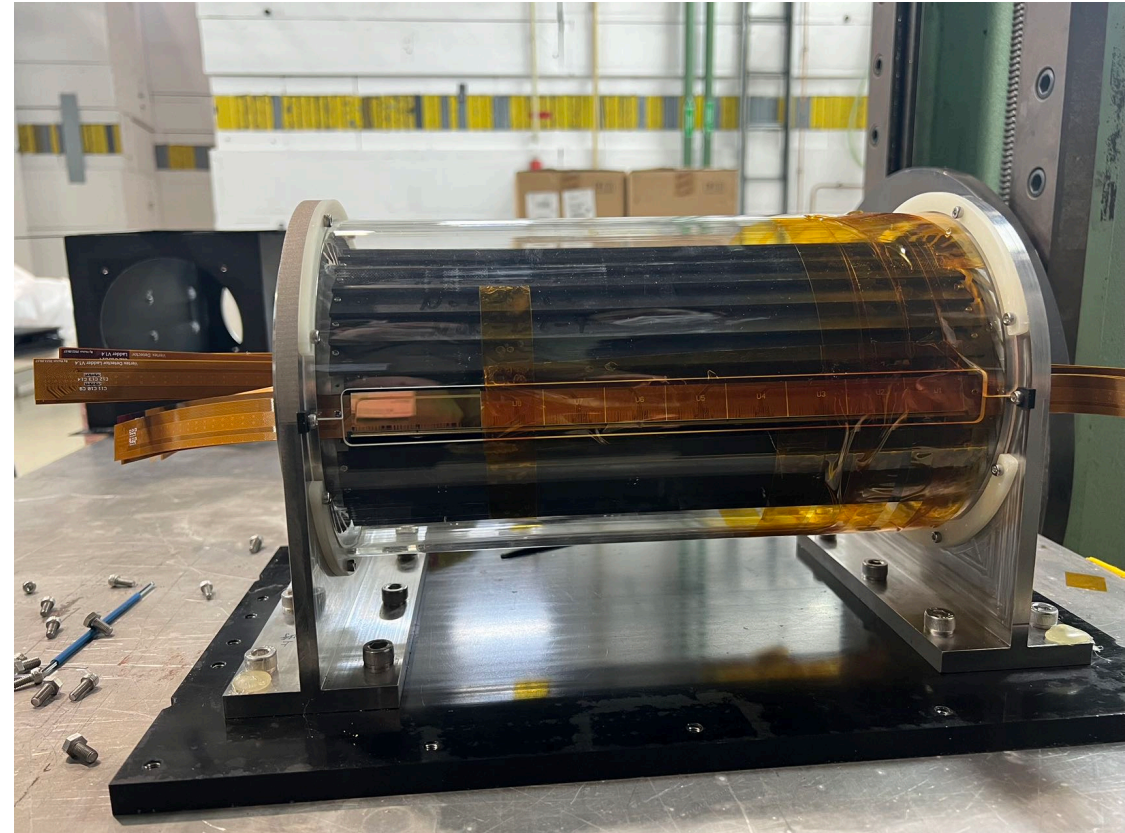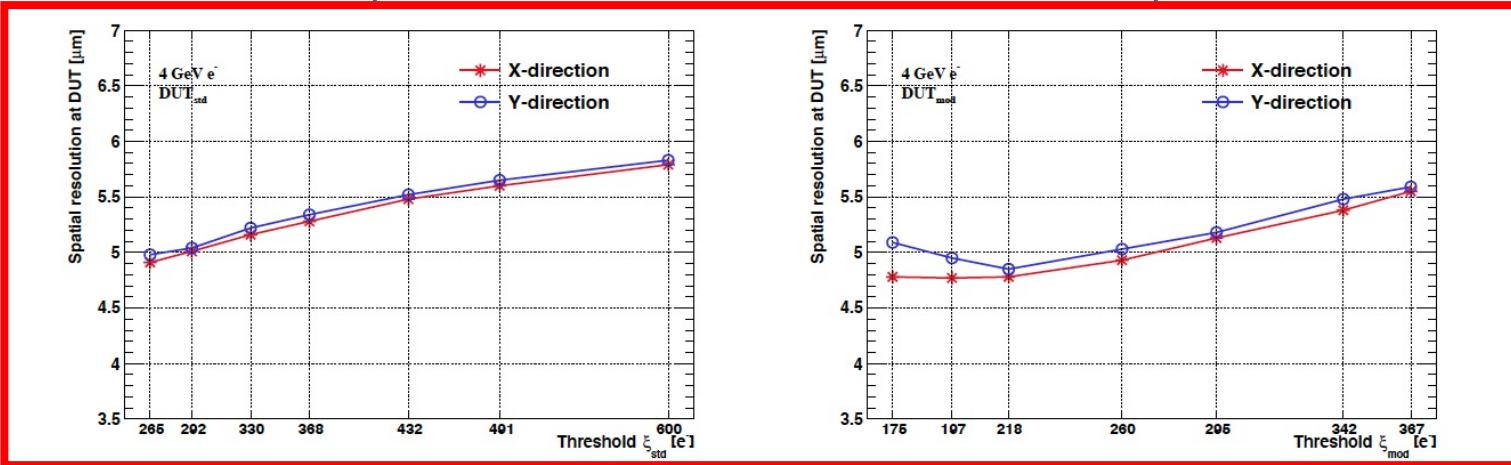
Reminder of testbeam result last December

➢ The spatial resolution improved by lowering the threshold
  ➢ Can reach around 5μm resolution
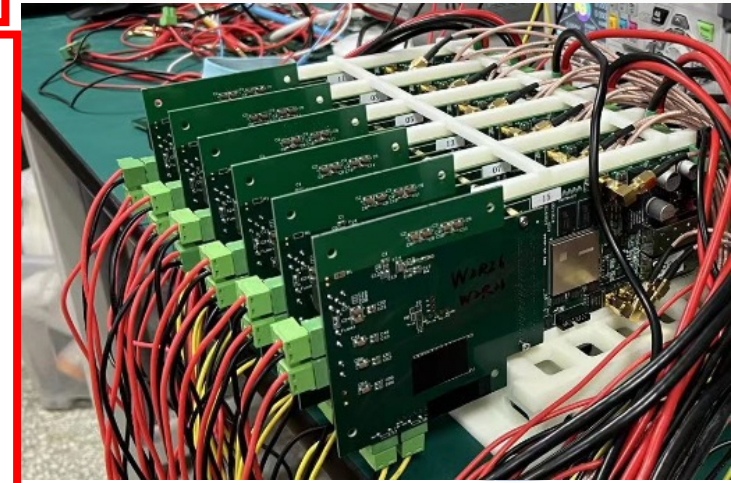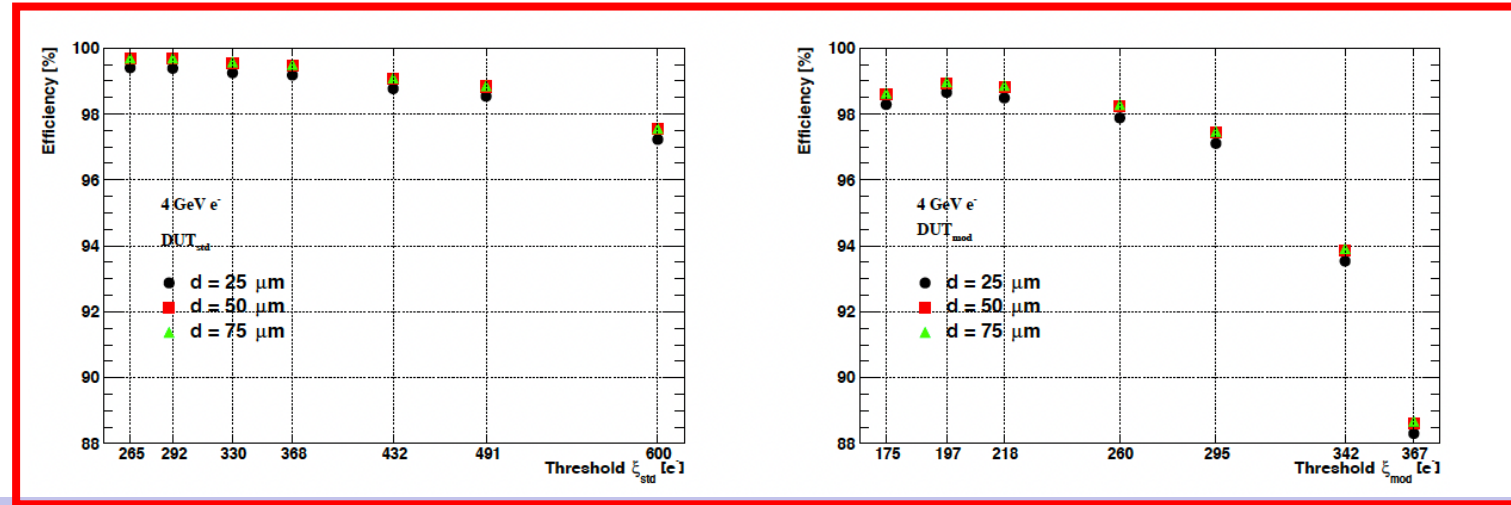 ➢ Lower operation temperature can reduce threshold

Modified process   Standard process

Standard : no full depletion

Modified : full depletion, faster charge collection

Resolution

Efficiency

Large-scale sensor TaichuPix-3

➤ **TaichuPix3 and Challenges for the CMOS sensor**

  ➤ Small pixel size -> high resolution (3-5 μm)

  ➤ High readout speed (<500ns deadtime @40MHz at Z pole) -> for CEPC Z pole high lumi
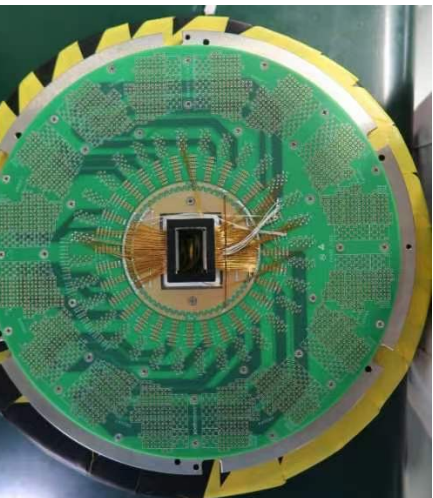
  ➤ Radiation tolerance (per year): 1 MRad
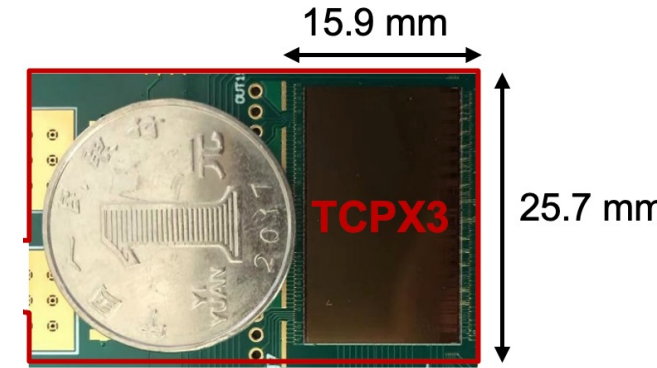
	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

15.9 mm

25.7 mm

TCPX3

TaichuPix-3 chip vs. coin

Wei Wei, Ying Zhang Tianya Wu

5 wafers tested

Wafer T212141-02E3

➤ 2 wafer based on standard process

  ➤ Reasonable yield achieved

➤ 3 wafer based on modified process

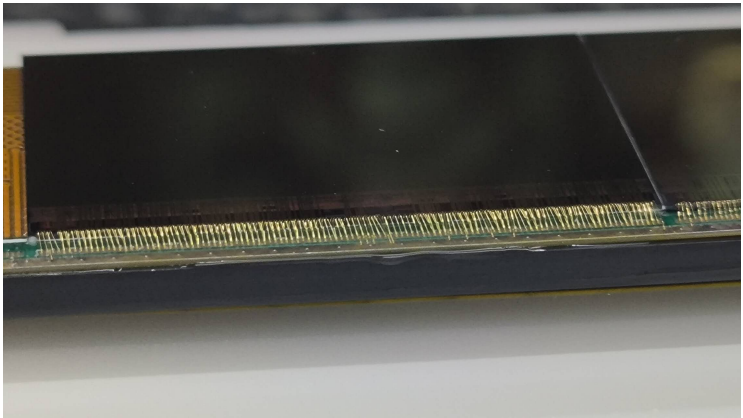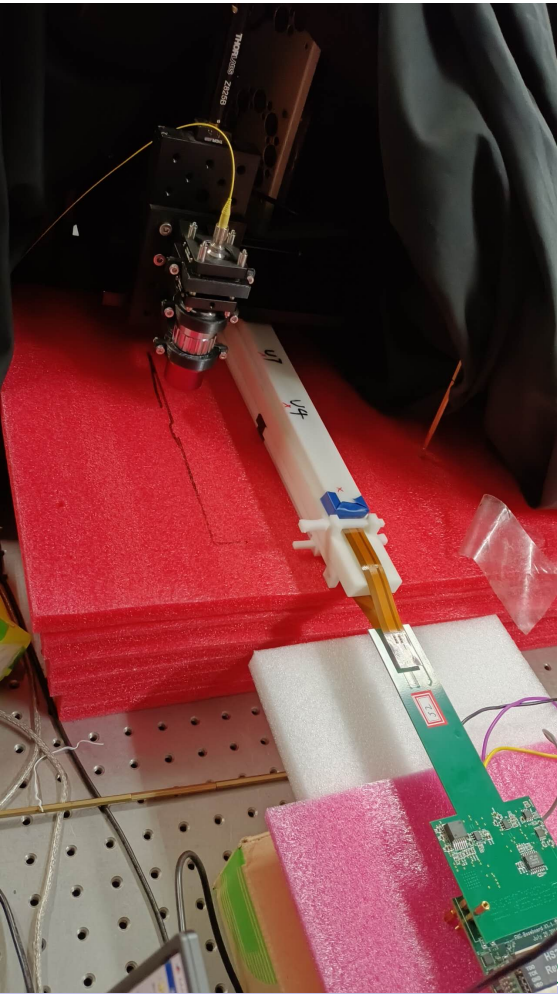 ➤ lower yield than the std. process

Probe card for wafer test
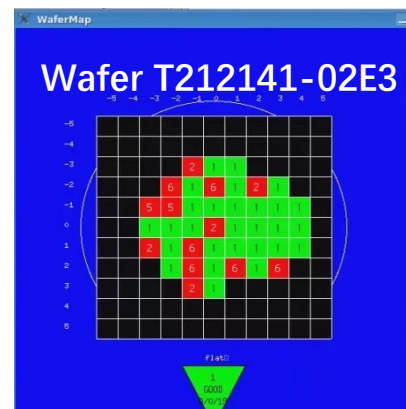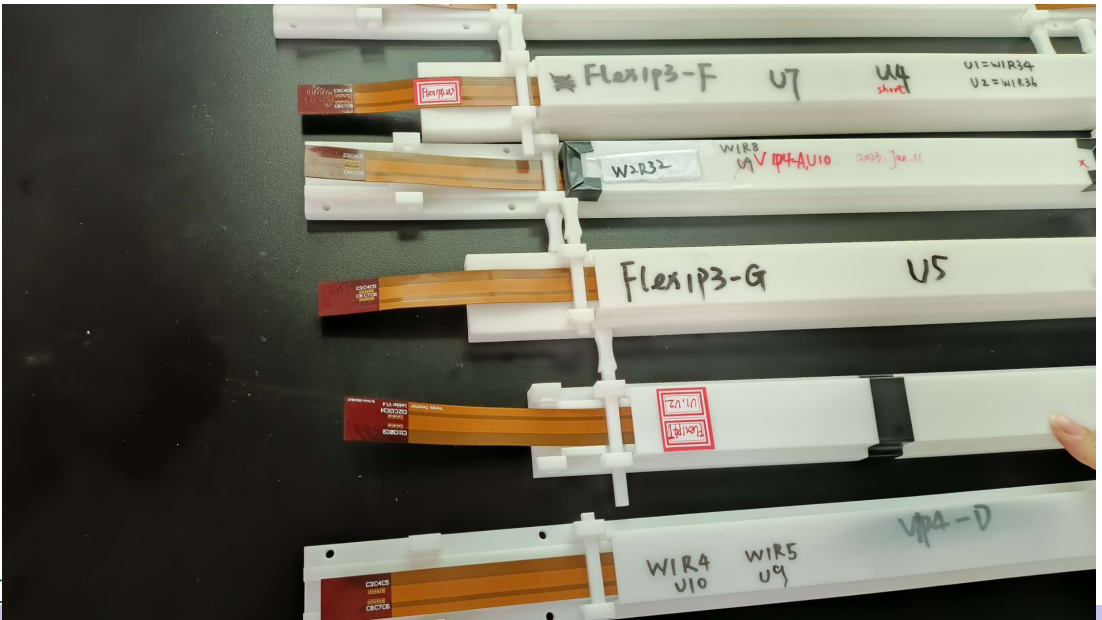
An example of wafer test result

CEPC

flex assembly and testing

- **Two Taichupix chip glued and wire-bonded on flexible PCB**

- **20+ flexible PCB has been assembled and tested.**

Two Taichupix chip wire bonded on FlexPCB

Ying Zhang,
Ziyue Yan
Jun Hu
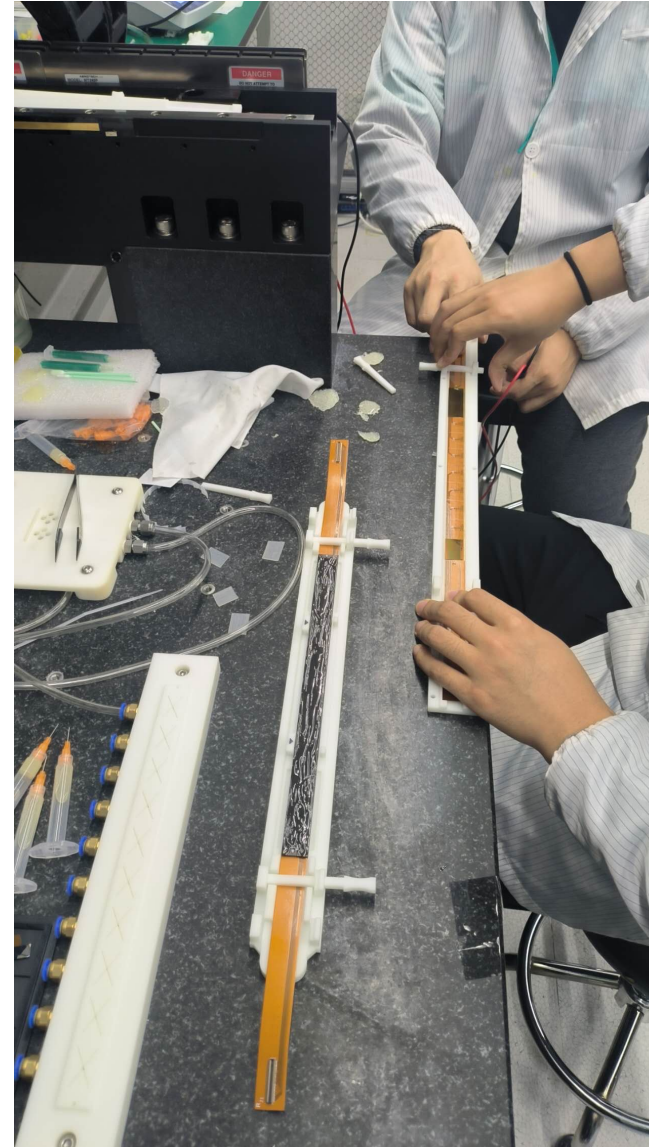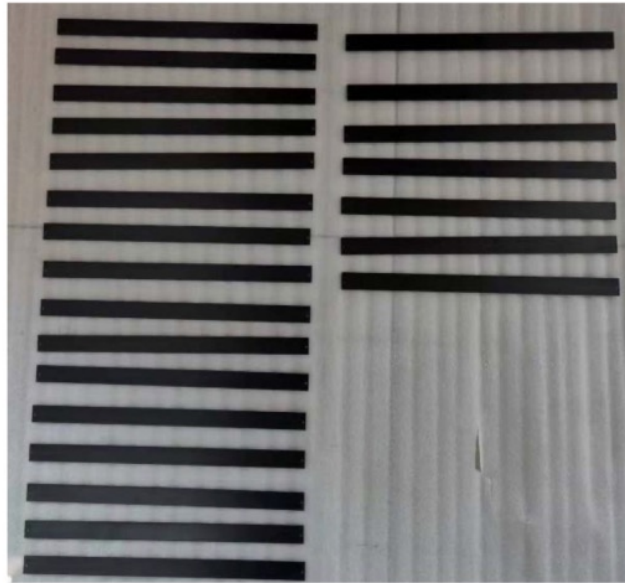Xiaoxu Zhang (NJU)
Tianya Wu
Wei Wang

double-side ladder assembly

- **Ladder in CEPC vertex detector is double-sided**
  - ➤ Two flexible PCB + one carbon fiber support

- **Both side has wire-bonding on chip → Challenging**

- **Dedicated tooling for double-side ladder assembly**
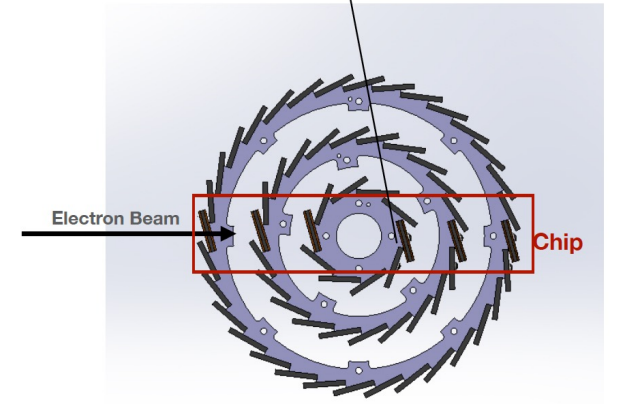

New batch ladder support

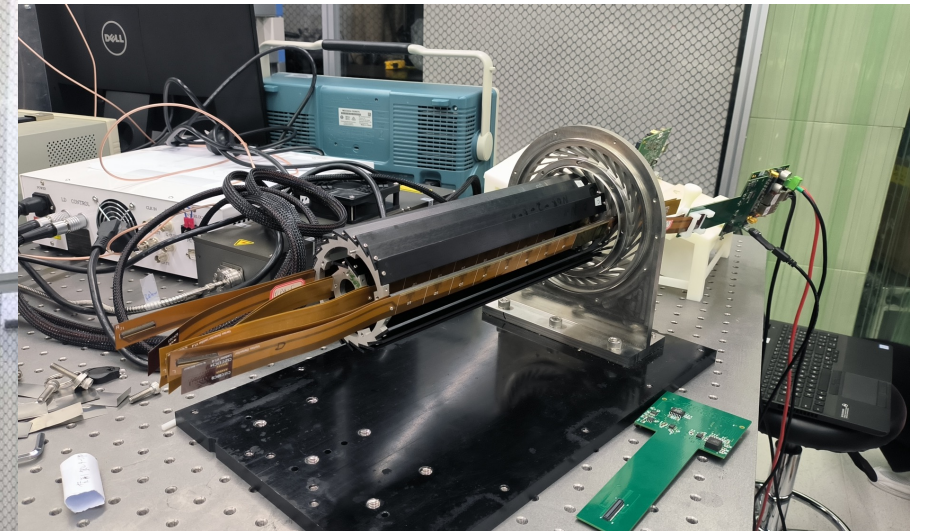Jinyu Fu
Xinhui Huang
Tianya Wu
Wei Wang

Prototype assembly

- **6 ladder installed on the vertex detector prototype for DESY testbeam**

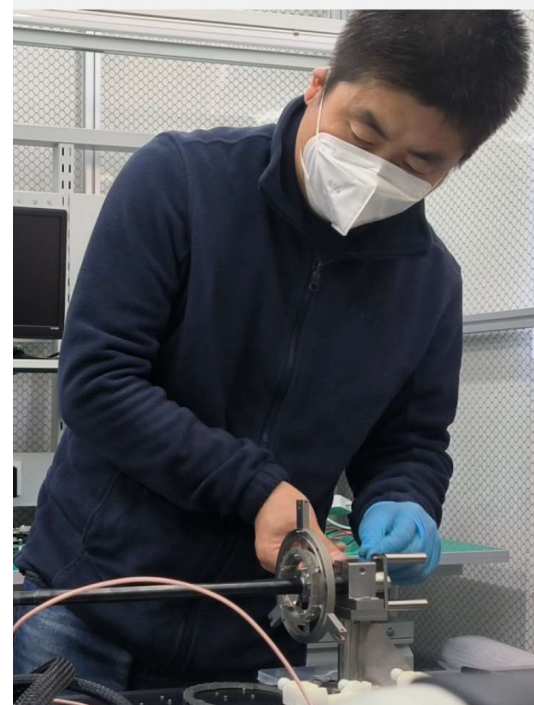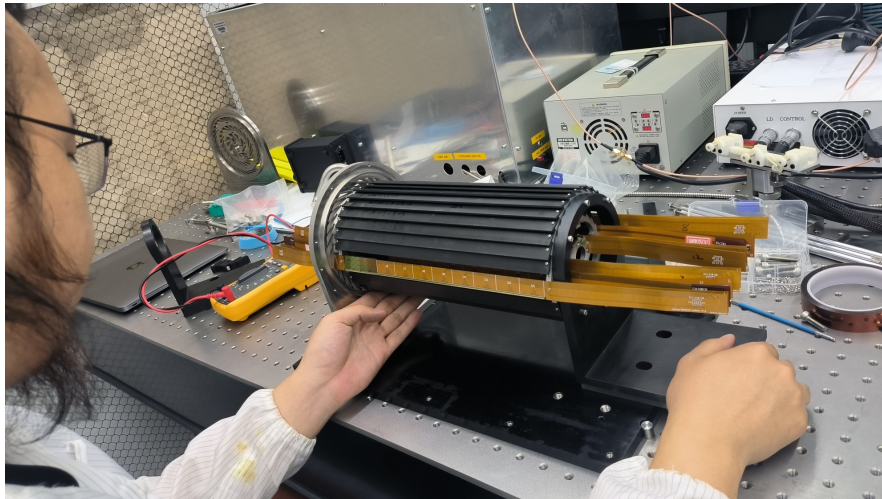 ➢ 12 flex PCB , 24 Taichupix chip operation

  ➢ DESY beam spot is about 2*2cm

a medium chip will not participant track reconstruction
the residual plot of fit position and measured position decide the spatial resolution

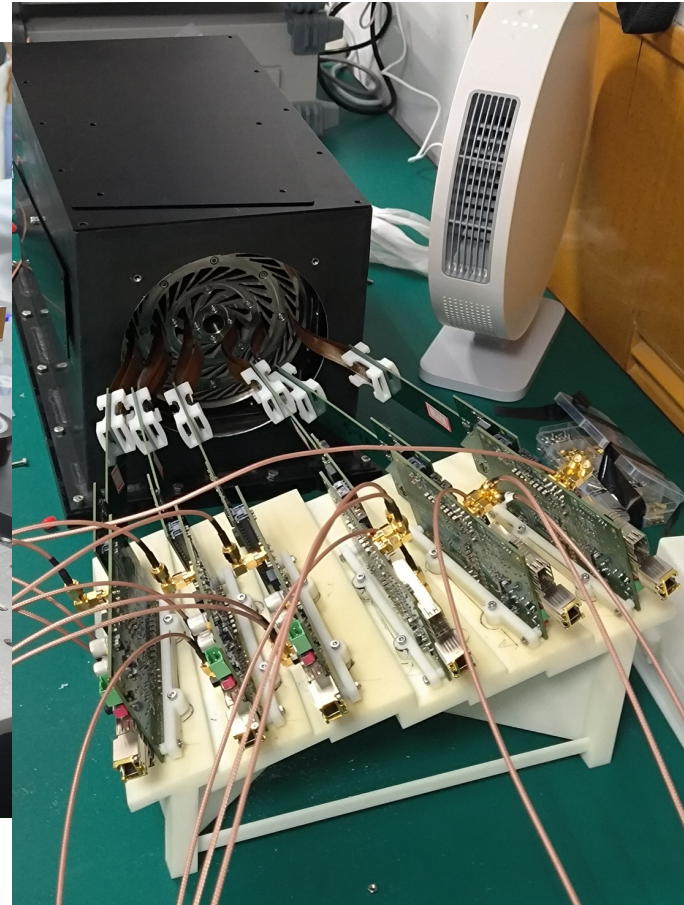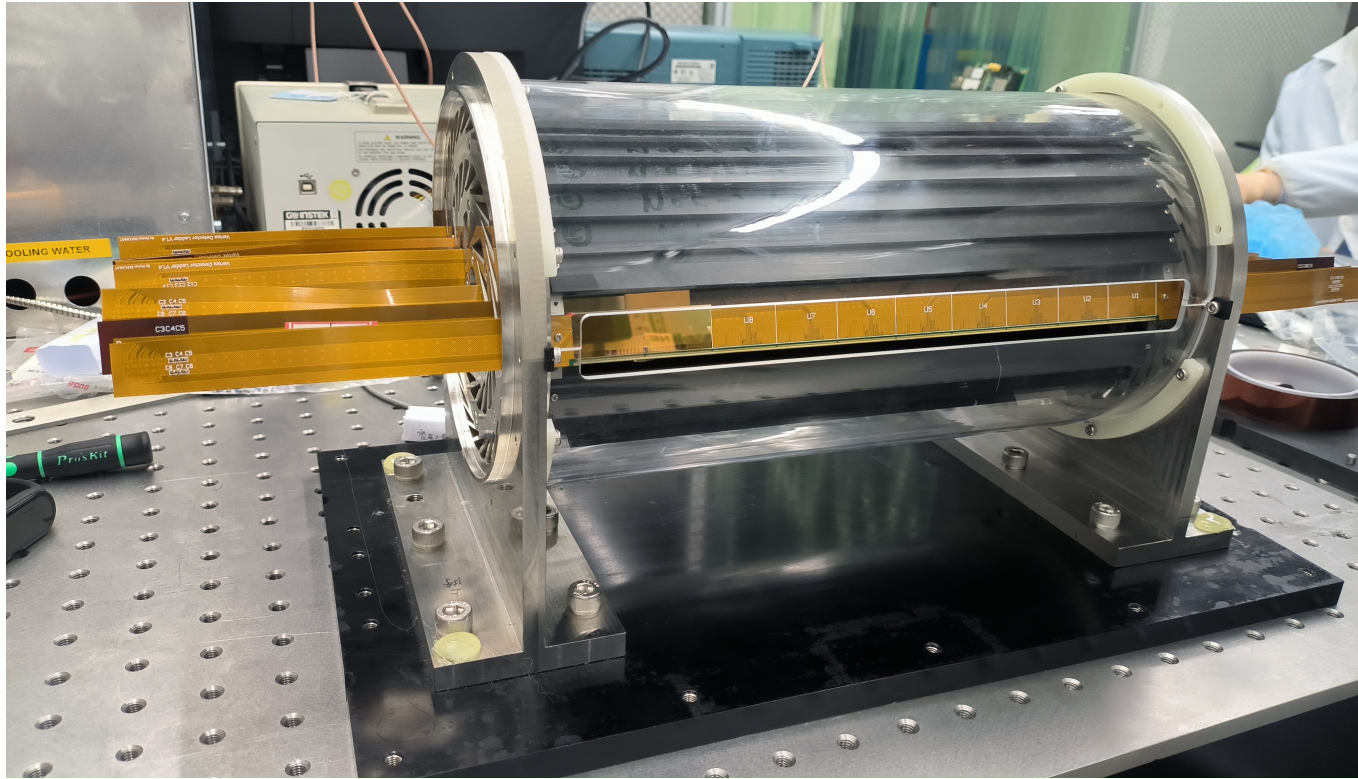Electron Beam

Chip

Jinyu Fu
Xinhui Huang

Prototype assembly and test@IHEP

- **After prototype assembly, beta source test and noise scan performed at IHEP**

Tianya Wu
Xiaoxu Zhang
Wei Wang
Ziyue Yan
Jia Zhou

• On Site team (DESY)

- Joao （IHEP）Project leader

- Tianya Wu （IHEP） test beam coordinator, ASIC expert

- Zhijun Liang (IHEP) test beam coordinator

- Ming Qi （NJU） Shift leader

- Jia Zhou （IHEP） DAQ

- Xinhui Huang （IHEP）Assembly

- Shuqi Li （IHEP) Offline

- Wei Wang (IHEP) offline

- Hao Zeng （IHEP） Offline

27-Feb-23	9		STARTUP						
6-Mar-23	10		CMS-HGCAL	X	CMOS Strips Detectors	X			
13-Mar-23	11		DSiPM	X	ATLAS-ITk-Strips	X		Telescope-Dev	X
20-Mar-23	12		DSiPM	X	ATLAS-ITk-Strips	X			
27-Mar-23	13		MONOPIX2	X	CMS-ETL	X		RSD	X
3-Apr-23	14								
10-Apr-23	15		CEPC Vertex	X	Tangerine	X			
17-Apr-23	16		CEPC Vertex	X	BTTB	X		BTTB	X
24-Apr-23	17		CMS-InnerTracker	X	TelePix	X			
1-May-23	18		CMS-InnerTracker	X	TelePix	X			

Romate support

WeiWei, Ying Zhang (IHEP), Xiaomin Wei (NWU) : ASIC

Jun Hu, Ziyue Yan （IHEP） firmware

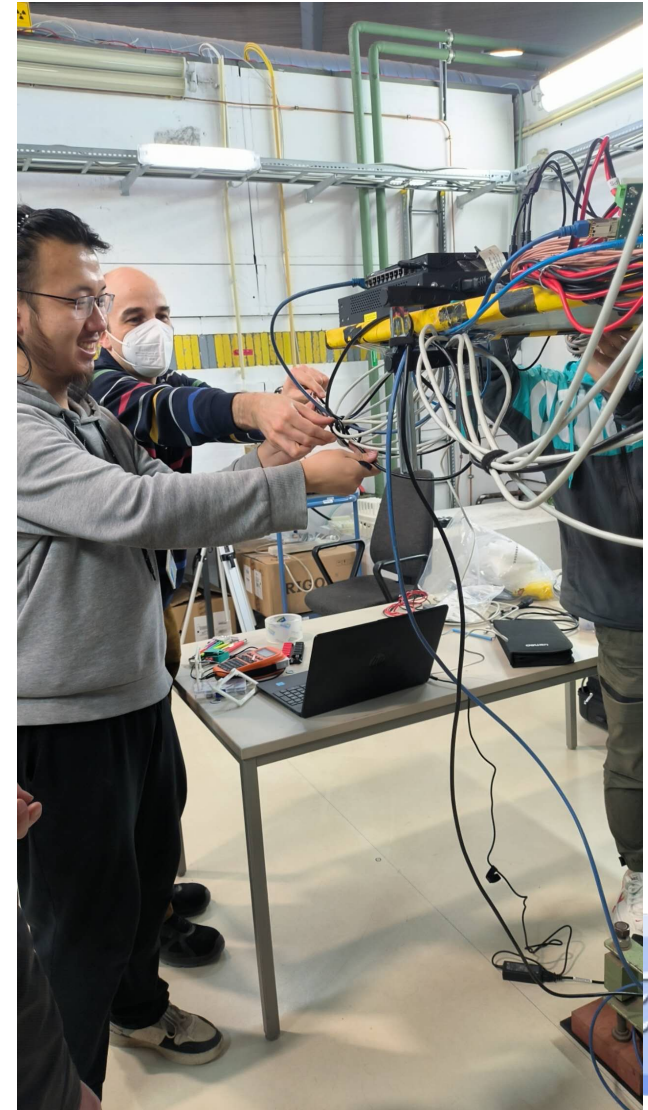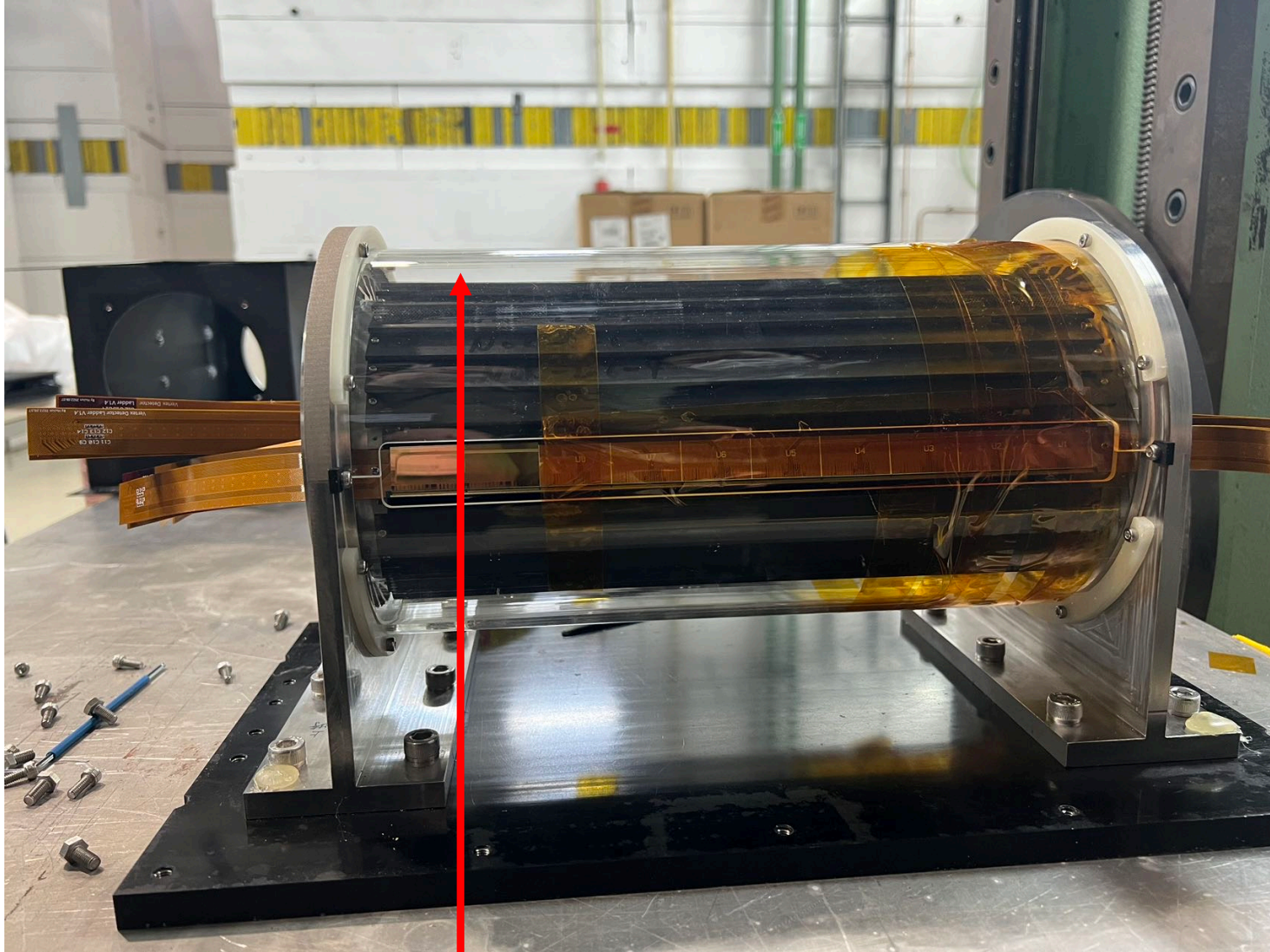Hongyu Zhang （IHEP） DAQ

Jinyu Fu, Mingyi Dong （IHEP） Assembly

Wei Wang, Gang Li, Linhui Wu （IHEP） Offline

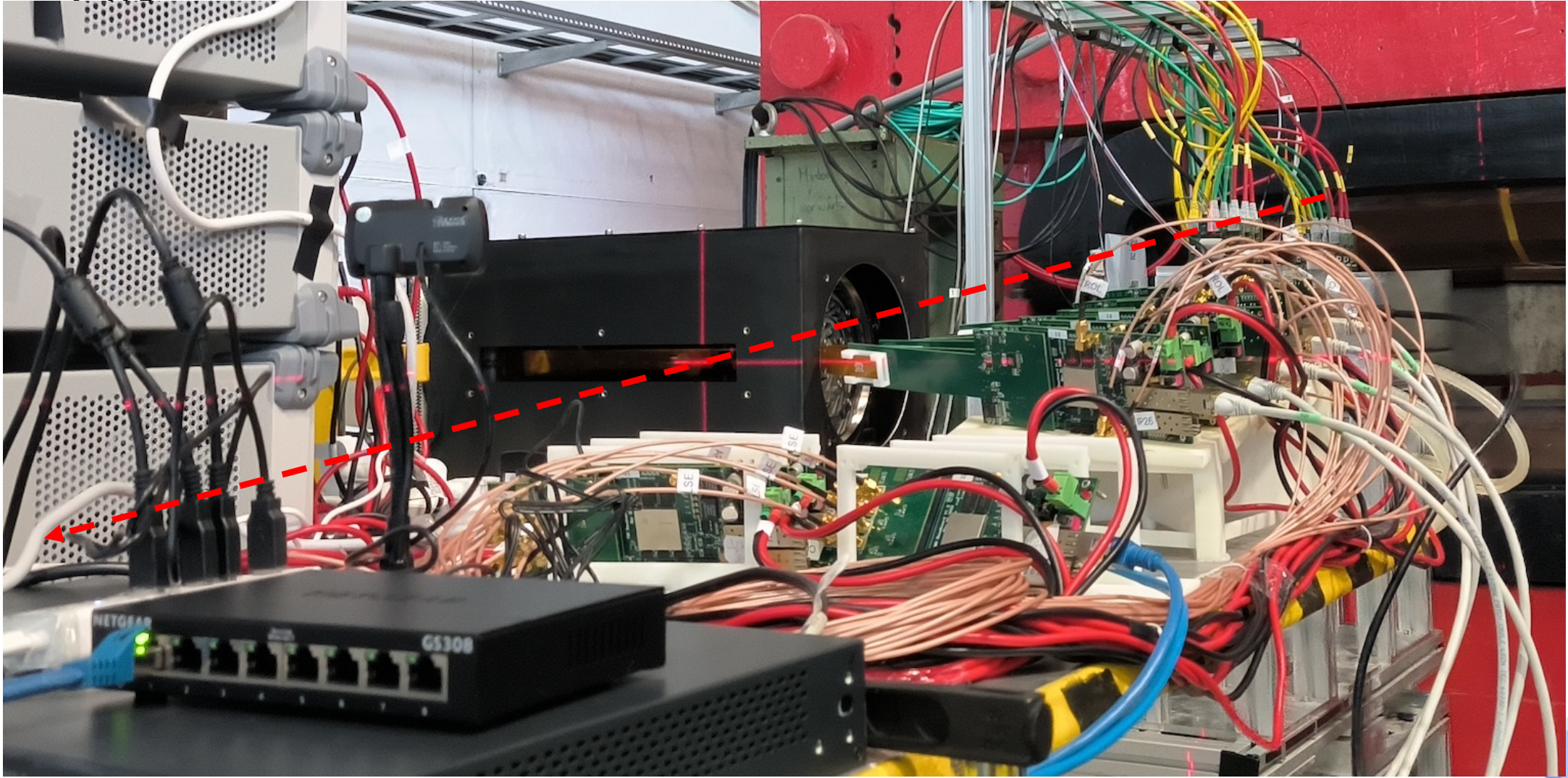Yiming Hu, Xiaoxu Zhang (NJU)…Offline/ ASIC

Prototype assembly@ DESY
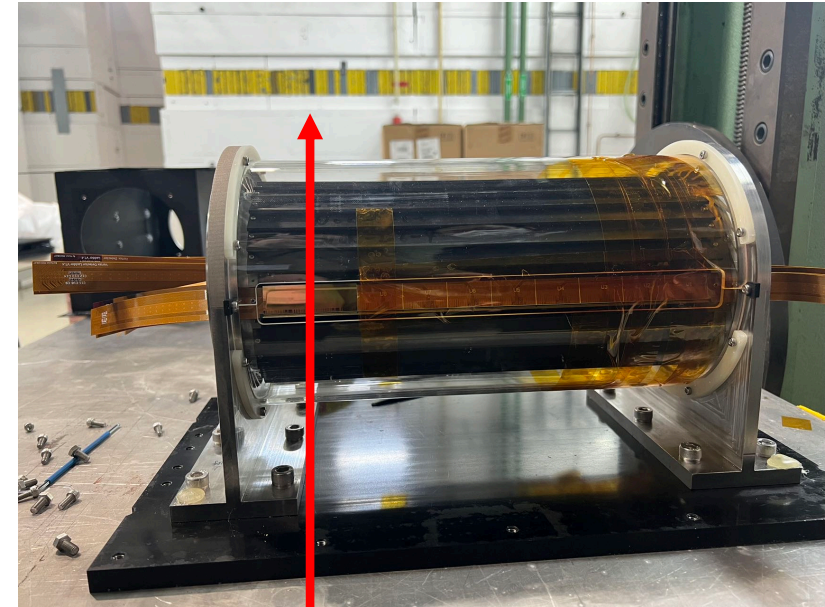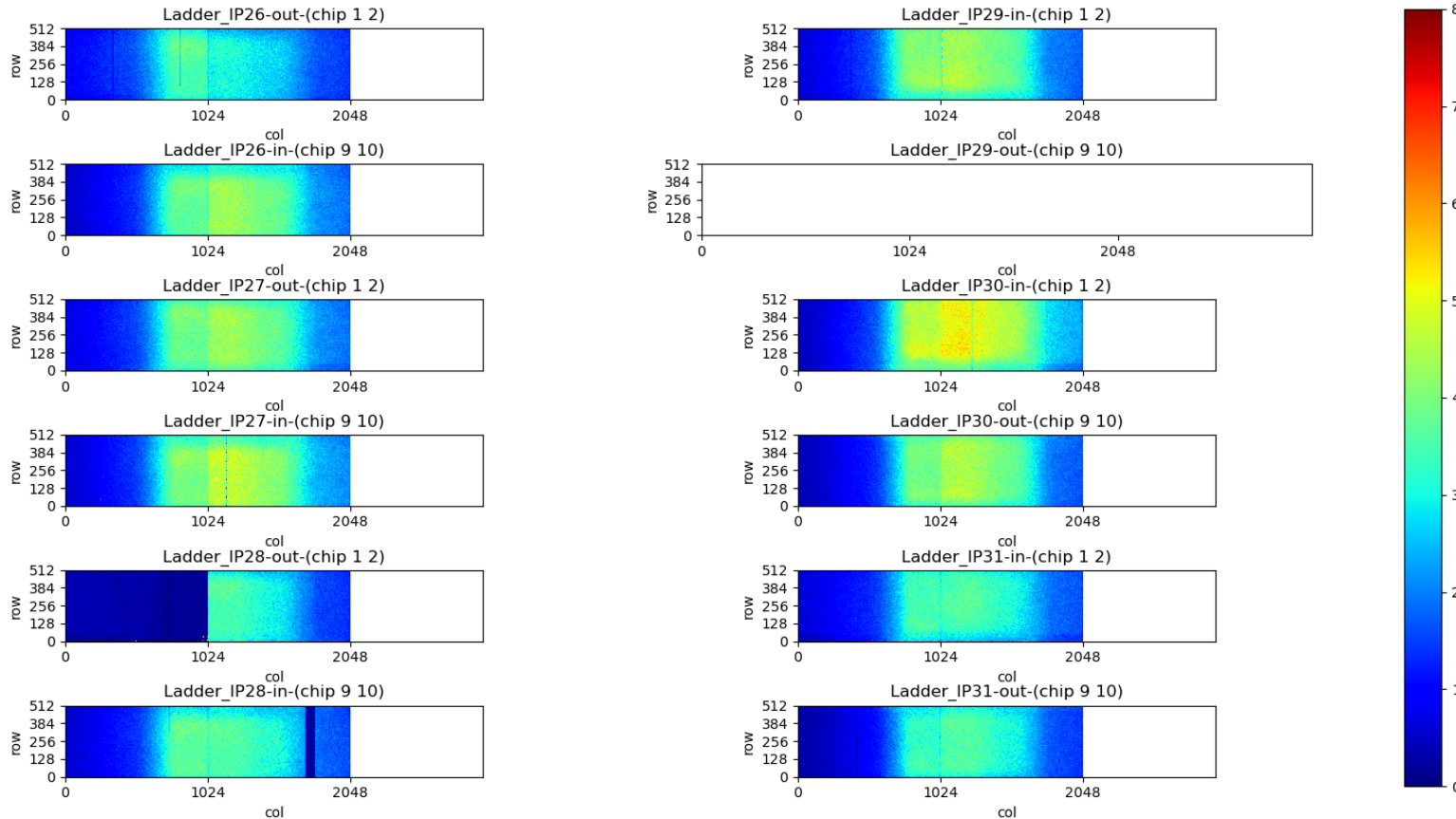
Setup at DESY

Hit maps in testbeam

- Beam is going through 12 layers of TaichuPix chip
  - Hitting at middle of two chips
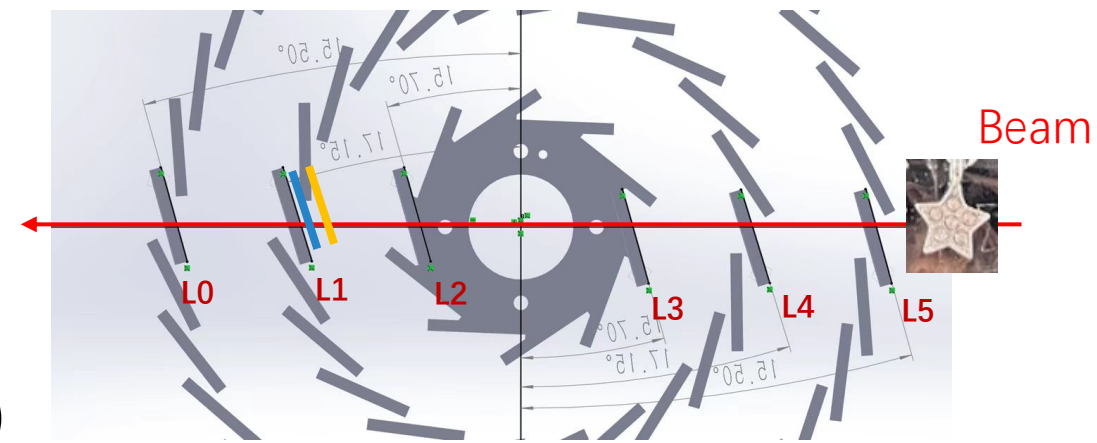 - Threshold of the chip are optimized during operation

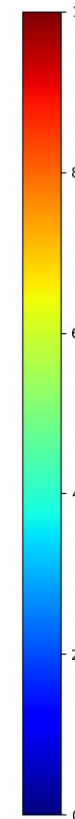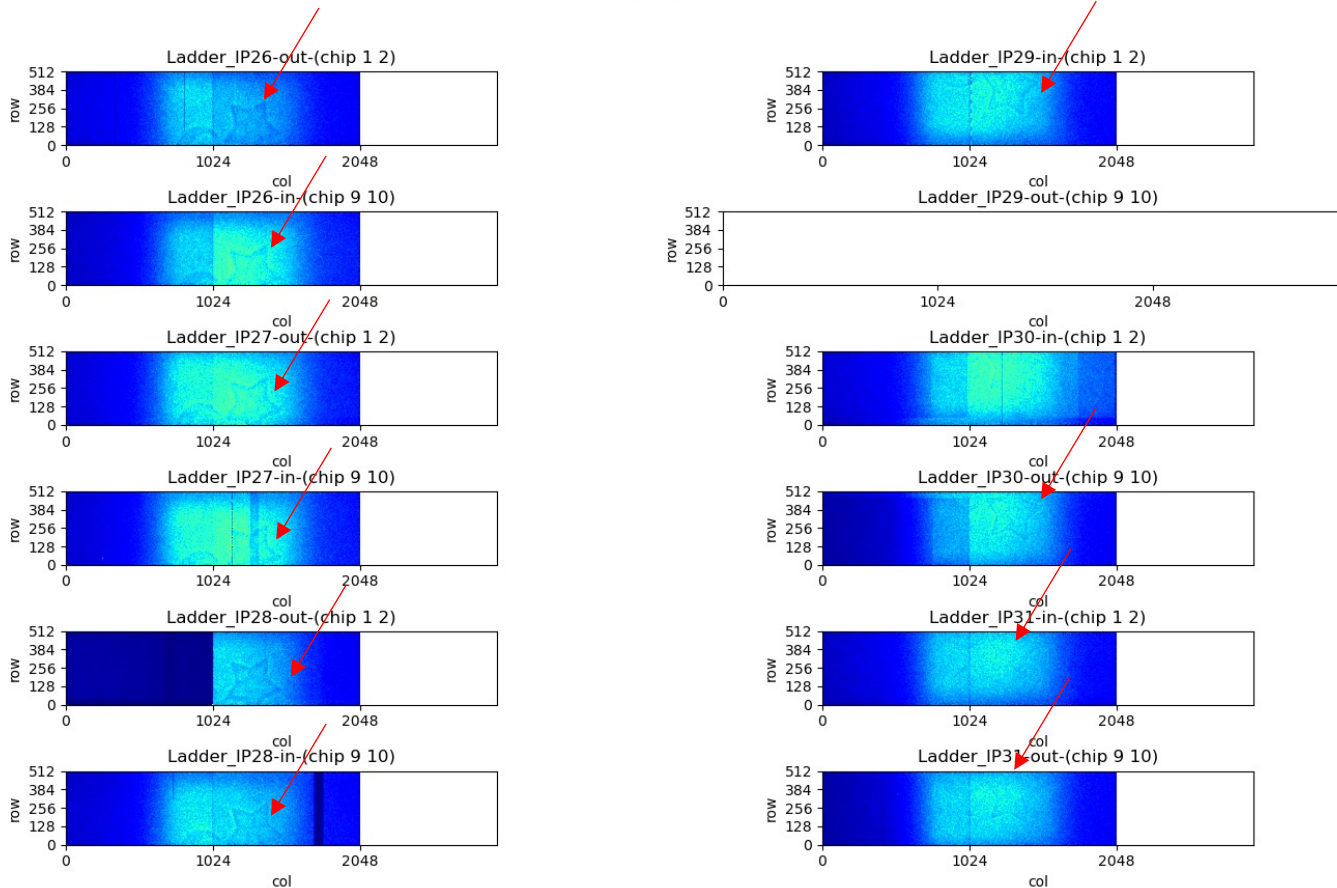DAQ,On-line monitoring
Jia Zhou
Hongyu Zhang

Hit maps in testbeam

- To understand the hitmap and geometry
- Put a metal star in upstream
- Star is visible in the hit maps (Imaging experiment)

Prototype assembly @DESY

- **Dedicated air cooling channel designed in prototype.**

  ➢ Measured Power Dissipation of Taichu chip: ~60 mW/cm²

  ➢ Before turning on the fan, chip temperature can go above 41 ℃.

  ➢ With air cooling, chip temperature can reduced to 25 ℃ (in average).

  ➢ No visible vibration effect observed in position resolution offline analysis due to the fan
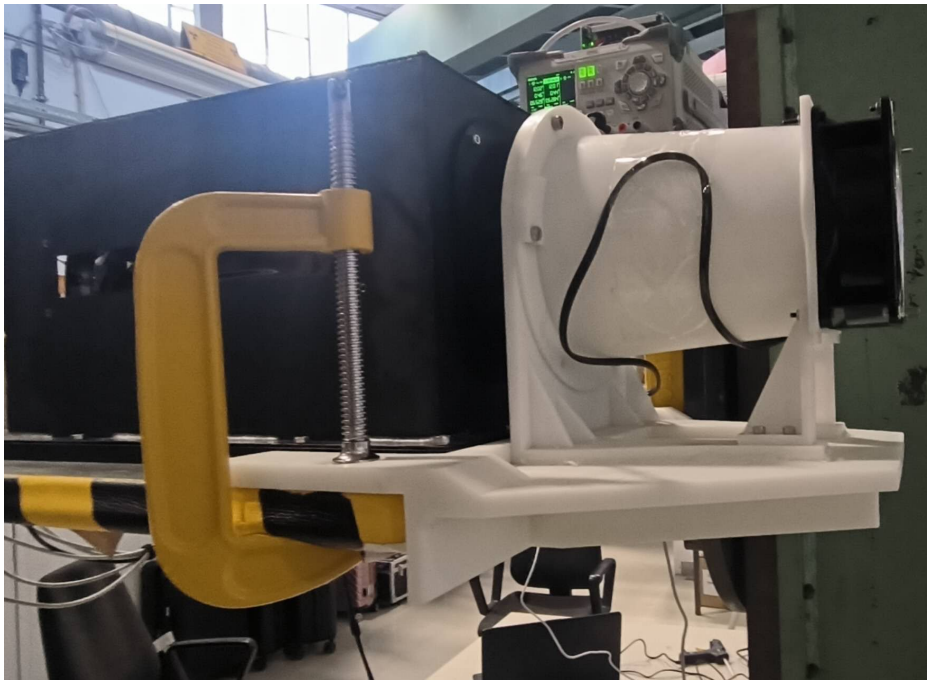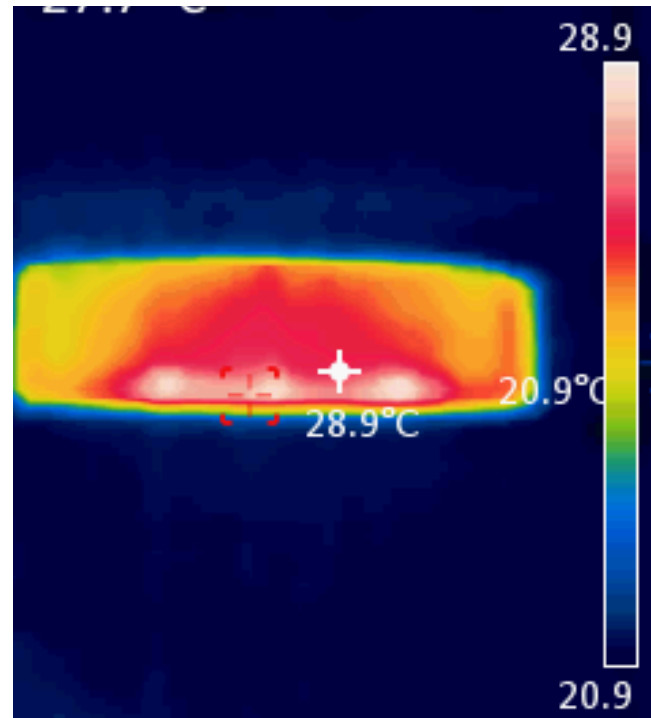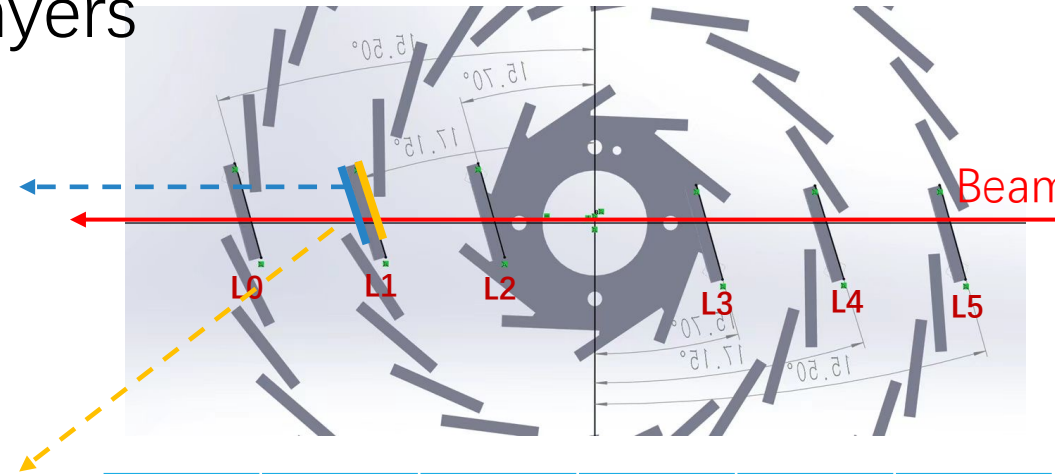
fan turned on   fan turned off
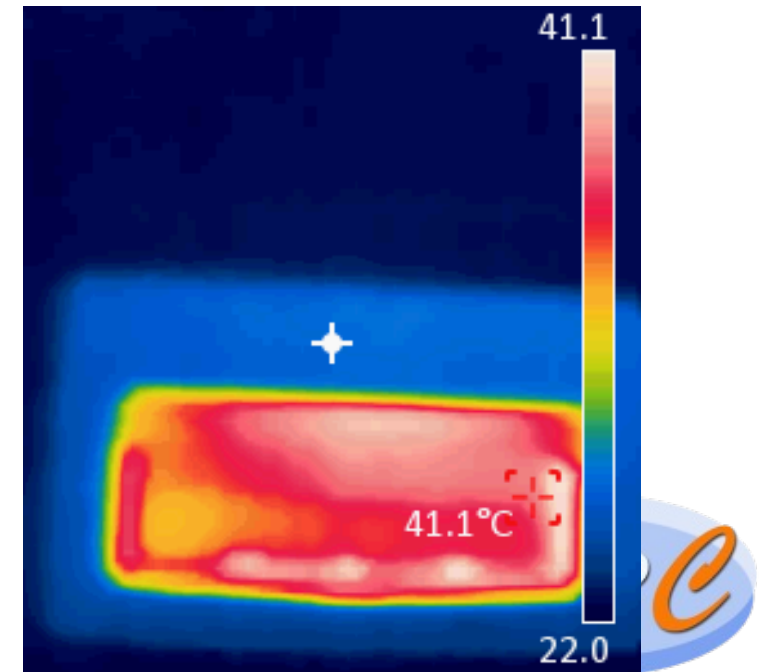
Preliminary spatial resolution

- Track fitting with 6 double layers/ 3 double layers
  - Resolution fitted with 3 layers is better
  - Material effect → multi scattering
  - Straight line fit is not good for more layers
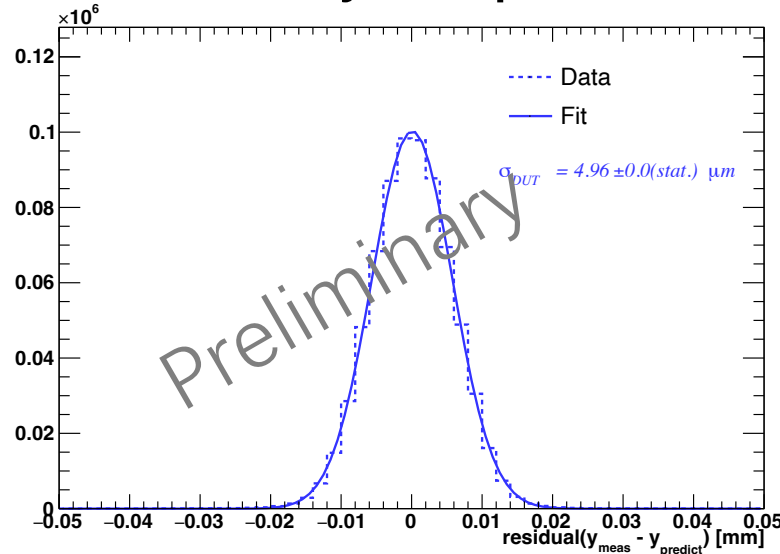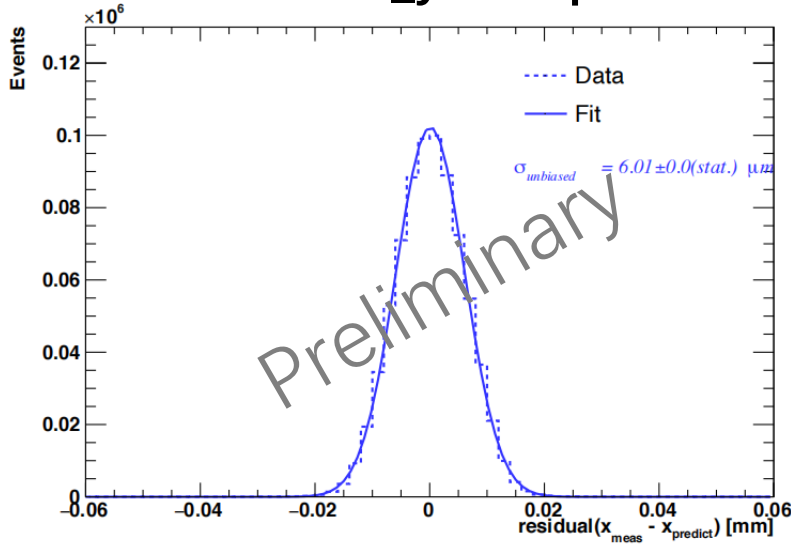   - Kalman filter is implementing in next step

Beam

L0 L1 L2 L3 L4 L5

Fitting tracks with
L0、L1、L2、L3、L4、L5

Resolution _y ~ 6 µm

Fitting tracks
with L0、L1、L2

Resolution_y ~ 5 µm

	L0-L1	L1-L2	L2-L3	L3-L4	L4-L5
L(mm)	21.2	20.6	37.46	20.6	21.2

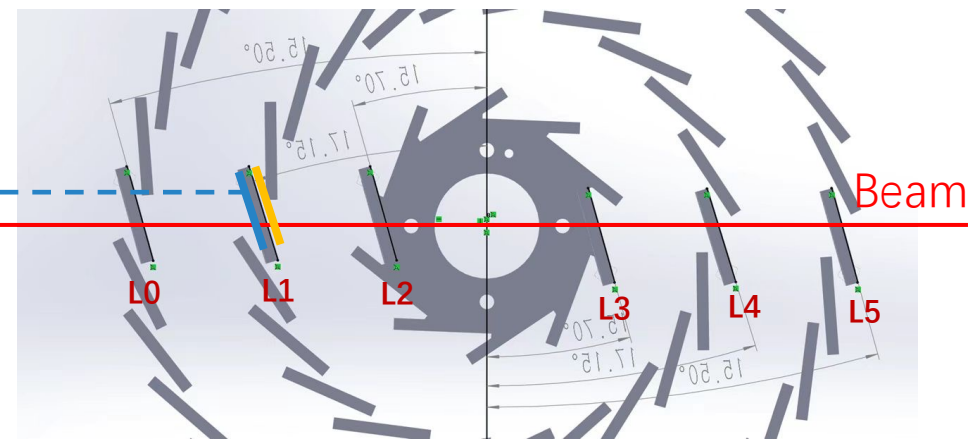The thickness of one ladder is around 0.796 mm.

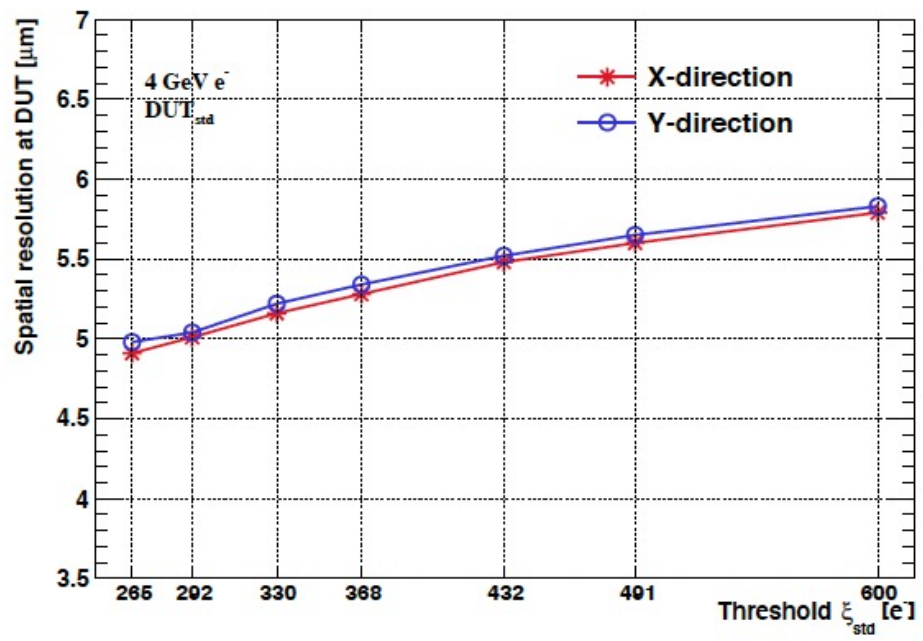by Shuqi Li

Preliminary threshold scan result

- Spatial resolution in 2023 testbeam is worse
  - Disadvantage in 2023 testbeam
    - Detector-level: more realistic material budget
  - Advantage in 2023 testbeam
    - Smaller Distance between layers (~2cm)
    - Beam energy increased to 6GeV

Beam

L0 L1 L2 L3 L4 L5

Shuqi Li

**Spatial resolution Vs threshold
2023 detector-level testbeam**

6 GeV e⁻
planeID = 7
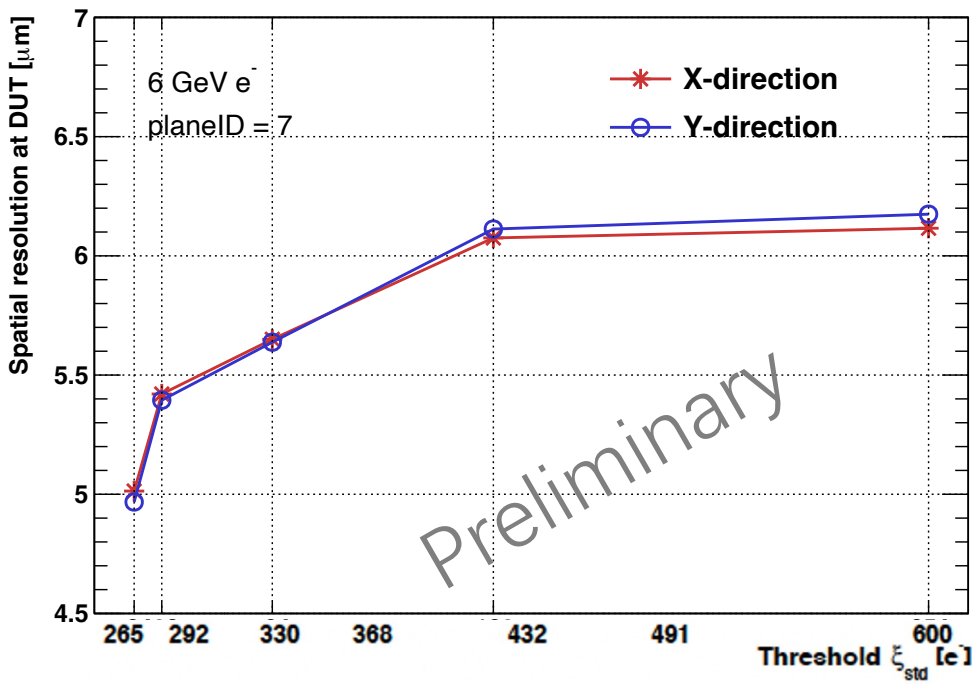
Preliminary

**Spatial resolution Vs threshold
2022 telescope testbeam**

4 GeV e⁻
DUT_{std}

17

Summary

- The vertex detector project review is supposed to be finished in June 2023.

- The preliminary offline results shows a single point spatial resolution less than 5 µm, more analysis is going on.

- A full size ladder with 10 TaichuPix-3 chips is under installation, more results are analyzing

- Plan to do the proton irradiation test for TaichuPix-3 in CSNS at the end of May
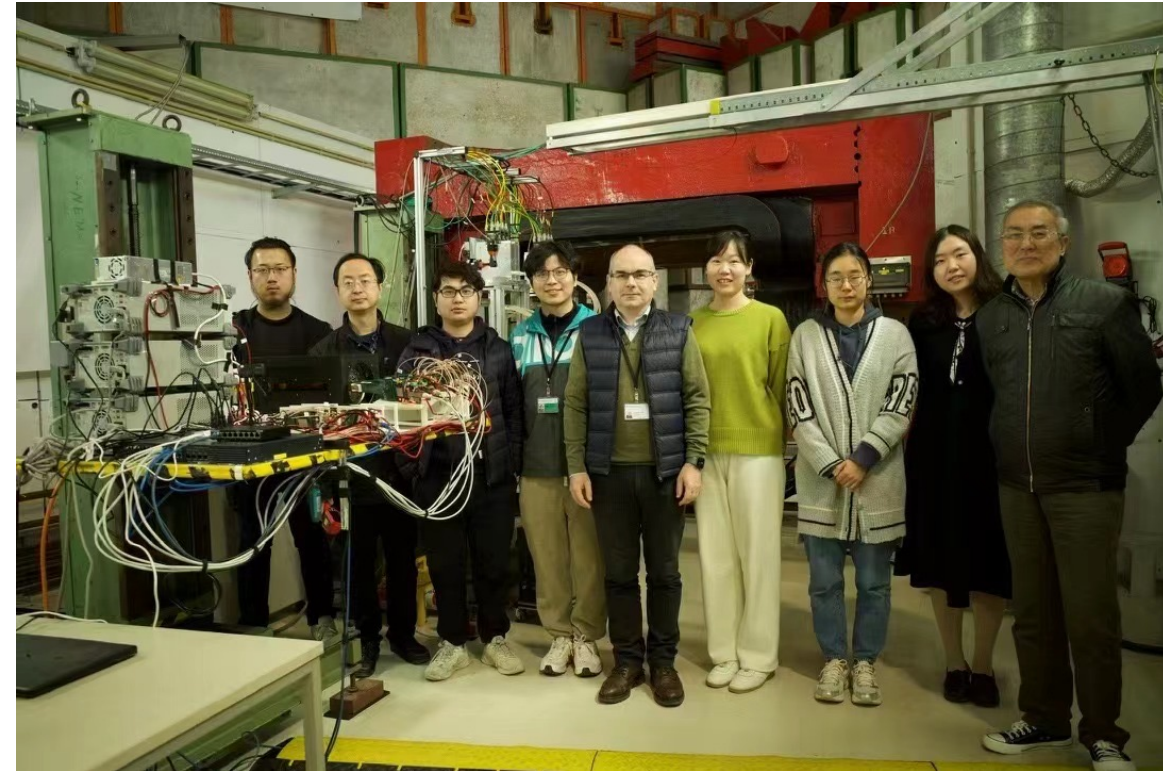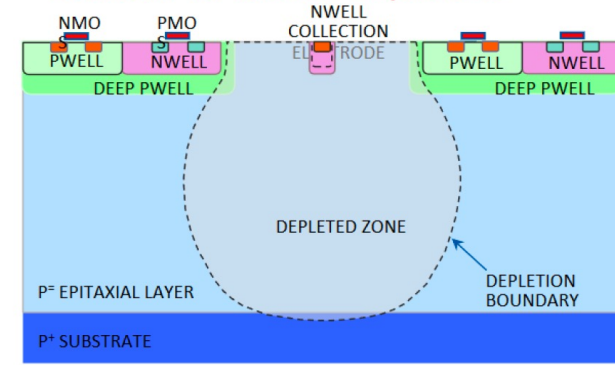
Resolution vs. chip threshold

➢ The spatial resolution improved by lowering the threshold
  ➢ Can reach around 5μm resolution
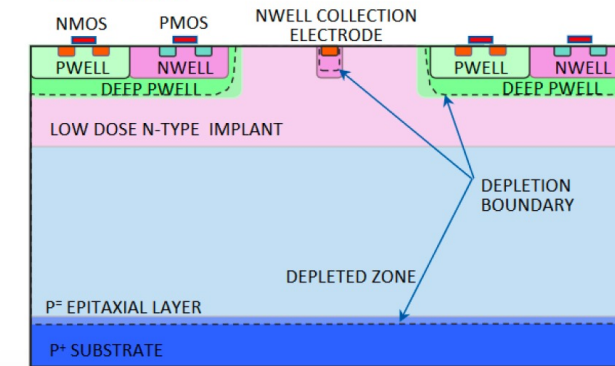 ➢ Lower operation temperature can reduce threshold
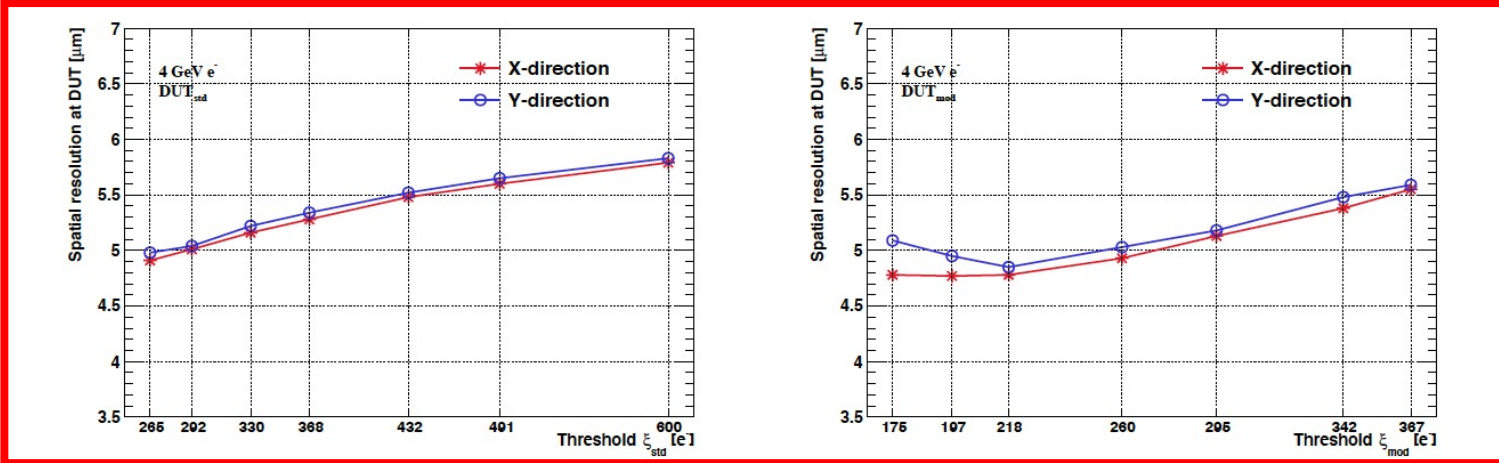
Modified process   ## Standard process

Resolution

Efficiency

Standard : no full depletion
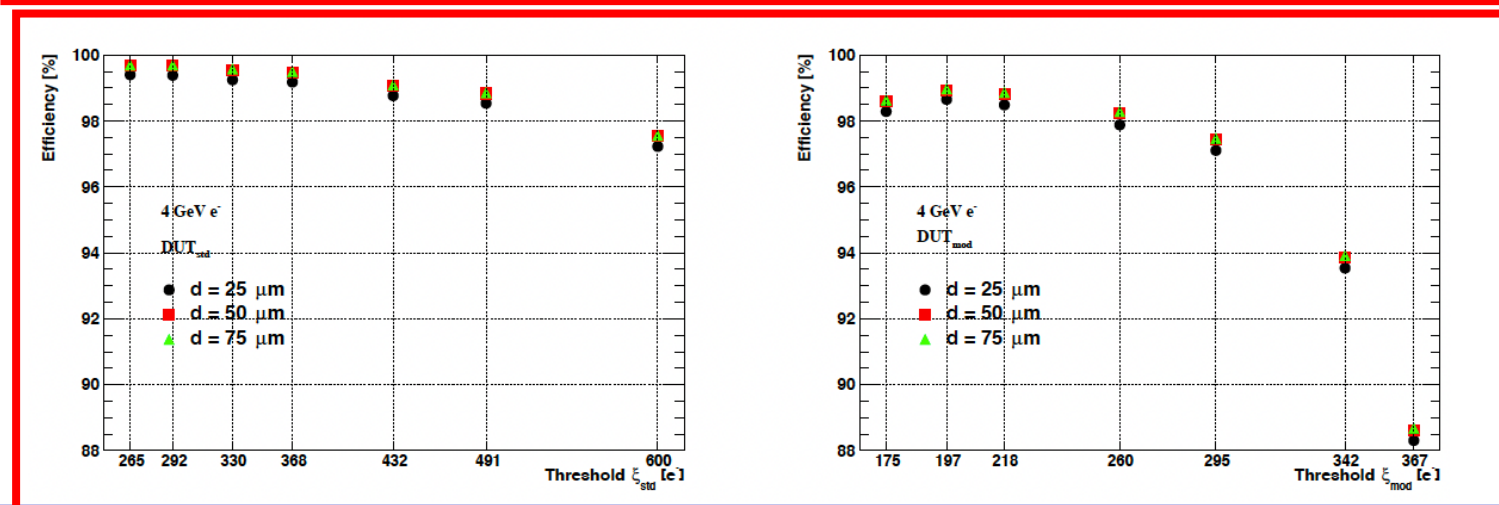
Modified : full depletion, faster charge collection

Shuqi Li
Linghui Wu
Gang L
Zhijun Liang
Xuewei Jia
Joao

CEPC

Prototype assembly @DESY

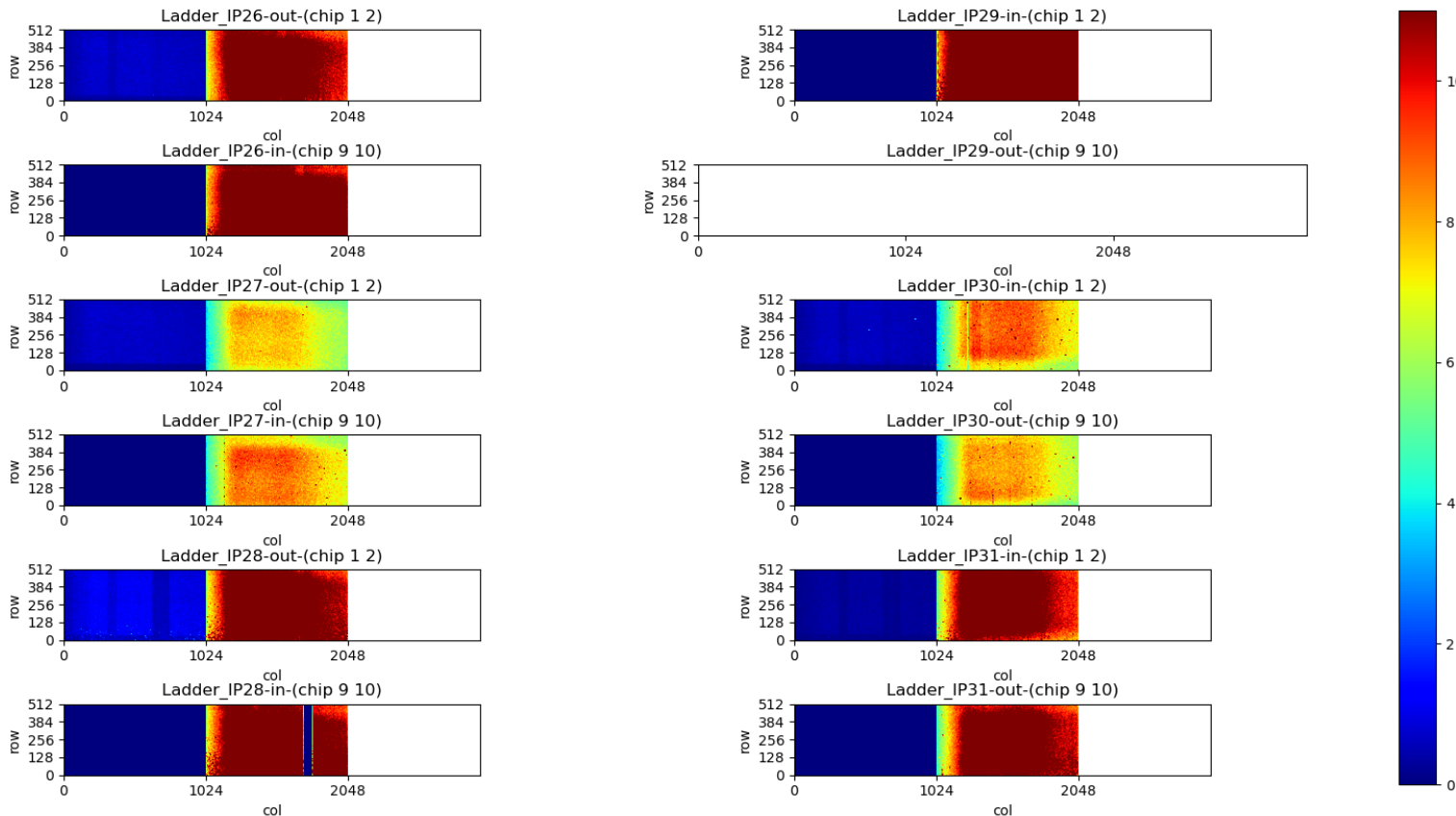- **D f**

Prototype assembly @DESY

Lower down Thresholds by each chip

- With air cooling, we can lower down the threshold of each chips
- After tuning the threshold, hit maps looks more uniform

Hitmap

a medium chip will not participant track reconstruction
the residual plot of fit position and measured position decide the spatial resolution

Electron Beam

Chip