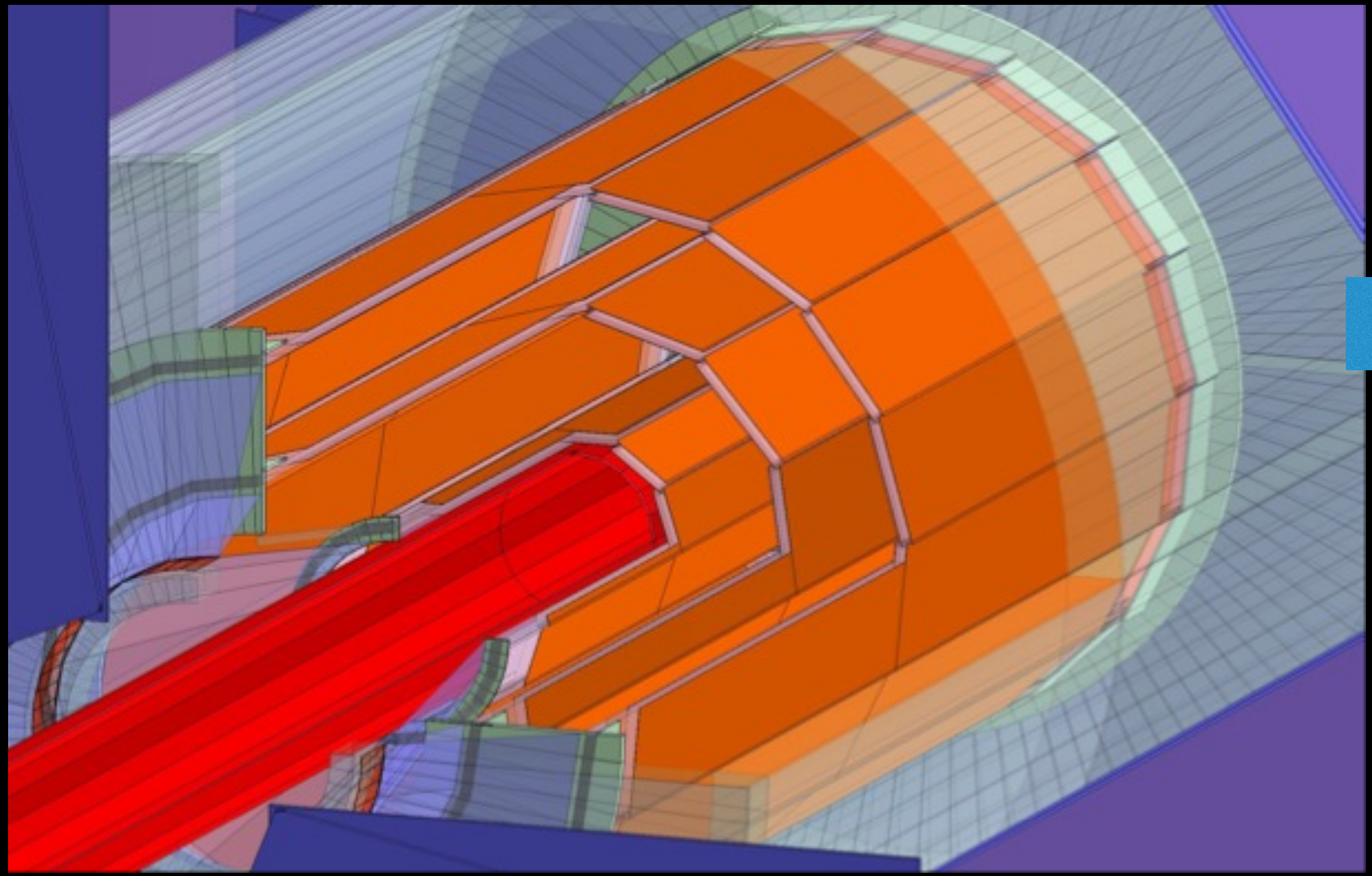
CEPC vertex detector prototype status

Zhijun Liang (IHEP)
For the CEPC vertex detector prototype team

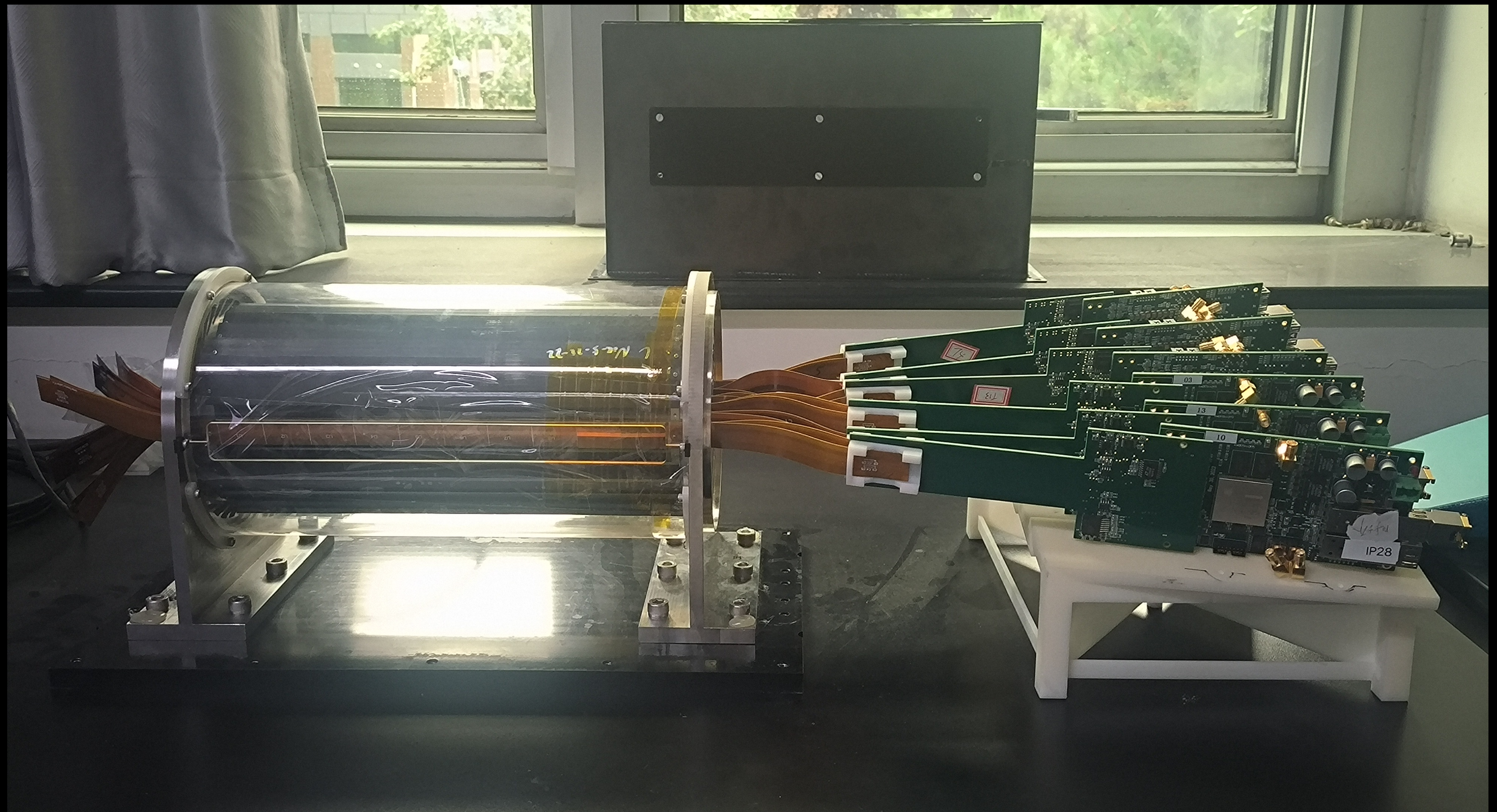
Vertex detector prototype structure optimization

- Based on CEPC vertex detector conceptual design → Three double-layer barrel detector
  - This project plan to prototype the important part of vertex detector (CDR design)
  - The cost for the full vertex detector is high (eg: ~50 M CHF for ATLAS ITk pixel detector)
    - → Plan to build full mechanical part of the detector
    - → install a sector of ladders in prototype , not necessary to build full vertex for R & D
- Optimize the geometry based on real ASIC and electronics dimension
  - Optimize geometry based on its physics performance from simulation
  - Engineering design of prototype structure

CEPC Vertex detector
Conceptual design (2016)

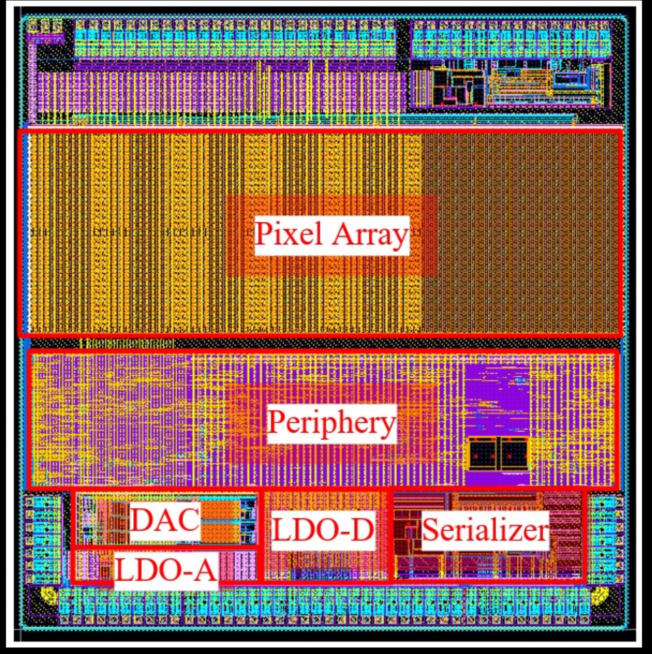


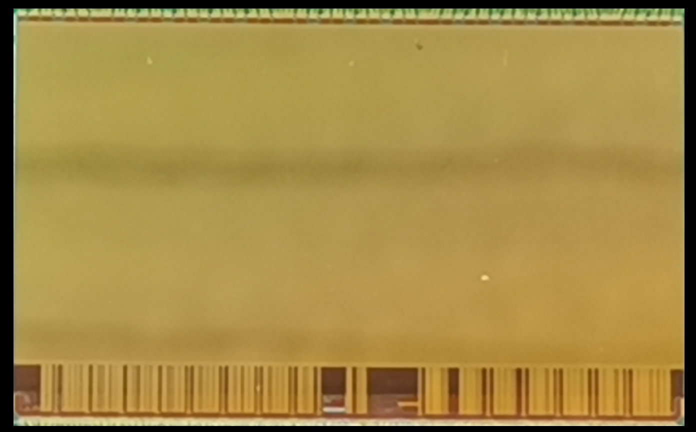
This project
Vertex detector prototype design



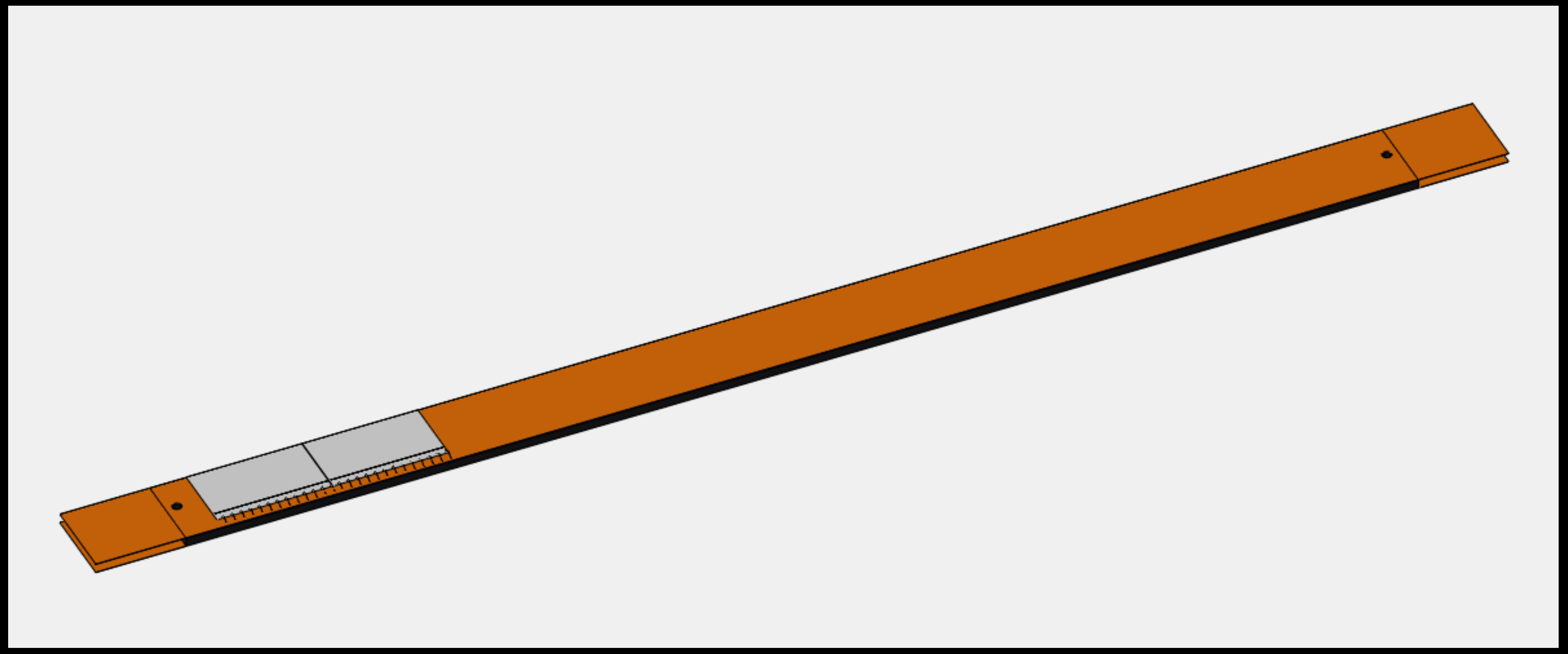
Overview of MOST2 vertex detector R & D

CMOS imaging sensor prototyping

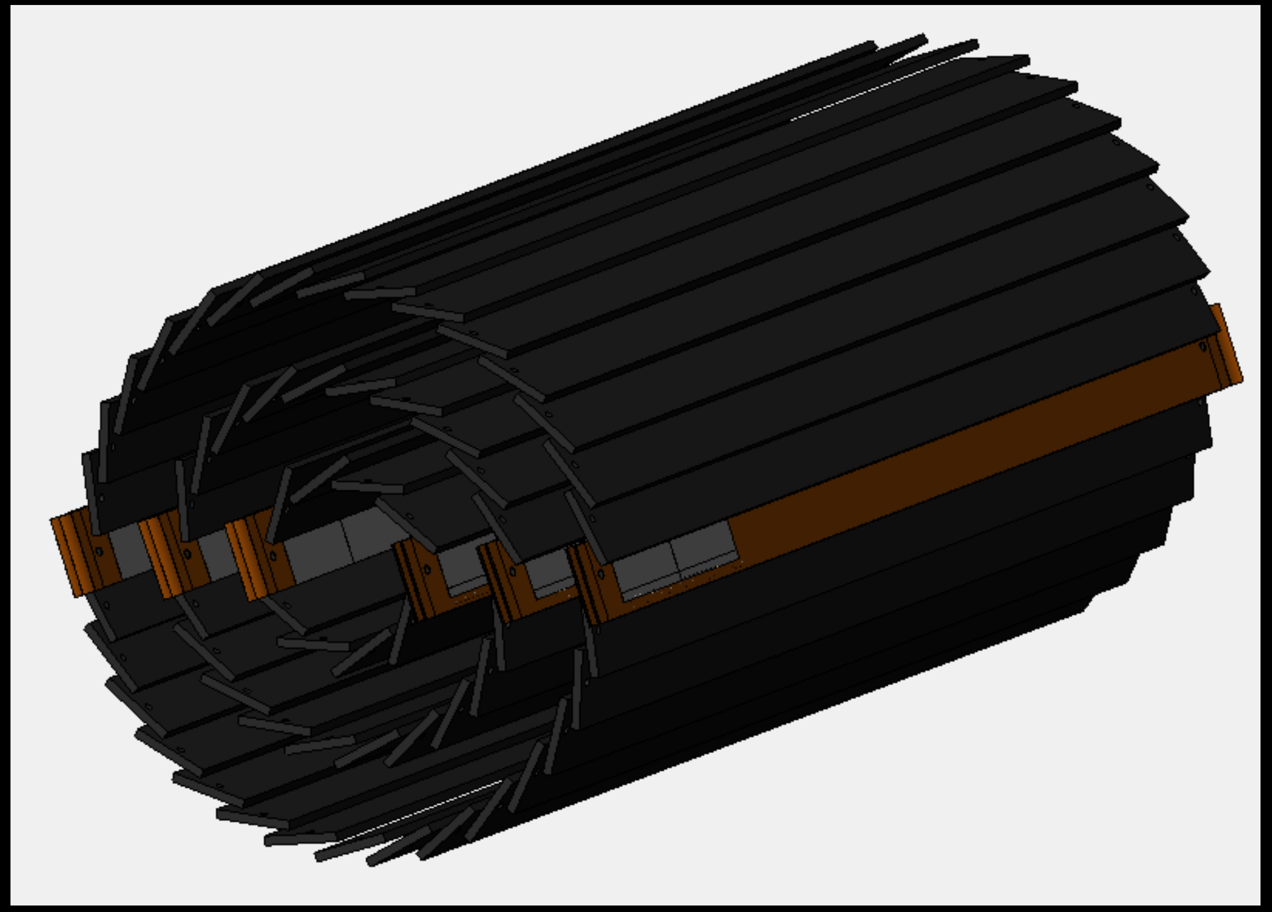


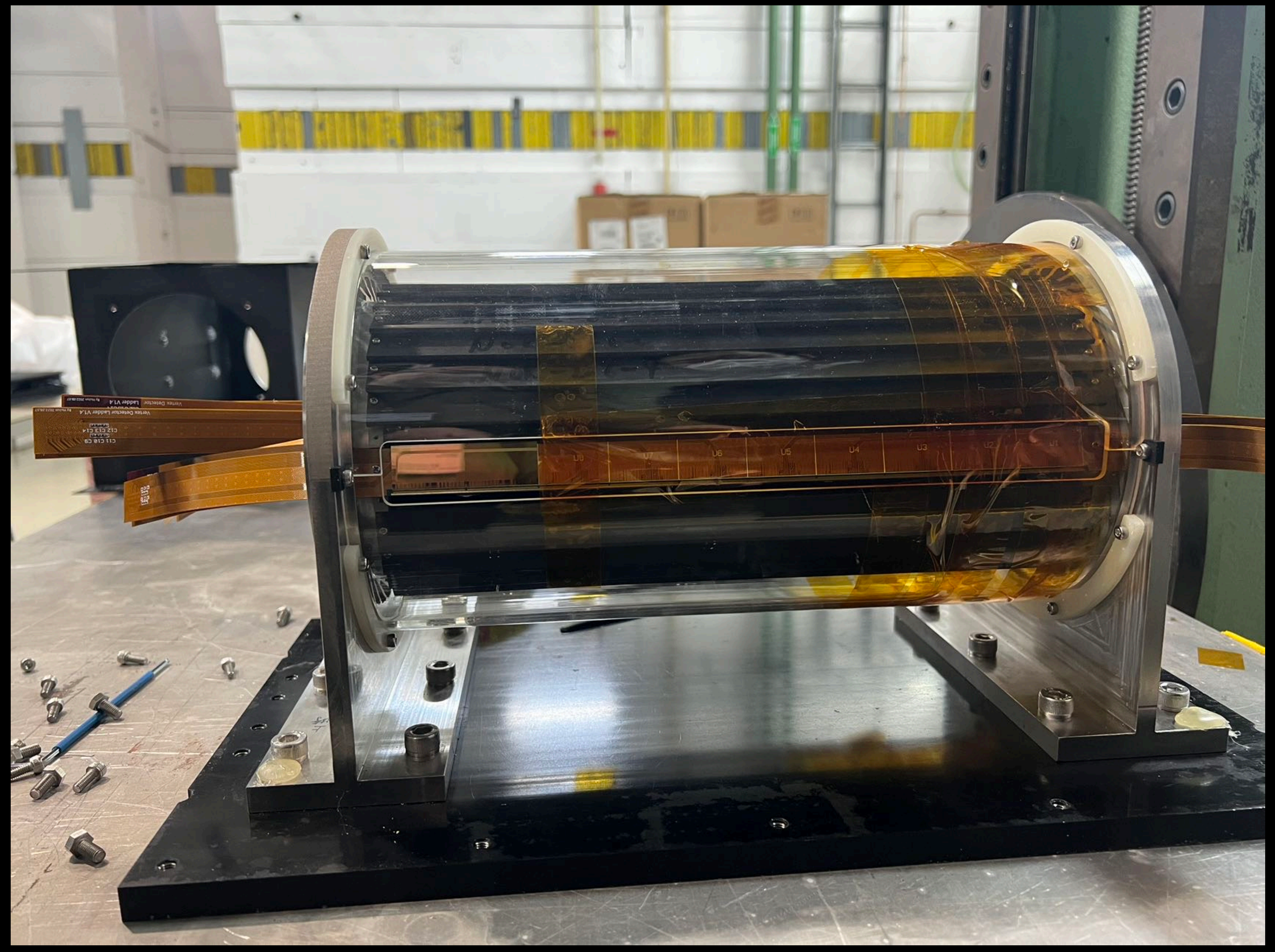


Detector module (ladder) Prototyping



Vertex detector Prototype for beam test



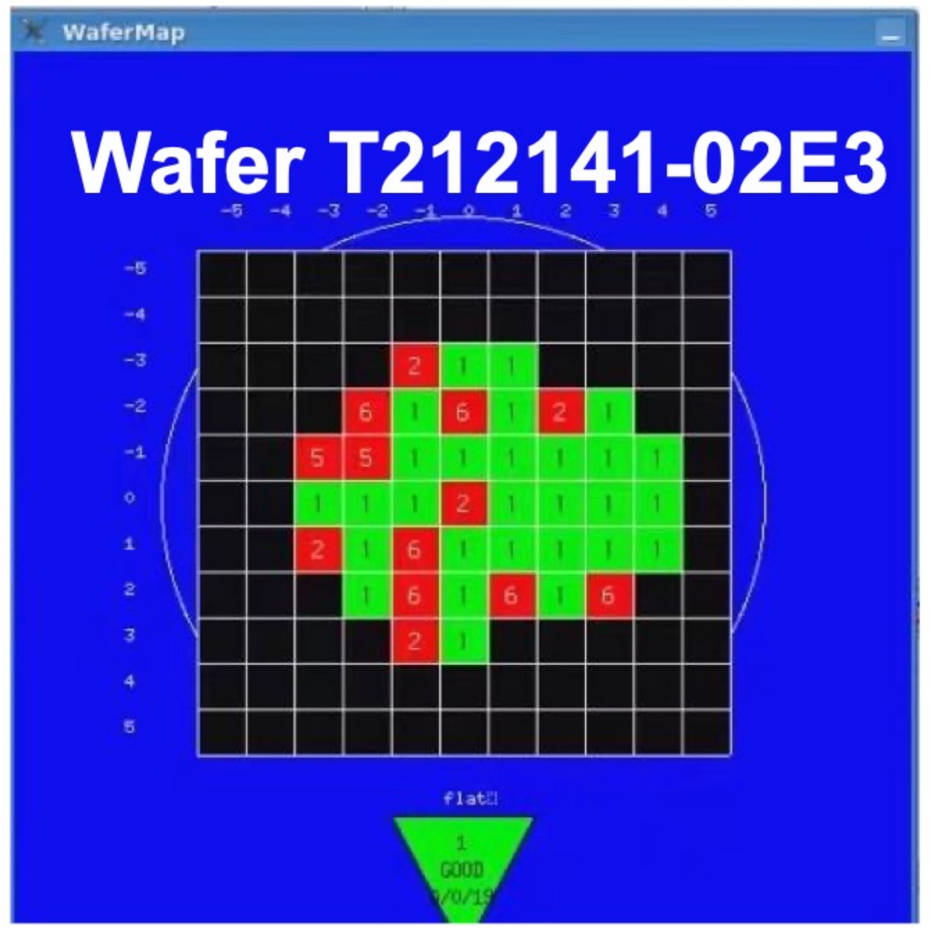


- Design CMOS imaging sensor chip
- Detector Module prototyping
- Vertex Detector assembly and testbeam

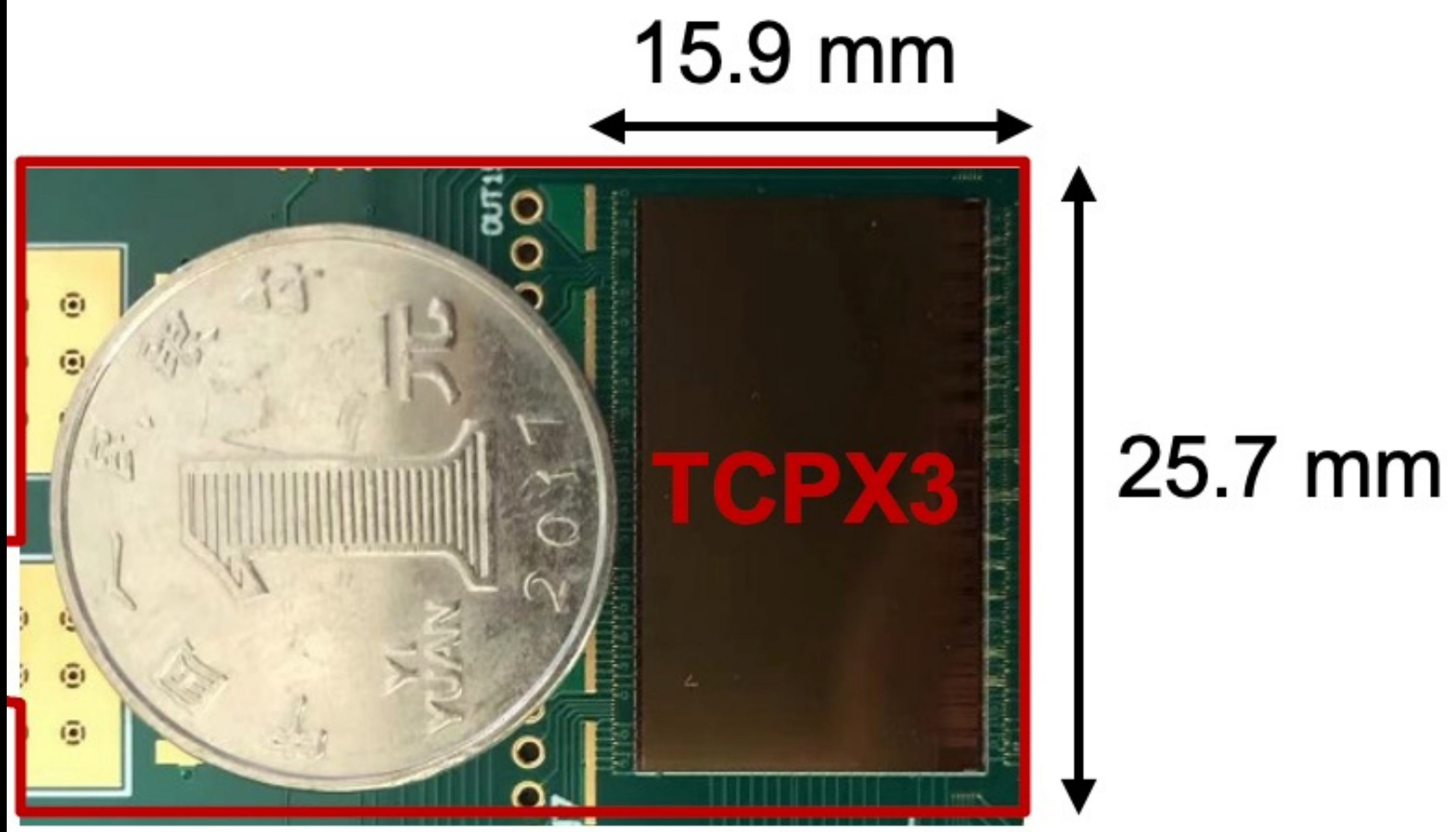
Full-size TaichuPix3 prototyping (engineering run)

- **Developed the first full-size CMOS pixel sensor for particle detector in China**
  - Full size 1024×512 Pixel array, Chip Size： 15.9×25.7mm
    - 25μm×25μm pixel size → high spatial resolution
    - Process: Towerjazz 180nm CIS process
  - Fast Periphery digital readout , high-speed data interface

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	√	X	√
Readout Speed	X	√	X
TID	X (?)	√	√



An example of wafer test result

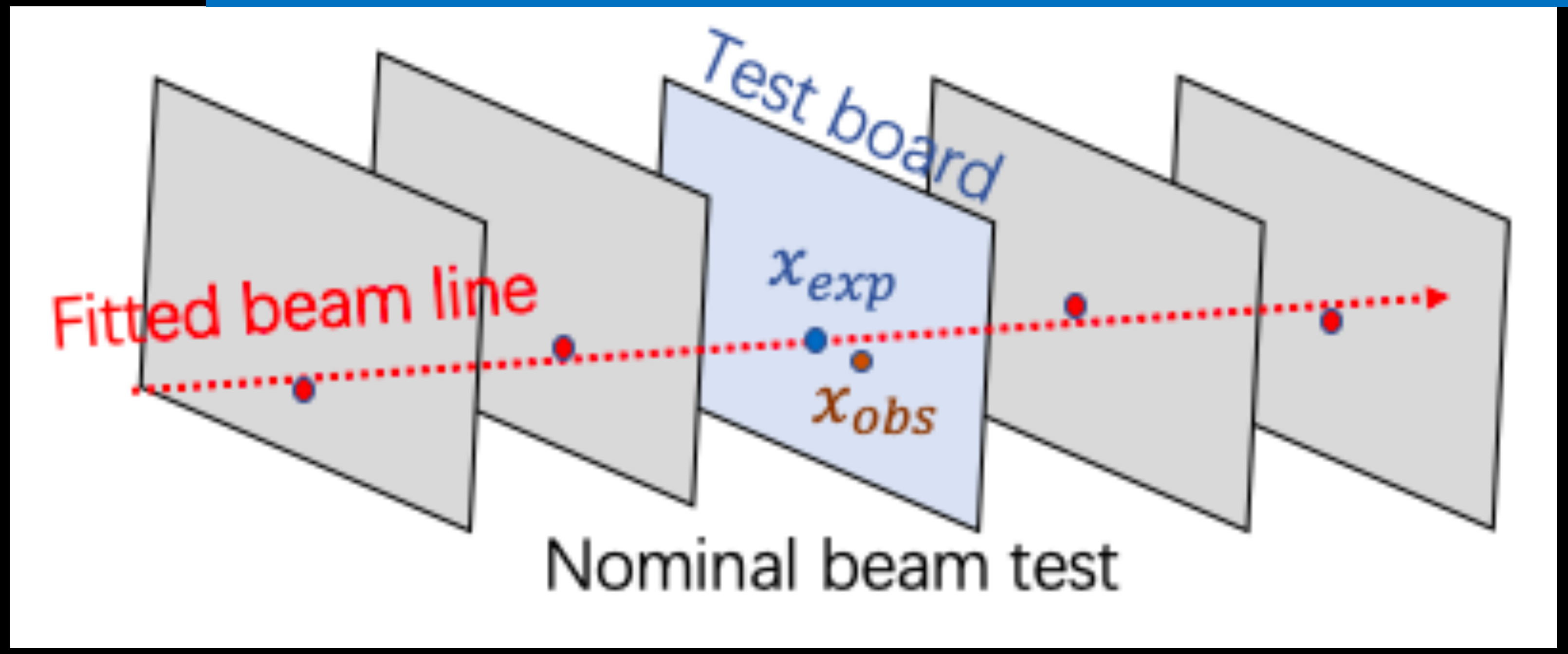


TaichuPix-3 chip vs. coin

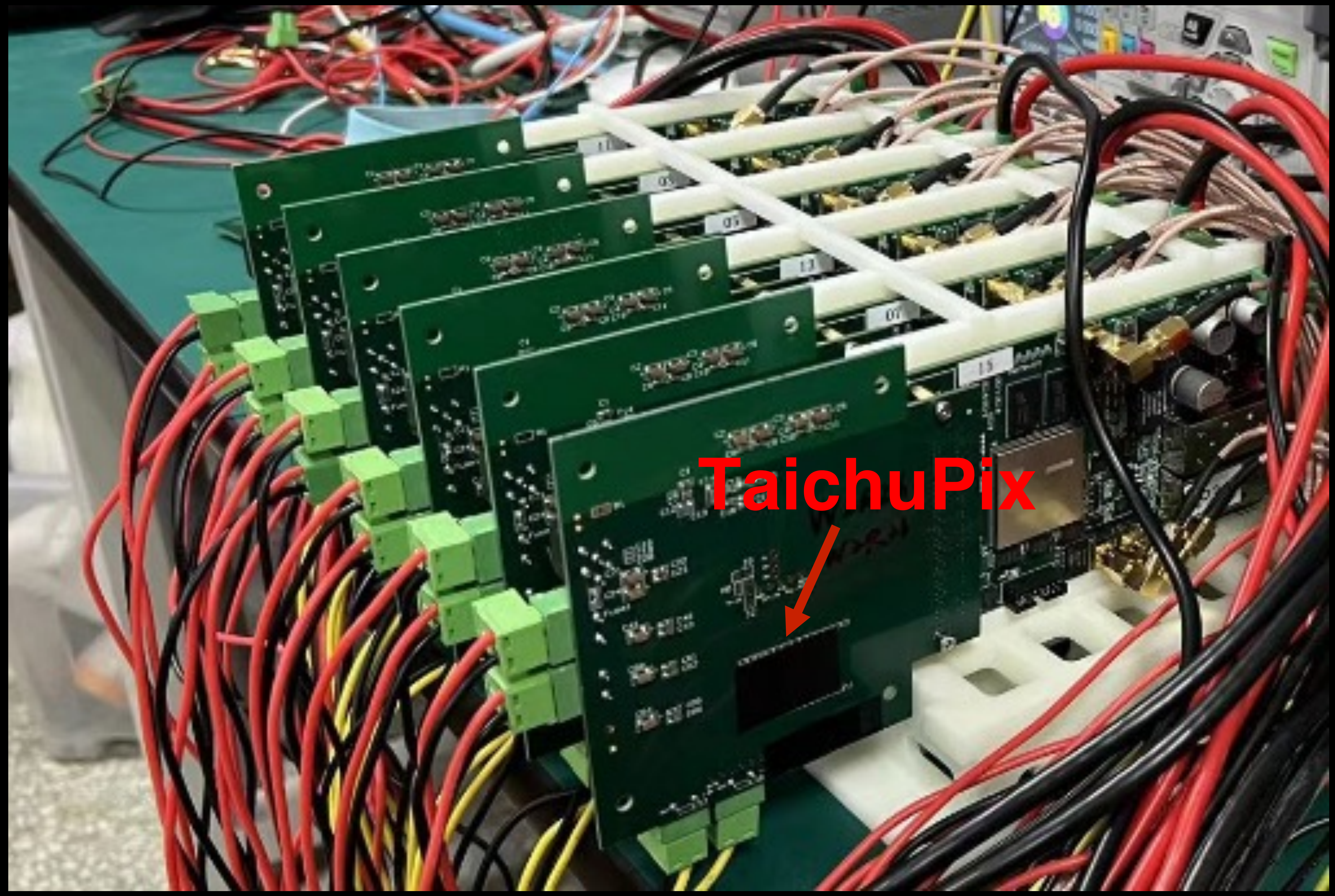
Spatial resolution measured by testbeam

Shuqi Li, Gang Li, Linghui Wu

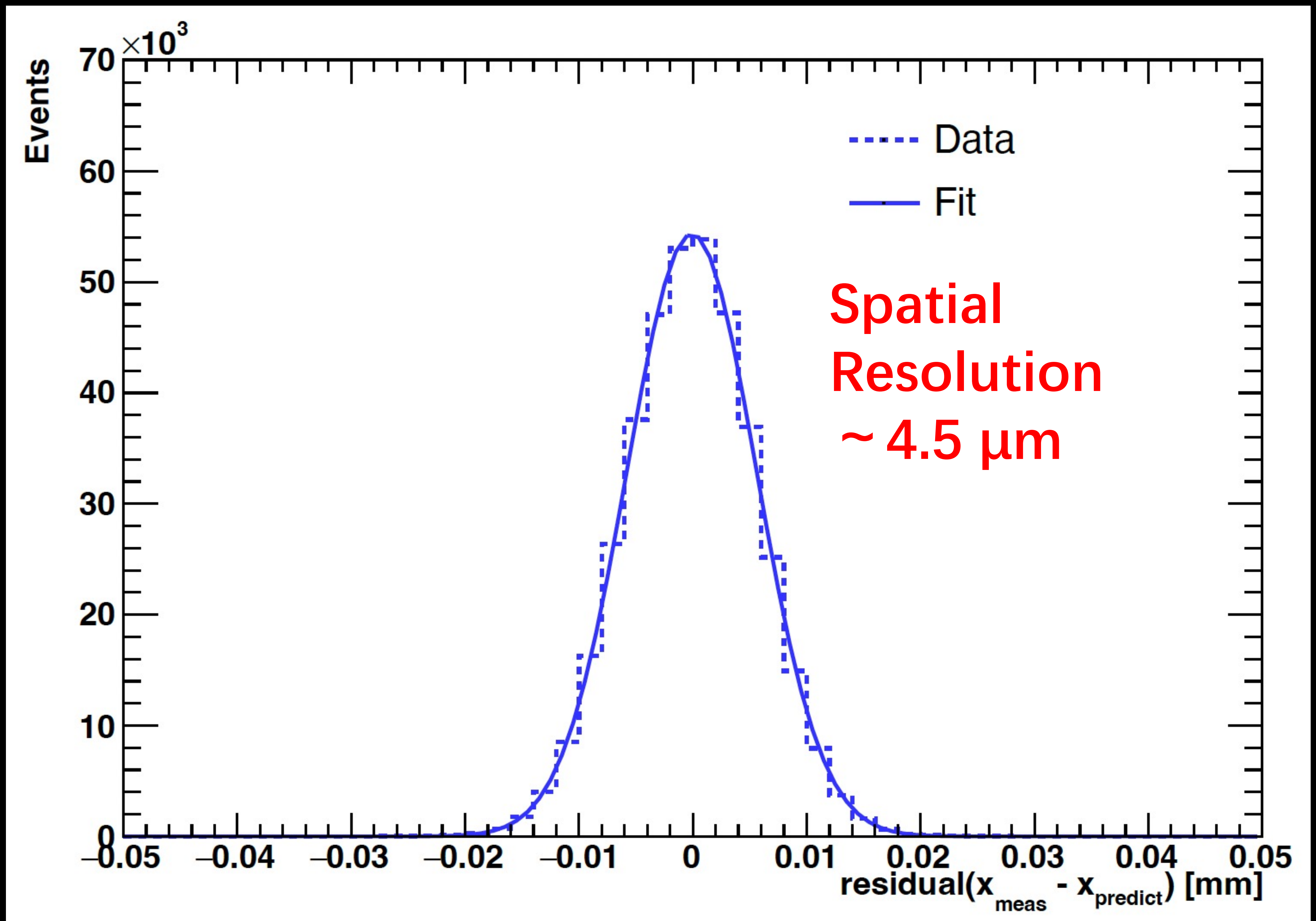
- The 6-layer of TaichuPix-3 telescope built
  - Tested at DESY with 4-5 GeV electron beam, 1kHz rate
  - One layer of TaichuPix used as Detector-Under-Test (DUT)
  - Other five layers as beam telescope used for track fitting
  - Spatial resolution of TaichuPix reach 4.5 μm
    - Reach the goal of the project (3-5 μm)



Setup for Taichupix beam telescope



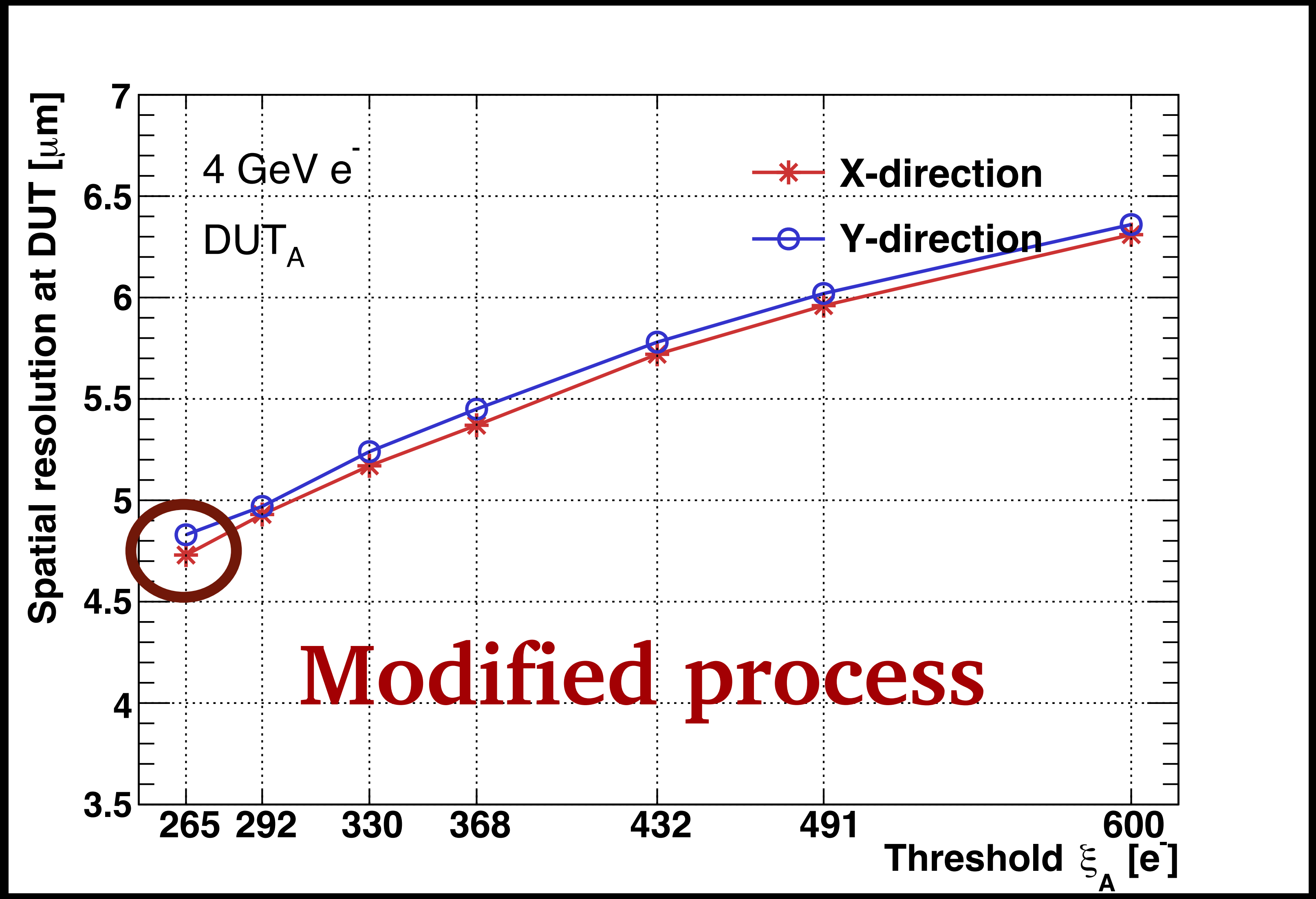
Residual distribution
DUT measured position – expected position from track

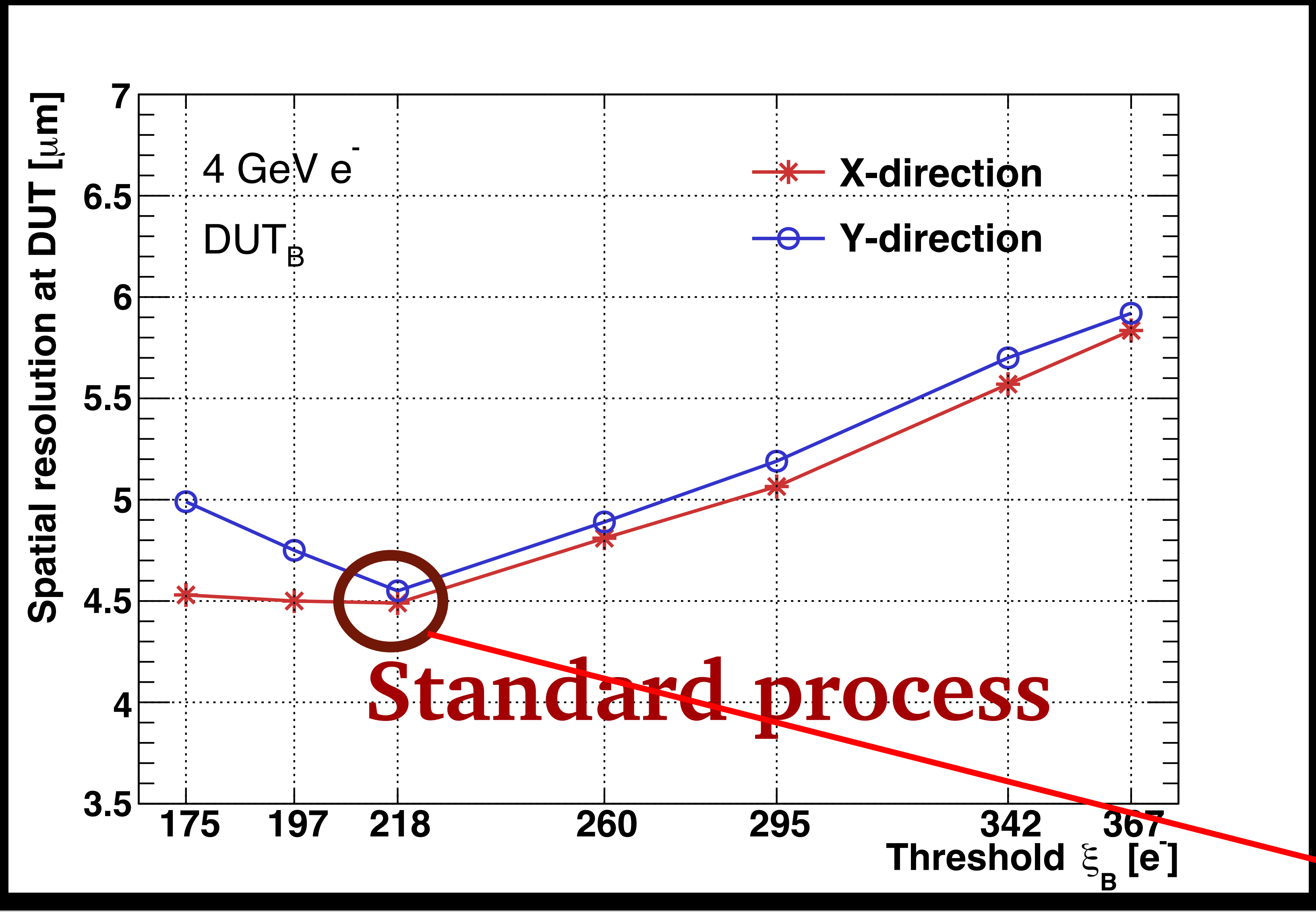


Spatial resolution and cluster size VS threshold

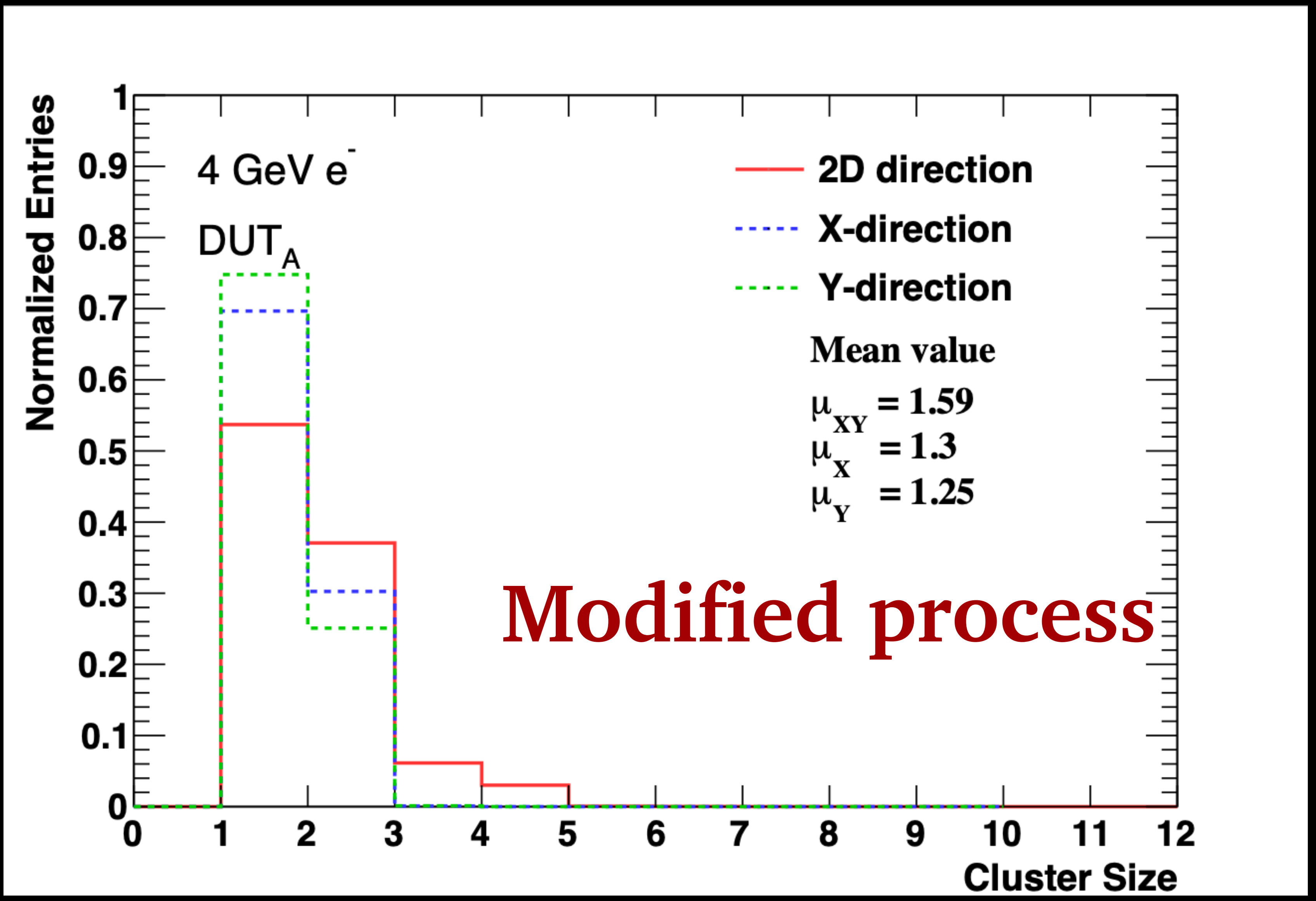
- The spatial resolution extracted by the unbiased residual distribution after substracting the track uncertainty→ **The spatial resolution less than 5 um**

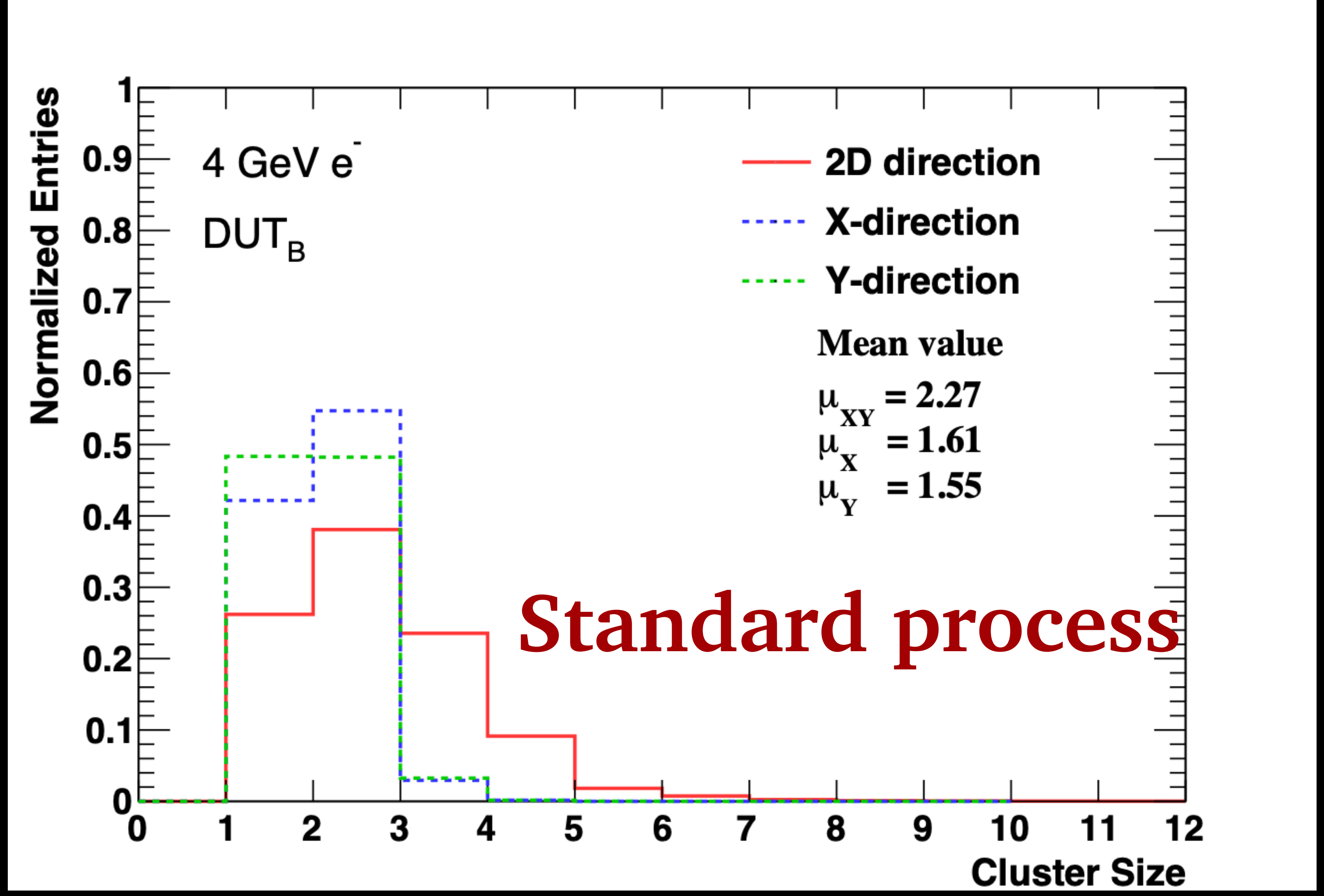
Shuqi Li, Gang Li, Linghui Wu

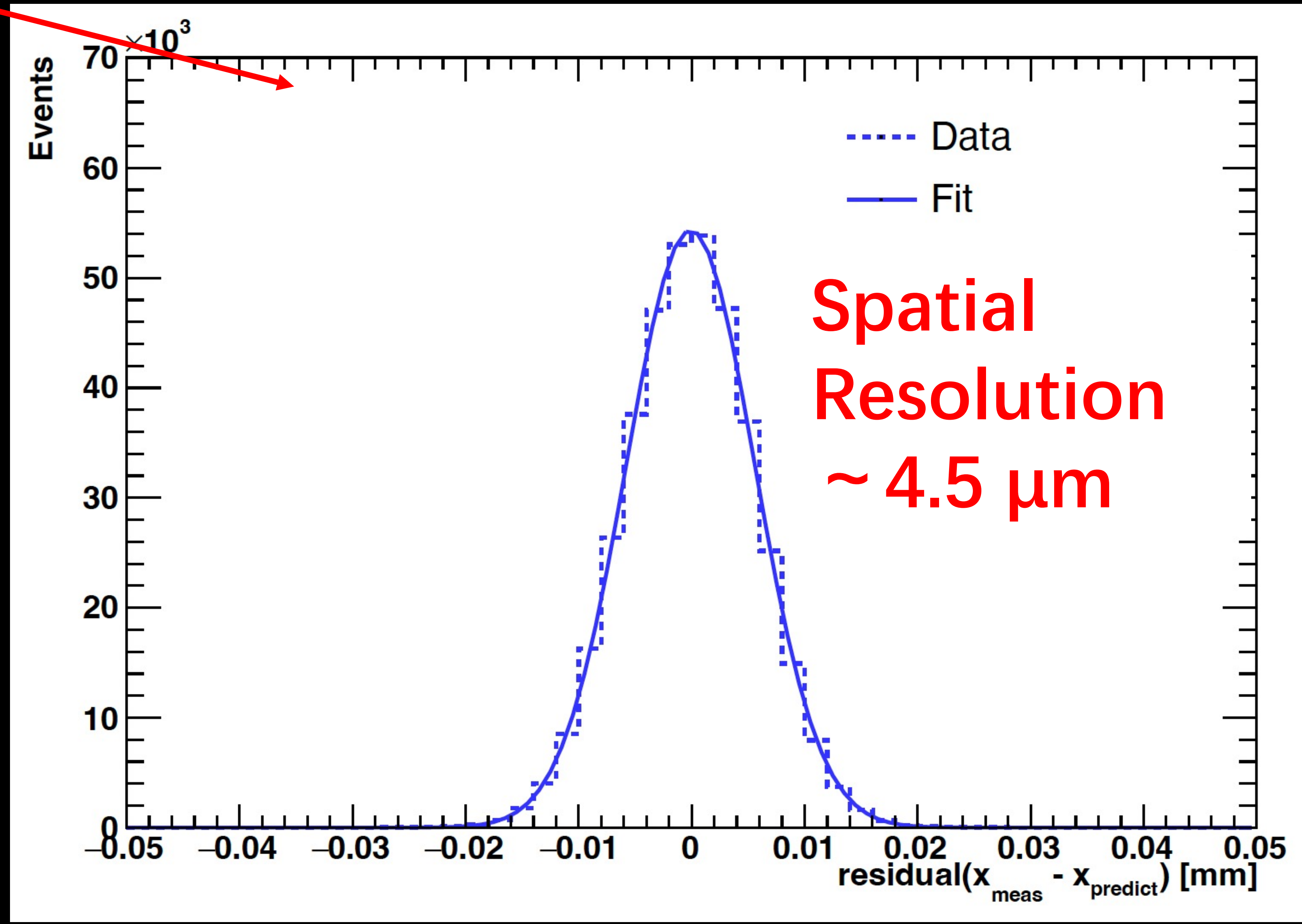




- **Less charge sharing effects in modified process with full depletion**
- **If lowering the threshold, cluster size will be dominated by noise**





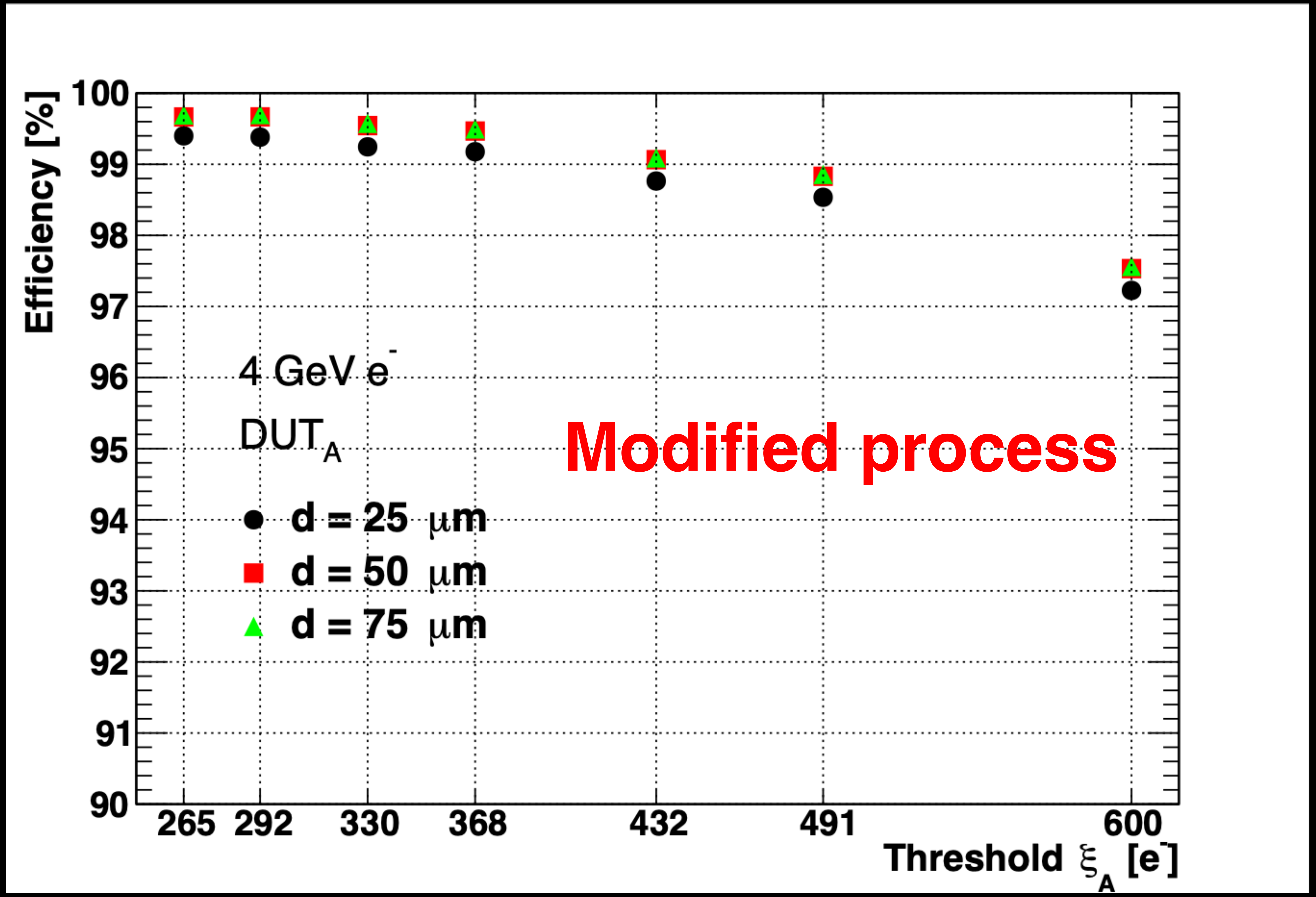


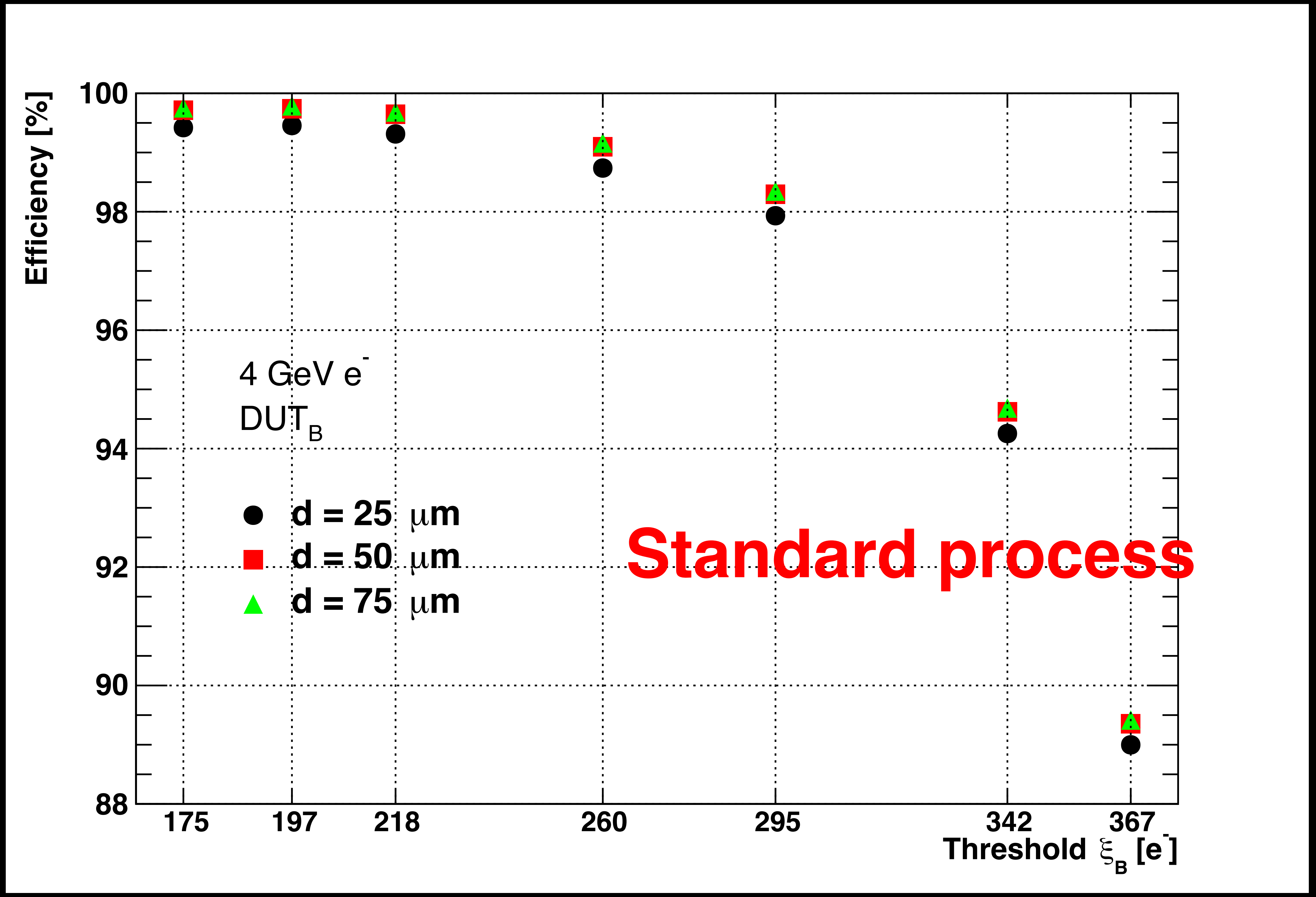
Efficiency Vs threshold

Shuqi Li

- Efficiency is the ratio of tracks that match the hit on the DUT within a distance around the predicted hit from the telescope to all tracks of the telescope
  - It can reach about 99.4% efficiency in optimized threshold

$$\epsilon = \frac{N^{matched\ Tracks}_{|x_{meas}, y_{meas} - x_{pre}, y_{pre}| < d}}{N^{Tracks}_{tel}}$$



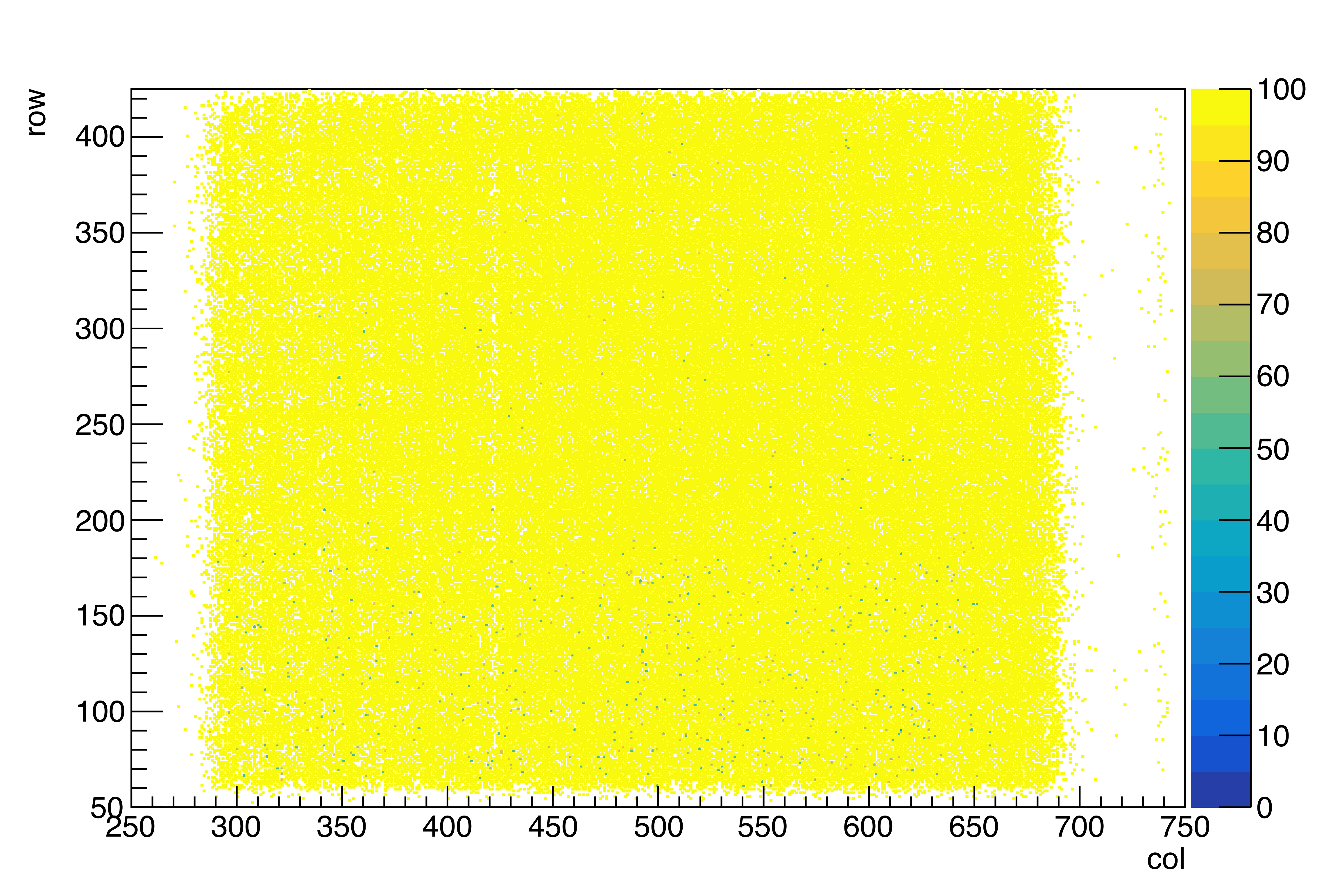


Efficiency maps

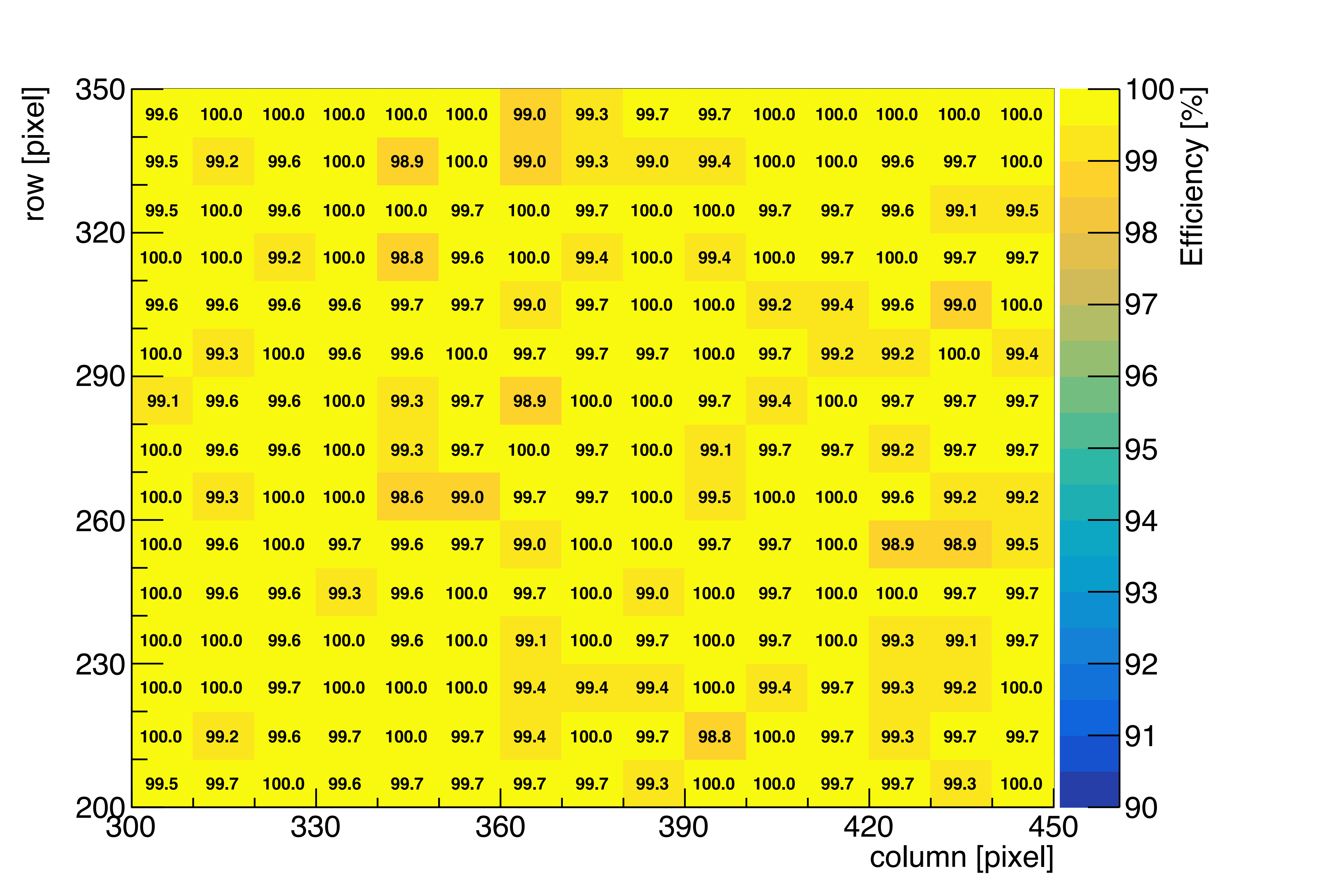
- Efficiency is the ratio of tracks that match the hit on the DUT within a distance around the predicted hit from the telescope to all tracks of the telescope
  - It can reach about 99.4% efficiency in optimized threshold
  - Reasonable uniformity in single pixel and in pixel matrix

Shuqi Li

Single pixel Efficiency: 99.4%



10*10 pixel Efficiency

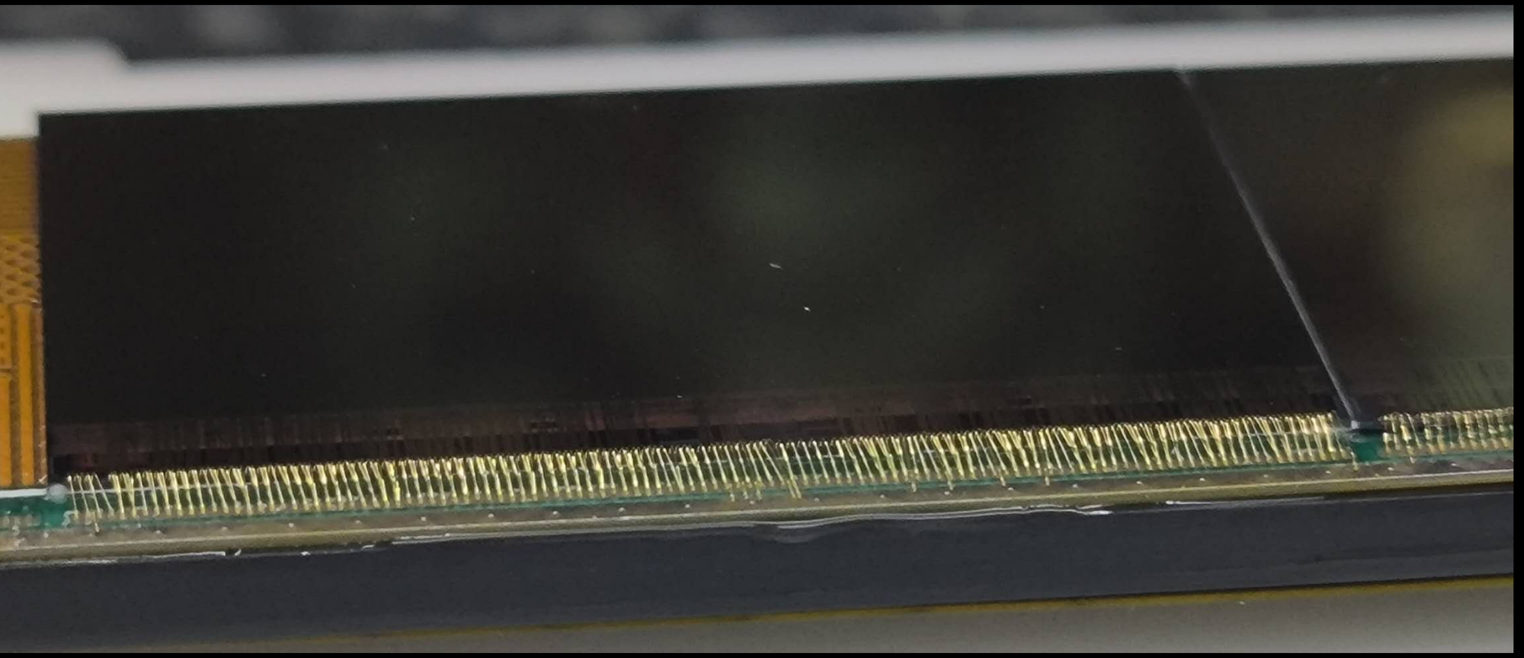


Detector module (ladder) R & D

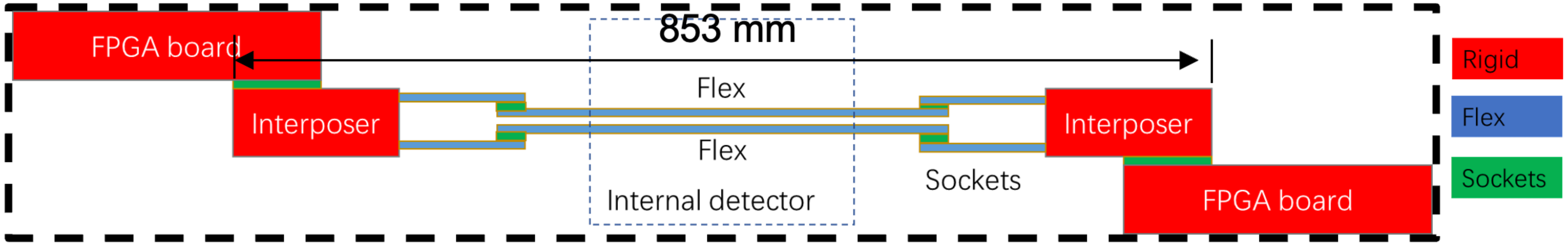
- Completed detector module (ladder) design
  - Detector module (ladder) = 10 sensors + readout board + support structure + control board
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- Challenges
  - Long flex cable→ hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals

Ying Zhang,
Ziyue Yan
Jun Hu
Xiaoxu Zhang
Tianya Wu
Wei Wang

Taichupix chip wire bonded on FlexPCB



Ladder readout system



- Solutions
  - Readout from both ends, readout compose of three parts, careful design on power placement

Laser test result of ladder

- A full ladder includes two identical fundamental readout units
  - Each contains 5 TaichuPix chips, a interposer board, a FPGA readout board
- Functionality of a full ladder fundamental readout unit was verified
  - Scanning a laser spot on the different chips with a step of 50 μm,

→Clear and correct letter imaging observed

→Demonstrating 5 chips working together → one ladder readout unit working

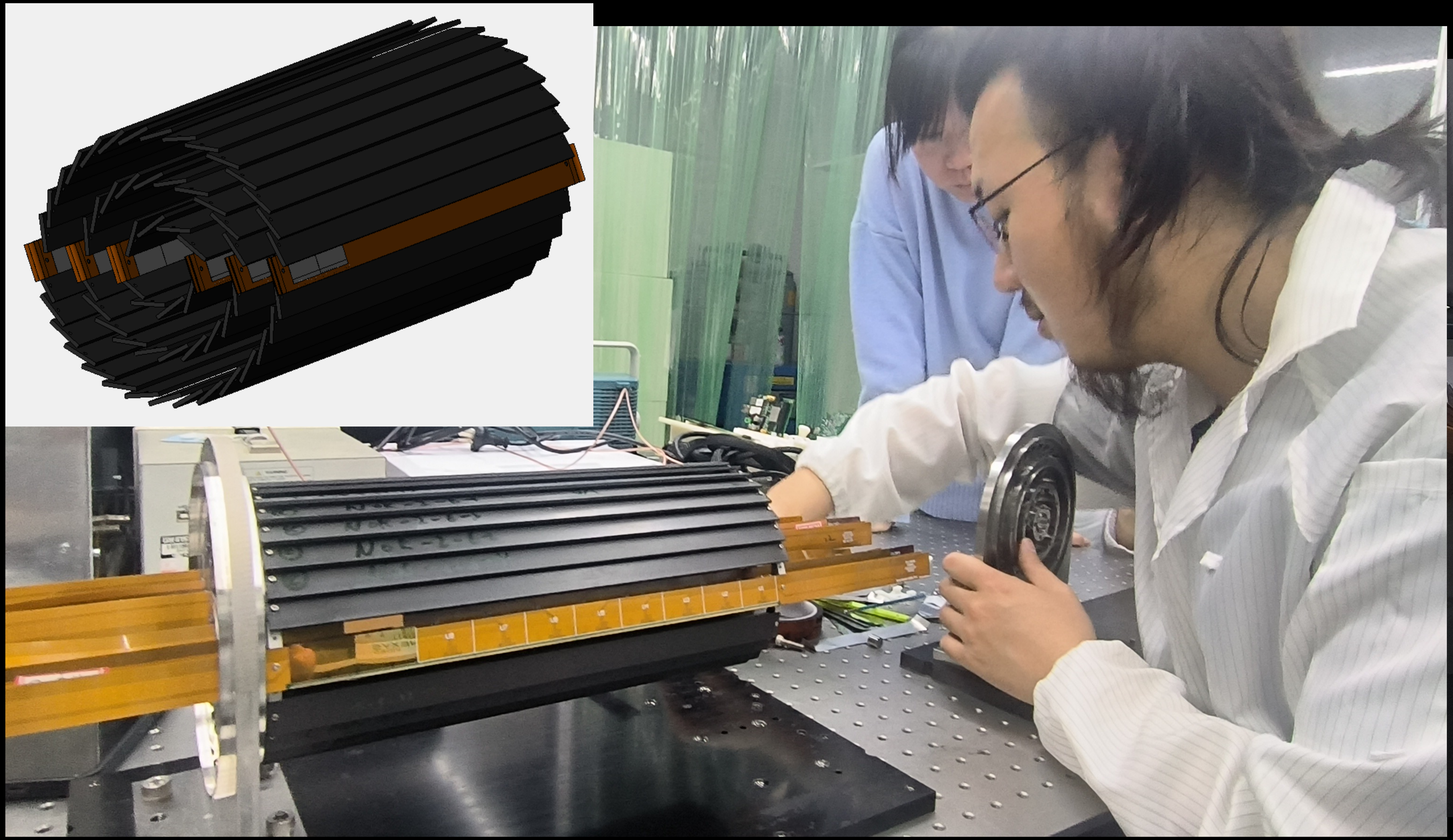
Tianya Wu
Wei Wang
Ying Zhang,
Ziyue Yan
Jun Hu
Xiaoxu Zhang

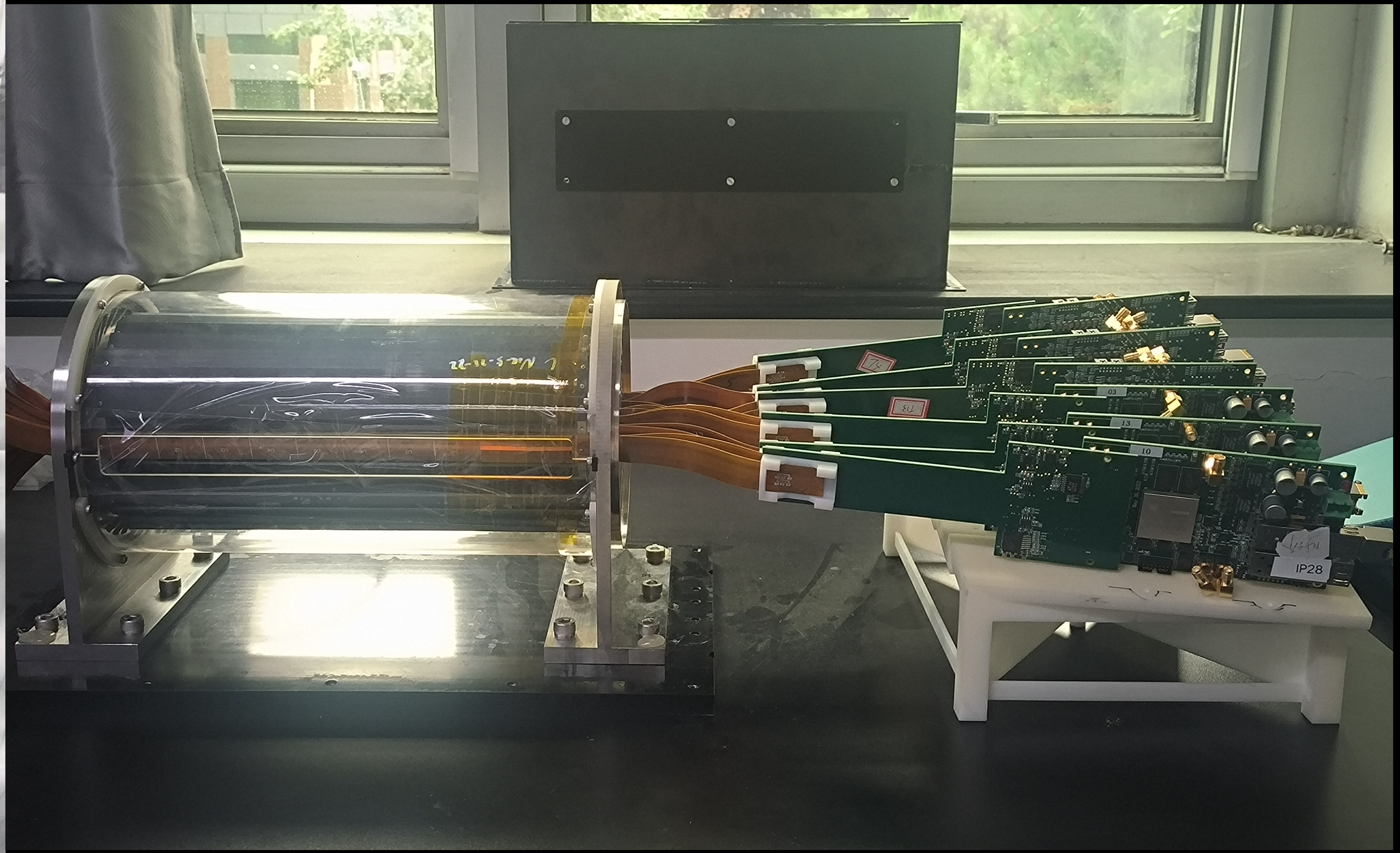
Laser tests on Taichupix chip on full ladder
（"CEPCV" pattern by scanning laser on different chips on ladder ）

Vertex detector Prototype assembly

Jinyu Fu
Tianya Wu
Xinhui Huang
Wei Wang

- Six double-side ladders installed on the vertex detector prototype
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype



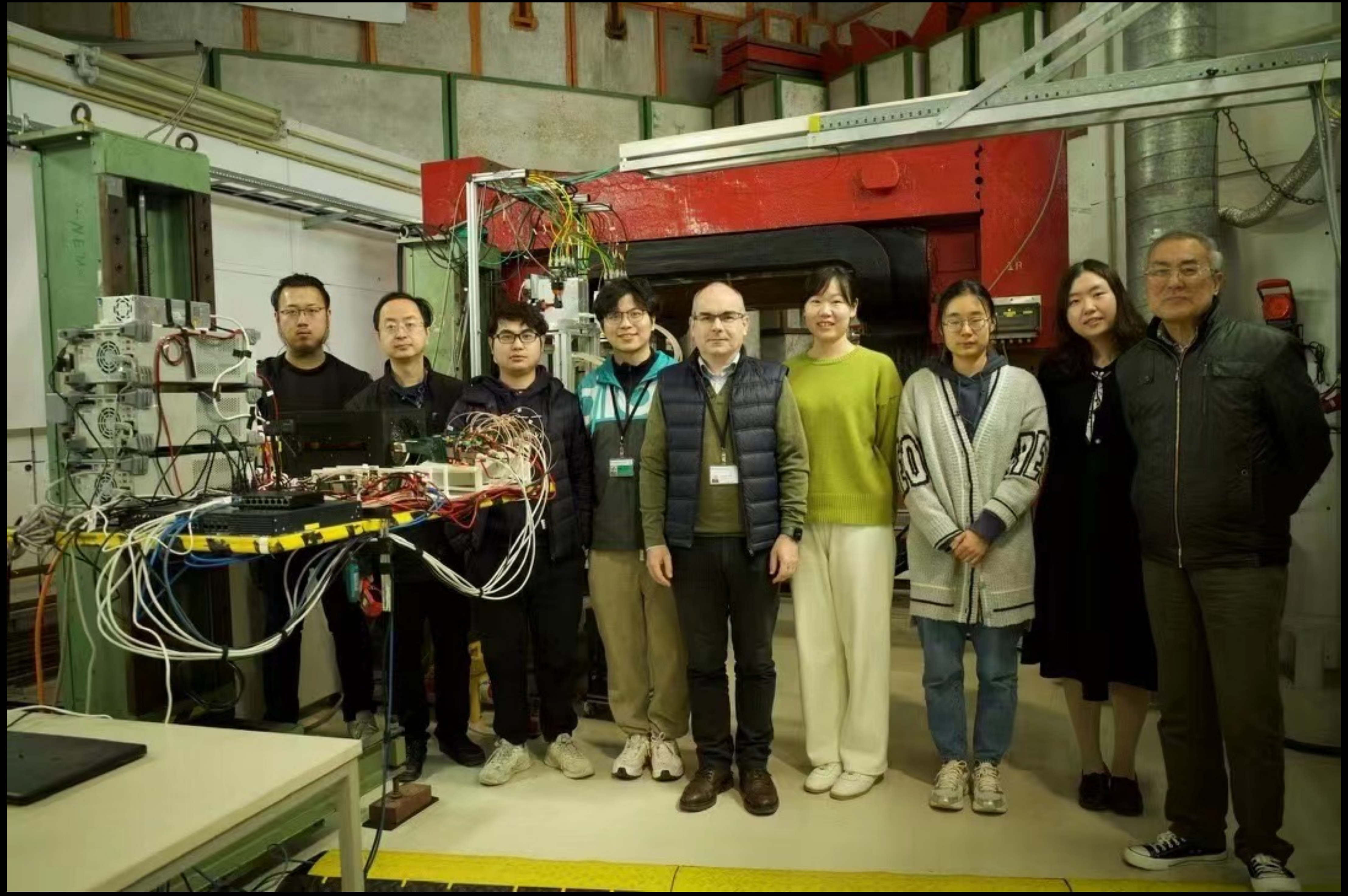


Test beam @ DESY

- 2nd testbeam: April 11-23 2023 DESY test beam in Germany (4-6GeV electron)
  - Vertex detector prototype testbeam
- 1st testbeam: Dec 12-22 2022 DESY test beam in Germany (4-6GeV electron)
  - TaichuPix Beam Telescope testbeam

2022 DESY test beam

2023 DESY test beam

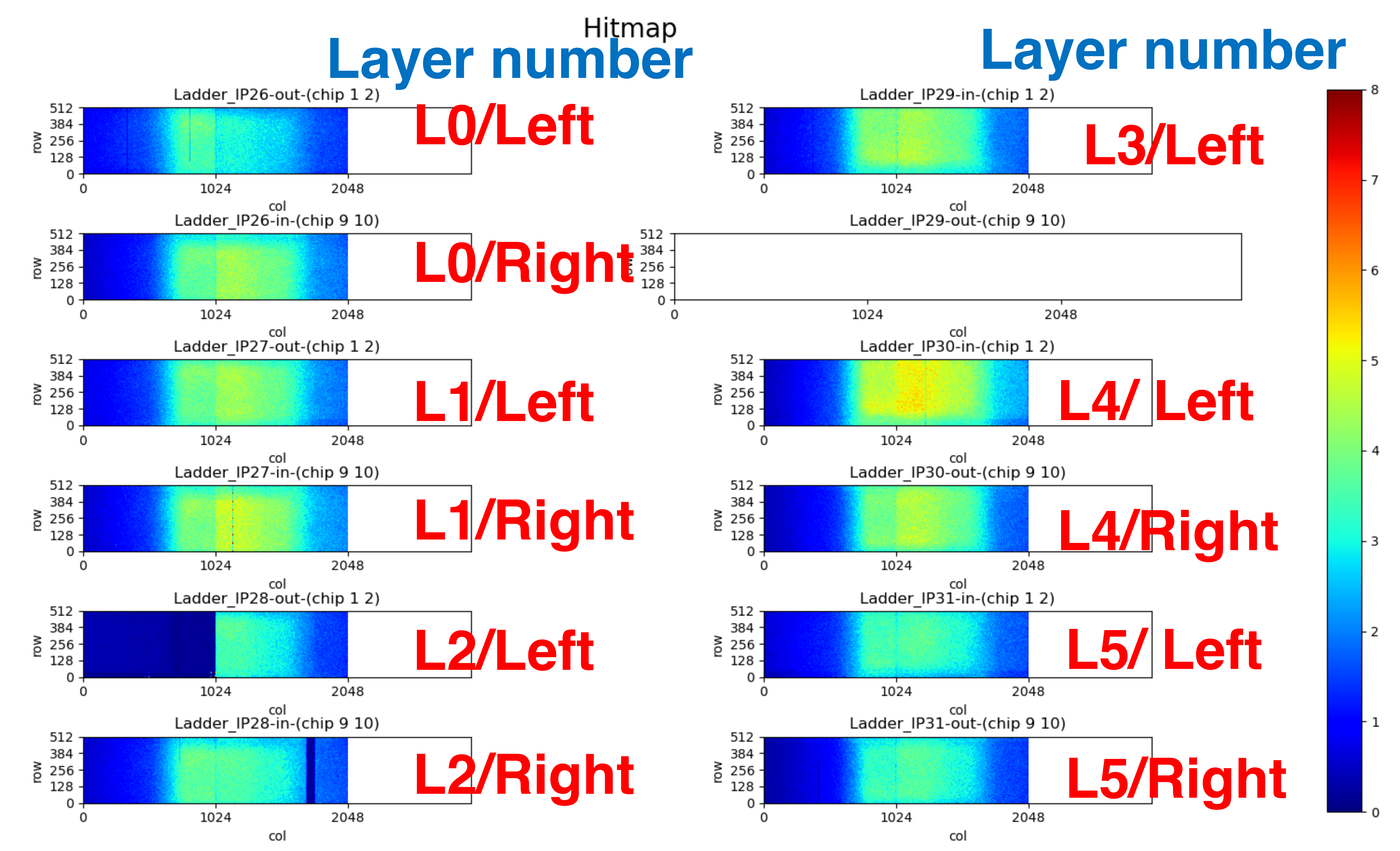


Test beam @ DESY for detector prototype

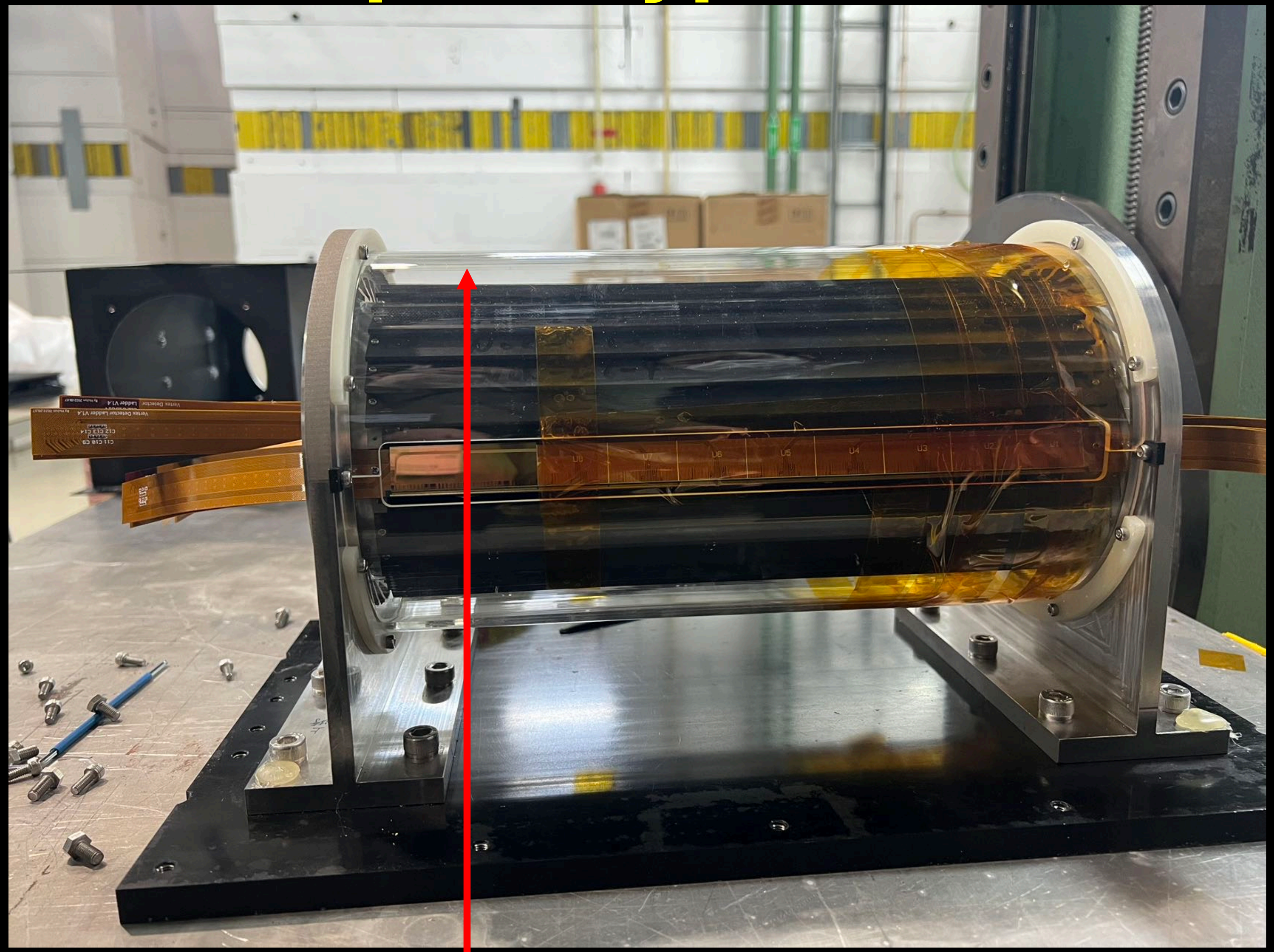
Jia Zhou
Hongyu Zhang

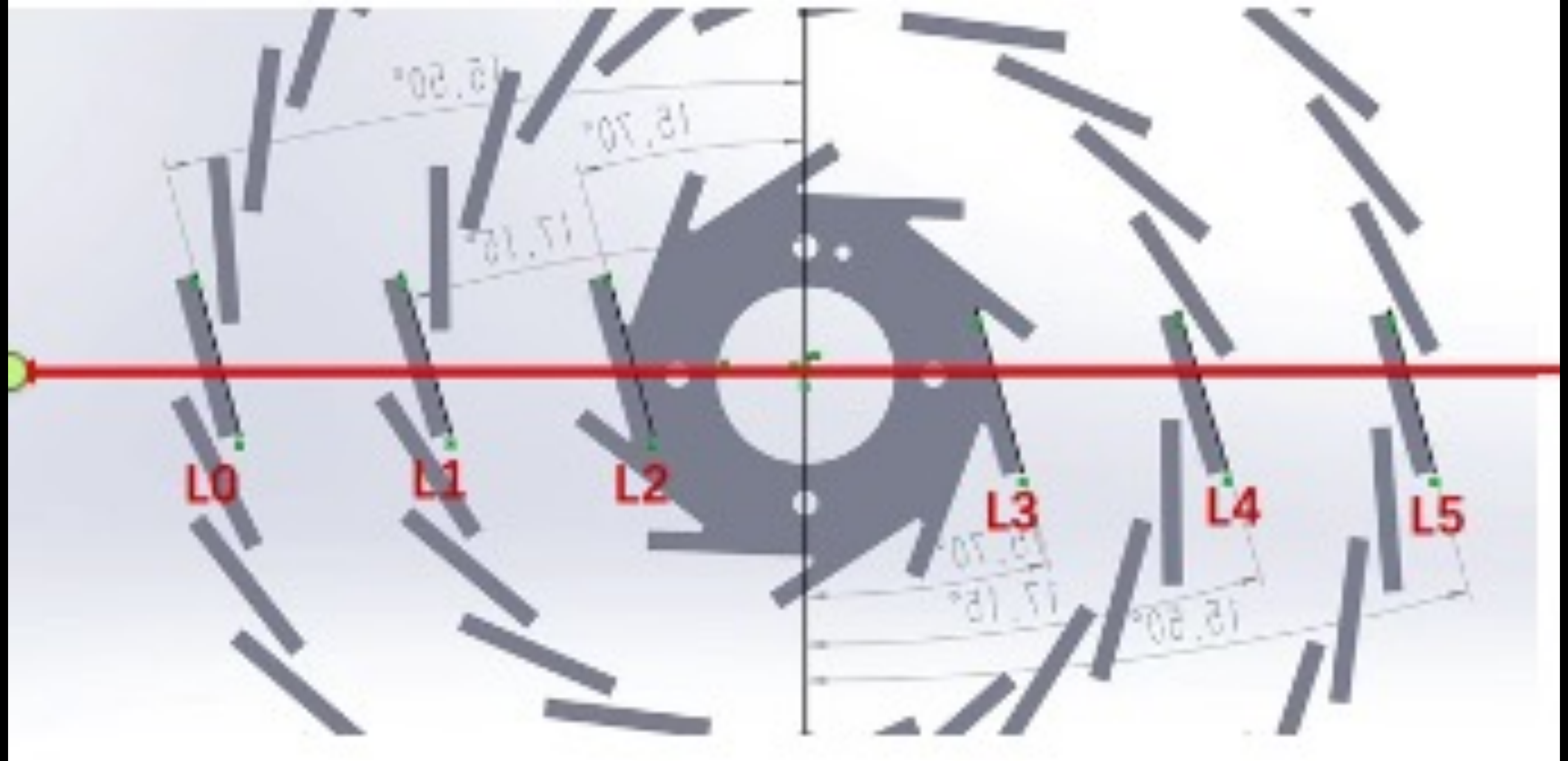
- Six double-side ladders installed on the vertex detector prototype for DESY testbeam
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype
  - Beam spot (~2×2cm) is visible on detector hit map
  - Record about one billion tracks in two weeks

Hit maps of all layers taichupix on prototype



Detector prototype in testbeam

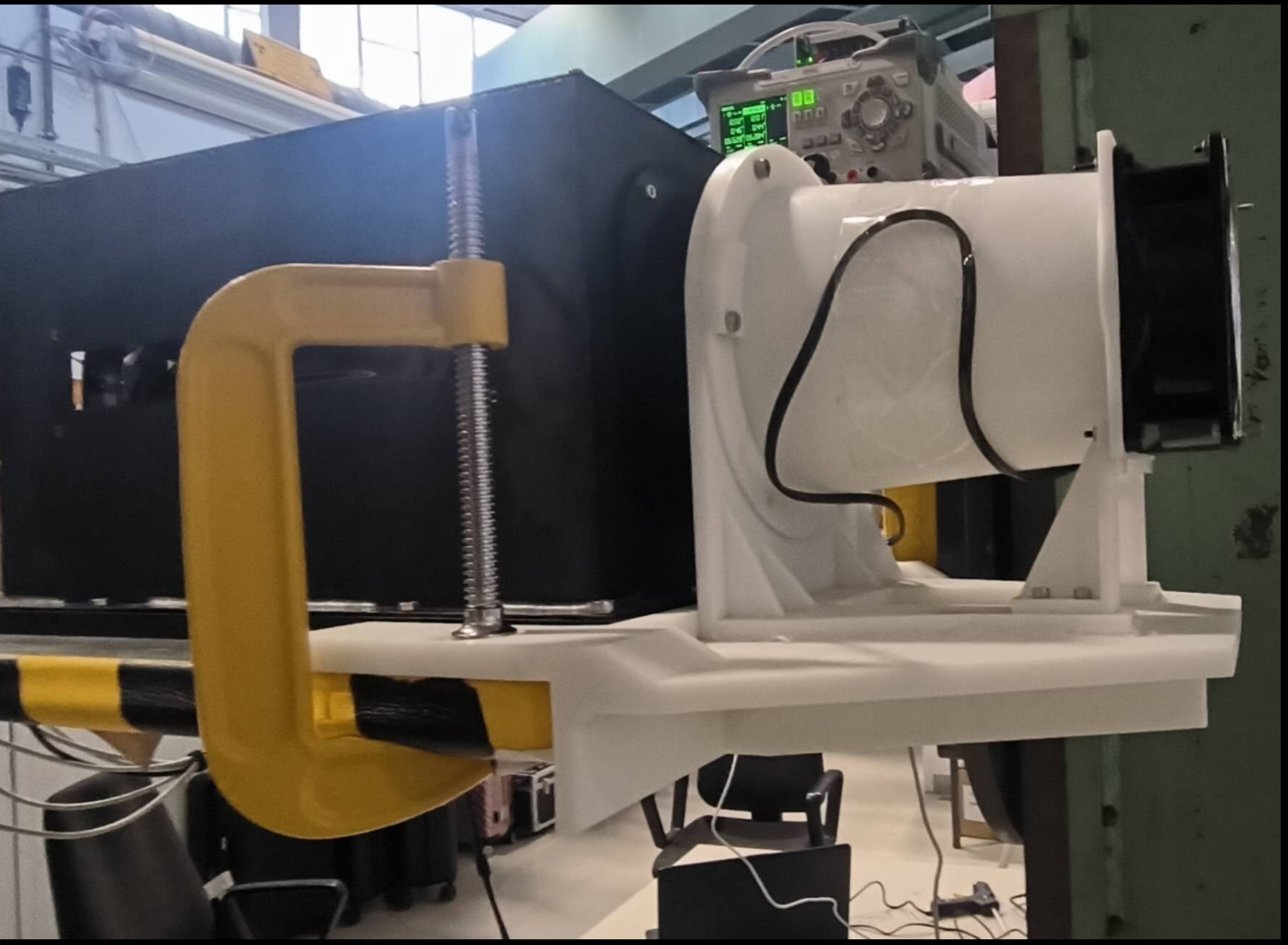




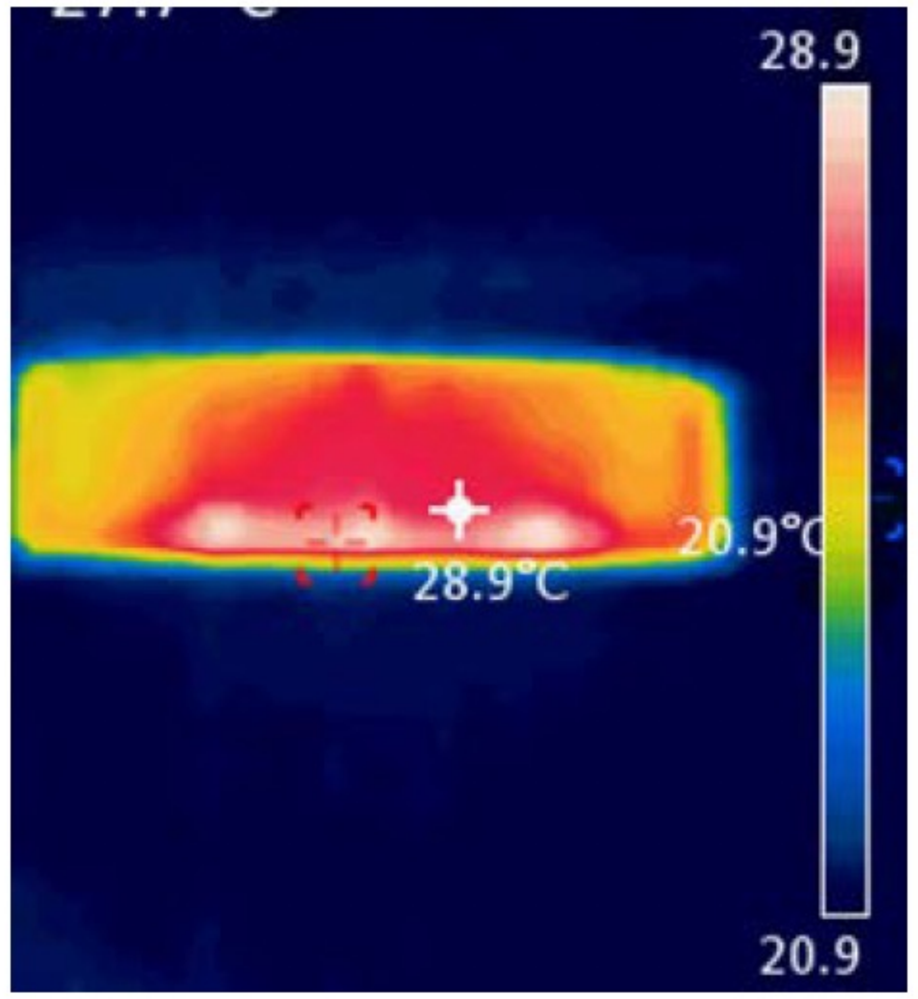
Air Cooling for vertex prototype

Jinyu Fu
Xinhui Huang

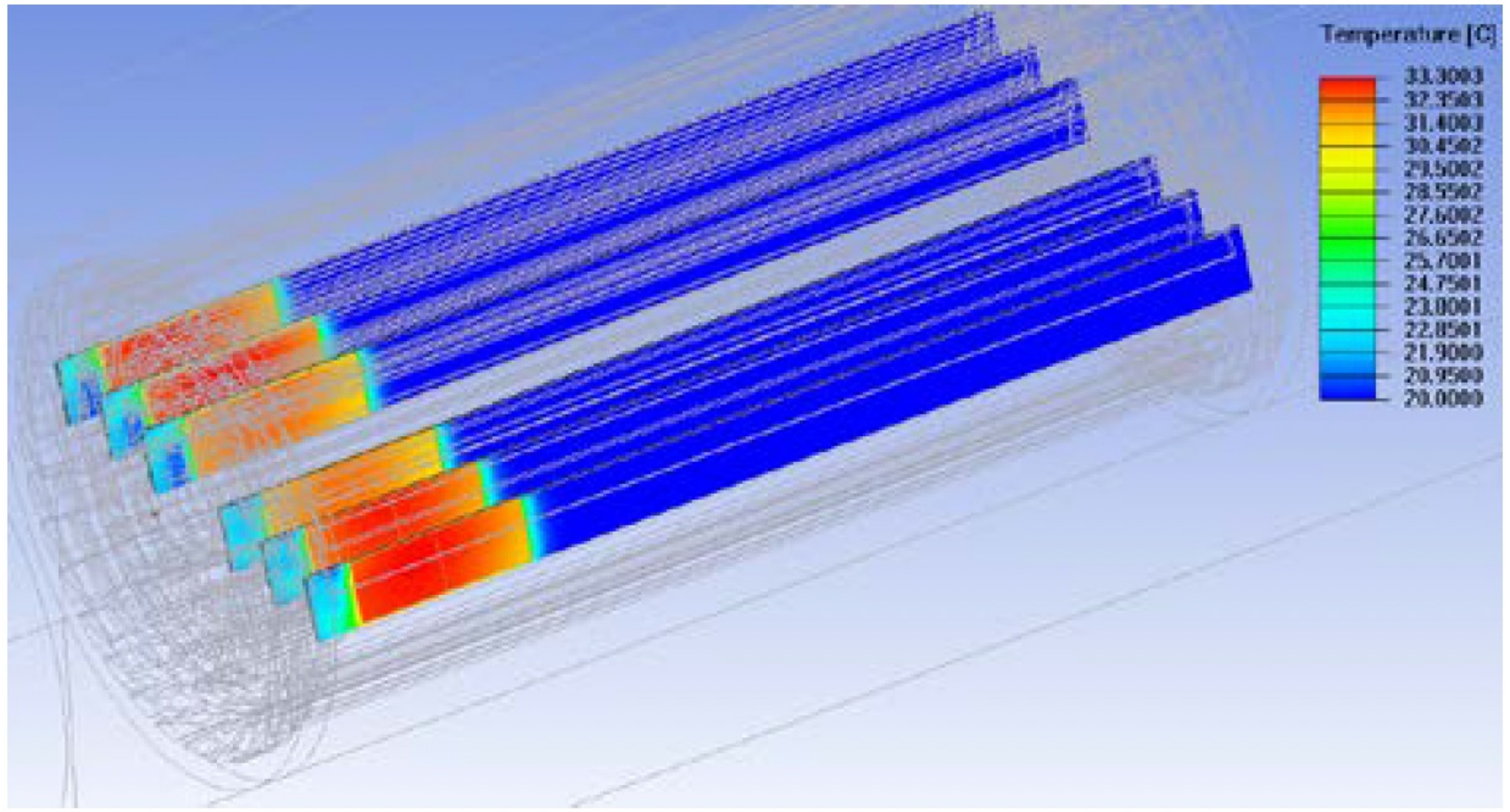
- Feedback on Edinburgh Workshop is mainly on vertex detector cooling and intergration
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm2 (17.5 MHz clock in testbeam)
  - Before turning on the fan, chip temperature can go above 41 °C.
  - With air cooling, chip temperature can reduced to 25 °C (in average)
    - In good agreement to our cooling simulation
  - No visible vibration effect observed in position resolution offline analysis when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃

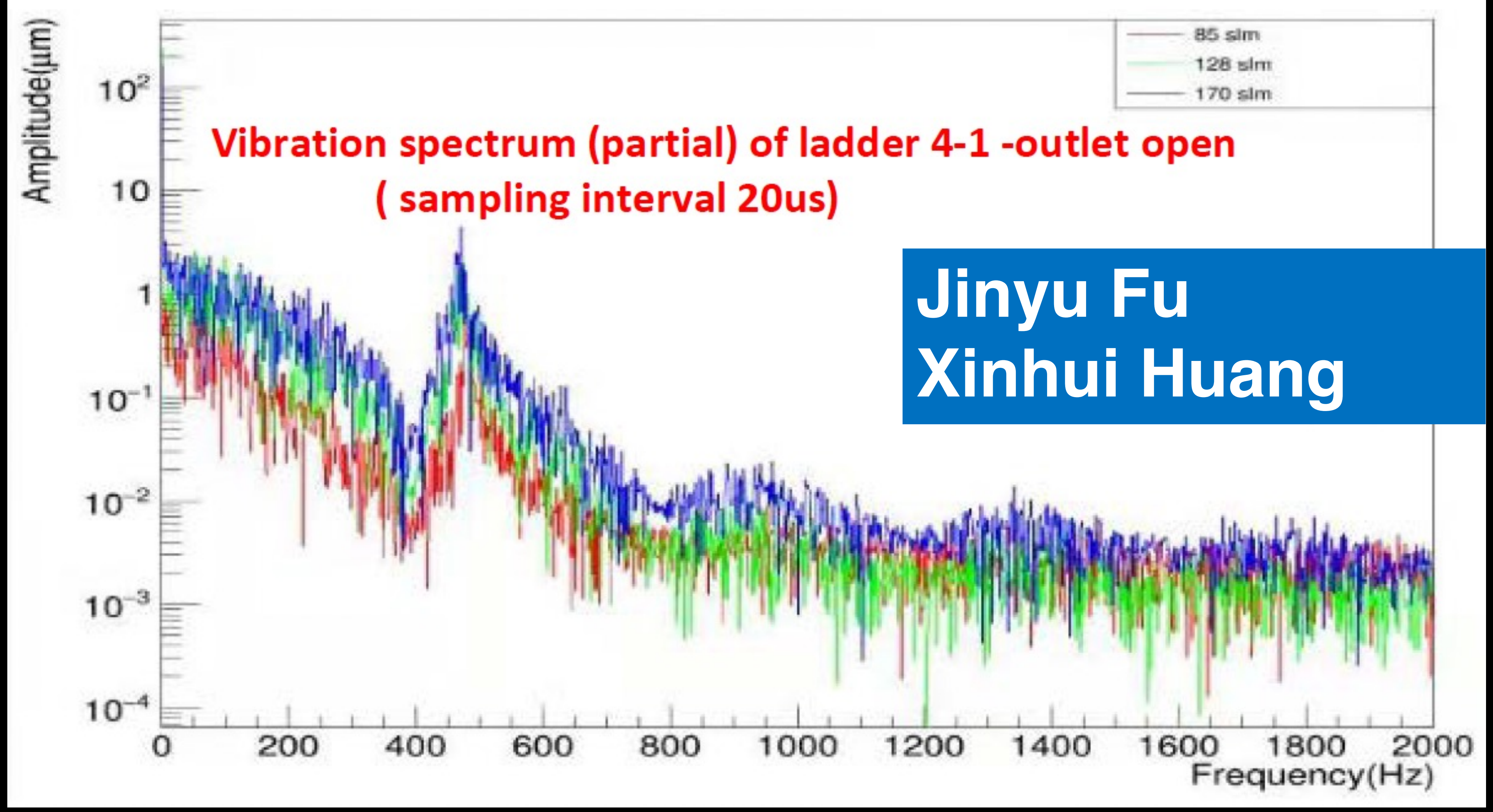


Prototype cooling simulation： Max 33.3 ℃

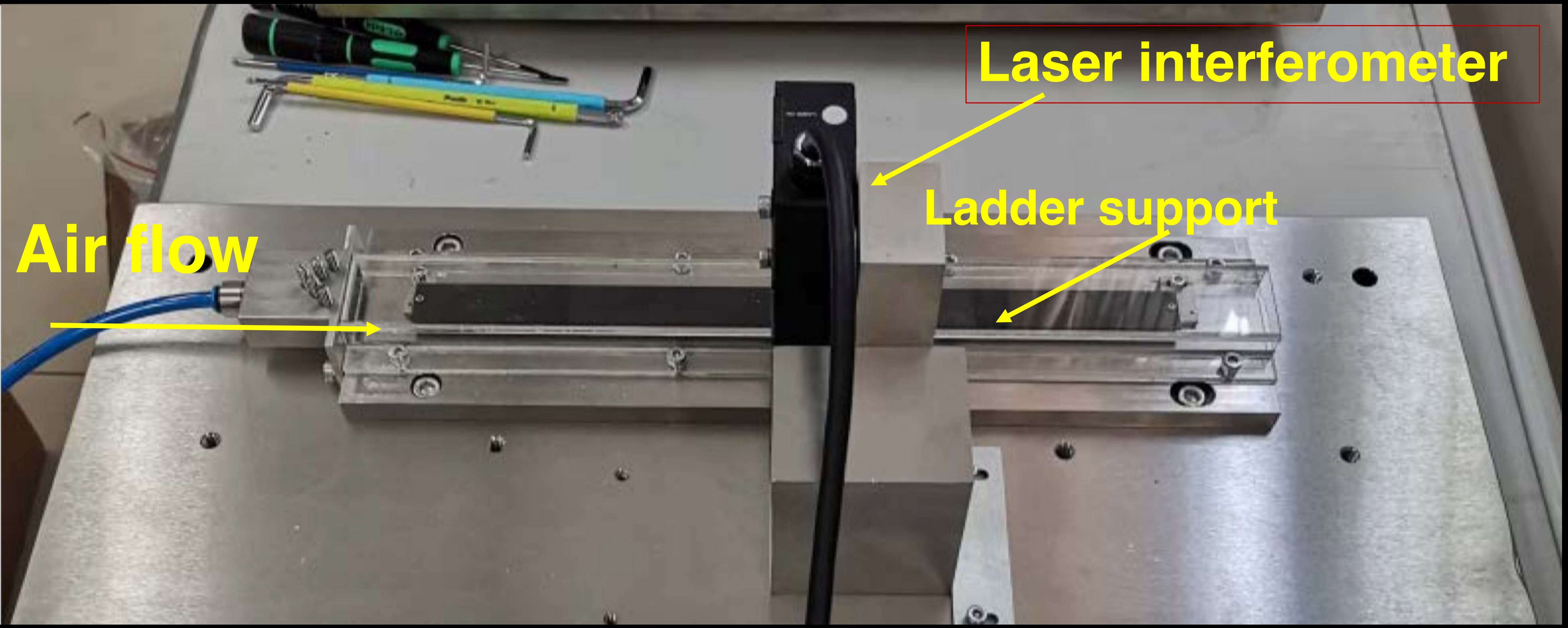


Air Cooling test on ladder

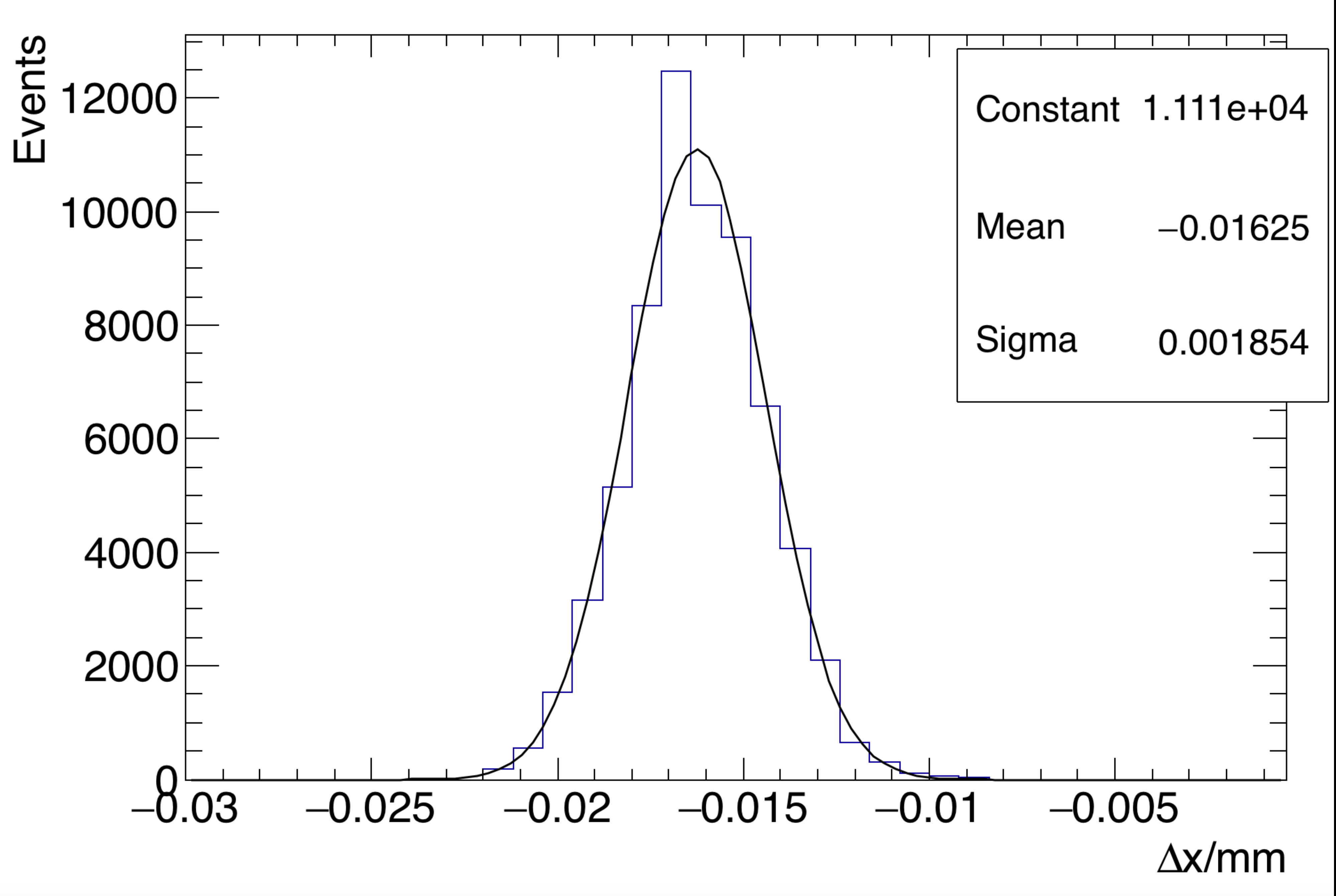
- Test bench setup for ladder air-cooling
- Vibration follows Gaussian distribution
  - Core of Gaussian is still under control 1~2μm



Test setup prototype for ladder cooling
Use compressed air for cooling

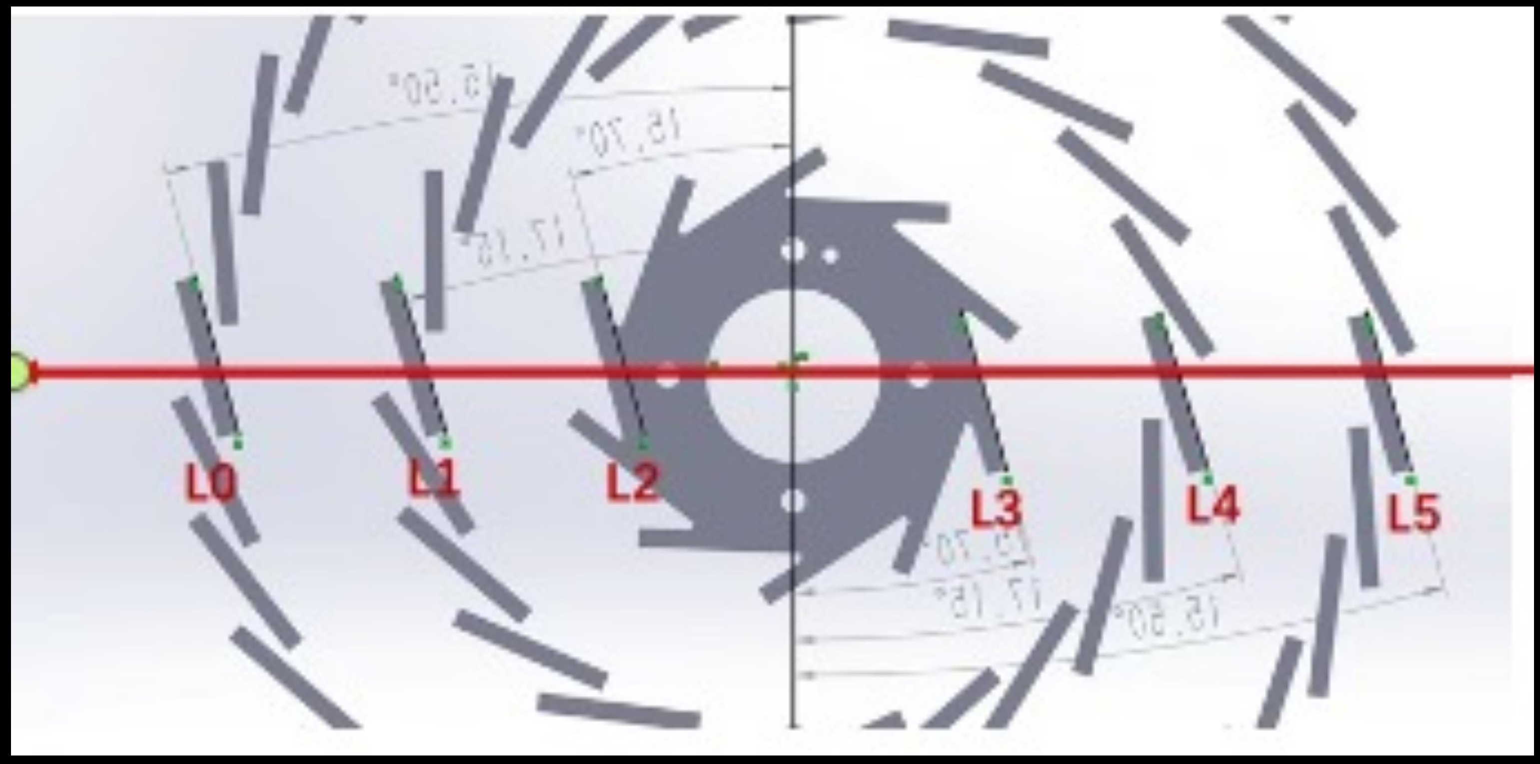


Typical Vibration displacement during air cooling



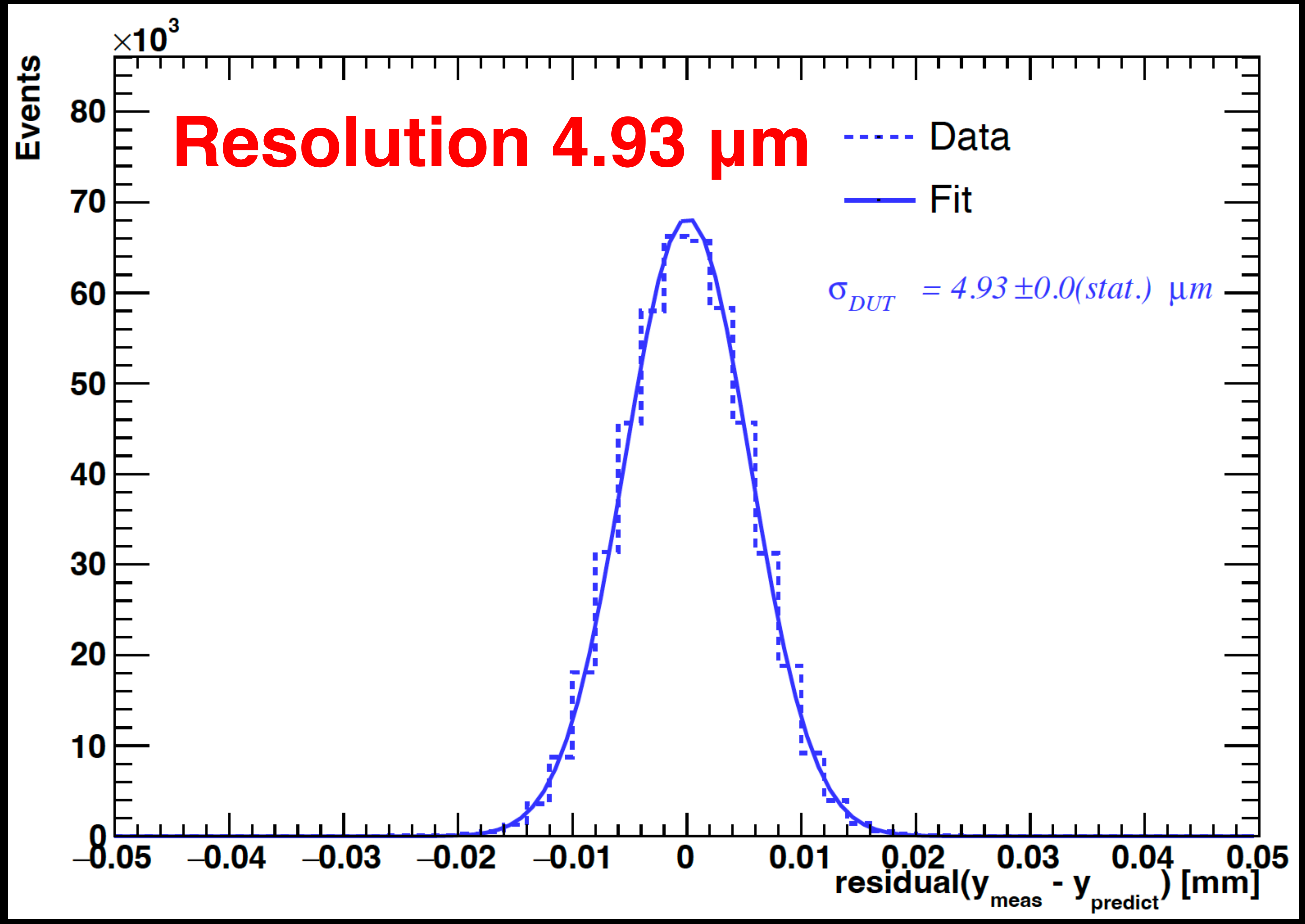
Test beam results (April 2023)

- Extract Spatial resolution from detector prototype testbeam data
  - One layer (L1) of TaichuPix used as Detector-Under-Test (DUT)
  - Other layers of vertex detector prototype used for track fitting
  - Spatial resolution reached 4.9μm (Y axis→ bending direction)
    - Spatial Resolution met the requirement (3-5μm)

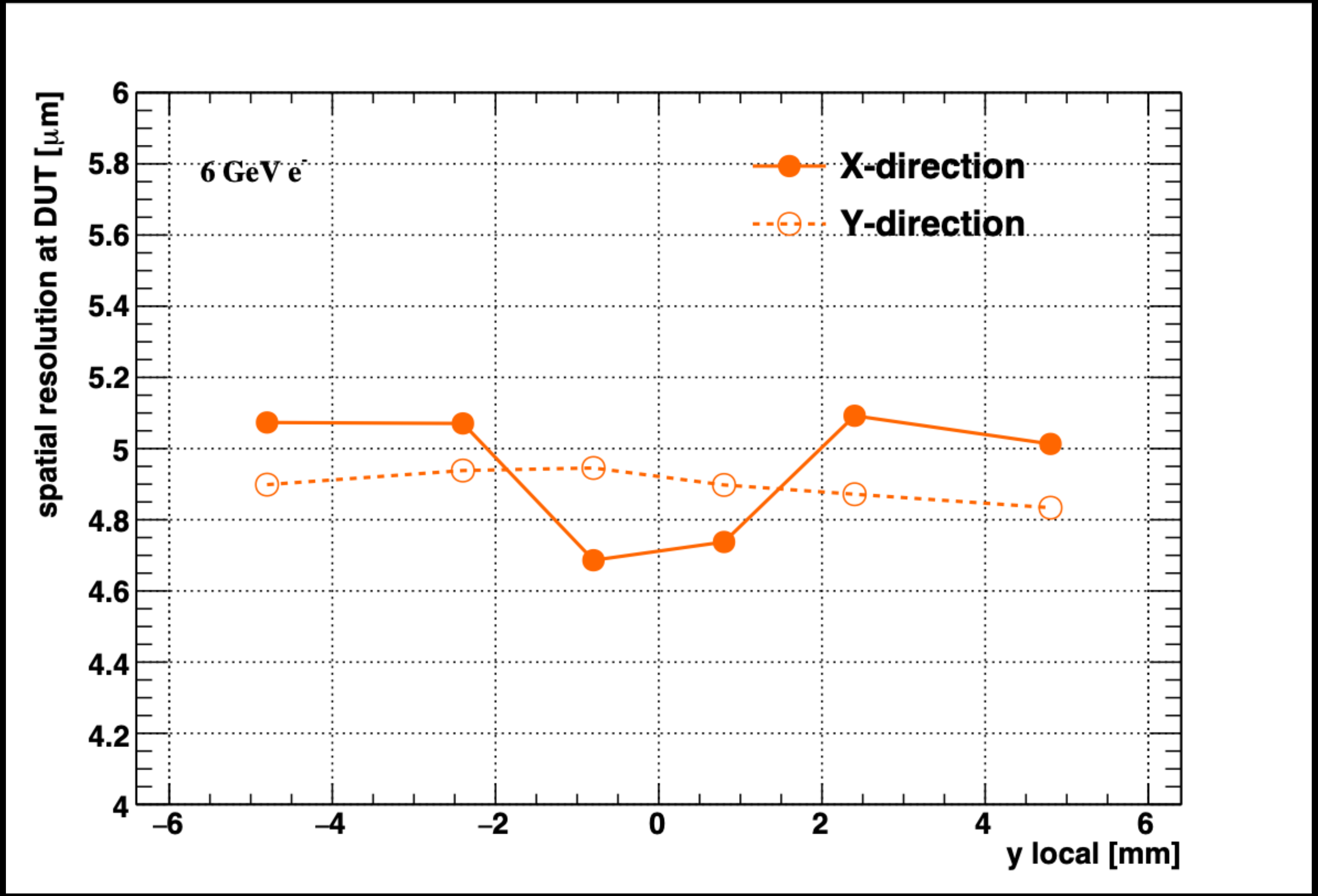


Shuqi Li

Residual distribution in Y axis
DUT measured position – expected position from track



Spatial resolution vs hit positions
Y axis is bending direction

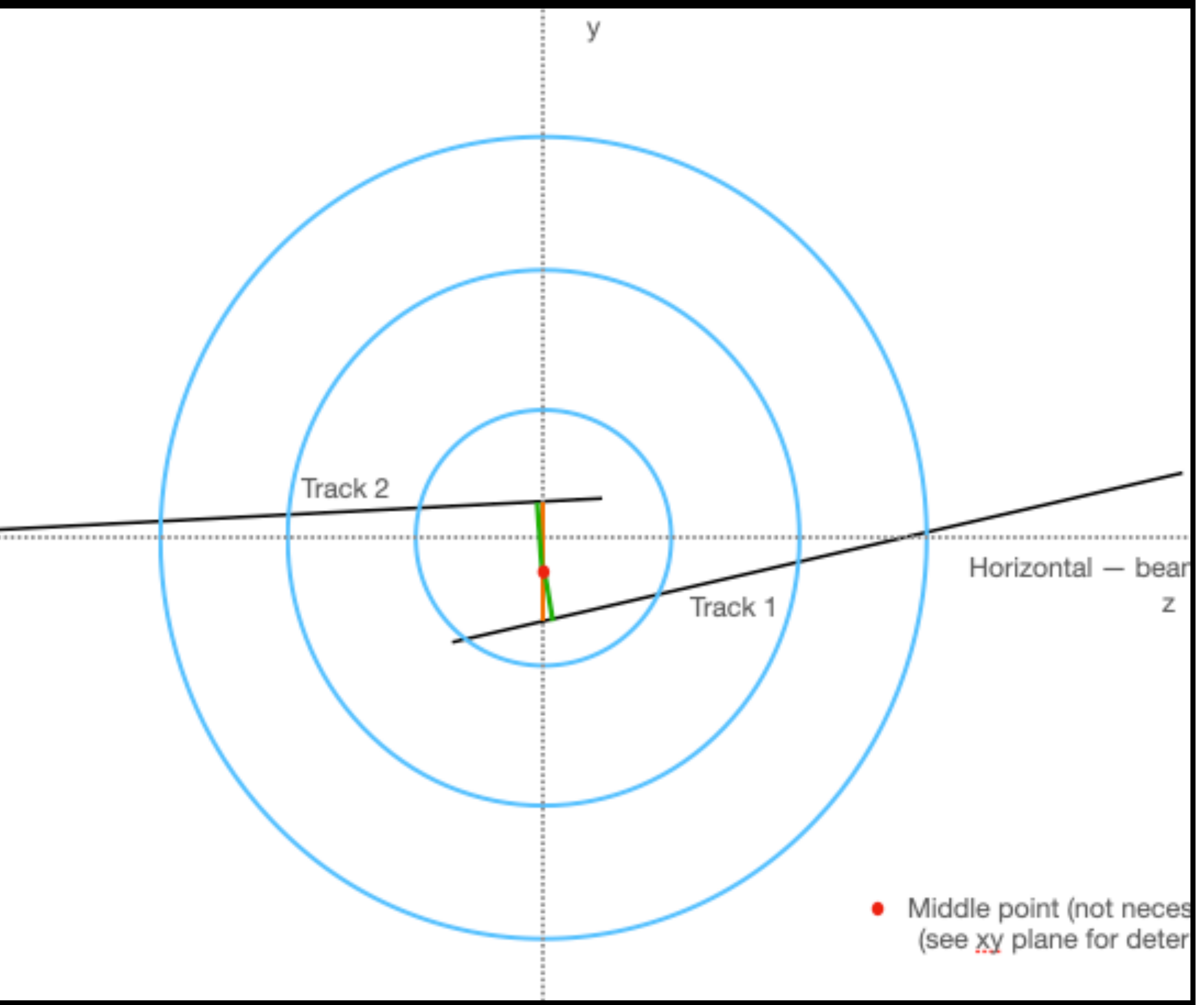


Preliminary result of impact parameter resolution

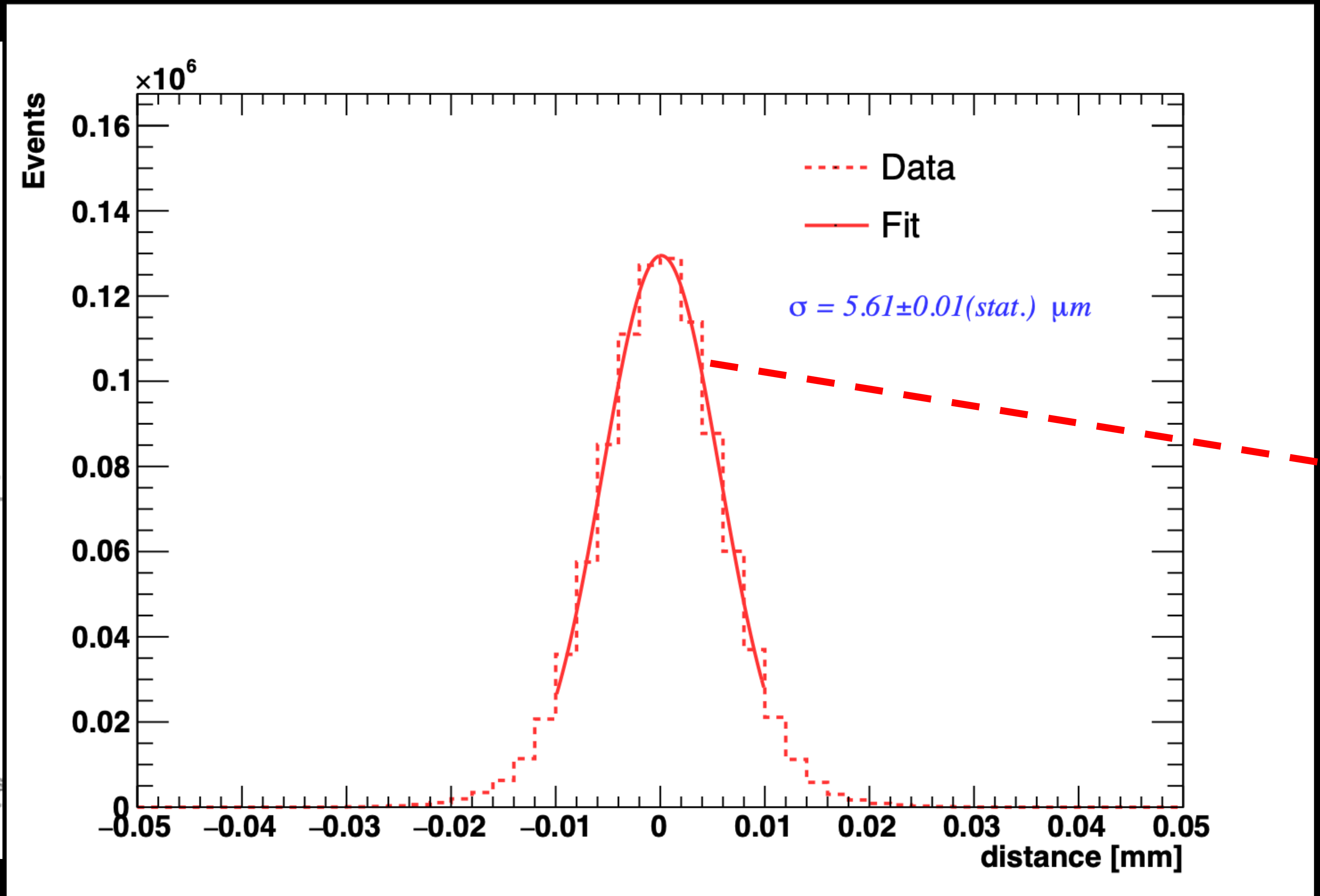
Shuqi Li, Joao

- No real interaction point or real primary vertex (PV) in testbeam setup
  - Define PV as the center of the point in xy plane extrapolated from the up/downstream
  - Calculate the impact parameter between primary vertex and upstream/downstream tracks
  - CEPC impact parameter requirement: 5~6um for 4-6 GeV track
  - Preliminary result met the CEPC requirement

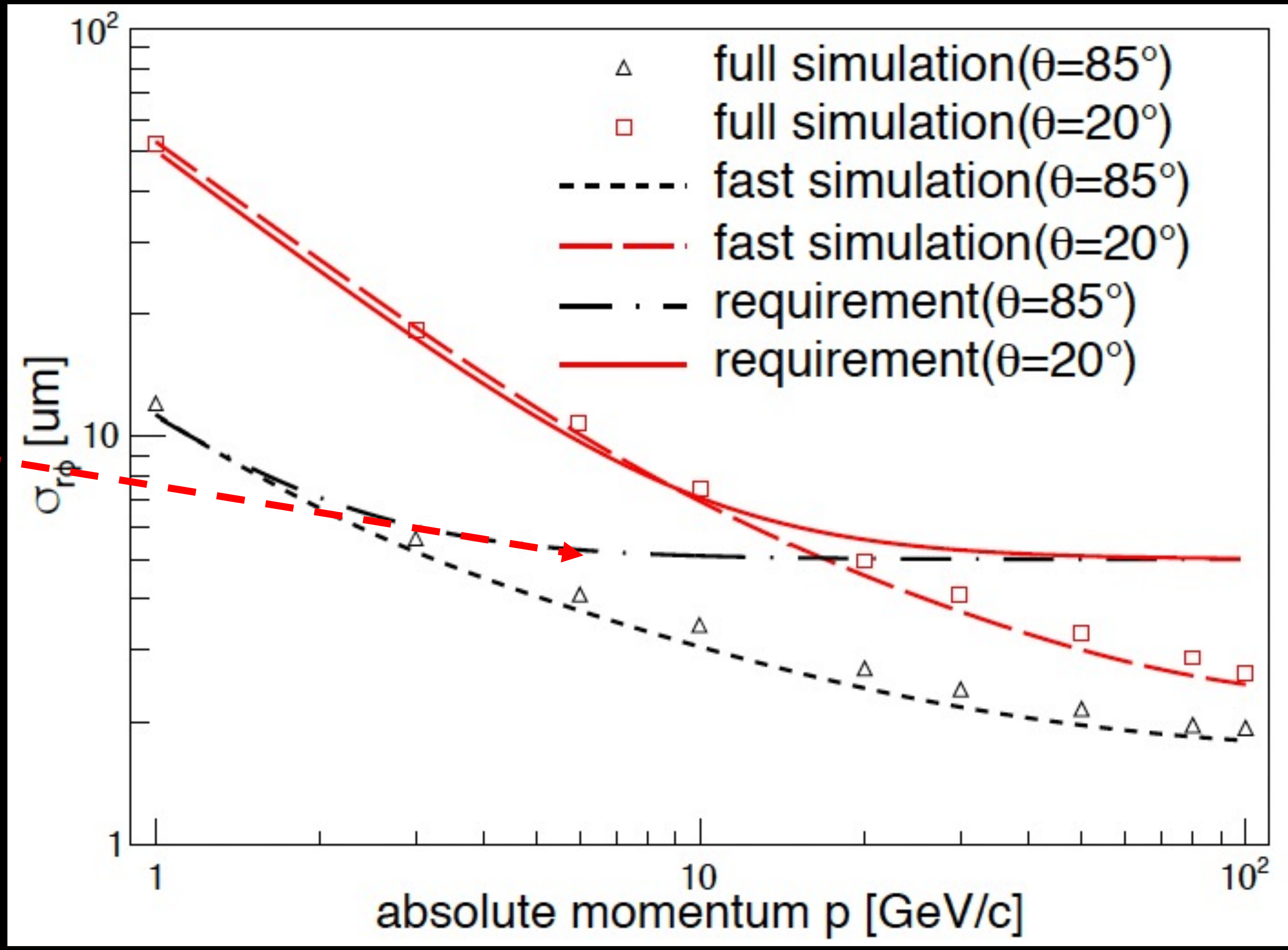
Impact parameter Defined by two tracklets



Impact parameter resolution



Impact parameter resolution In CDR



Latest Publications and conference talk

- Paper:
  - Taichu2 Laser test (NIMA): Submitted, 2nd revision
  - DESY Test beam 1st paper: submission date (NIMA): Submitted, 1st revision
  - Paper about vertex prototype testbeam : Preparing
  - Electronics for ladder and prototype (JINST): Accepted
  - Paper about the prototype assembly and cooling : Preparing
  - Paper of TaichuPix3 : Preparing
- International Conference:
  - BTTB 2023: One Talk (Shuqi Li)
  - FEE 2023 (front-end electronics): one Talk (Ying Zhang)
  - Lepton Photon 2023: One Poster accepted (Shuqi Li)
  - EPS-HEP: One Talk accepted (Xinhui Huang)
  - PSD 2023: Submitted abstract for talk (Tianya Wu)
  - TIPP 2023: One talk and one poster accepted (Ying Zhang, Tianya Wu)
  - TWEPP 23: One Talk accepted (Ying Zhang)
  - HSTD 2023: Submitted abstract for talk

MOST2 project Final assessment Meeting (项目结题自评价会议)

- CEPC Vertex detector R & D Reach world-class level
- Suggest to strength the testbeam analysis, and provide feedback to detector optimization
  - Will work with Offline team to implement this analysis in software framewrok (WeiDong and others)
- Suggest to continue this R & D, to boost domestic advanced silicon detector development
  - Continue R & D by in MOST3 project

Task2 课题二：硅径迹探测器关键技术验证

2018YFA0404302... | Group review com... | paperlist-silicon.do... | Task2 self-assess...

1:20 PM Lab visit 参观样机和实验室

2:00 PM Overview 课题二整体汇报 （20'+5'）
Speaker: 梁志均 LIANG Zhijun
20230619MOST2-s...

2:25 PM Sensor chip design and testing 传感器芯片设计与测试（20'+5'）
Speaker: Ying ZHANG (IHEP)
Chip design_0619_...

2:50 PM Structure and assembly of detector prototype 探测器样机的结构与组装（20'+5'）
Speaker: Jinyu Fu (高能所)
Mechnical VTXD m...

3:15 PM Coffee break

3:35 PM Analysis of beam test result 束流测试 (20'+5')
Speaker: Shuqi Li
review_testbeam.pdf

4:00 PM Discussion (Project group only)
Main building A511

4:00 PM Discussion (Refrees only) 评委内部讨论与撰写评审意见

Review Expert assessments

该课题针对环形正负电子对撞机实验探测器的关键技术与挑战，按照课题任务书计划，在高分辨硅像素芯片、内层硅径迹探测器原型机开展了一系列研究，研制出全尺寸的单片集成型像素传感器和硅径迹探测器原型机，并利用高能电子束流测试性能，验证了技术方案，达到了预期目标，对项目的完成具有重要的支撑作用。课题组按照任务书中关于考核指标的考核方式，利用1 – 6 GeV/c的电子束流测试得到原型机的空间分辨率达到 4.9 微米（探测效率好于 99%）；在辐照测试中，课题所研制的硅像素传感器芯片可以承受超过 3Mrad 电离辐照，好于课题任务书要求的承受 1Mrad 电离辐照的考核指标。

该课题在高性能硅像素传感器芯片研究方面攻克了高空间分辨、低物质量和抗辐照等一系列关键技术难题，达到了国际先进水平，对整个项目的目标作出关键贡献，适用于未来高精度硅径迹探测器，且在医学成像等方面也有广泛的应用前景。发表文章 5 篇，申请专利 12 项（其中已授权 3 项）；国际会议学术报告 20 余次。

该课题组织管理规范，保证了课题关键技术的顺利完成。在课题执行期间，培养了博士研究生 8 名，硕士研究生 23 名，并开展了广泛的国际合作，显著提升了我国在高性能粒子探测器核心技术的创新能力和国际影响力。

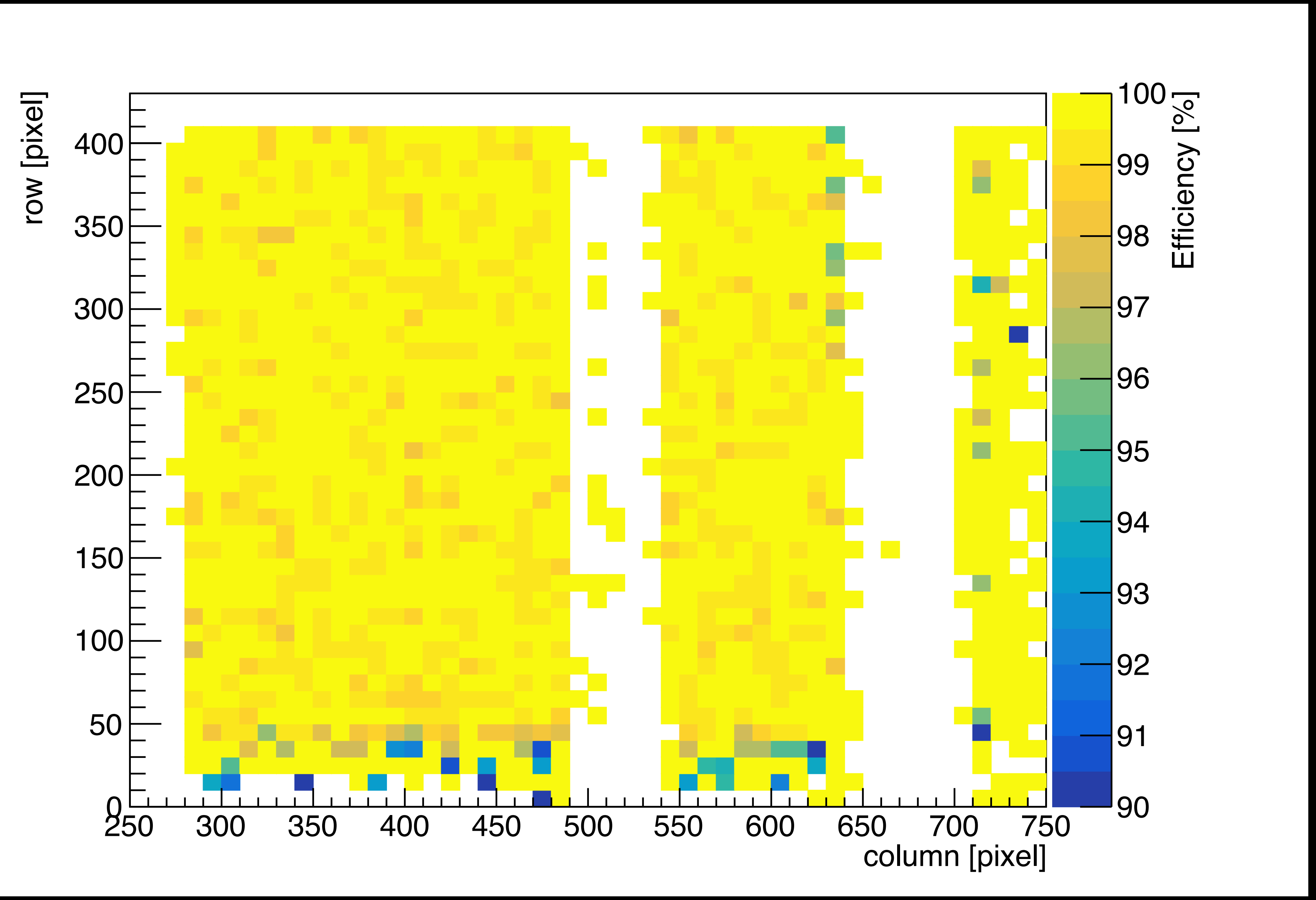
建议加强束流实验数据的分析处理，为探测器的进一步优化设计提供参考。同时，建议持续开展该技术的研发，以促进国内先进传感器芯片技术的发展。

A few known issue in Taichu development

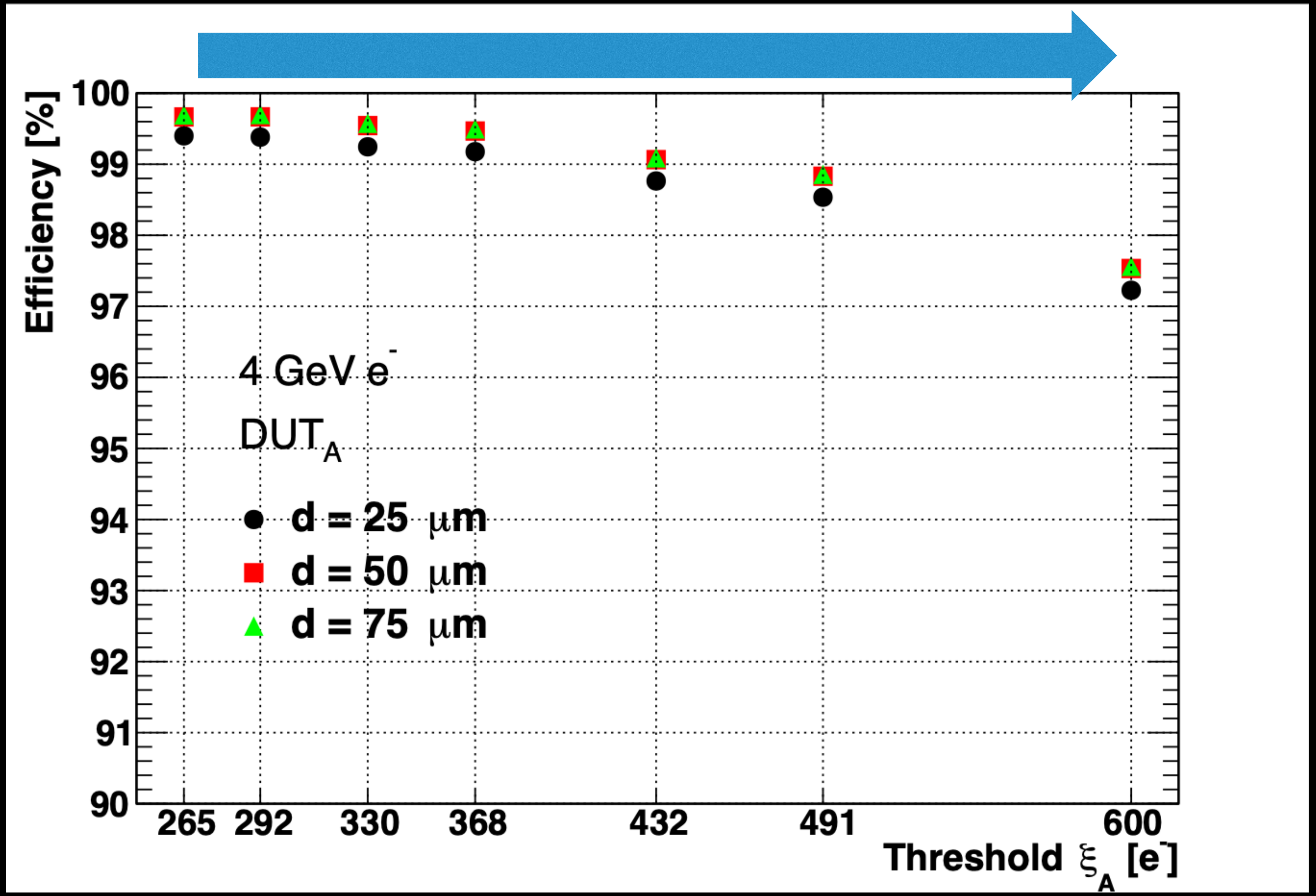
Wei Wei

- A set of columns will die after a long time of working, can only be waken up by re-config.
  - It maybe related to hit rate and FIFO, data transmission error in high speed data
- When multiple chips work together in flexible PCB, Threshold need to raised, efficiency decreased
  - Reason: No local LDO on chip , significant cross talk due to powering
  - Solution: Implement LDO in next chip submission, re-design the flex
- Ghost hit in high-rate data taking
  - Current solution :Lower down the system clock from 40MHz -> 20MHz (test board) -> 15.6MHz (ladder)
  - Solution :refined time constraint on circuit synthesis

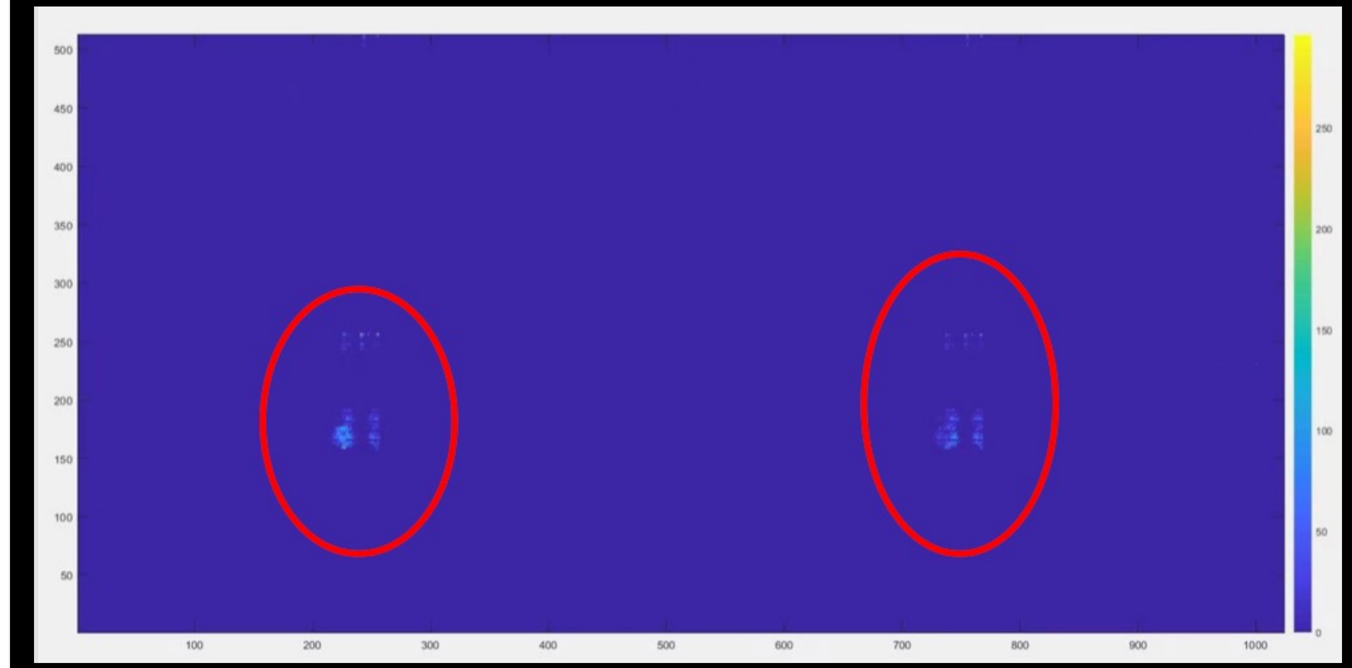
Data loss in Long term data taking



Threshold raised with multi-chip



Ghost hit in high-rate data taking



Summary of CMOS Sensor chip R & D

- **Developed the first full-size CMOS pixel sensor for particle detector in China**
  - **High spatial resolution and radiation hard**
- **Developed three double-layer vertex detector prototype**
  - **Readout electronics and data acquisition for detector prototype was developed**
- **Completed beam tests for the sensor prototype and the detector prototype at DESY**
  - **The Assessment indicators of the project have been achieved**
- **Some issue in the chip and vertex detector integration need follow up R & D**

	Requirement	Result	
Spatial resolution	3-5 μm	Laser test: ~ 4 μm Chip-level Beam Test : 4.5 μm ✓ Prototype level Beam Test: 4.9μm	World leading
Radiation hardness (total ionization dose, TID)	>1 Mrad	>3 Mrad ✓	First in China

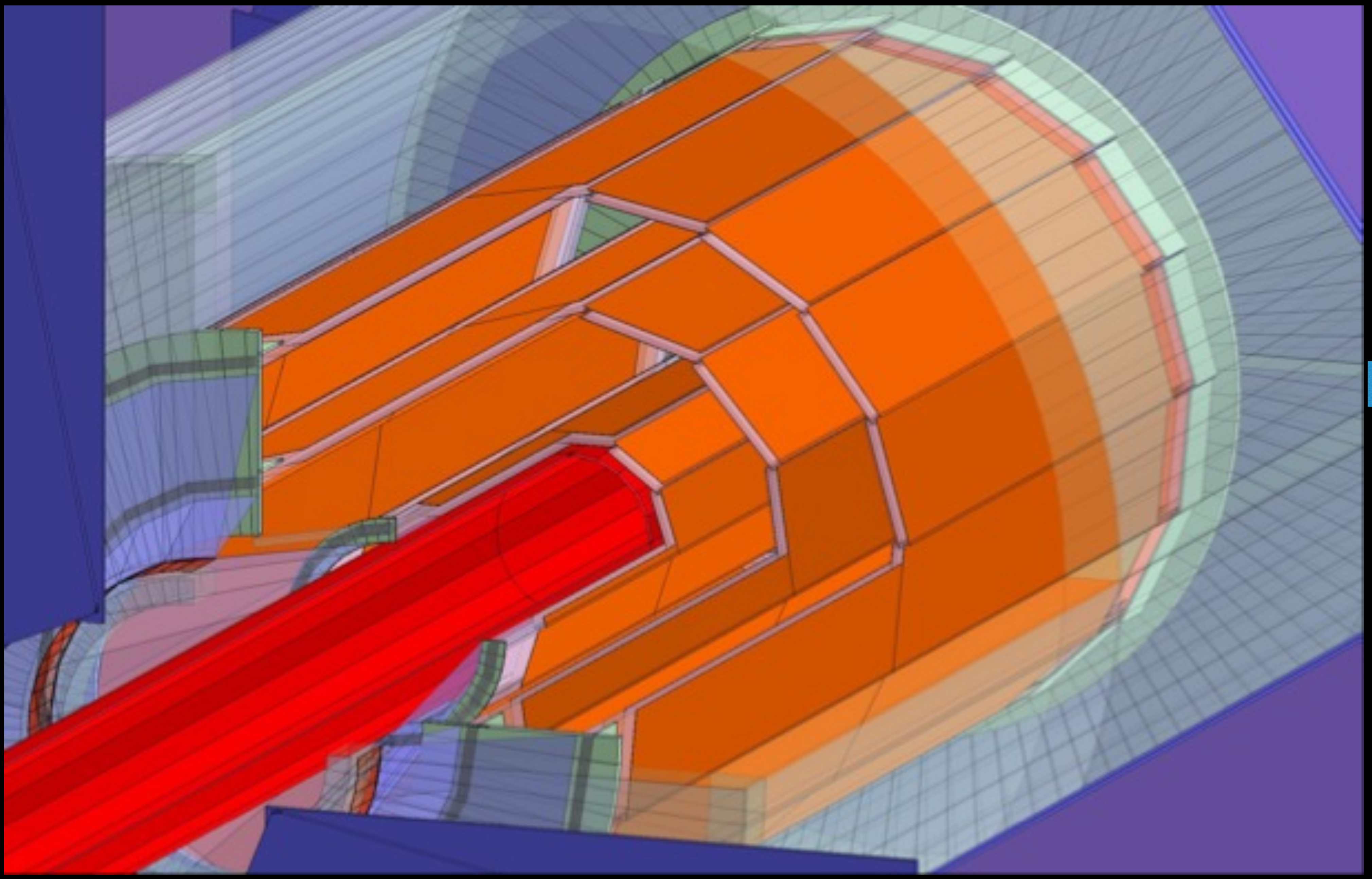
Research Team in MOST2 silicon project

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning Irradiation, test beam organization
IFAE(Spain)/CCNU	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
ShanDong University	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
Nanjing University	Irradiation, test beam

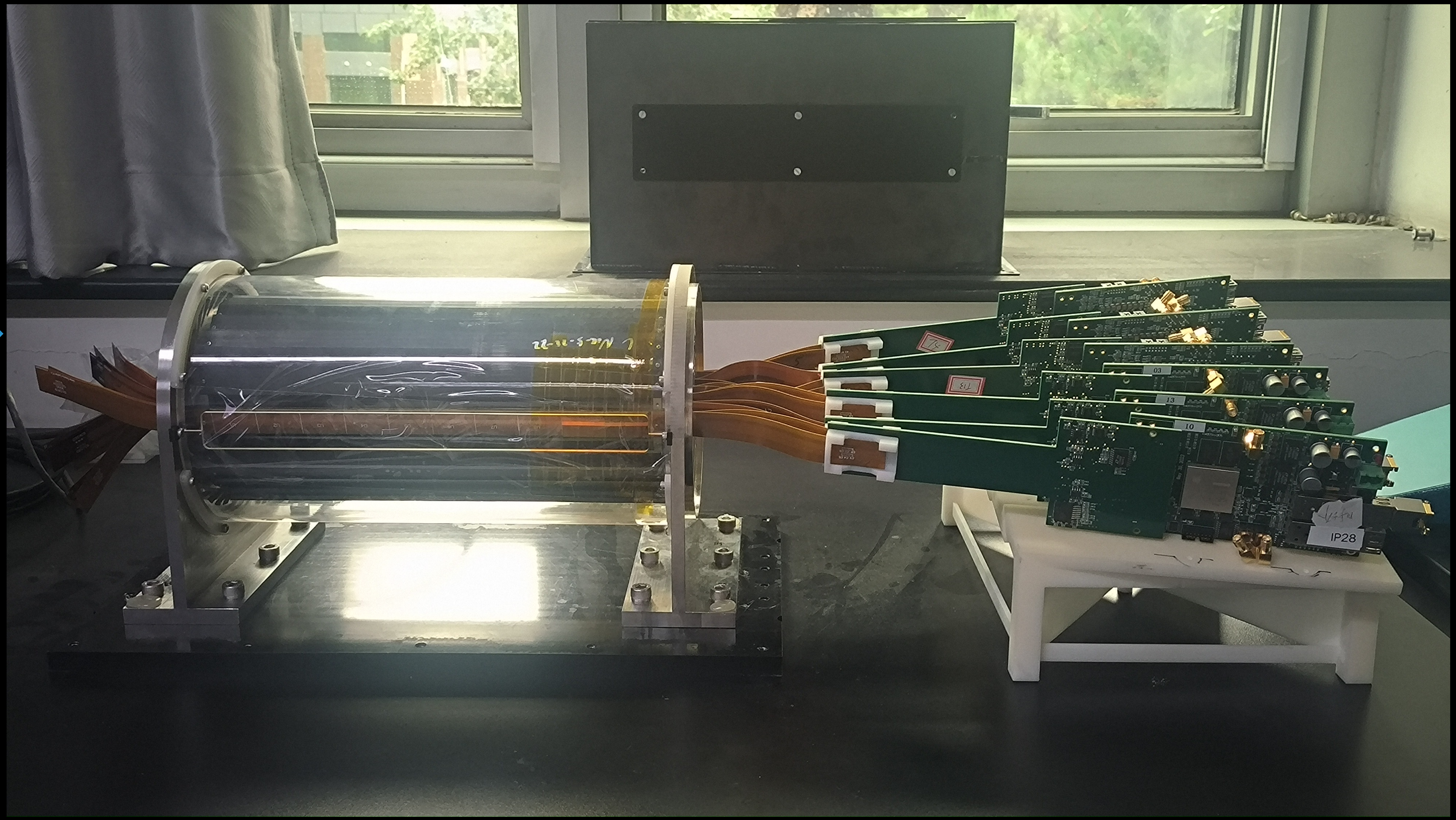
Summary of CECP vertex detector prototype (2)

- **Developed three double-layer vertex detector prototype**
  - **From CDR design to vertex detector prototype**

CEPC design (2016)



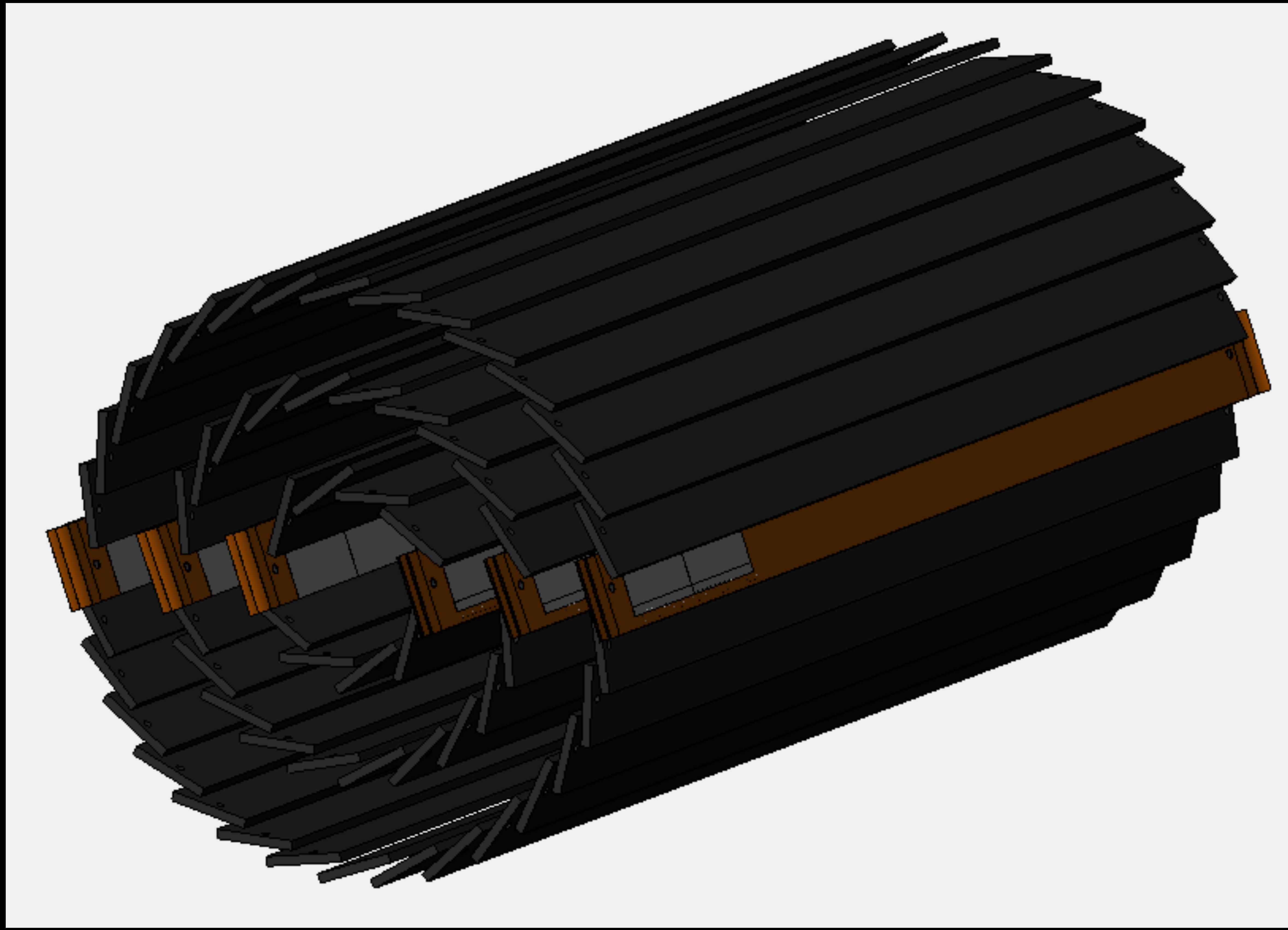
Vertex detector prototype (2023)



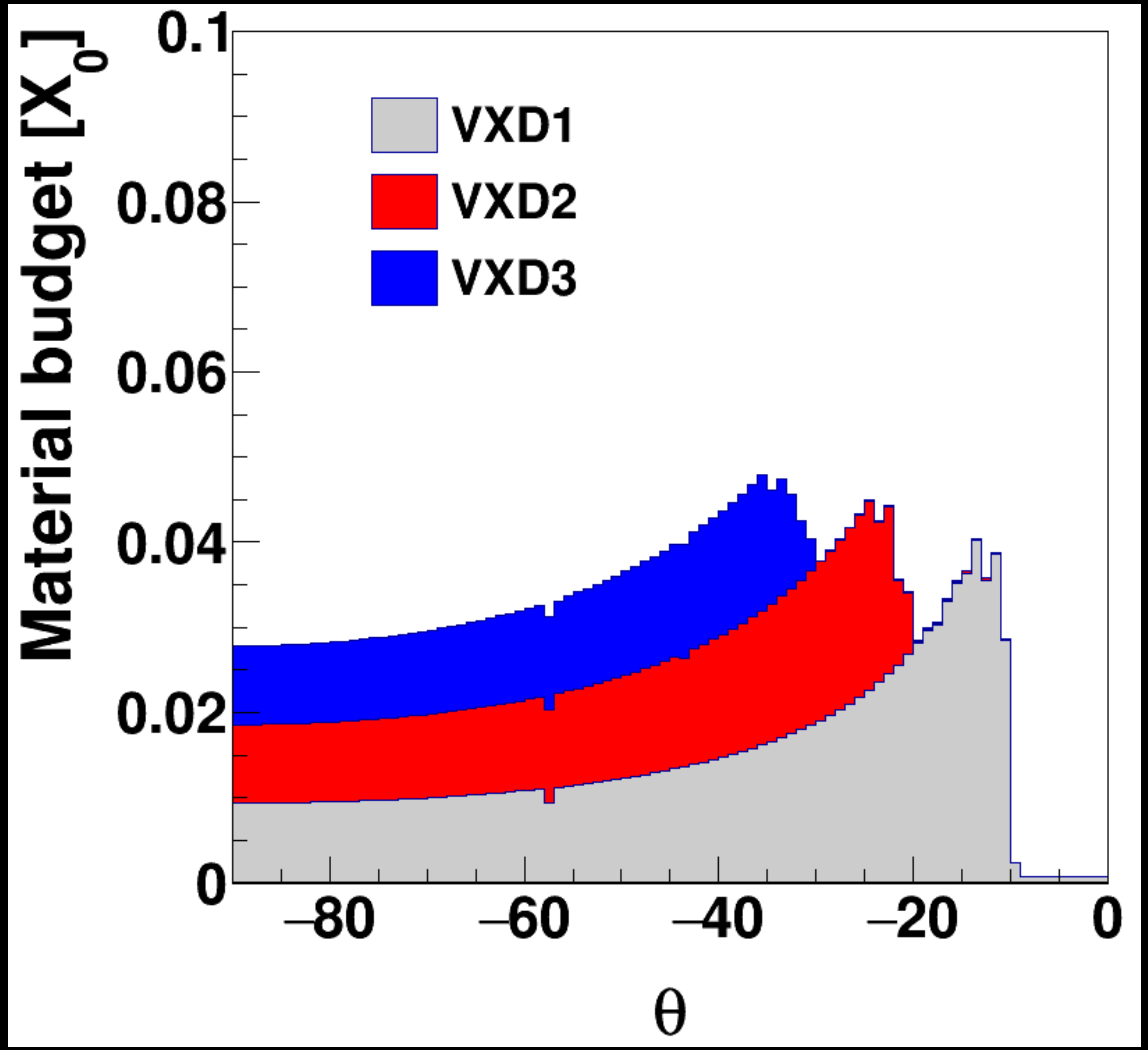
backup

Estimated Material budget for vertex detector prototype

- Estimated material budget 0.026 X0 for three double ladders vertex detector (6 layers)
  - Target for final CEPC vertex detector is 0.009 X0 (0.015% X0 per layer)
  - Copper in flexible PCB are major contributions
  - Plan to replace copper into Aluminum in final CEPC vertex detector
  - Further thinning of silicon wafer (150um → 50um)



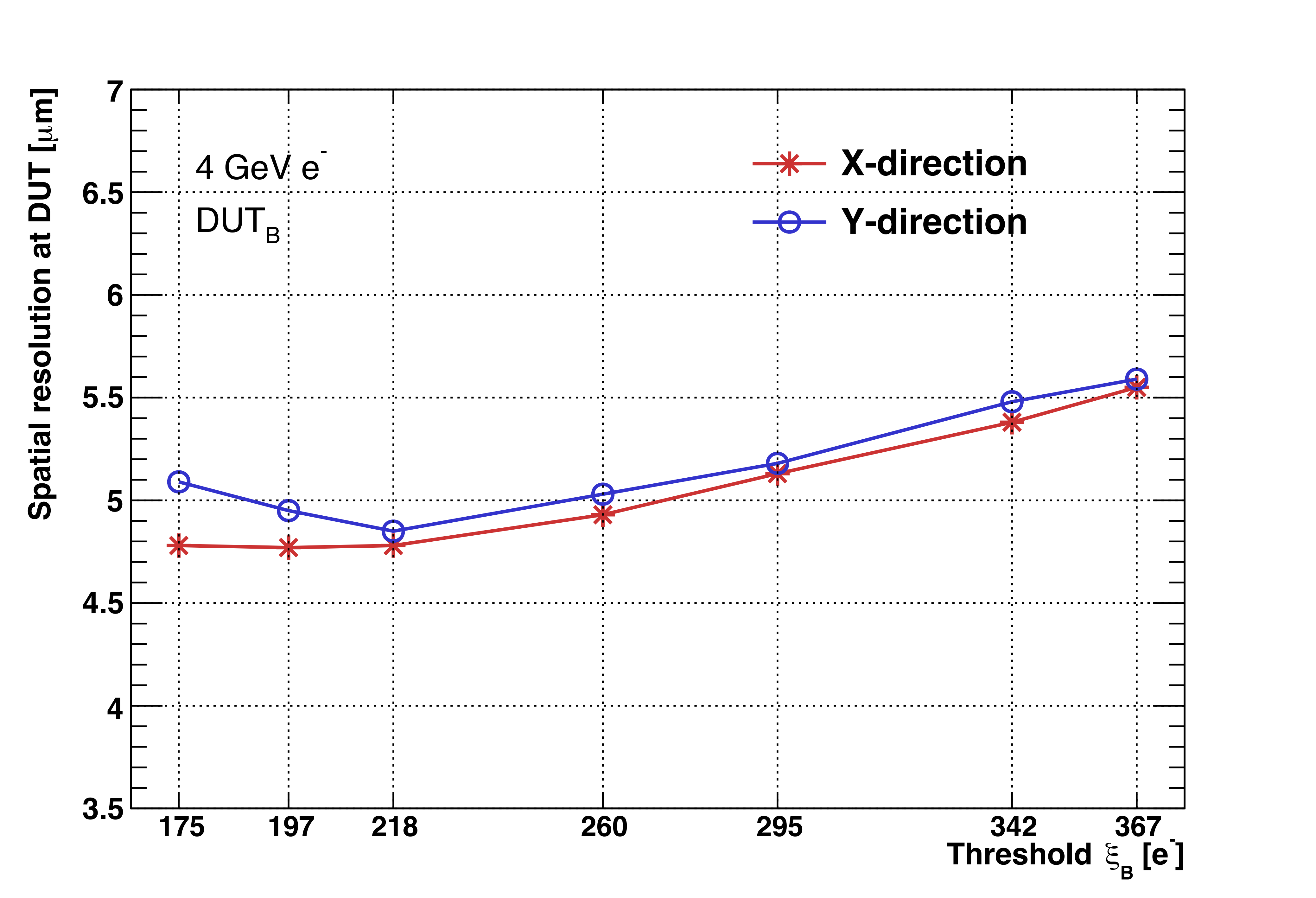
Estimated material budget for this prototype

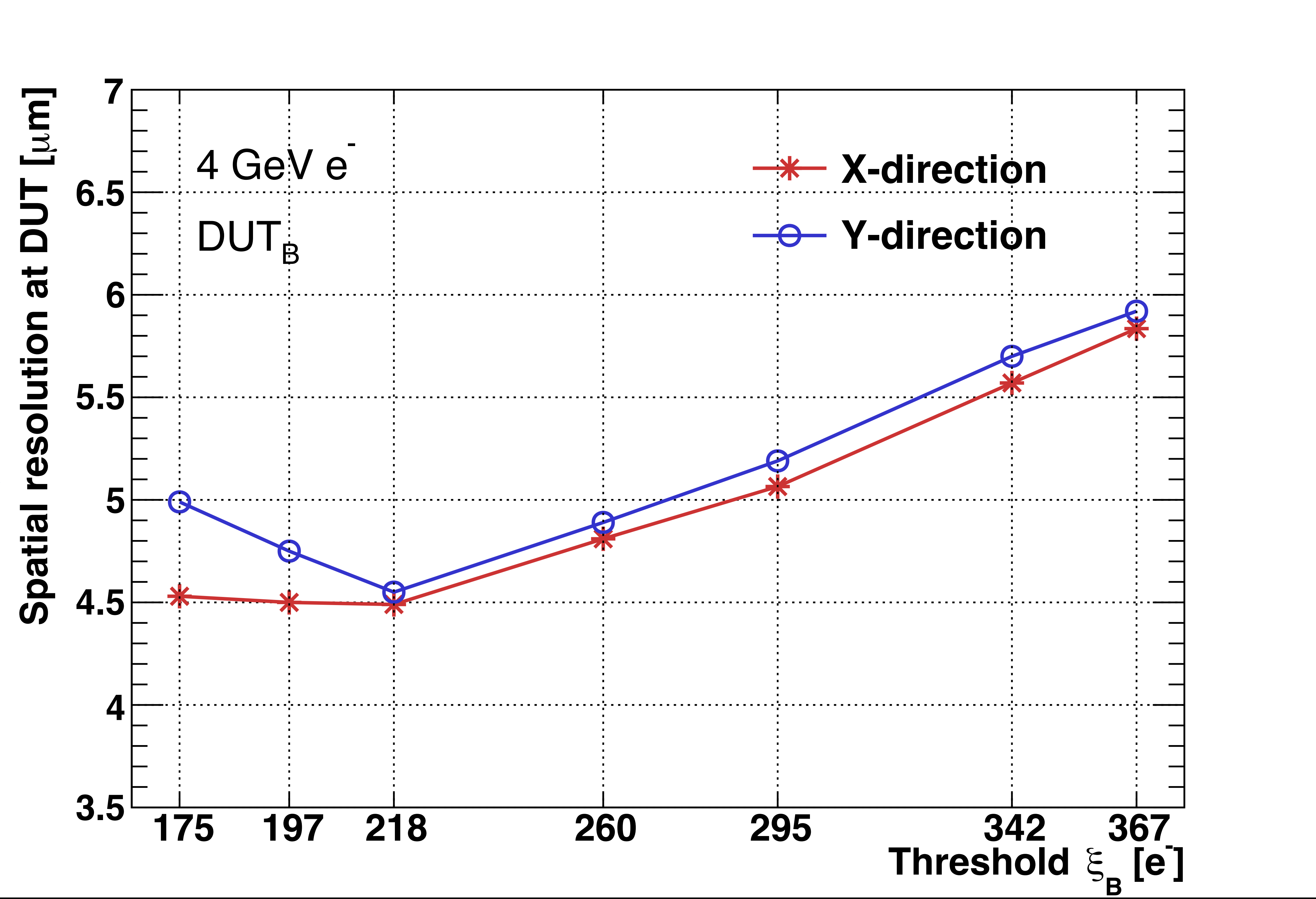


- D f

$$\mathrm{pull_b} \equiv p_\mathrm{b} = \frac{r_\mathrm{b}}{\sqrt{{\sigma_\mathrm{int}}^2 - {\sigma_\mathrm{t,b}}^2}}.$$

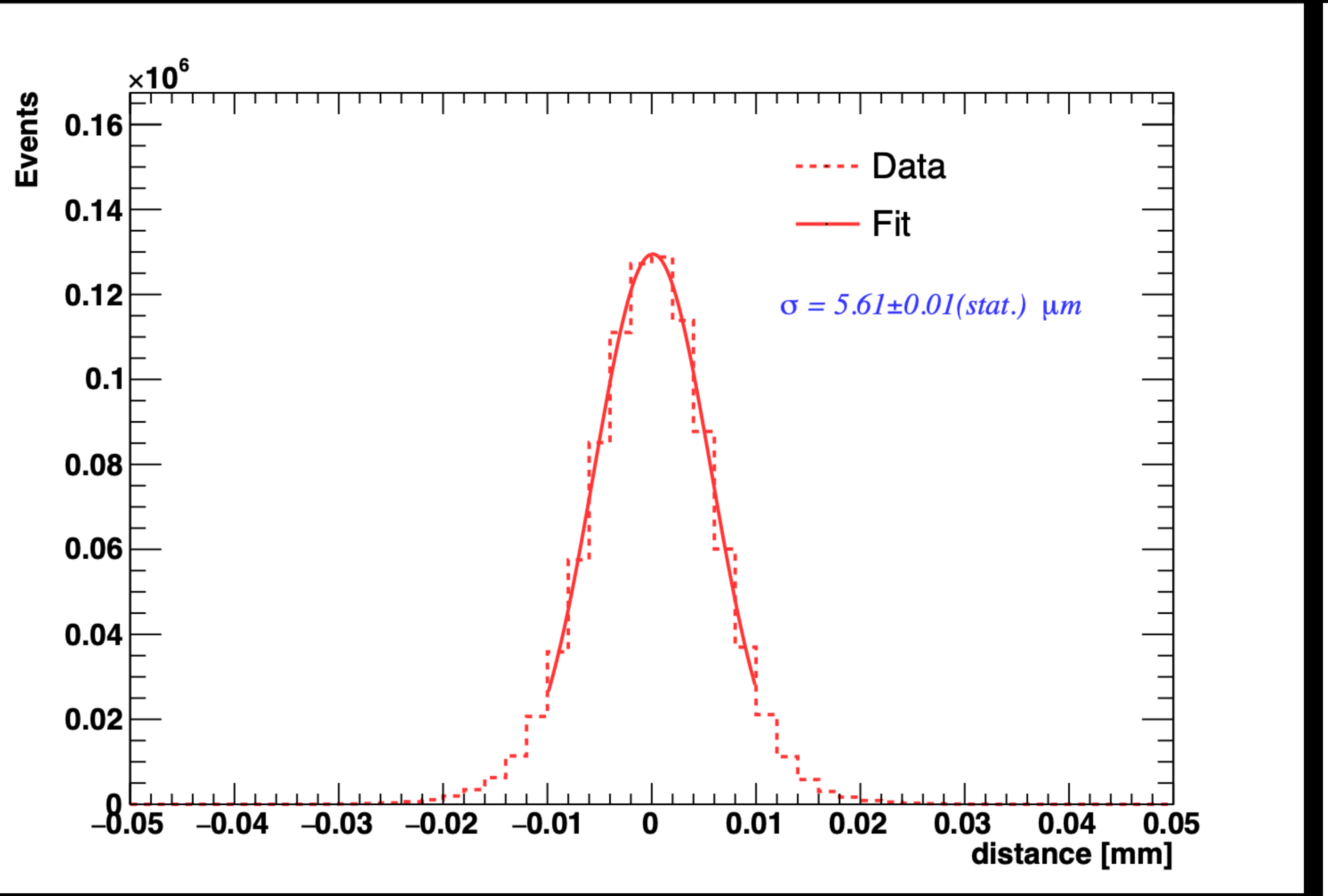
r_b: biased residual
sigma_int: intrinsic resolution
sigma_t,b: telescope resolution

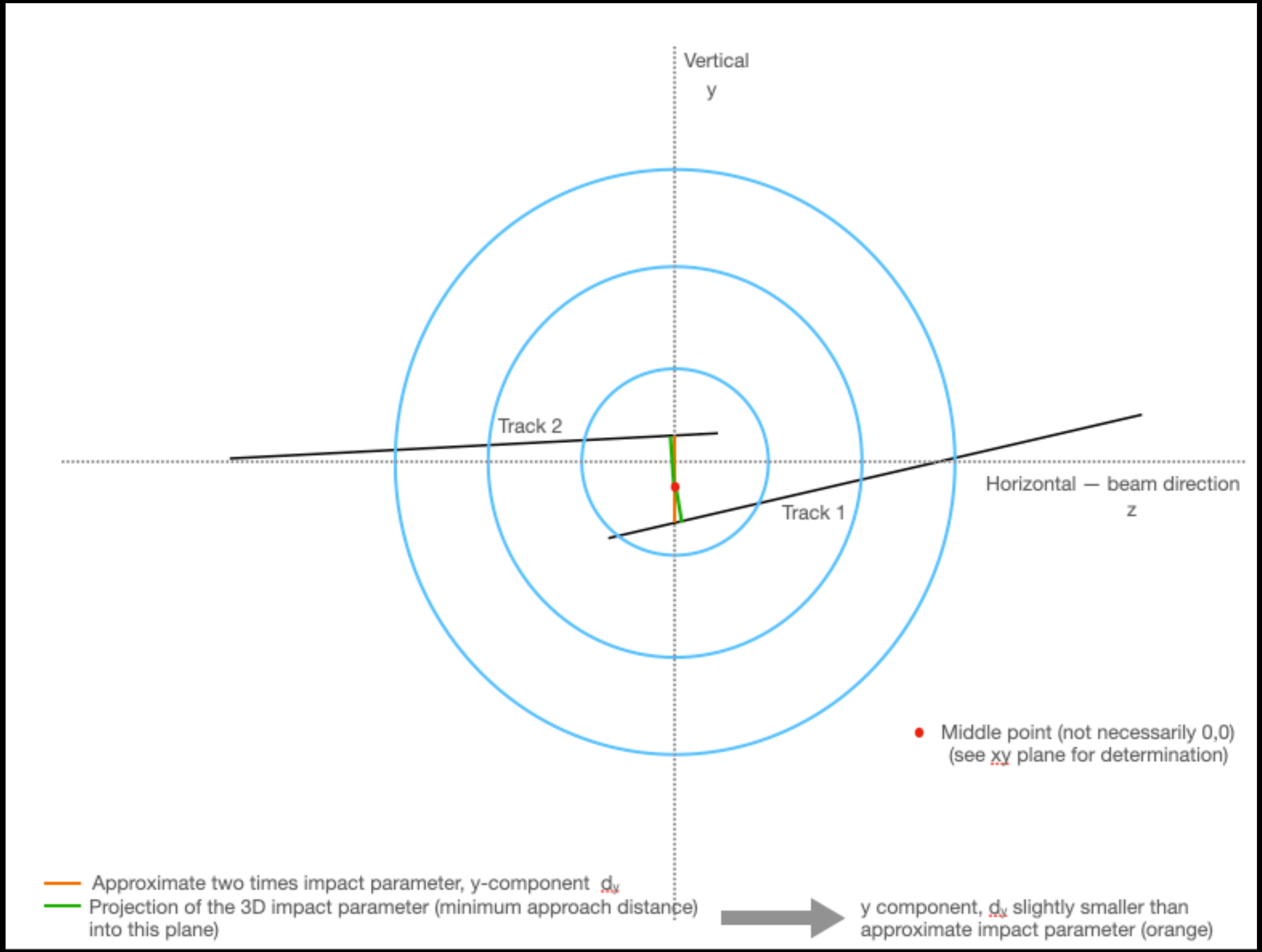




Preliminary result of impact parameter resolution

- No real interaction point or real primary vertex (PV) in testbeam setup
  - Define PV as the centre of the point in xy plane extrapolated from the up/downstream
  - Calculate the impact parameter between primary vertex and upstream/downstream tracks





Carbon fiber Support structure of the ladder

- Fabricated support structure prototype of the ladder (IHEP designed)
  - **4 layer of carbon fiber, 0.12mm thick for the whole support**
    - **Shallow design inside ladder support to reduce material**
  - **2~3 time thinner than conventional carbon fiber in China**

Air cooling for CEPC vertex detector

- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix design : $\leq$ 100 mW/cm^2. (trigger mode), $\leq$ 150 mW/cm^2 (triggerless mode),
  - Taichupix measured result: ~60 mW/cm^2(triggerless mode, 17.5MHz)
  - CEPC final goal : $\leq$ 50 mW/cm^2
- Cooling simulations of a single complete ladder with detailed FPC were done.
  - Need 2 m/s air flow to cool down the ladder

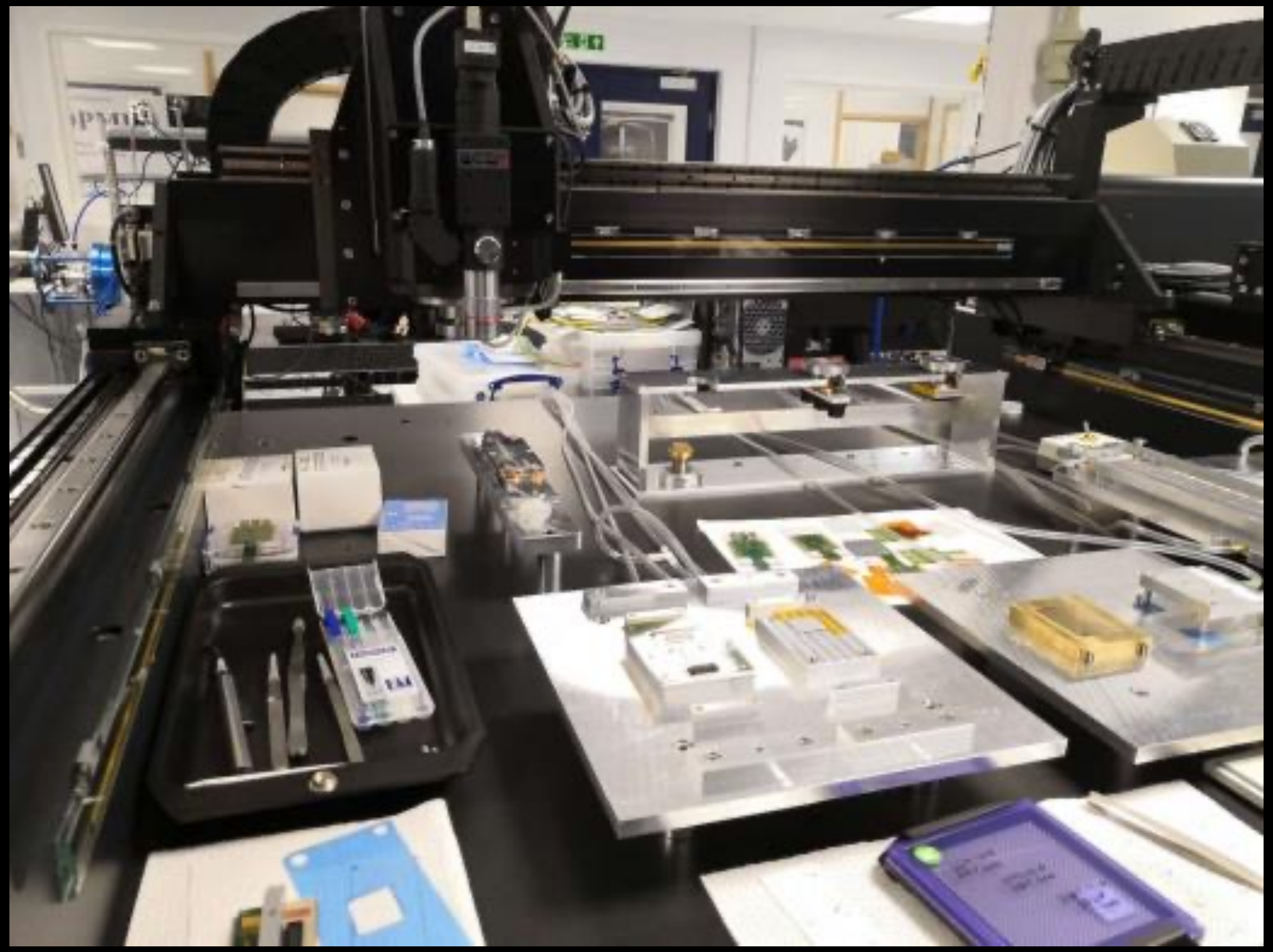
Max temperature of ladder (℃) (air temperature 5 ℃)					
Air speed (m/s) / Power Dissipation (mW/cm2)	5	4	3	2	1
100	19.6	21.8	25.0	*30.6*	*43.4*
150	26.9	30.1	35	*43.4*	*62.6*

International Collaboration

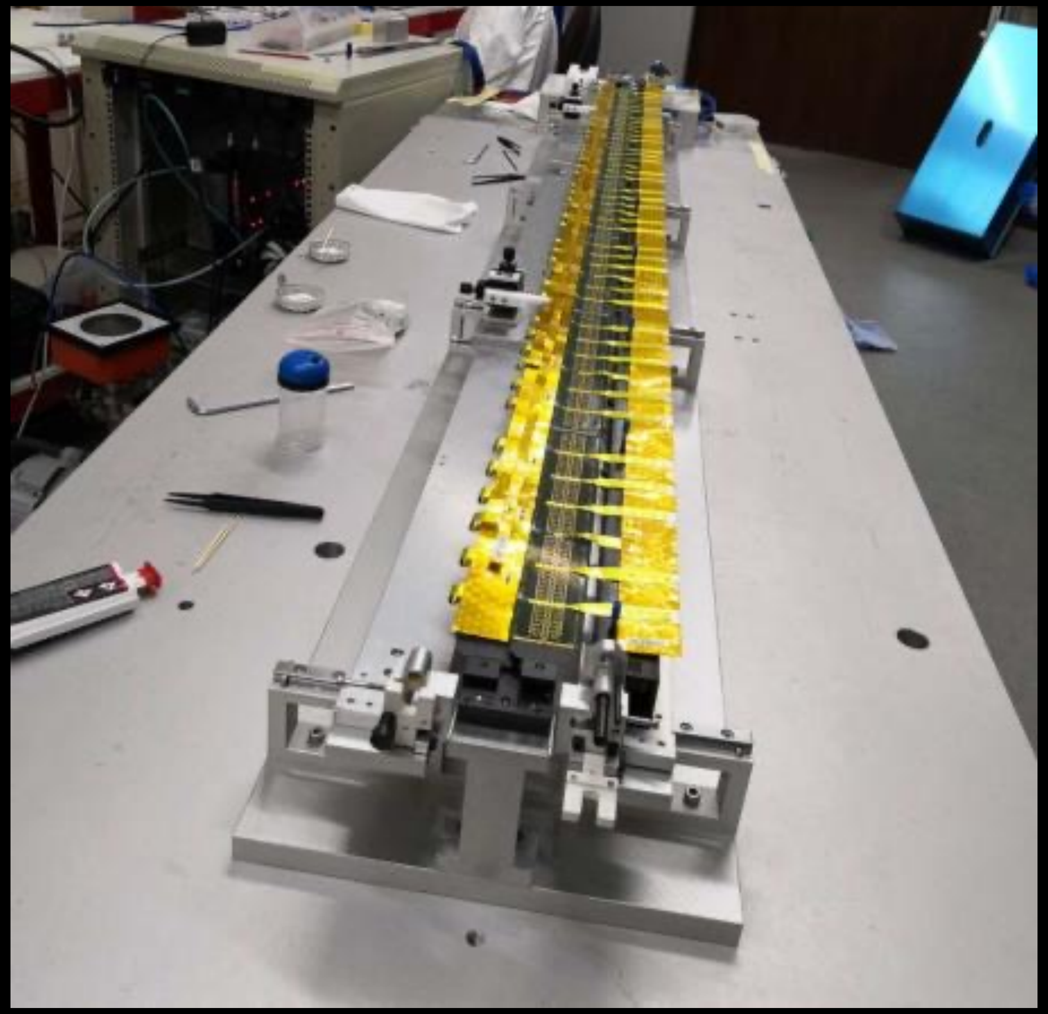
- ➢ **Active collaboration with IFAE (Spain) in sensor chip design.**
- ➢ **We have one engineer visited Oxford and Liverpool for 4 weeks in 2019**
- ☐ **Planning to collaborate on module and detector structure**
- ☐ **Unfortunately, Collaboration didn’t continue due to CovID**

Lab visit in Oxford

Mu3e ladder, Atlas barrel strip stave prototype.

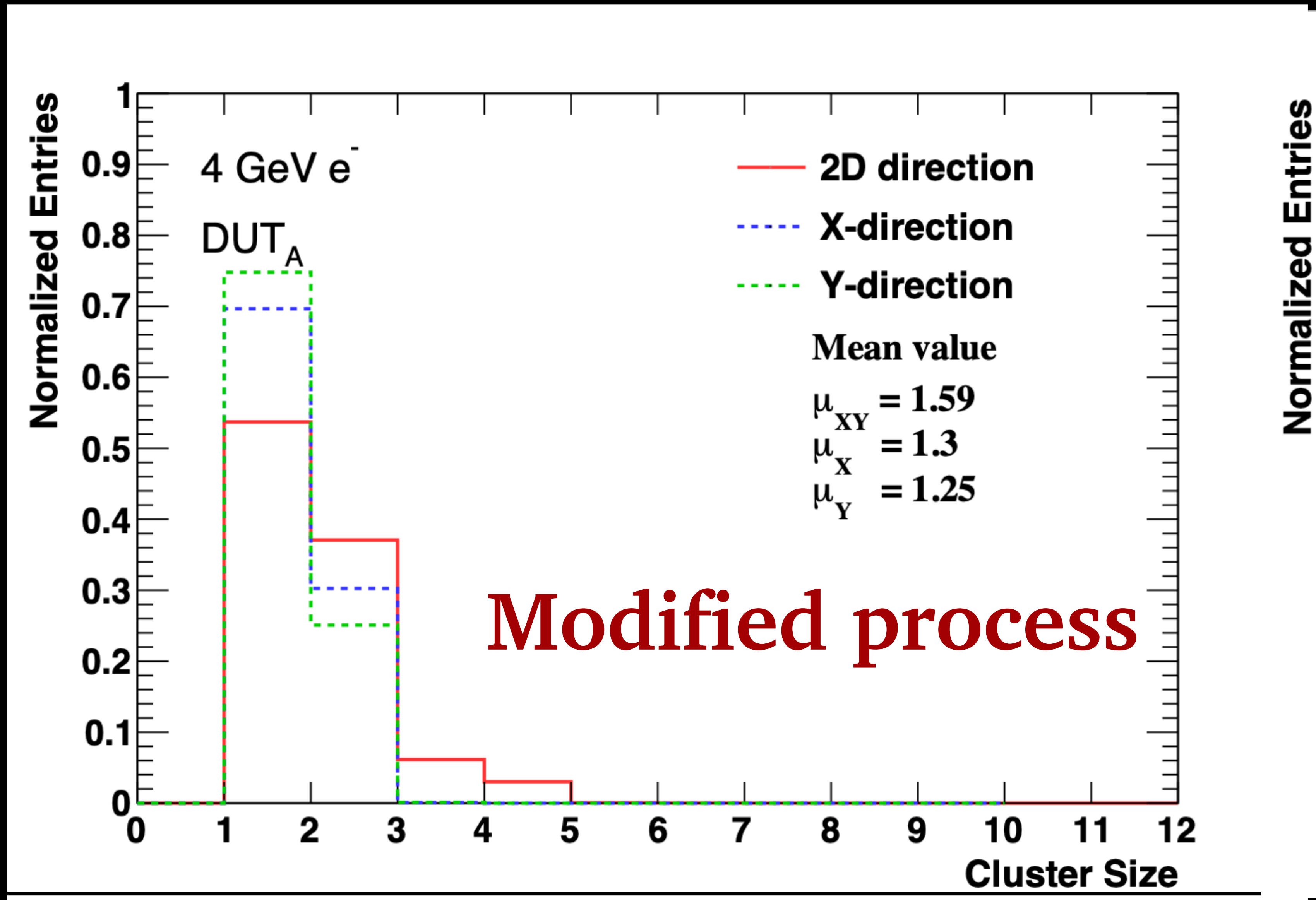


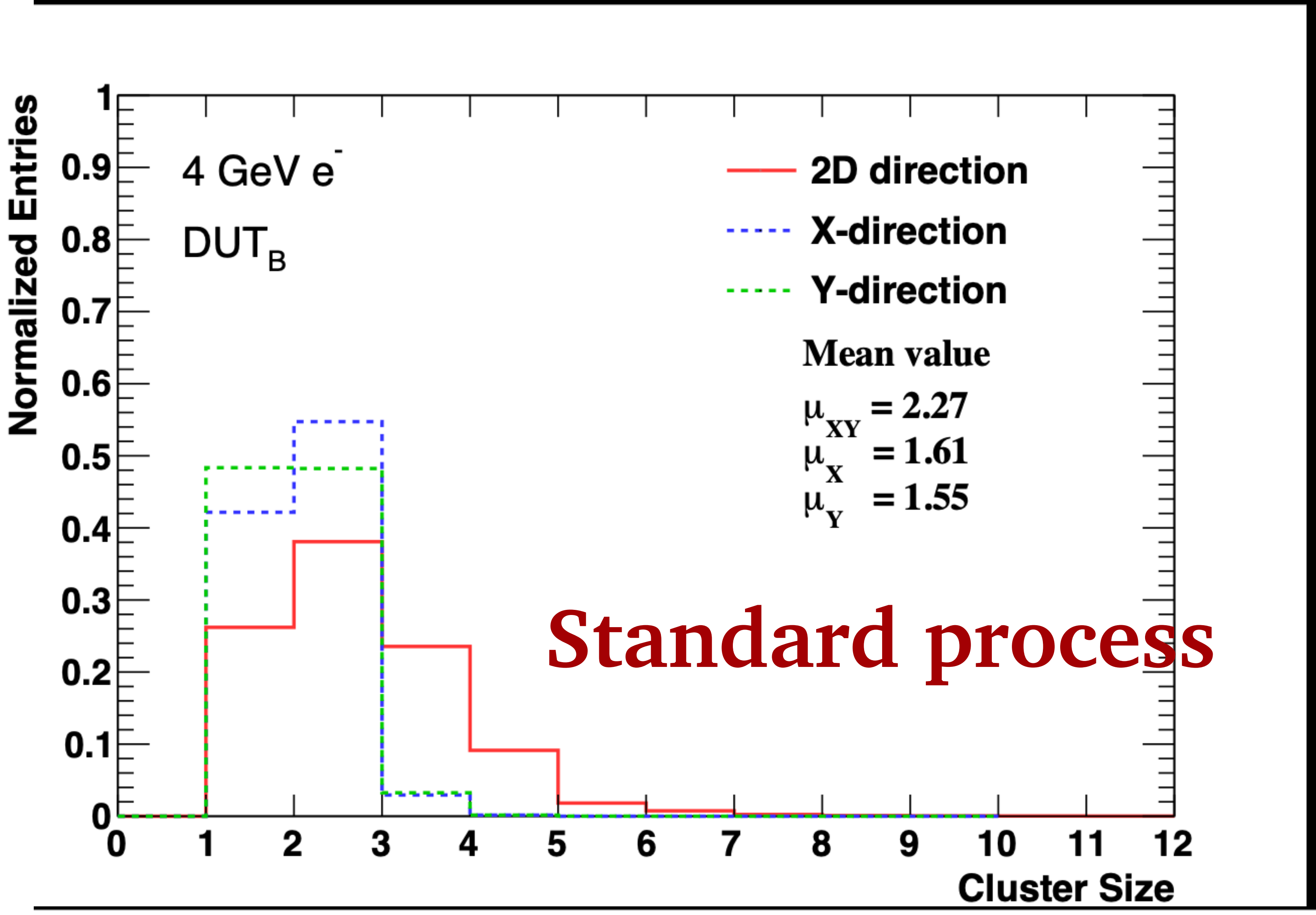
Labs visit in Liverpool

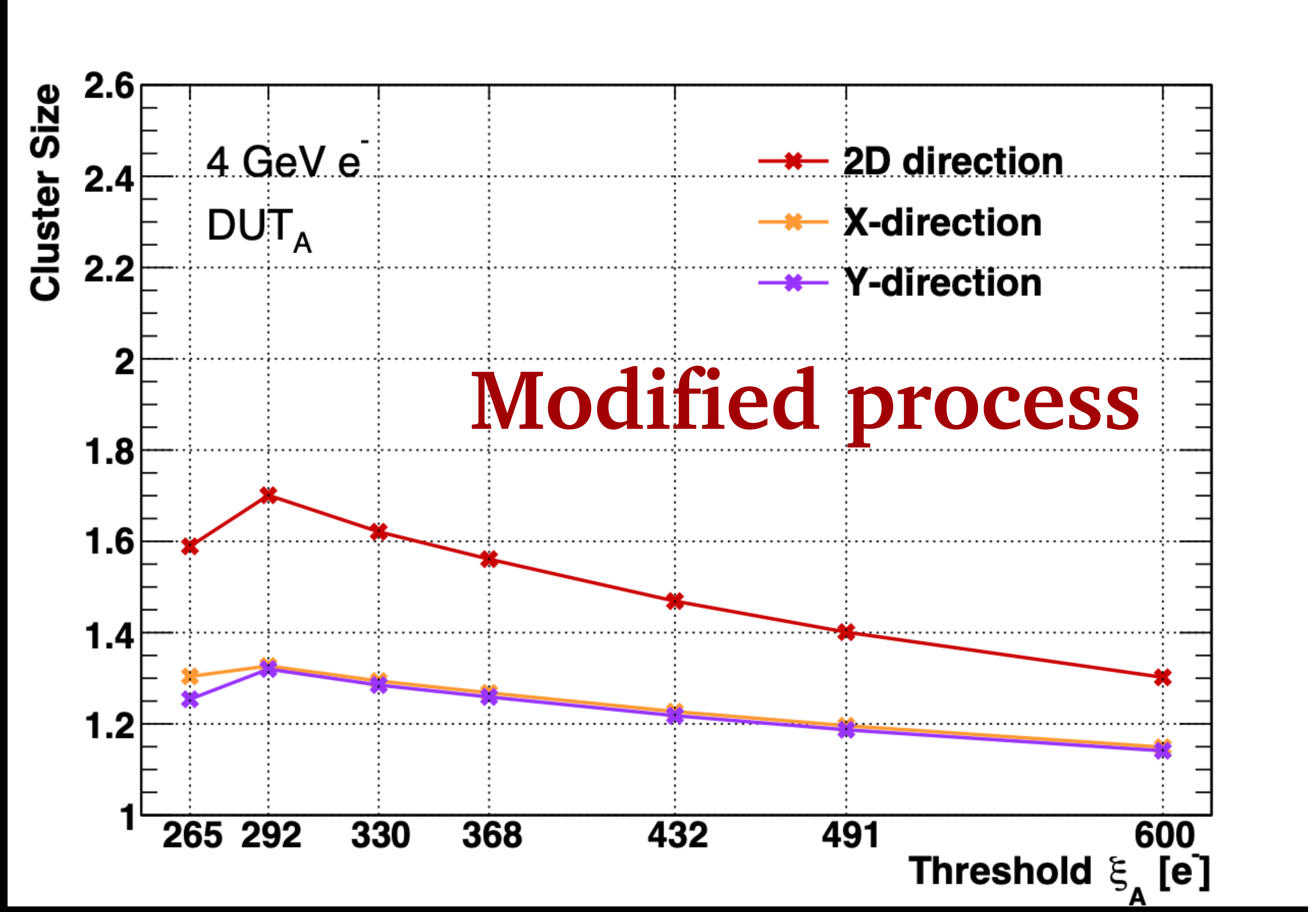


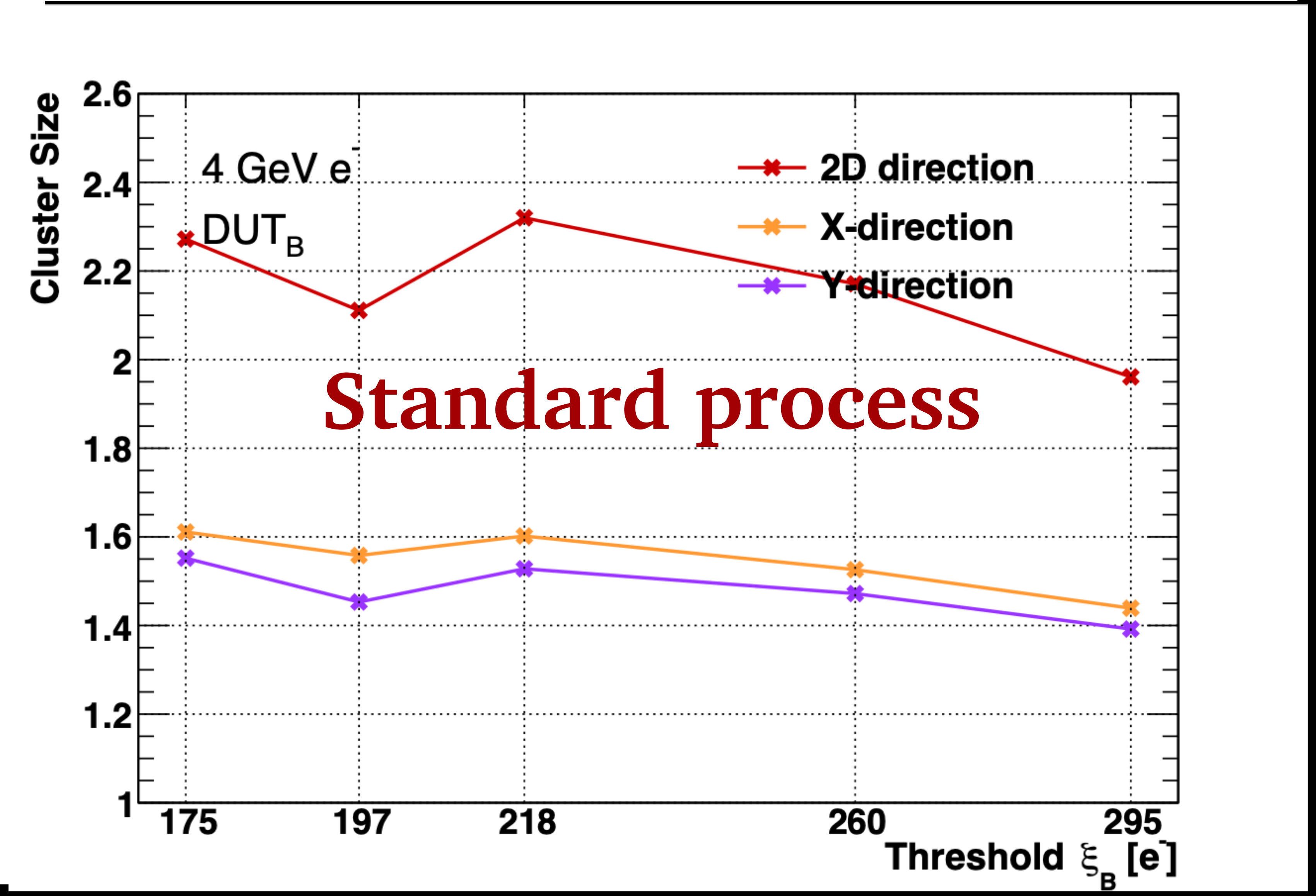
Module of Alice’s OB tracker, Advance material Lab

Offline analysis results of first test beam









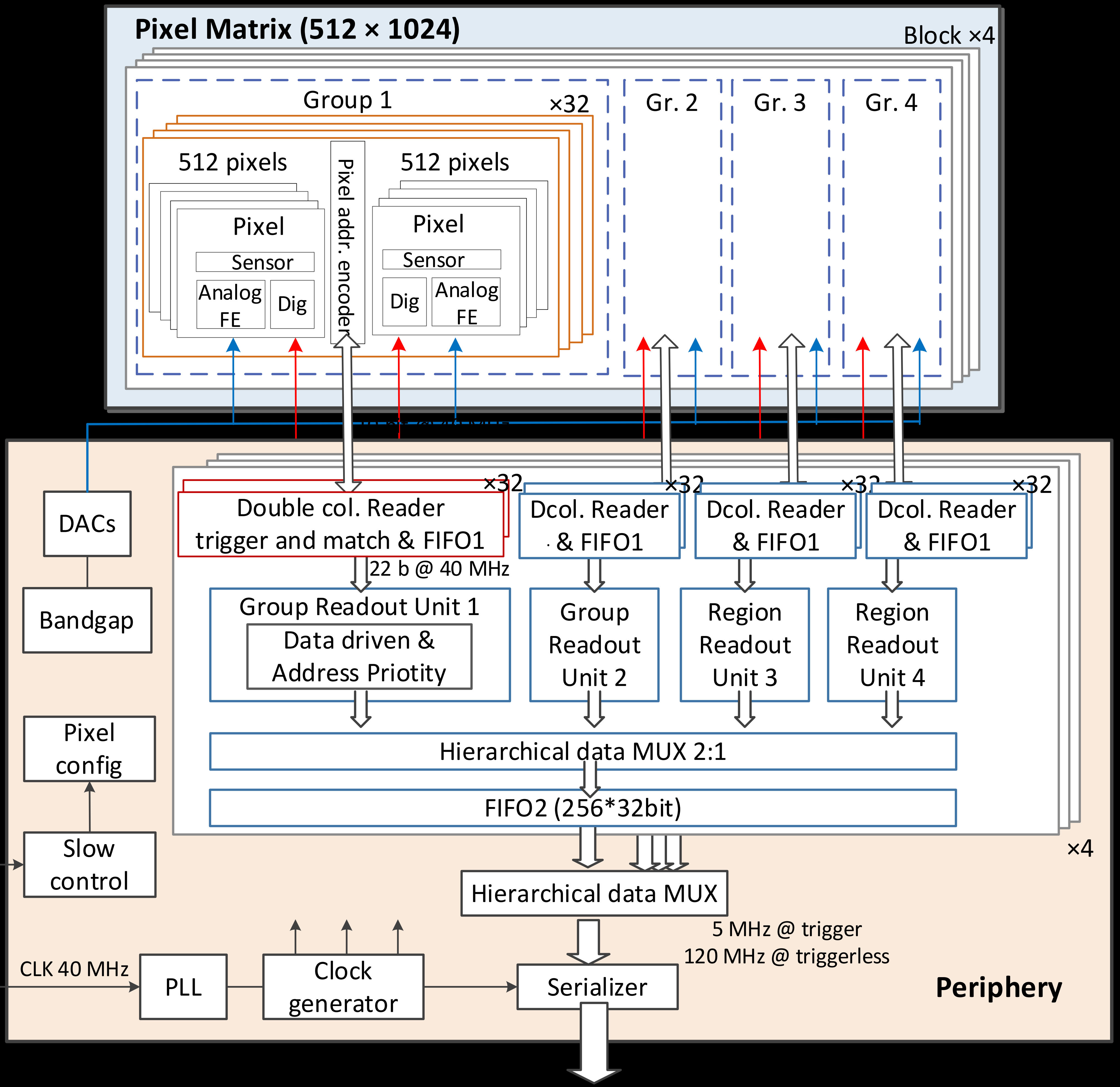
- **Less charge sharing effects in modified process with full depletion**
- **If lowering the threshold, cluster size will be dominated by noise**

CEPC vertex detector R & D

- Three on-going R & D programs on vertex detector
  - Previous update in CEPC day (June 15th)   https://indico.ihep.ac.cn/event/11875/
- This talk focuses on MOST2 project
  - MOST2 aims to build full-size vertex detector prototype

Funding agency	Process	International collaborators	Objectives of the project	schedule
CEPC MOST1	CMOS	Strasburg IPHC	Small pixel size design with in-pixel digitization and low power frontend	2016.6-2021.5
MOST2	CMOS	IFAE/Oxford/ Livepool …	vertex detector prototyping (Full-size sensor support structure, module …)	2018.5-2023.4
NSFC	SOI	KEK/SOIPIX collaboration	Verification of SOI process with small pixel size and low noise design	2016-

TaichuPix sensor architecture



- **Pixel 25 µm × 25 µm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at EOC
  - Readout time: 50 ns for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

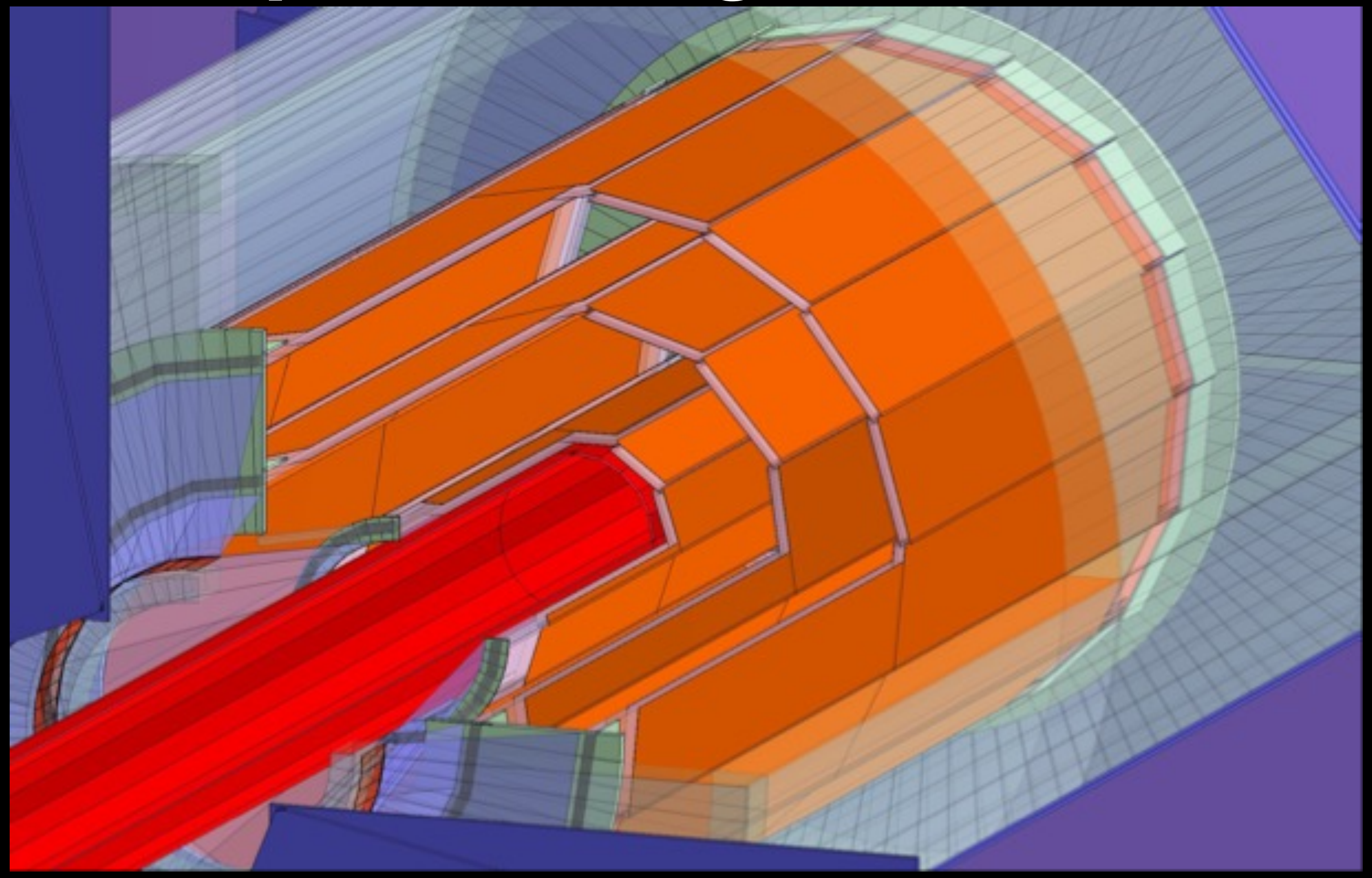
Vertex detector prototype structure optimization

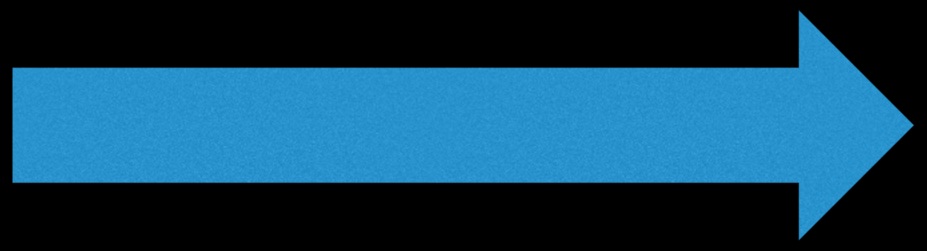
- Based on CEPC vertex detector conceptual design → Three double-layer barrel detector
  - This project plan to prototype the important part of vertex detector (CDR design)
  - The cost for the full vertex detector is high (eg: ~50 M CHF for ATLAS ITk pixel detector)

    → Plan to build full mechanical part of the detector

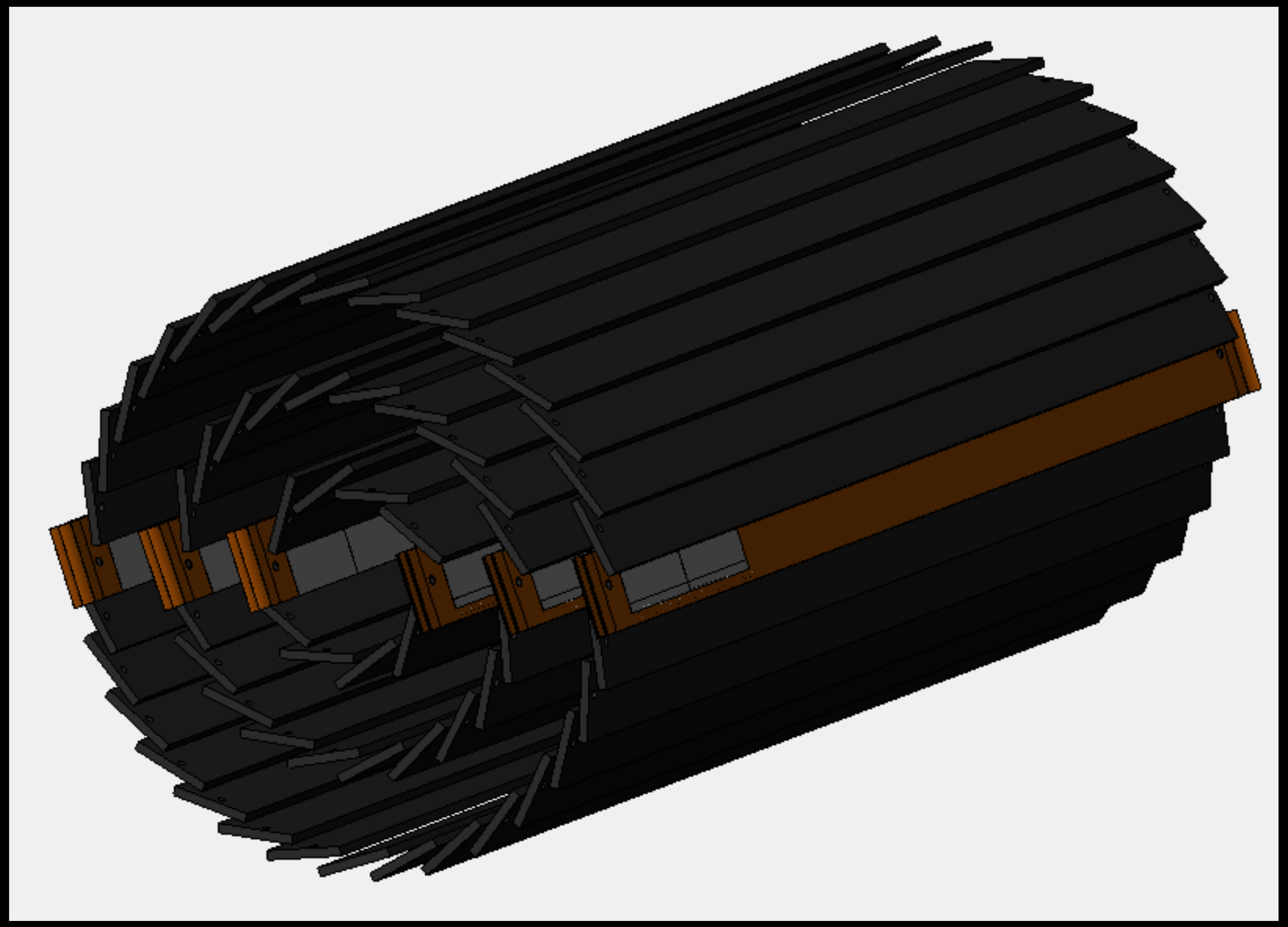
    → install a sector of ladders in prototype , not necessary to build full vertex for R & D
- Optimize the geometry based on real ASIC and electronics dimension
  - Optimize geometry based on its physics performance from simulation
  - Engineering design of prototype structure

CEPC Vertex detector
Conceptual design (2016)





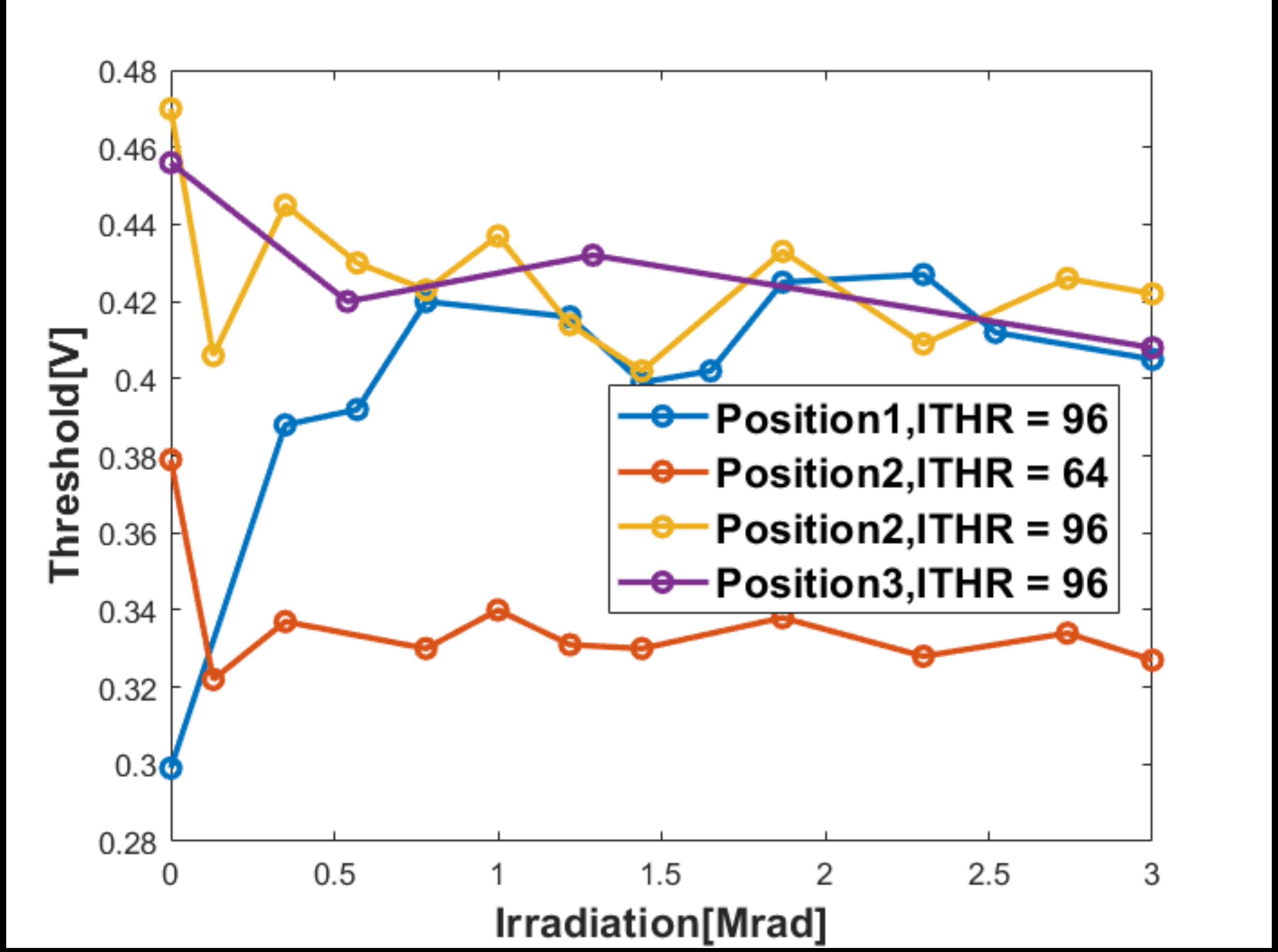
This project
Vertex detector prototype design



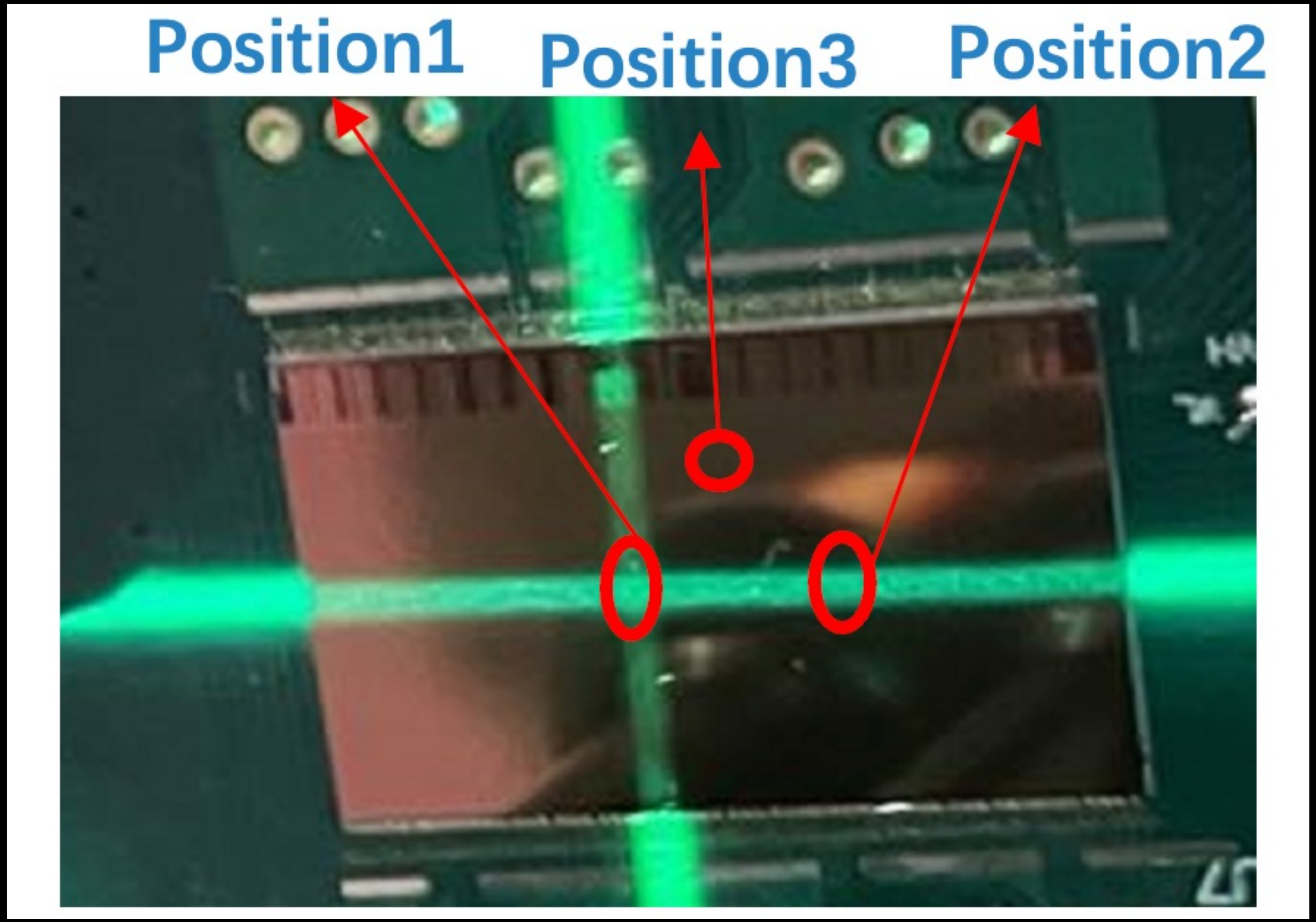
Radiation tests

- Taichupix3 was irradiated in-situ tested up to 3 Mrad
  - Normal chip functionality and reasonable noise performance
  - Reach the goal of the project: radiation hardness on total ionization does >1 Mrad

Taichupix3 irradiation test
Pixel threshold vs. TID

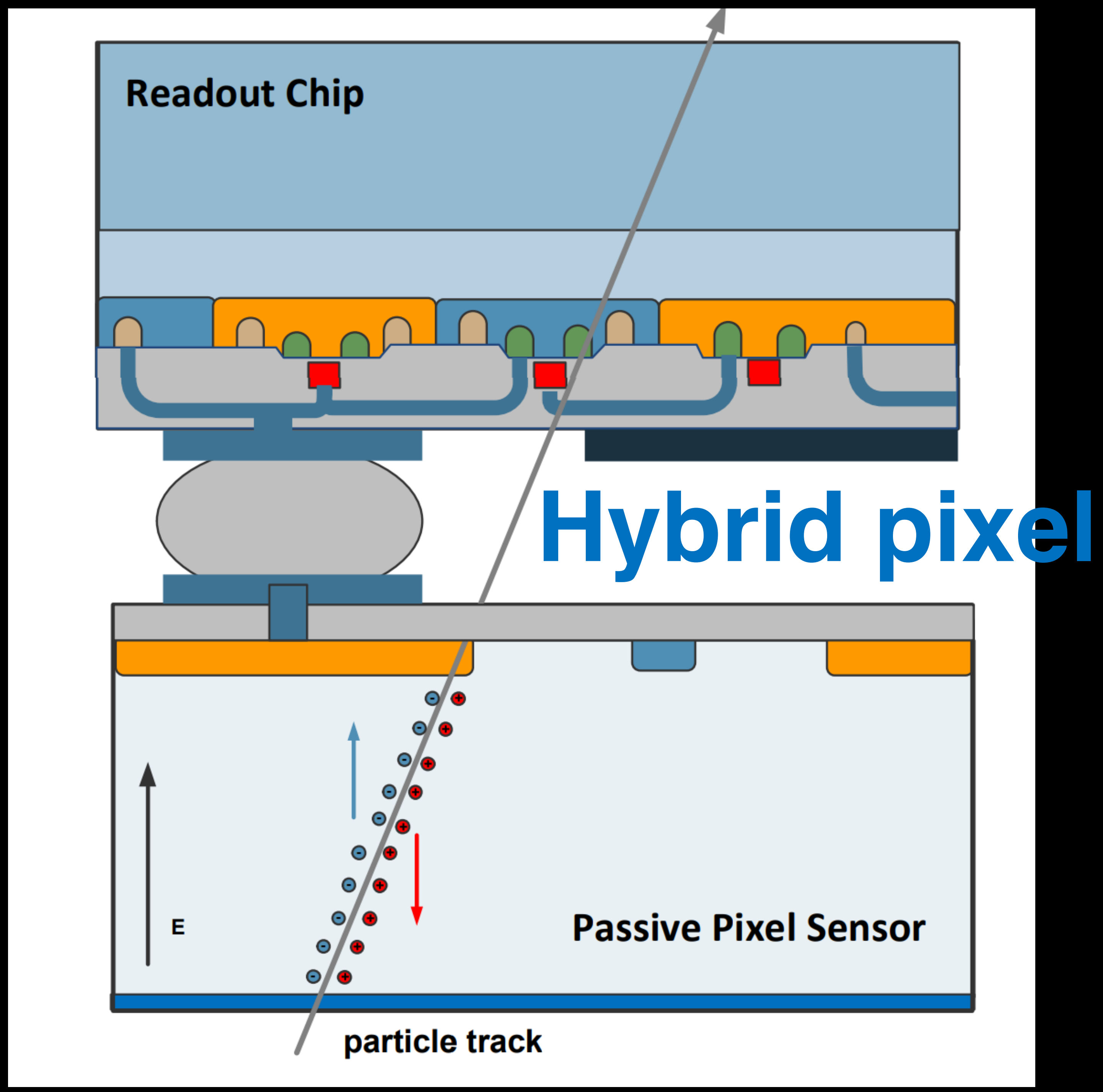


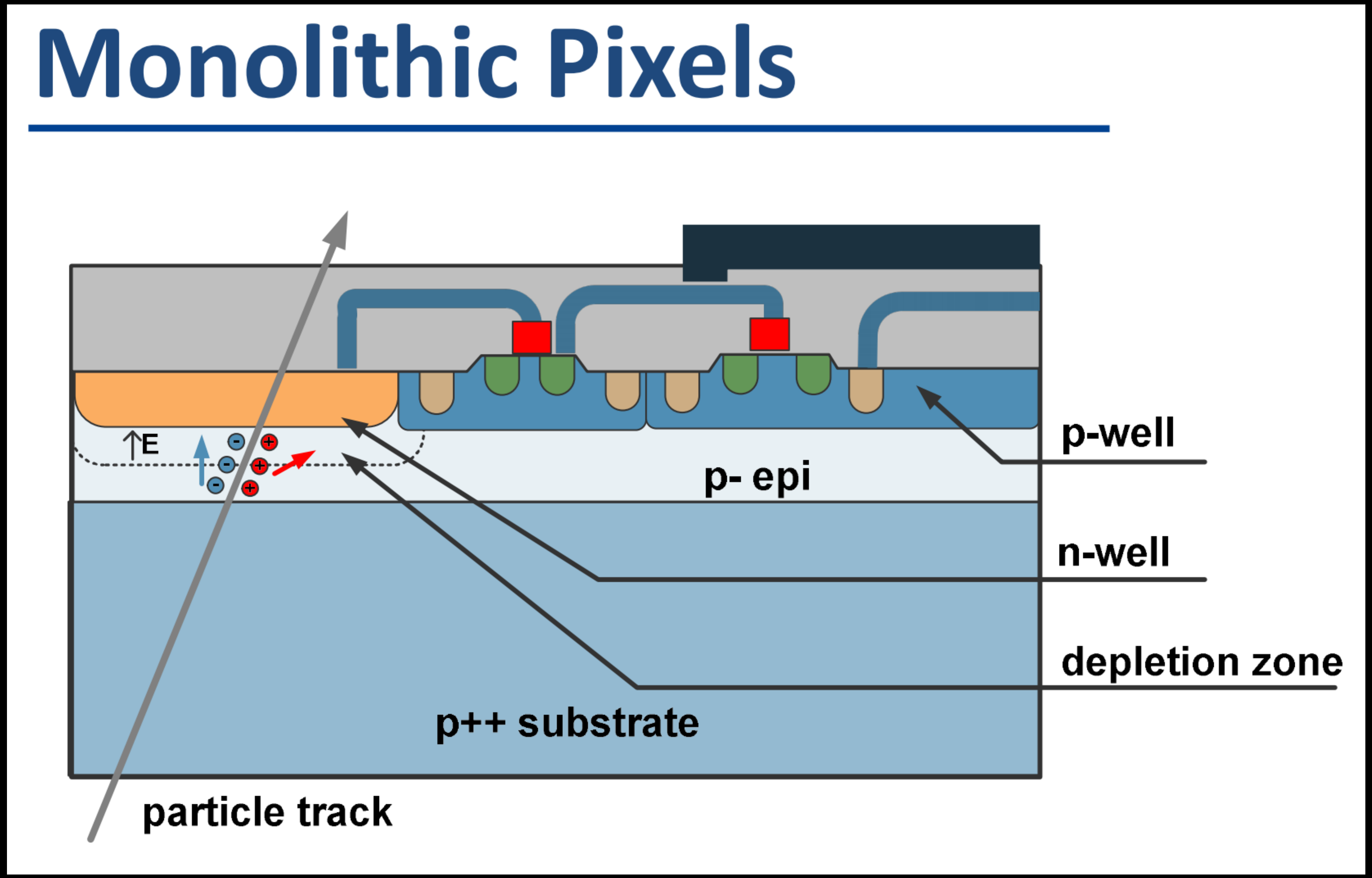
TaichuPix-3 irradiated at Synchrotron radiation beamline (12 keV X-ray)



CMOS Monolithic pixel sensor

- Conventional Hybrid pixel technology at Large Hadron Collider
  - Need to bump bonding with readout ASIC
  - Typical pixel size >=50μm, much more difficult for bump bonding with smaller pixels
- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - Sensor and ASIC high integrated in one chip, easier for detector assembly
  - Can have compact structure in pixel array design.
    - Pixel size can be reduced to 25um or below → can achieve better spatial resolution





CMOS Sensor chip R & D

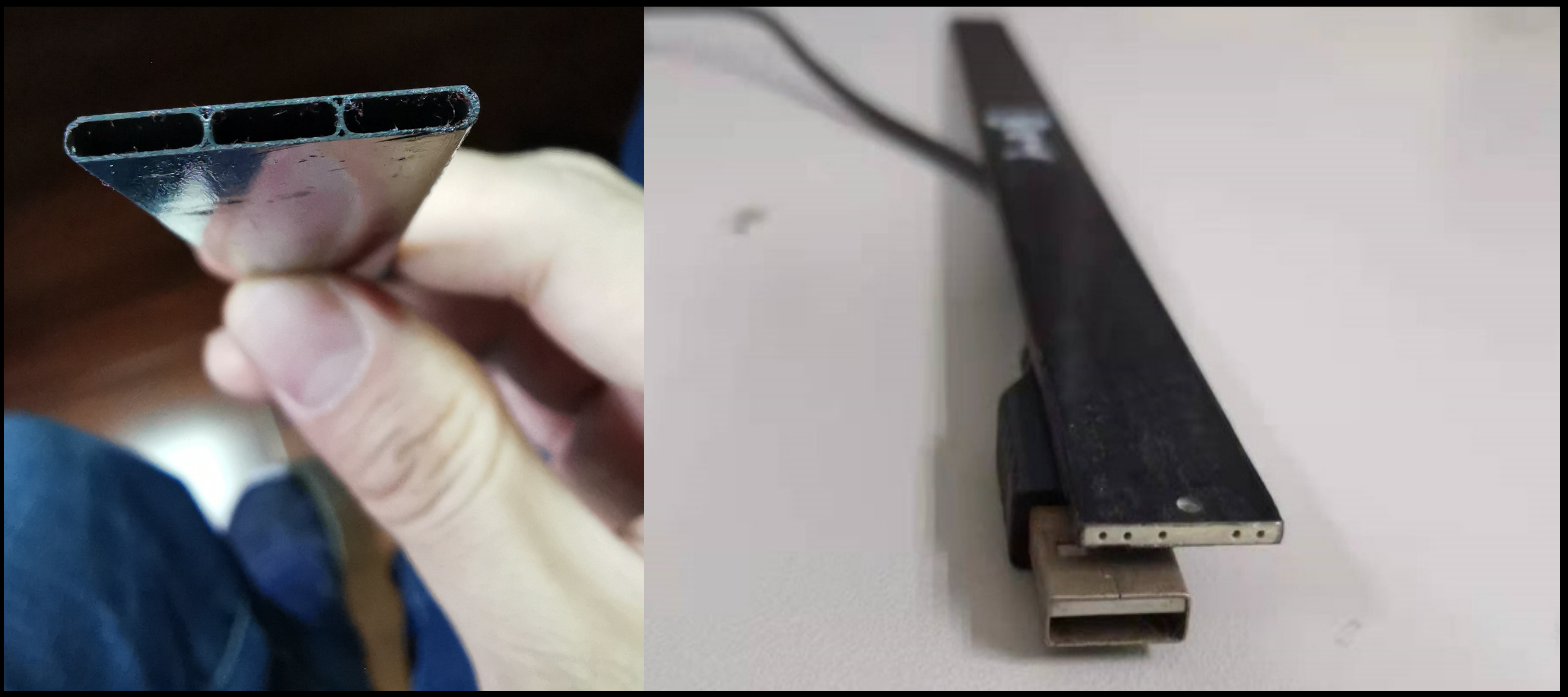
- The existing CMOS monolithic pixel sensors can’t fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - Radiation tolerance **(per year):** **>**1 Mrad
  - High readout speed -> for high luminosity CEPC Z pole running (40MHz)

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

Double-side ladder in CECP vertex detector

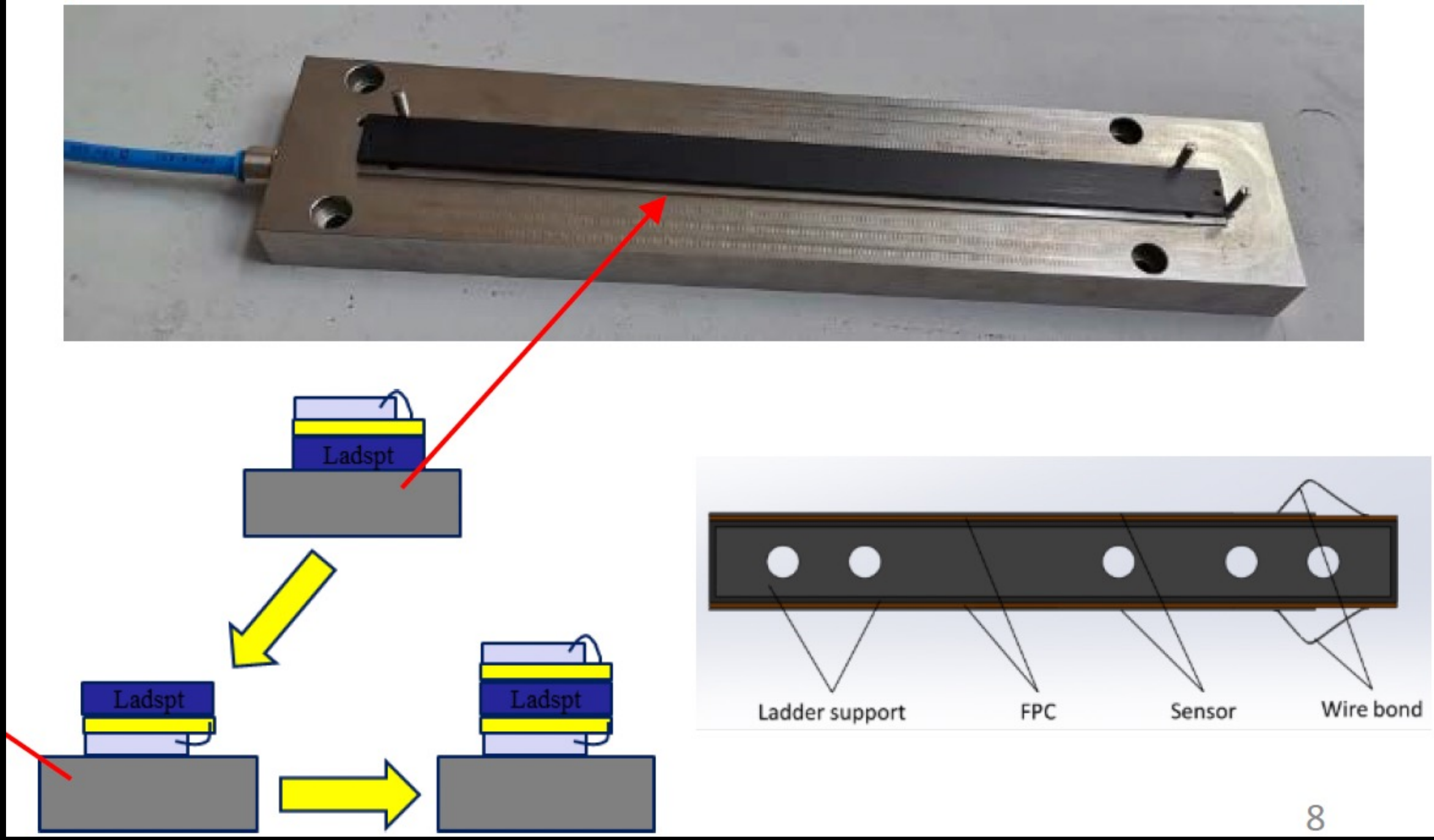
- Ladder in vertex detector is double-sided
  - Two flexible PCB + one carbon fiber support
- Both side has wire-bonding → Challenging
- Dedicated tooling for double-side assembly

Designed and fabricate carbon fiber support



Module fixation and protection components

Vacuum plate for flex and CFRP support fixation



Vertex detector: Physics goal

- Produce a world-class vertex detector prototype
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (>1 MRad)
- Physics motivation
  - Higgs precision measurement
  - $H \rightarrow bb$ precise vertex reconstruction
  - $H \rightarrow \mu\mu$ (precise momentum measurement)

Need tracking detector with high spatial resolution

- Main technology
  - Develop the know-how in China to build such detector
  - High spatial resolution technology $\rightarrow$ pixel detector
  - Radiation resistance technology