

### Timing Readout Electronics for T-SDHCAL

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饮水思源•爱国荣校



#### Introduction

- Design of the front-end board (FEB) prototype
- Timing performance evaluation
- Double-FEB setup for mRPC cosmic ray test
- DAQ development
- Conclusion

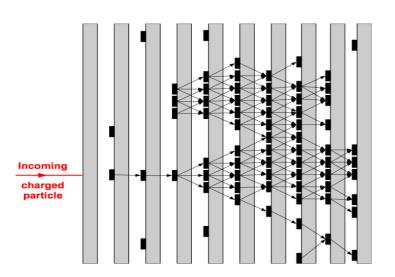
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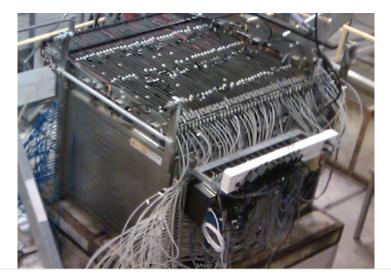




SDHCAL is one of the high granularity PFA (Particle Flow Algorithm) calorimeters

- Connect first hits and then their clusters using distance and orientation information
- The energy information helps to optimize the connections of hits belongs to the same shower.
- A SDHCAL prototype built based on Glass RPC
  - >48 layers with GRPC as sensitive medium
- Semi-digital readout (HARDROC): hits associated to three different thresholds (2-bit)
  - Ist threshold = 110fC
  - > 2nd threshold = 5pC
  - > 3rd threshold = 15pC





SDHCAL prototype at testbeam in 2015



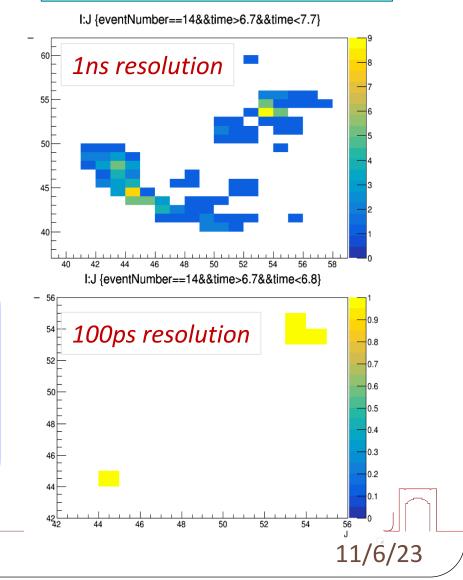
# Timing Electronics

- Timing information can be very helpful to separate close-by showers and reduce the confusion for a better PFA application.
- Method: Adding some mRPC layers in the SDHCAL
- Front-End Electronics for mRPC readout
   High resolution timing measurement



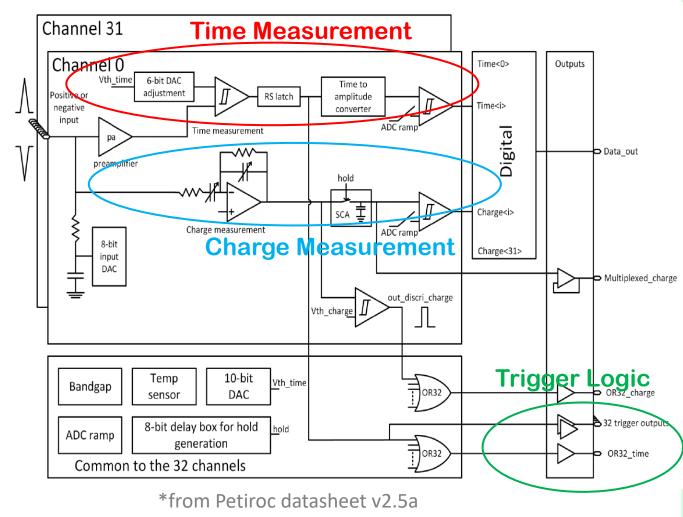
- Time measurement with 10 bits TDC interpolating 40MHz clock
- ≻ Timing resolution below 100 ps
- ➤ 32 input channels
- ➢ Power consumption: ∼6mW/channel

Example: Pi-(20 GeV), K-(10 GeV) separated by 15 cm





Petiroc2B ASIC



- ➤ A 32-channel front-end ASIC designed for SiPMs readout (mRPCs as well).
- Charge and timing measurement
- ➤ 40 ps bin size of on-chip TDC
- Readout time: 12us
- Fast trigger line output
- Dynamic Range 0-480 pC i.e. 3000
  - photoelectrons @ 10^6 SiPM gain
- Fast fixed gain (40) inverting voltage preamplifier
- Slow shaper with adjustable shaping time from 25 to 100 ns
- Charge measurements by Track&Hold

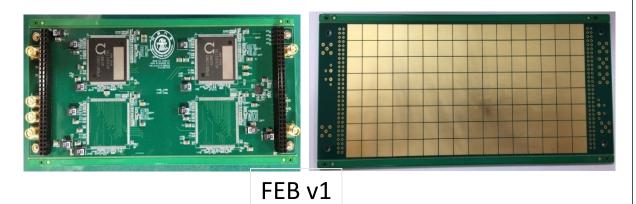
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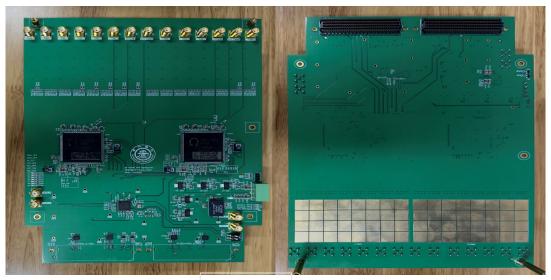
Power consumption 6mW/channel



### Front-end Board (FEB)

- A small FEB prototype
  - Timing performance validation
  - Readout scheme with mRPC detectors
- 2<sup>nd</sup>-version of FEB has been designed and fabricated
  - 2 Petirocs on-board
  - On-board power rails
  - ≻64-channel input pads
  - SMAs to inject signals
  - Crosstalk issue in injection test has been fixed





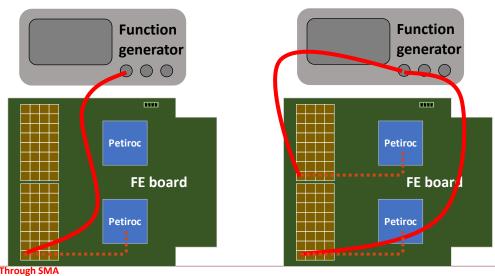
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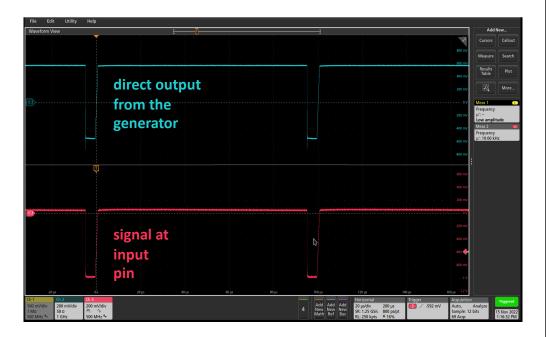
FEB v2



#### **Injected Test**

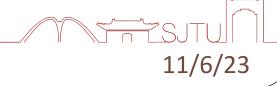
- Injection Test has been performed and verified.
- Timing performance has been evaluated based injection test
  - Setup 1: inject periodic signals to one channel, then measure the timing information between neighbor hits
  - Setup 2: inject signals to two channels, then measure the timing output of two chips





#### Signal profile:

- Negative pulse
- ➢ freq: 10kHz (period of 100  $\mu$ s) or 25kHz (period of 40 $\mu$ s)
- 20mV amplitude
- leading of 1us, trailing of 2ns



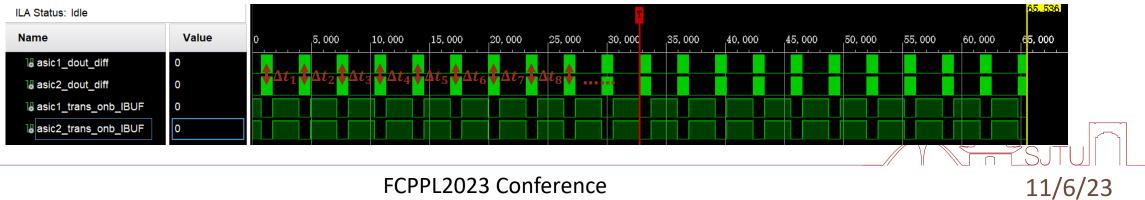
### **Timing Performance Tests**

- > Timing tests of a single input channel, with periodic injections
  - If Petiroc2B works properly, every two neighbor hits output should have the same time gap. Analyzing the time gaps can get us the timing performance.

ILA Status: Idle			$\Lambda t_{\star}$ $\Lambda t_{\star}$	At.	$\Lambda t$ , $\Lambda t_{-}$	$\Lambda t_{\star} = \Lambda t_{\star}$	$t_{-} \Lambda t_{0}$	Т							65, 536
Name	Value	0	5, 000	10,000	15, 000	20,000	25, 000	30, 000	35, 000	40, 000	45, 000	50, 000	55, 000	60, 000	6 <mark>5, 000</mark>
🖁 asic1_dout_diff	0														
🖁 asic2_dout_diff	0														
₿ asic1_trans_onb_IBUF	1														T.
lasic2_trans_onb_IBUF	0														

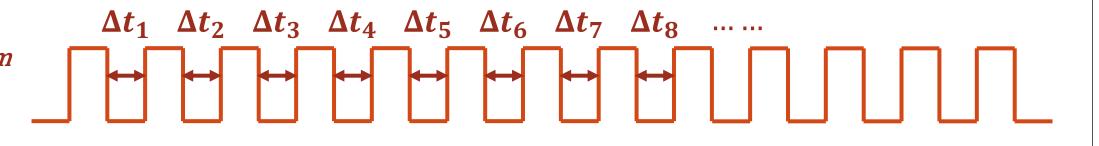
Timing tests of two clock-synchronized chips

> For the same single hit, the time gap between the two chips' output should be constant.



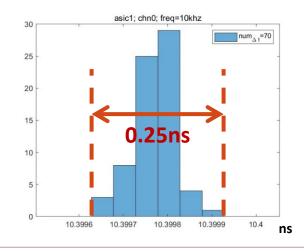
## Timing between Neighbor Hits

*Signal from ASIC 1* 



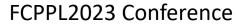
- > Inject signal into one chip.
- ➤ Calculate the timing differences (Δt) between every two neighbor hits.
- $\succ$  Check if  $\Delta t$  is consistent.

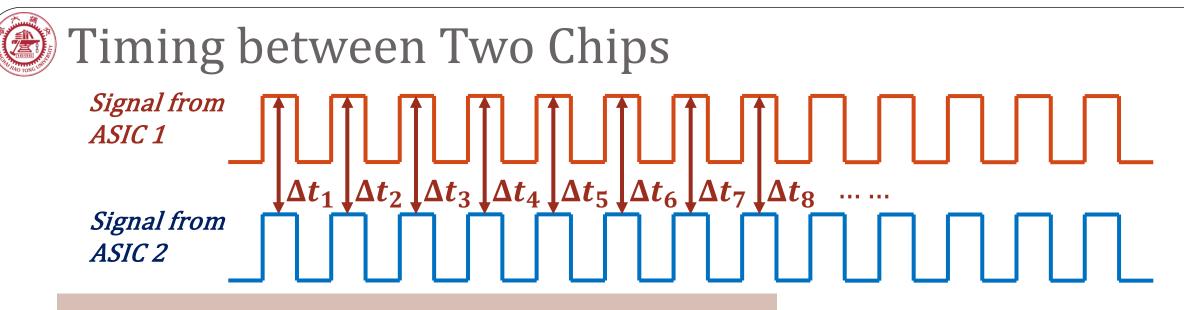
Results: ✓ The std of **Δt** is 45.8ps ✓ **Δt** is consistent





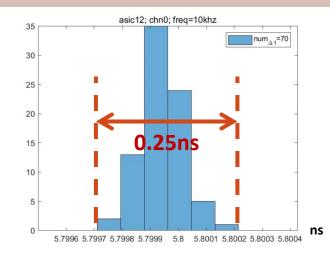
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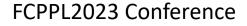
- > Inject the same signal into two chips (with a double-pass).
- $\succ$  Calculate the  $\Delta t$  between two Petiroc2B chips of each hit.
- $\succ$  Check if  $\Delta t$  is consistent.

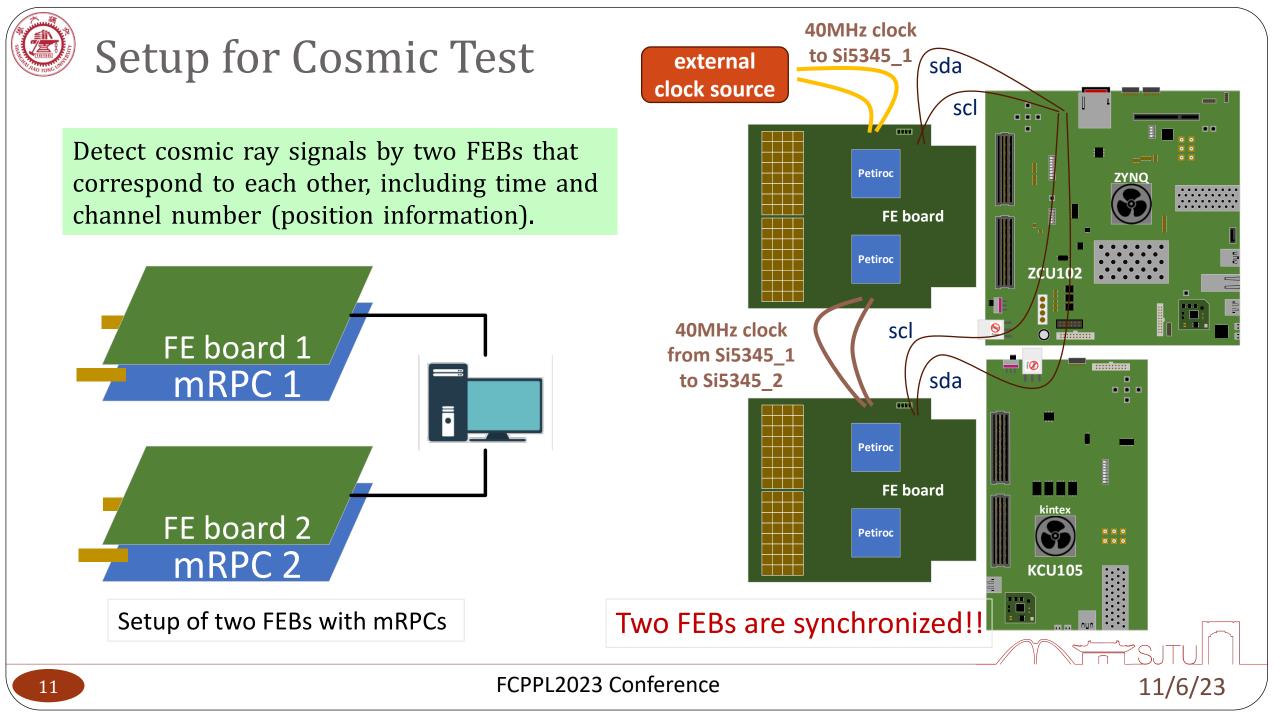
Results: ✓ The std of Δt is 53.6ps ✓ Δt is consistent



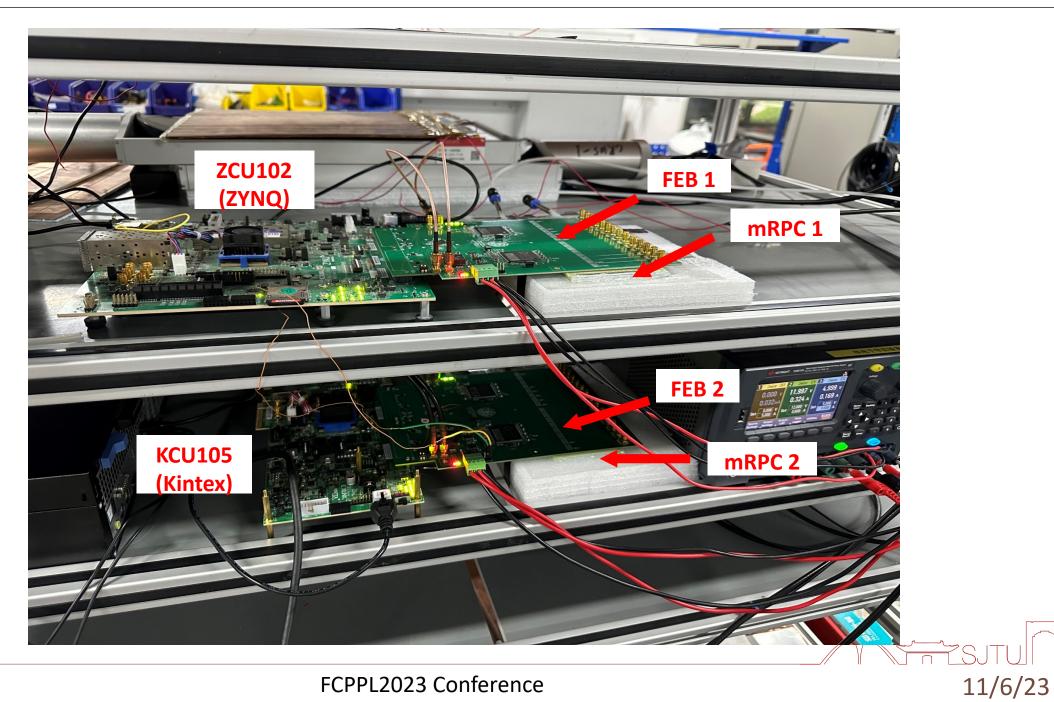


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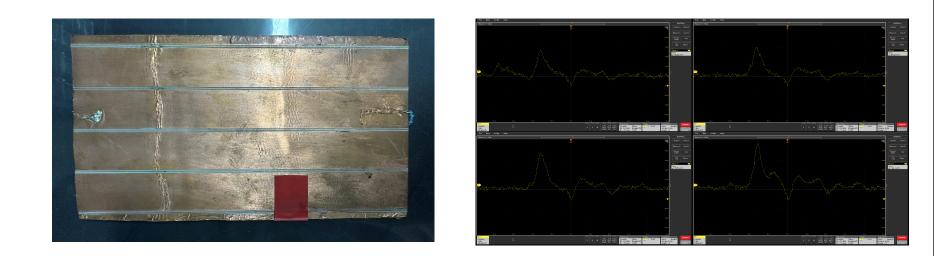


#### mRPC Test

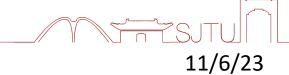


mRPC detector

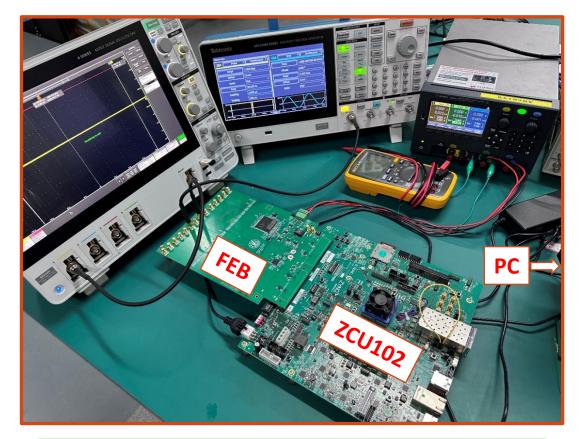
- > The test conditions are:
  - ➤ voltage: 7500V
  - ▶ gas: 10% C4H10, 12% SF6, 18.9% F134a



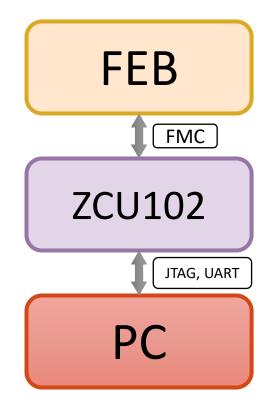
- Preliminary Test
- Use a readout pad with copper strips, and observe the signal from an oscilloscope
- > Can capture something, but probably noises only.
- Still working on the mRPC test, with our colleagues' help



# DAQ Development for FEB Prototype

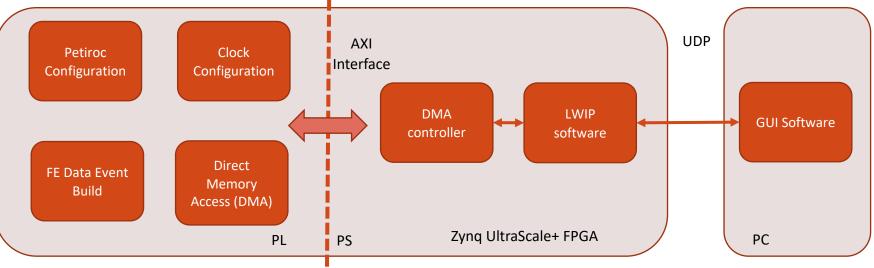


#### Xilinx ZCU102, with Zynq UltraScale+<sup>™</sup> MPSoC





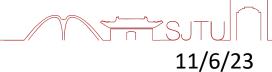
# DAQ Development for FEB Prototype



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(2)本地IP地址	37 33 36 30 37 33 33 66 63 37 30 33 37 38 37 37 33 66 38 37 36		9467 1139,663585 192,16		2.168.1.100	UDP	286 62510 + 5001 Len=244		
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✔ 十六进制显示	37 33 36 30 37 33 33 66 63 37 30 33 37 38 37 37 33 66 38 37 36	33	9564 1150.453439 192.16		2.168.1.100	UDP	286 62510 → 5001 Len=244		
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保存数据 清除显示	33 66 63 37 66 33 66 63 37 33 37 66 64 64 66 37 66 64 66 66 37		9584 1153.692142 192.16 9593 1154.770257 192.16		2.168.1.100	UDP	286 62510 → 5001 Len=244 286 62510 → 5001 Len=244		
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		54	9620 1159.082801 192.10		2.168.1.100	UDP	286 62510 → 5001 Len=244		
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按十六进制发送		~					its) on interface \Device\NPF_{	FB78D9BD-D56D-47B1-B462-A08AD	DEF72F15}, 1d
			> Ethernet II, Src: Xilinx_0 > Internet Protocol Version +				t:/2 (d0:8e:/9:10:8t:/2)		
数据流循环发送	目标主机: 192.168.1.10 目标端口: 62510		<ul> <li>Internet Protocol Version 4</li> <li>User Datagram Protocol, Sri</li> </ul>			8.1.100			
发送间隔 1000 毫秒		_	<ul> <li>User Datagram Protocol, Sri</li> <li>Data (244 bytes)</li> </ul>	. POPC: 62510, DS	. POPC: 5001				
aliziani 1000 jiziy	http://www.cmsoft.cm.QQ:10865600		<ul> <li>Data (244 bytes)</li> <li>Data: ffffffff3132303363</li> </ul>	21262022252121242	2622122202222721	22242225222	12022642121		
文件载入 清除输入	X	8E	[Length: 244]	513636555555151545	303313336333731	333433333333	13833043131		
			[rengen: 244]						

#### Ethernet data test - read from DMA

- The event data is sent to PS memory by a DMA in PL (FPGA)
- The ethernet transfer function is realized through PS (ARM core) of ZYNQ, using LWIP protocol
- Counter data has been tested and verified

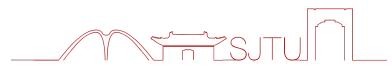


Main settings EN/PP Calibrat		pmenti	for FEB P	iototype
Mask disci charge         0         1         2         3         4         5	□ 8 □ 9 □ 10 □ 11 □ 12 □ 13	☐ 16 ☐ 17 ☐ 18 ☐ 19 ☐ 20 ☐ 21	24 25 26 27 28 29	
☐ 6 ☐ 7 Mask disci time	☐ 14 ☐ 15	22 23	30 31	The DAQ software is a Python GUI application.
□ 0 □ 1 □ 2 □ 3 □ 4 □ 5 □ 6 □ 7	8         9         10         11         12         13         14         15	☐ 16 ☐ 17 ☐ 18 ☐ 19 ☐ 20 ☐ 21 ☐ 22 ☐ 23	□ 24 □ 25 □ 26 □ 27 □ 28 □ 29 □ 30 □ 31	The GUI is designed via QT designer, which is set of cross- platform C++ libraries that implement high-level APIs.
ADC ramp compensation		Cin	Cf <ul> <li>100fF</li> <li>200fF</li> <li>300fF</li> <li>400fF</li> </ul>	PyQt5 modules binding with QT v5.
Polarity Negative ~	Z DAC delay 0	τ =25ns FCPF	τ =25ns PL2023 Conference	11/6/23

### Conclusion

- ◆ A FEB prototype based on Petiroc ASIC has been designed
- The timing performance of the FEB has been evaluated, which has a resolution better than 100*ps*.
- The commissioning test of the FEB and mRPC detectors is ongoing.
- A DAQ system based on Zynq FPGA and PyQT5, is being developed steadily.





#### Thank you for your attention

