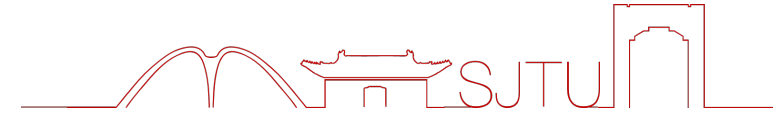




上海交通大学
SHANGHAI JIAO TONG UNIVERSITY



Timing Readout Electronics for T-SDHCAL



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On behalf of SJTU-IPNL Group



in collaboration with Imad Laktineh: Institut de Physique des 2 Infinis de Lyon

06/11/2023

饮水思源 · 爱国荣校



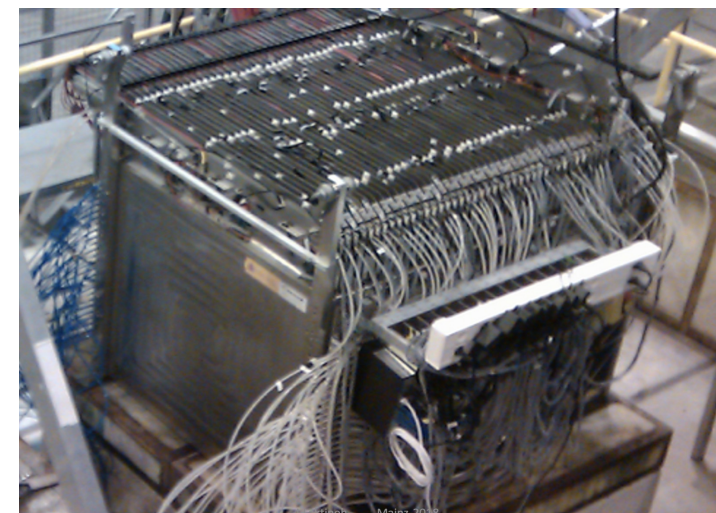
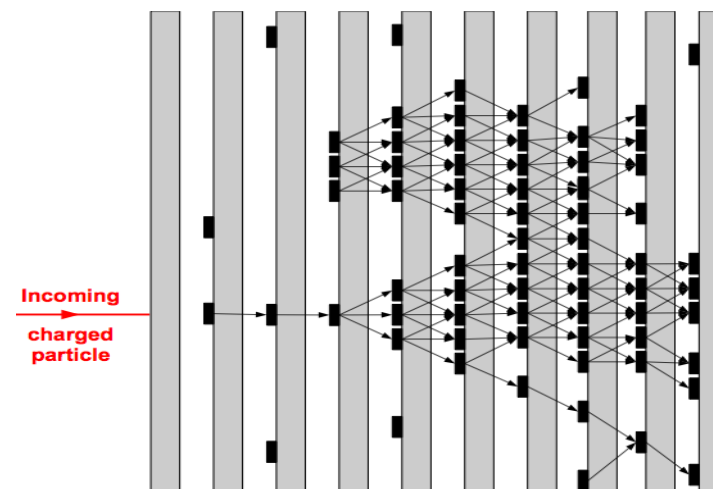
Outline

- Introduction
- Design of the front-end board (FEB) prototype
- Timing performance evaluation
- Double-FEB setup for mRPC cosmic ray test
- DAQ development
- Conclusion



Semi-Digital Hadronic CALorimeter

- SDHCAL is one of the high granularity PFA (Particle Flow Algorithm) calorimeters
 - Connect first hits and then their clusters using distance and orientation information
 - The energy information helps to optimize the connections of hits belongs to the same shower.
- A SDHCAL prototype built based on Glass RPC
 - 48 layers with GRPC as sensitive medium
- Semi-digital readout (HARDROC): hits associated to three different thresholds (2-bit)
 - 1st threshold = 110fC
 - 2nd threshold = 5pC
 - 3rd threshold = 15pC



SDHCAL prototype at testbeam in 2015



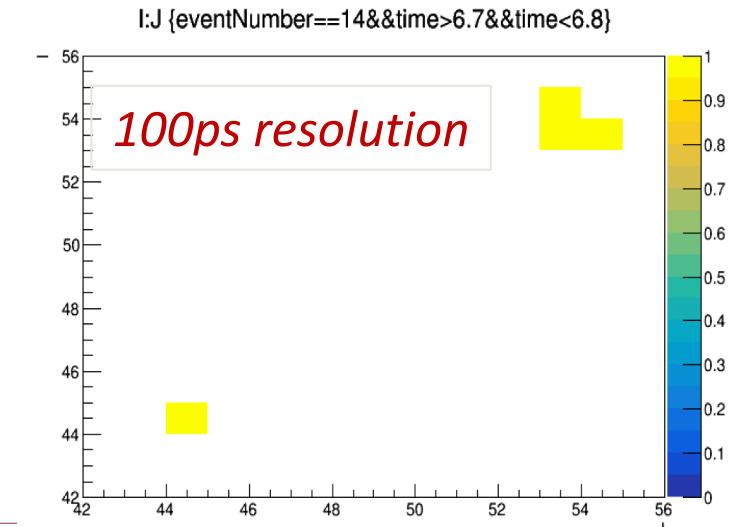
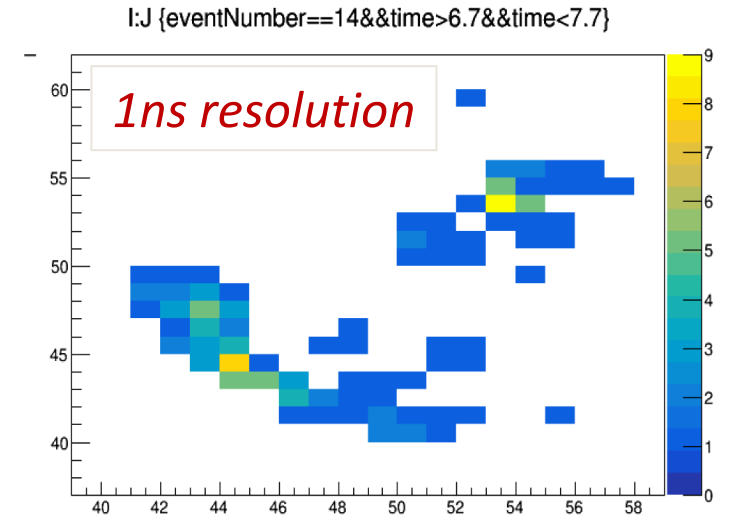
Timing Electronics

- Timing information can be very helpful to separate close-by showers and reduce the confusion for a better PFA application.
- Method: Adding some mRPC layers in the SDHCAL
- Front-End Electronics for mRPC readout
 - **High resolution timing measurement**



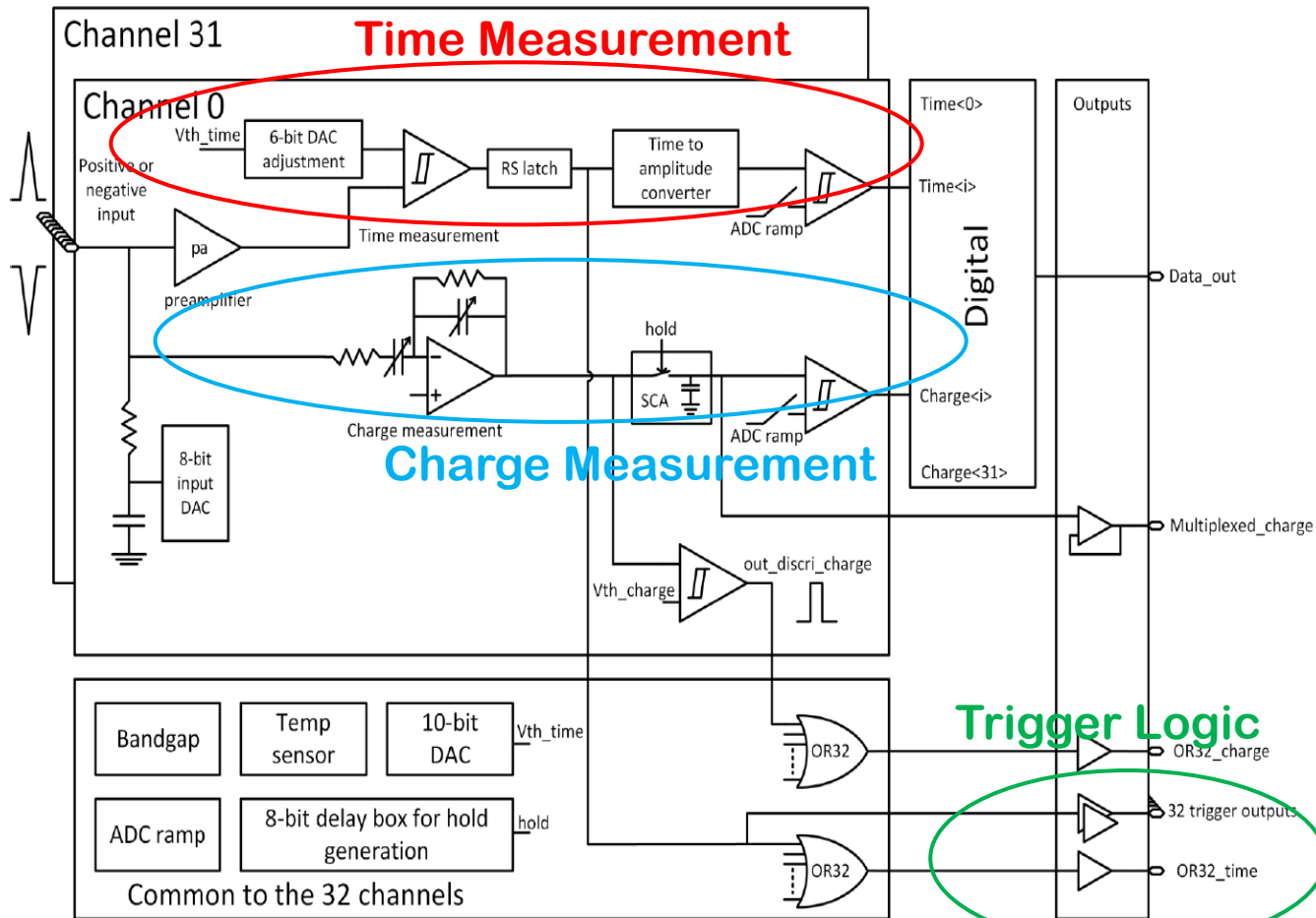
- Time measurement with 10 bits TDC interpolating 40MHz clock
- Timing resolution below 100 ps
- 32 input channels
- Power consumption: $\sim 6\text{mW}/\text{channel}$

Example: Pi-(20 GeV), K-(10 GeV) separated by 15 cm



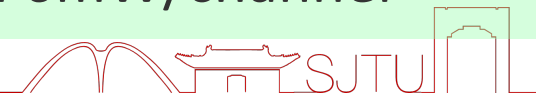


Petiroc2B ASIC



*from Petiroc datasheet v2.5a

- A 32-channel front-end ASIC designed for SiPMs readout (mRPCs as well).
- Charge and timing measurement
- 40 ps bin size of on-chip TDC
- Readout time: 12us
- Fast trigger line output
- Dynamic Range 0-480 pC i.e. 3000 photoelectrons @ 10^6 SiPM gain
- Fast fixed gain (40) inverting voltage preamplifier
- Slow shaper with adjustable shaping time from 25 to 100 ns
- Charge measurements by Track&Hold
- Power consumption 6mW/channel



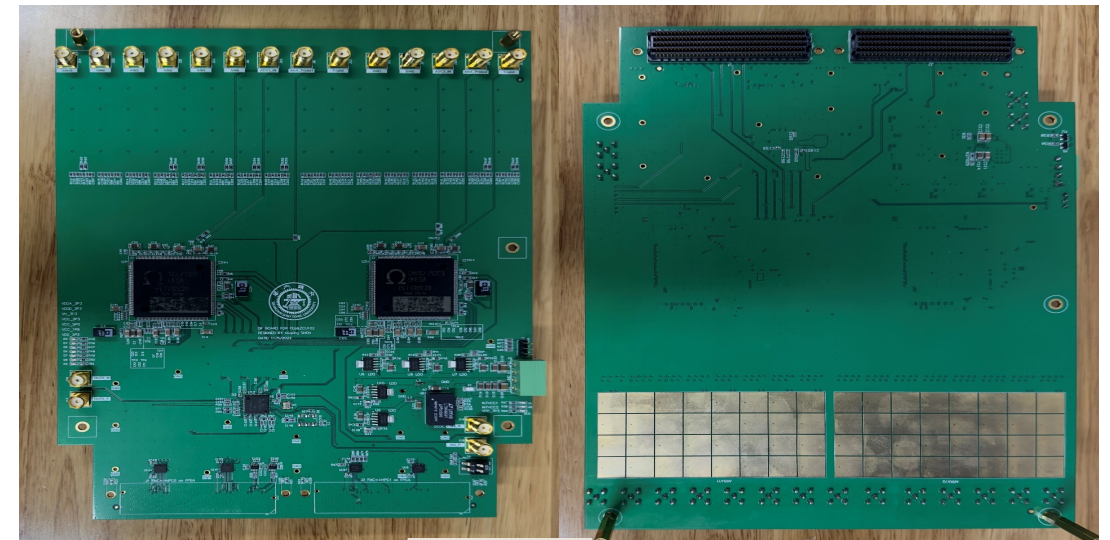
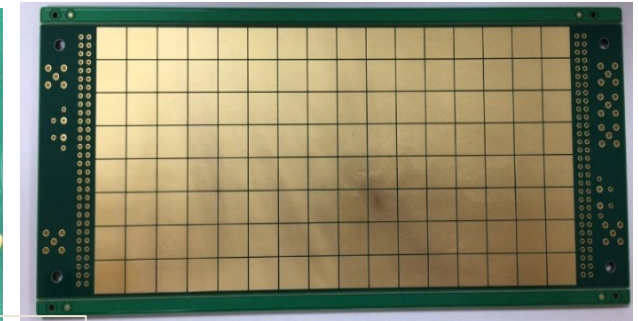


Front-end Board (FEB)

- A small FEB prototype
 - Timing performance validation
 - Readout scheme with mRPC detectors
- 2nd-version of FEB has been designed and fabricated
 - 2 Petirocs on-board
 - On-board power rails
 - 64-channel input pads
 - SMAs to inject signals
 - **Crosstalk issue in injection test has been fixed**



FEB v1



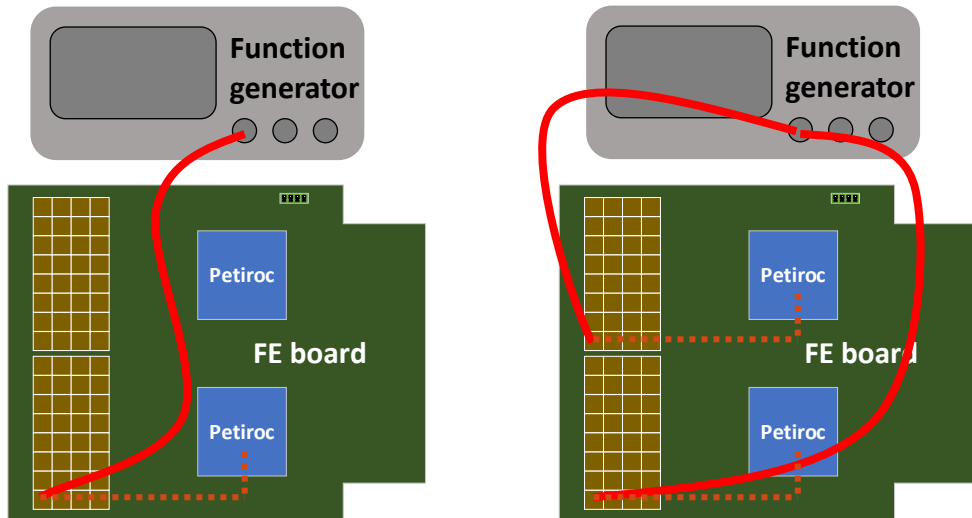
FEB v2



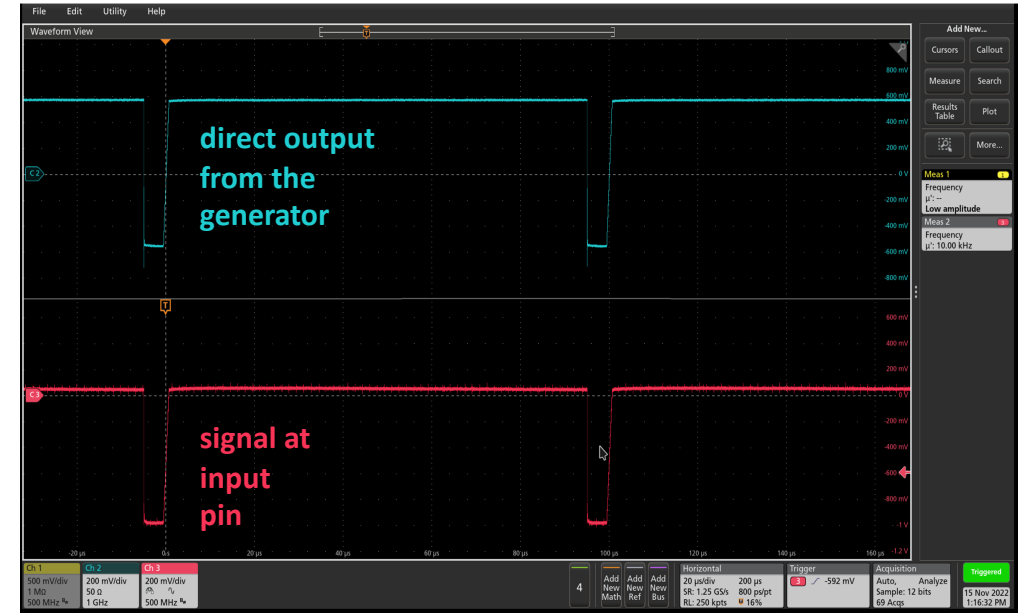
Injected Test

- Injection Test has been performed and verified.
- Timing performance has been evaluated based injection test

- Setup 1: inject periodic signals to one channel, then measure the timing information between neighbor hits
- Setup 2: inject signals to two channels, then measure the timing output of two chips

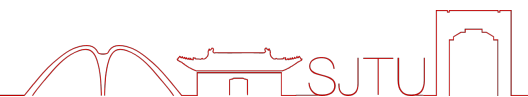


Through SMA



Signal profile:

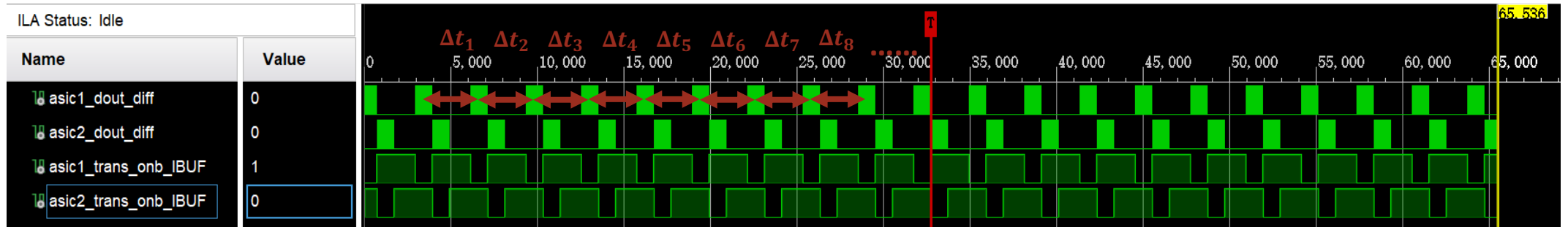
- Negative pulse
- *freq*: 10kHz (period of 100 μ s) or 25kHz (period of 40 μ s)
- 20mV amplitude
- leading of 1us, trailing of 2ns



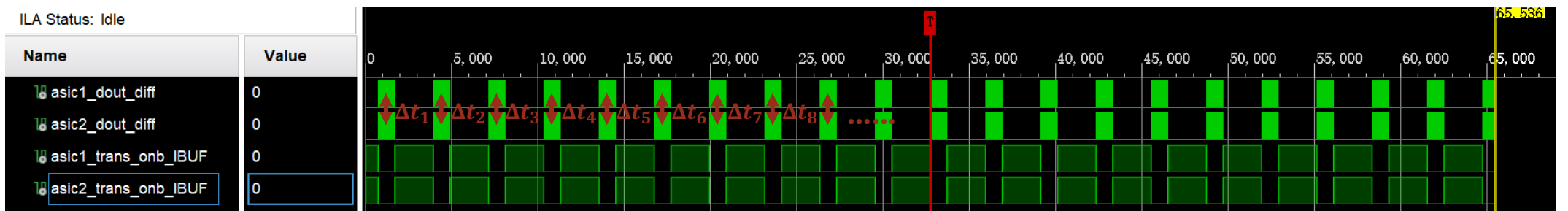


Timing Performance Tests

- Timing tests of a single input channel, with periodic injections
 - If Petiroc2B works properly, **every two neighbor hits output should have the same time gap**. Analyzing the time gaps can get us the timing performance.



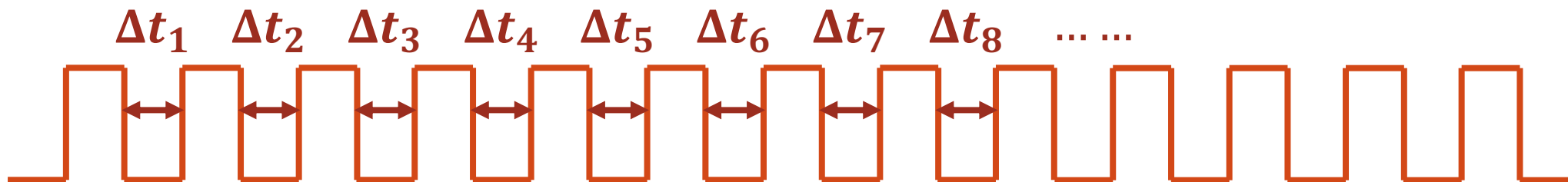
- Timing tests of **two clock-synchronized chips**
 - For the same single hit, **the time gap between the two chips' output should be constant**.





Timing between Neighbor Hits

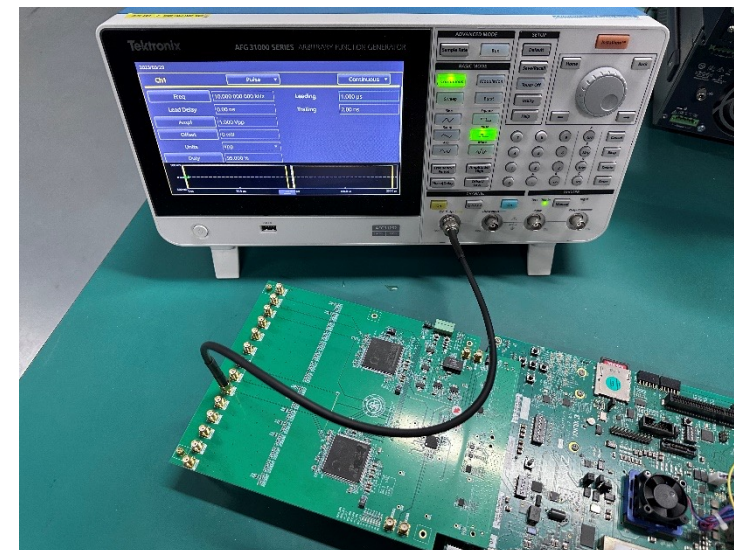
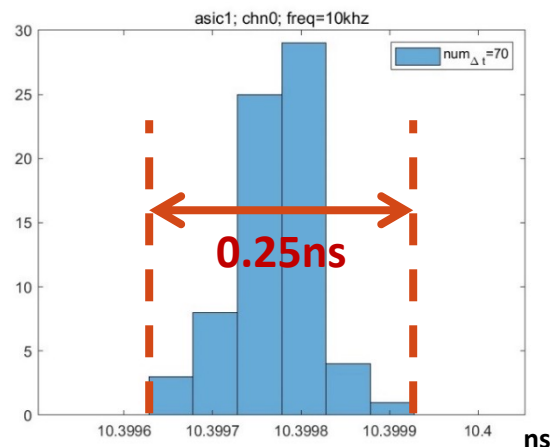
Signal from ASIC 1



- Inject signal into one chip.
- Calculate the timing differences (Δt) between every two neighbor hits.
- Check if Δt is consistent.

Results:

- ✓ The std of Δt is 45.8ps
- ✓ Δt is consistent



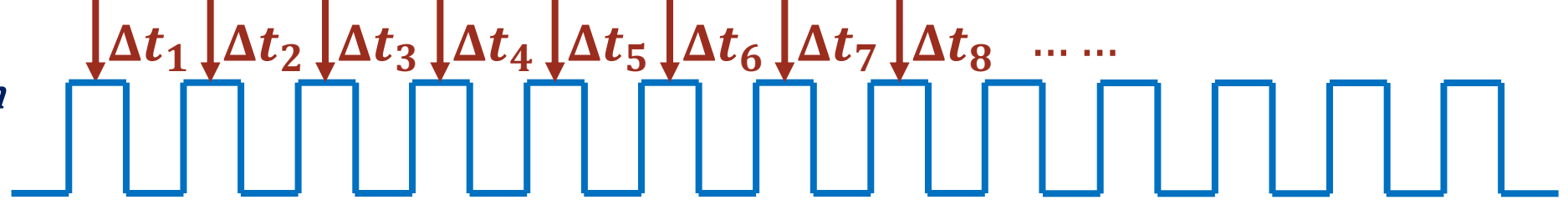


Timing between Two Chips

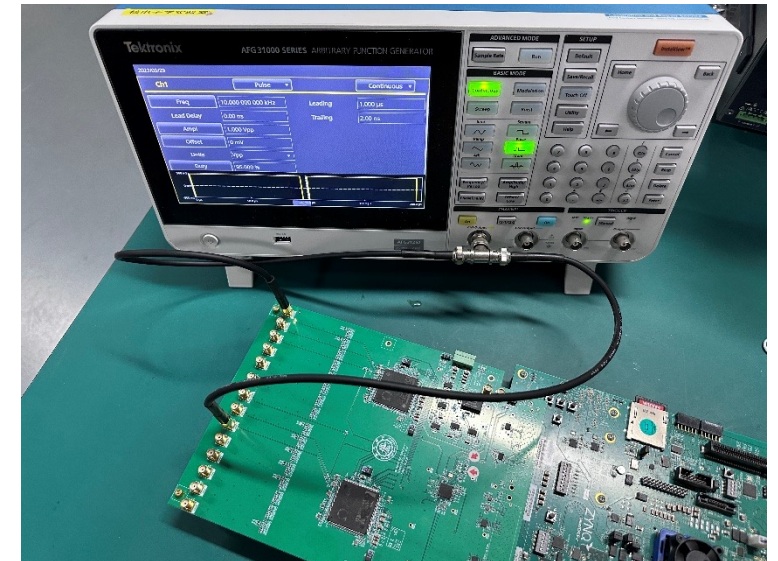
Signal from ASIC 1



Signal from ASIC 2

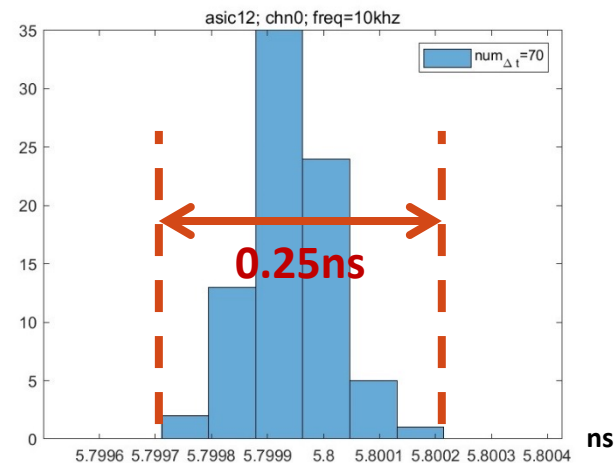


- Inject the same signal into two chips (with a double-pass).
- Calculate the Δt between two Petiroc2B chips of each hit.
- Check if Δt is consistent.



Results:

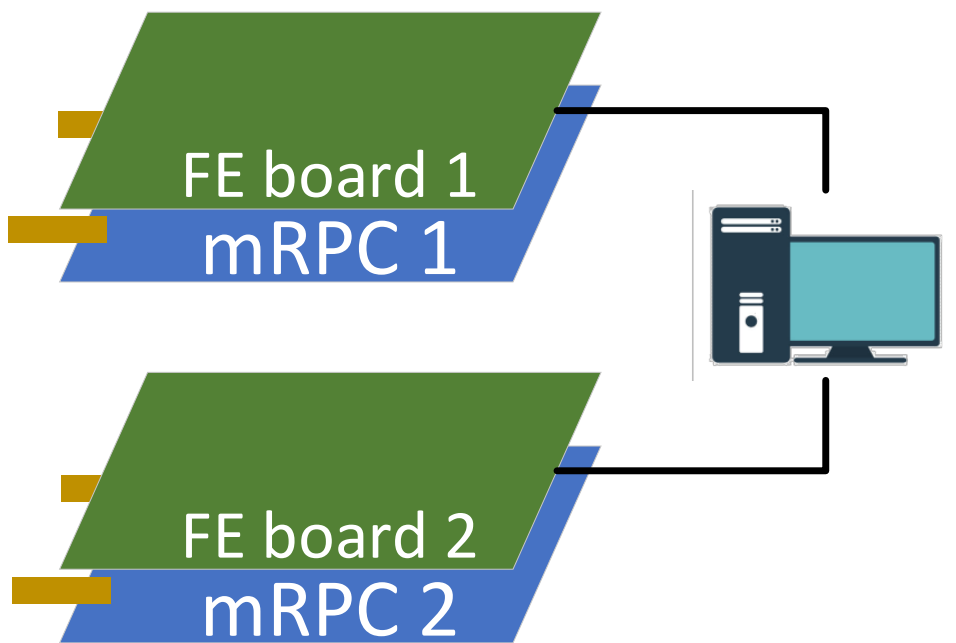
- ✓ The std of Δt is 53.6ps
- ✓ Δt is consistent



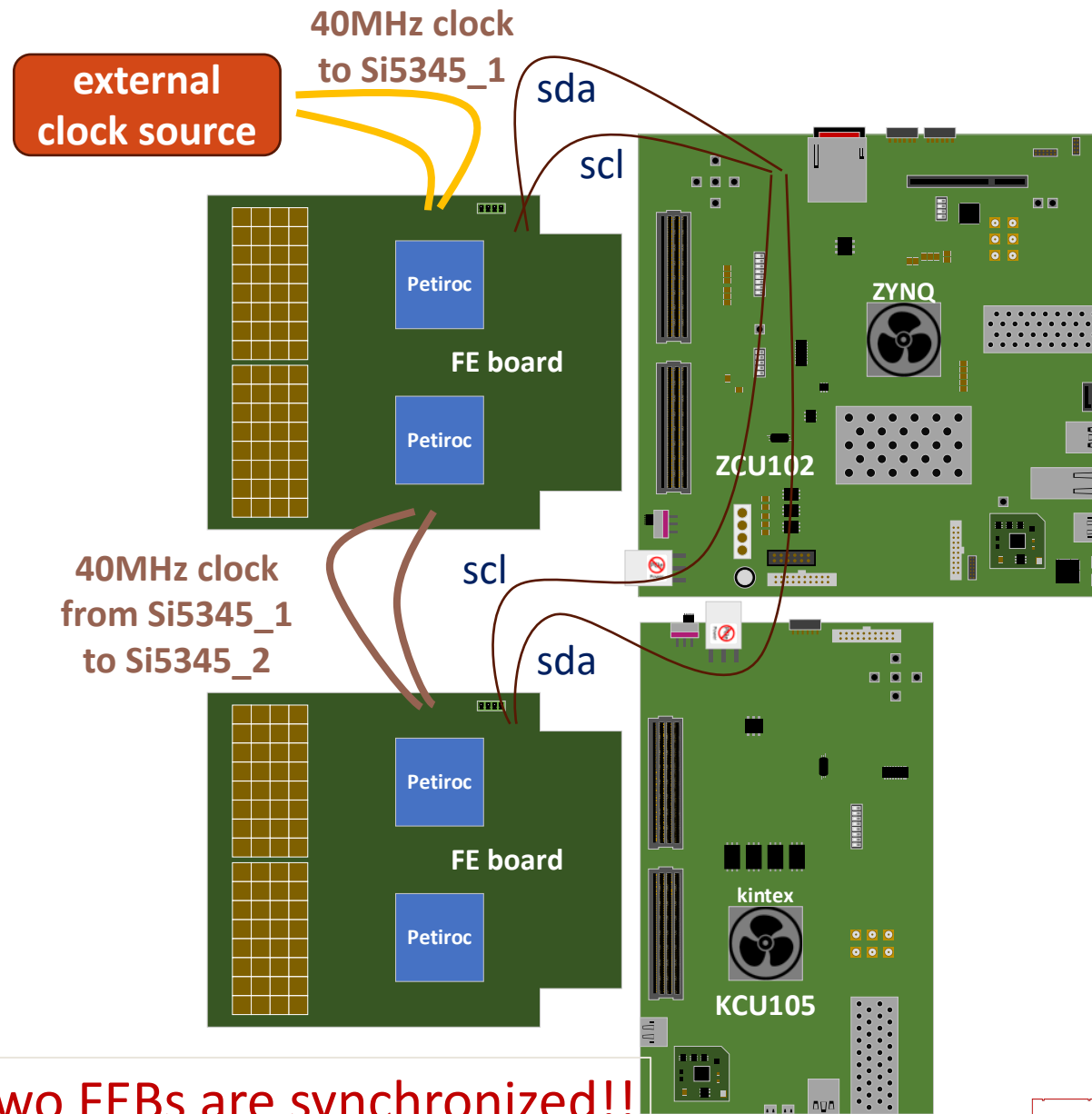


Setup for Cosmic Test

Detect cosmic ray signals by two FEBs that correspond to each other, including time and channel number (position information).

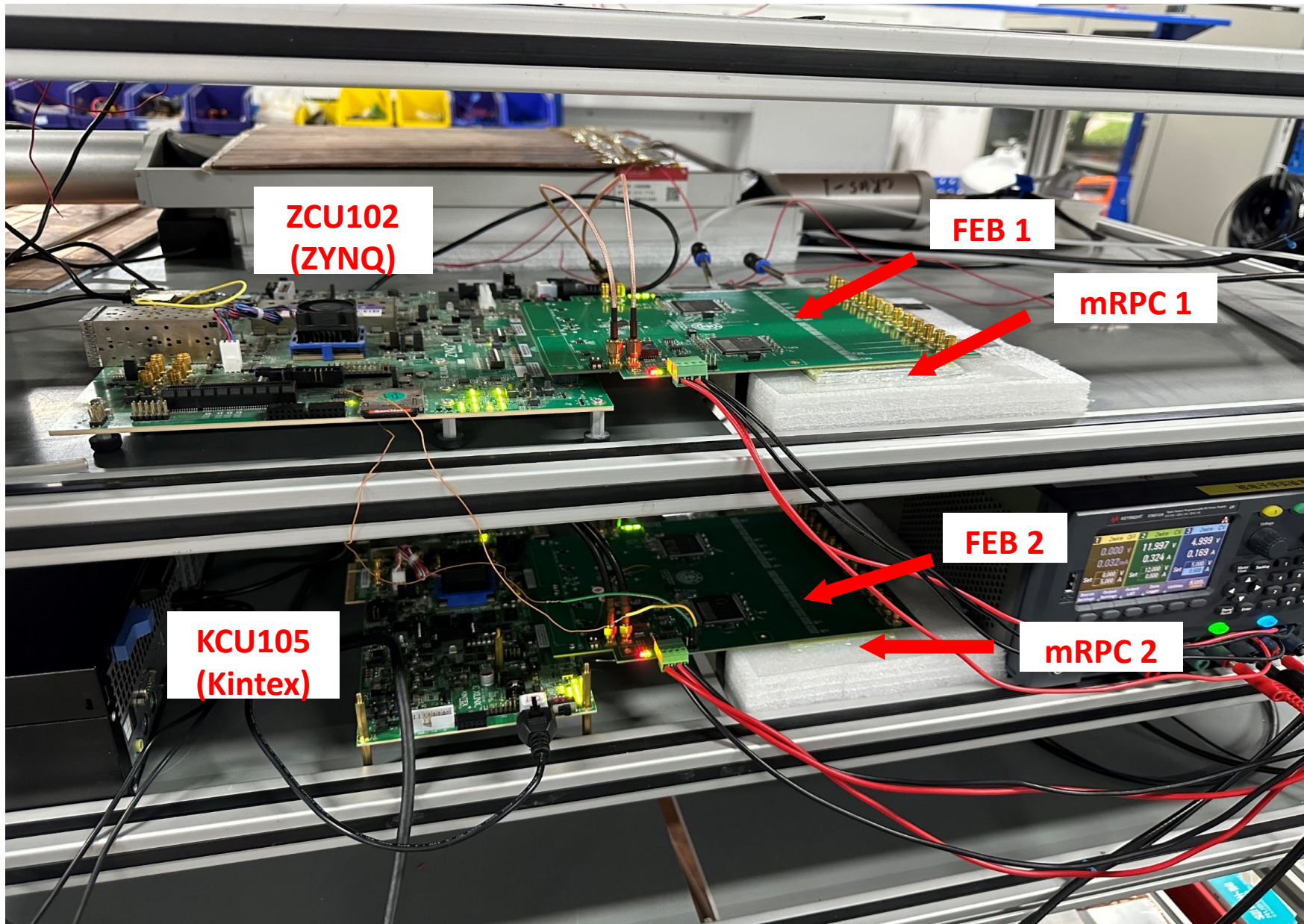


Setup of two FEBs with mRPCs



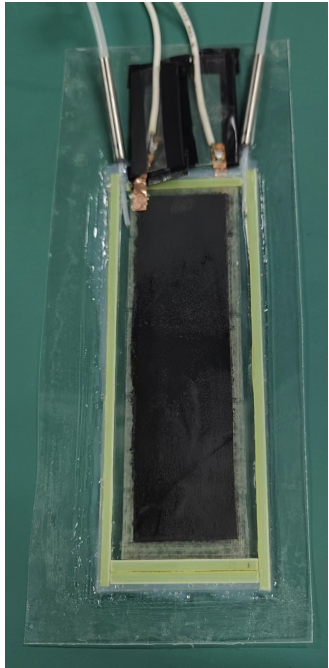
Two FEBs are synchronized!!



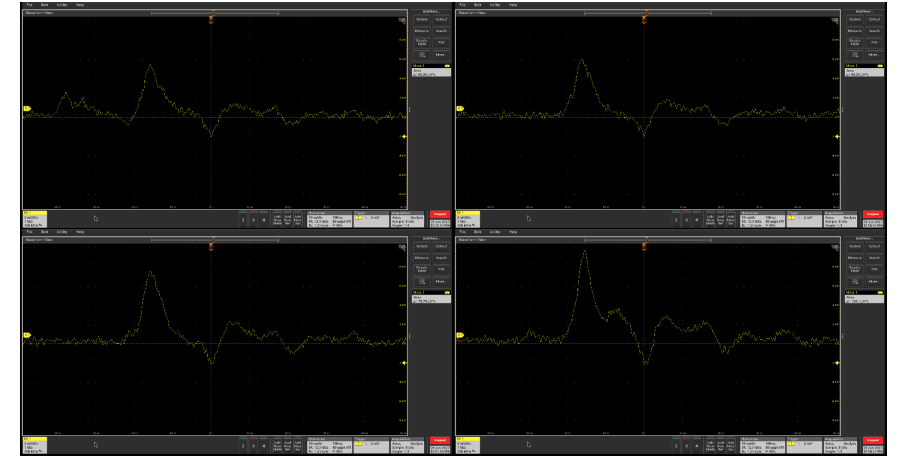
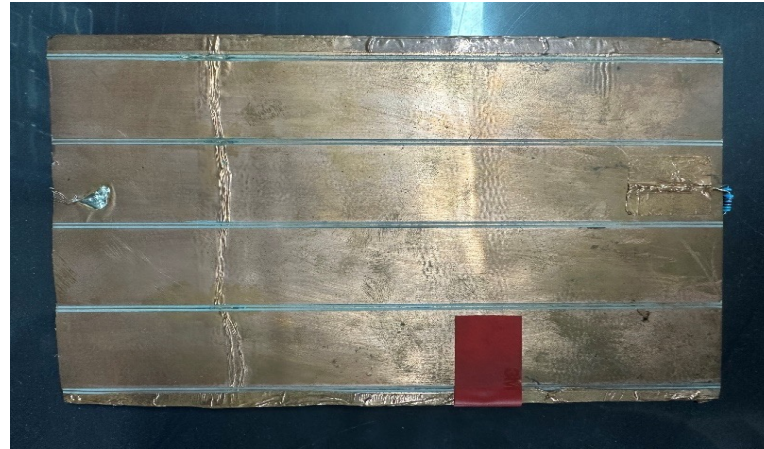




mRPC Test



mRPC detector



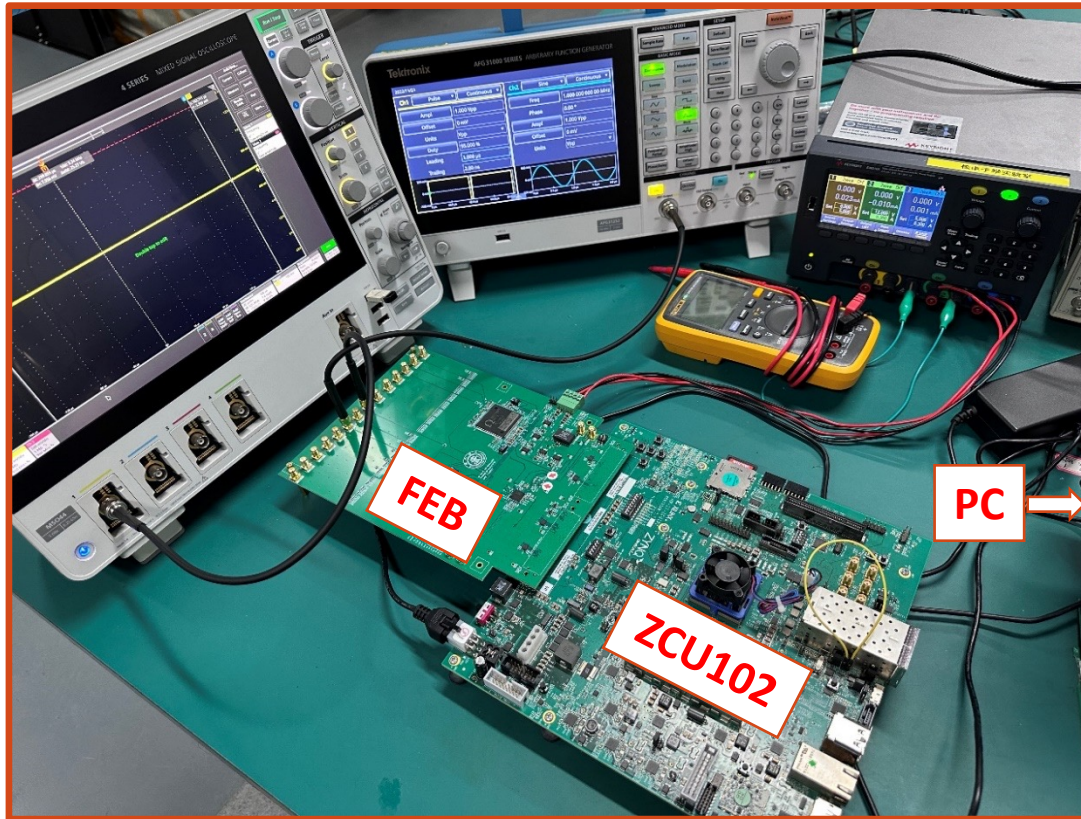
➤ The test conditions are:

- voltage: 7500V
- gas: 10% C₄H₁₀, 12% SF₆, 18.9% F134a

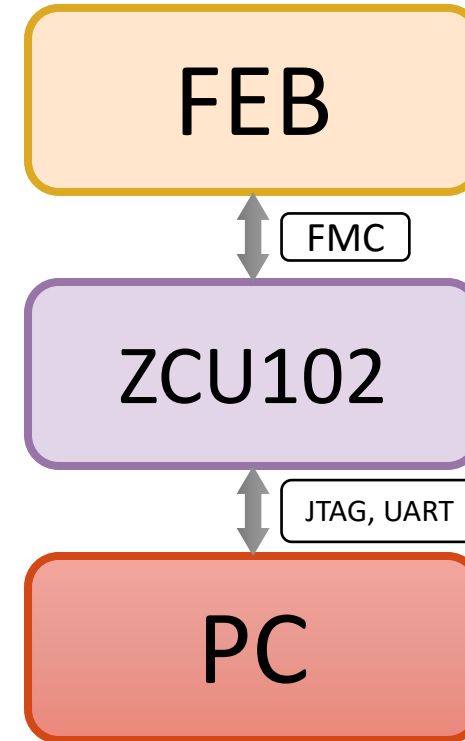
- Preliminary Test
- Use a readout pad with copper strips, and observe the signal from an oscilloscope
- Can capture something, but probably noises only.
- Still working on the mRPC test, with our colleagues' help



DAQ Development for FEB Prototype

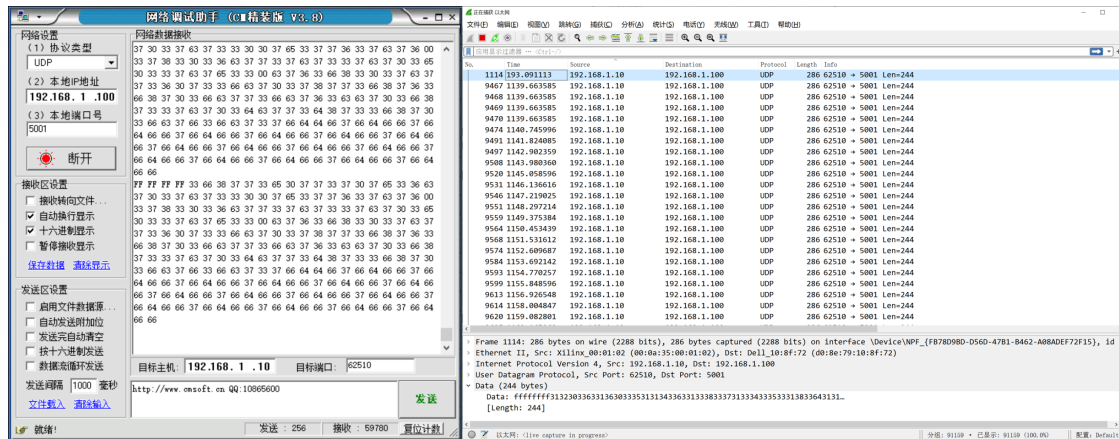
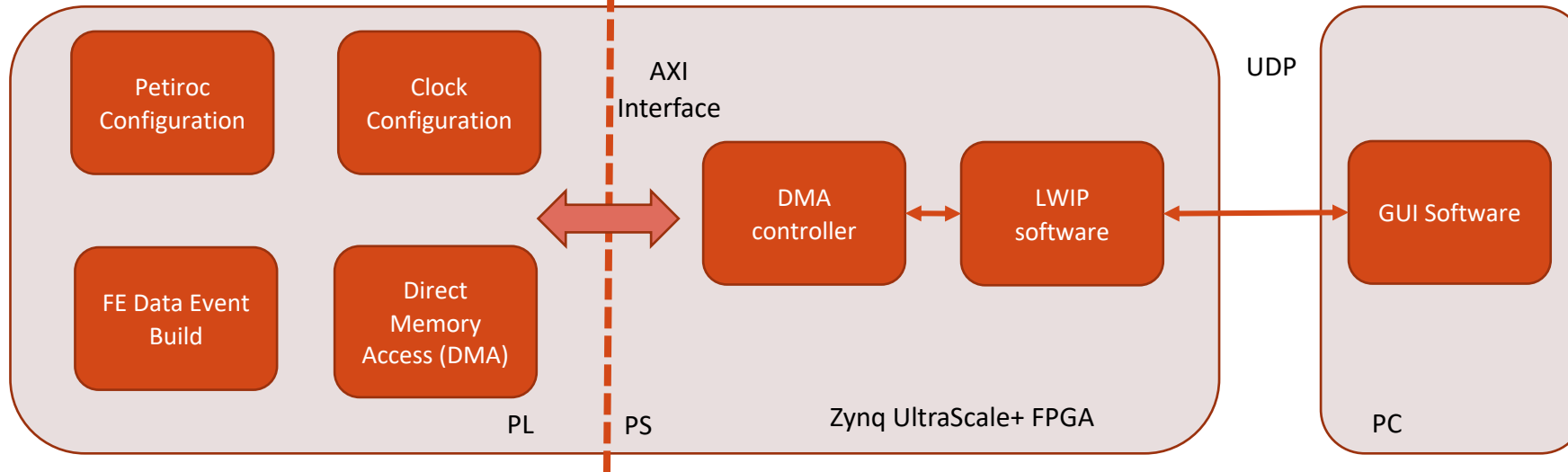


Xilinx ZCU102, with Zynq UltraScale+™ MPSoC





DAQ Development for FEB Prototype



- The event data is sent to PS memory by a DMA in PL (FPGA)
- The ethernet transfer function is realized through PS (ARM core) of ZYNQ, using LWIP protocol
- Counter data has been tested and verified

Ethernet data test - read from DMA

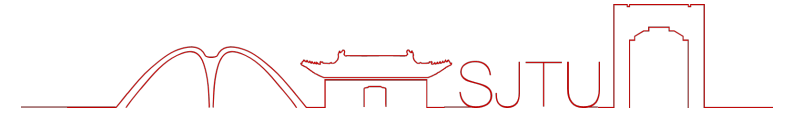


Conclusion

- ◆ A FEB prototype based on Petiroc ASIC has been designed
- ◆ The timing performance of the FEB has been evaluated, which has a resolution better than $100ps$.
- ◆ The commissioning test of the FEB and mRPC detectors is ongoing.
- ◆ A DAQ system based on Zynq FPGA and PyQT5, is being developed steadily.



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Thank you for your attention

Q&A

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