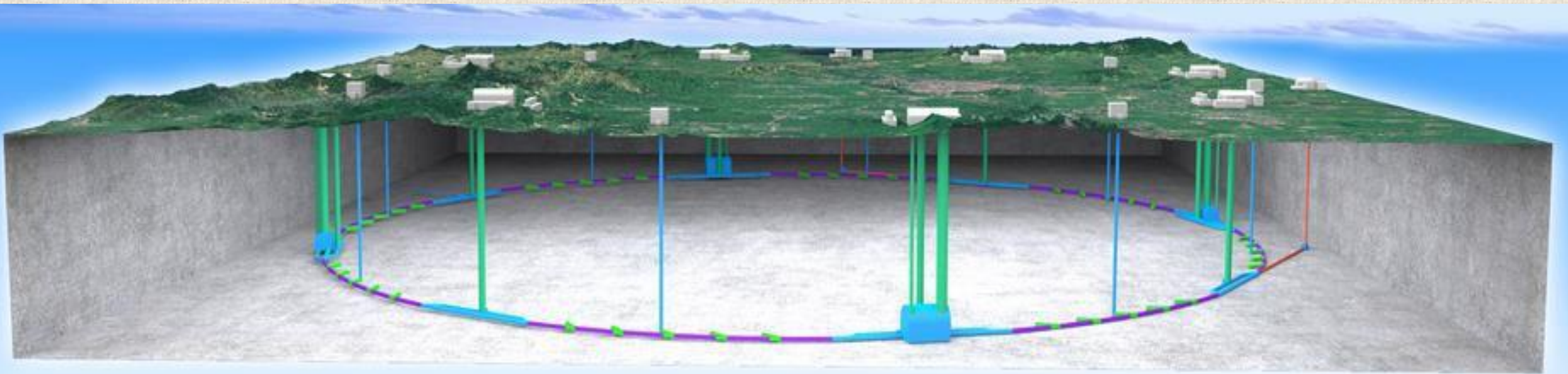


Towards TDR of a Reference Detector for CEPC

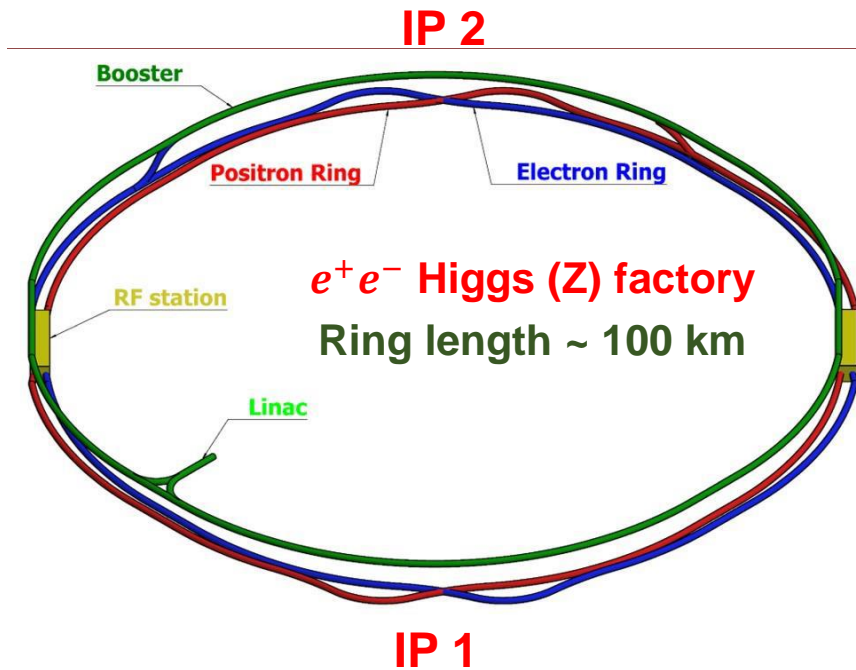
Jianchun Wang
IHEP

14th Workshop of the France China Particle Physics Laboratory
Nov 6-10, 2023, SYSU Zhuhai Campus





- ❑ The CEPC was proposed in 2012 right after the Higgs discovery. It aims to start operation in 2030s, as an e^+e^- Higgs / Z factory.
- ❑ To produce Higgs / W / Z / top for high precision Higgs, EW measurements, studies of flavor physics & QCD, and probes of physics BSM.
- ❑ It is possible to upgrade to a pp collider (SppC) of $\sqrt{s} \sim 100$ TeV in the future.

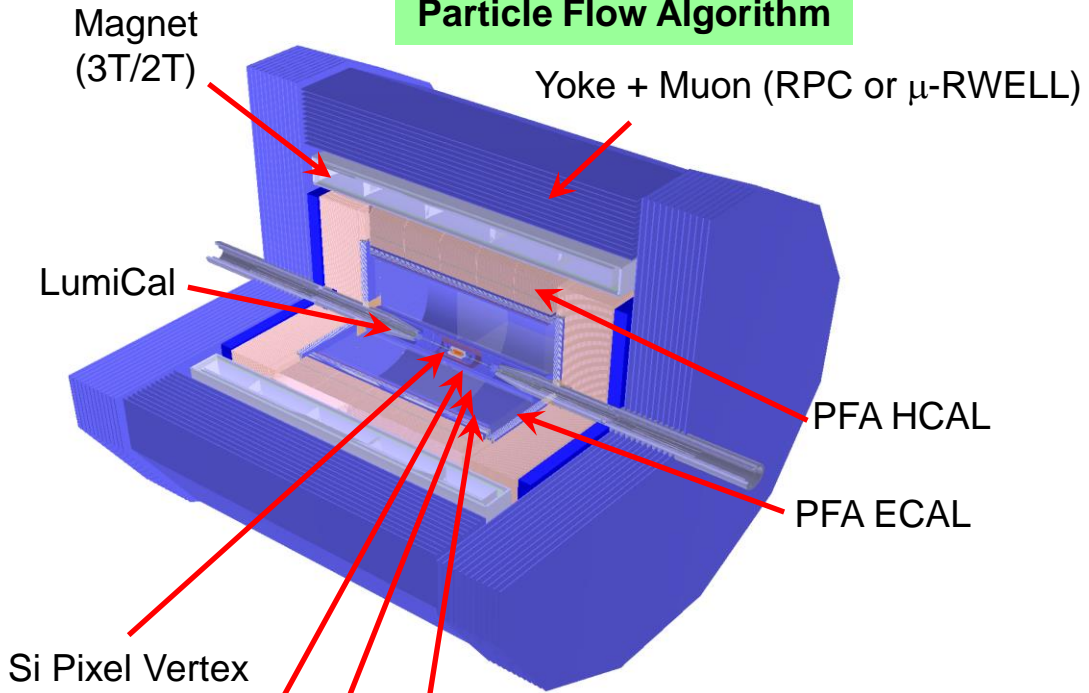


Operation mode		ZH	Z	W+W-	$t\bar{t}$	
\sqrt{s} [GeV]		~240	~91.2	~160	~360	
Run time [years]		7	2	1	-	
CDR (30 MW)	$L / IP [\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}]$	3	32	10	-	
	$\int L dt [\text{ab}^{-1}, 2 \text{ IPs}]$	5.6	16	2.6	-	
	Event yields [2 IPs]	1×10^6	7×10^{11}	2×10^7	-	
Run Time [years]		10	2	1	~5	
Latest	30 MW	$L / IP [\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}]$	5.0	115	16	0.5
	50 MW	$L / IP [\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}]$	8.3	191.7	26.6	0.8
		$\int L dt [\text{ab}^{-1}, 2 \text{ IPs}]$	20	96	7	1
		Event yields [2 IPs]	4×10^6	4×10^{12}	2×10^7	5×10^5

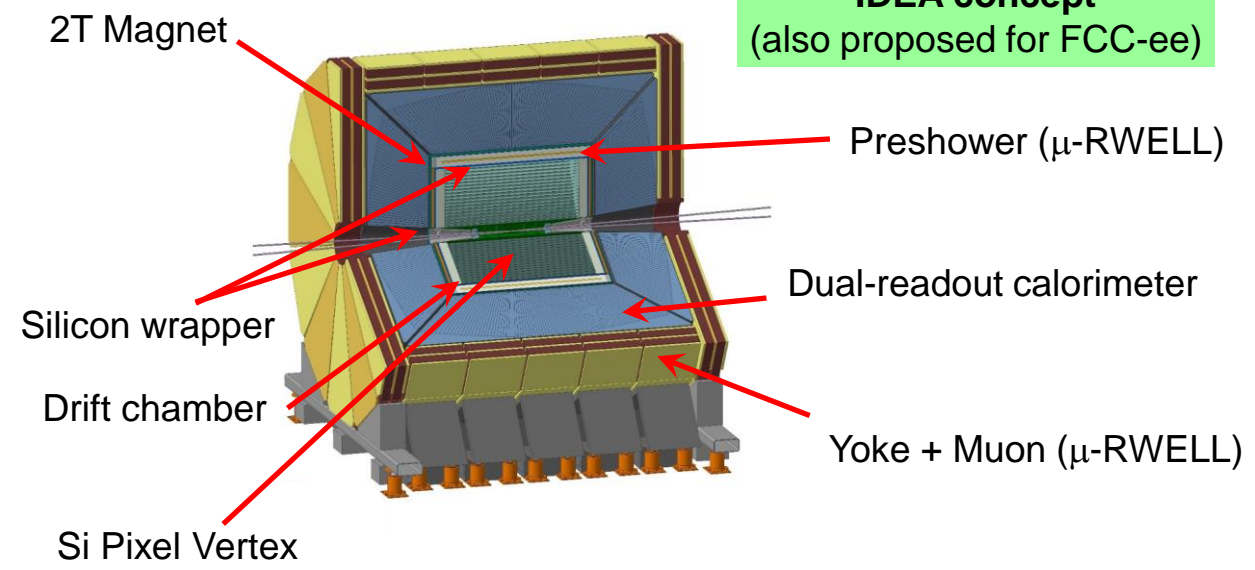
Both **50 MW** and $t\bar{t}$ modes are considered as upgrades



(Baseline Design) Particle Flow Algorithm

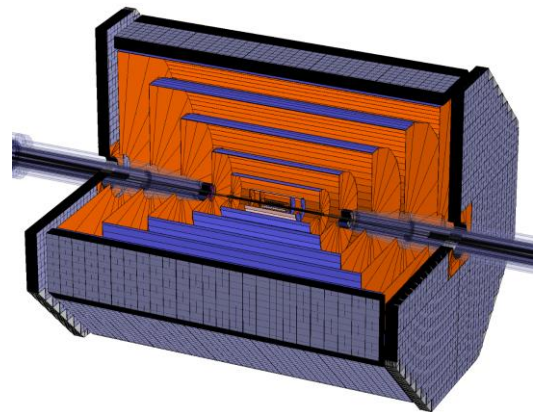


IDEA concept (also proposed for FCC-ee)

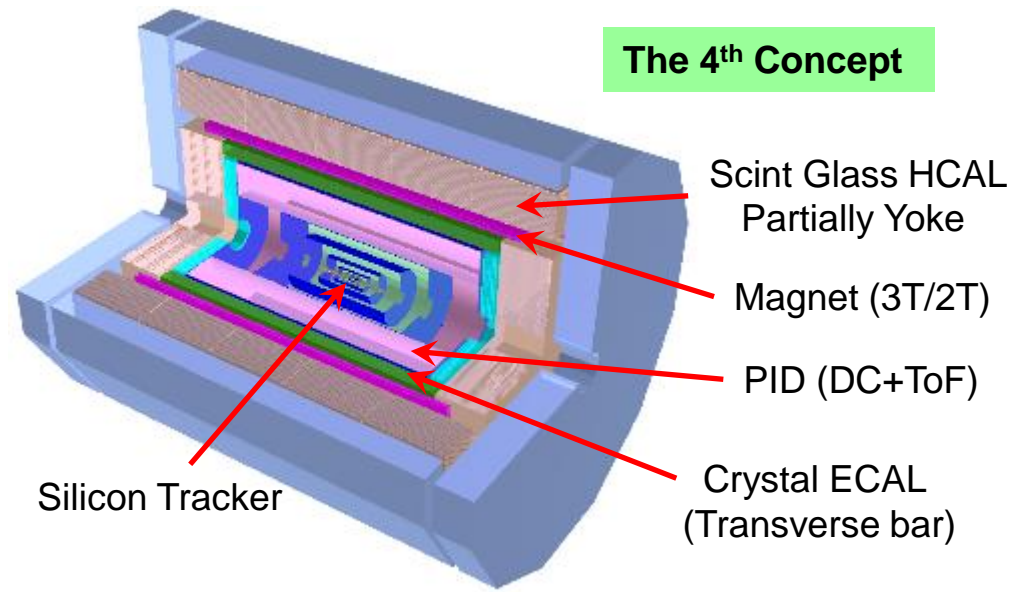


- SIT
- TPC
- SET
- FTD
- ETD

FST concept (Full Silicon Tracker)



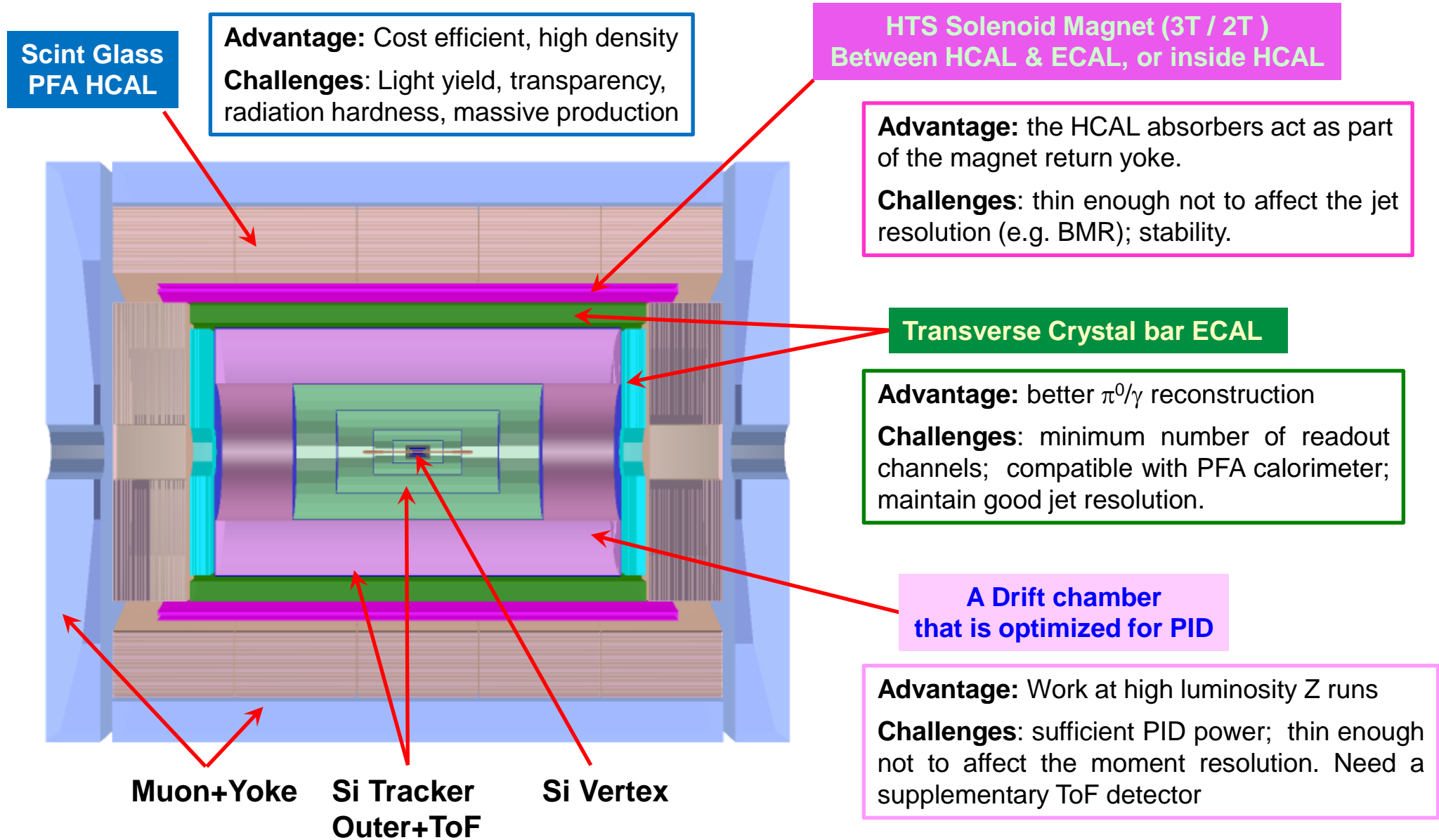
The 4th Concept





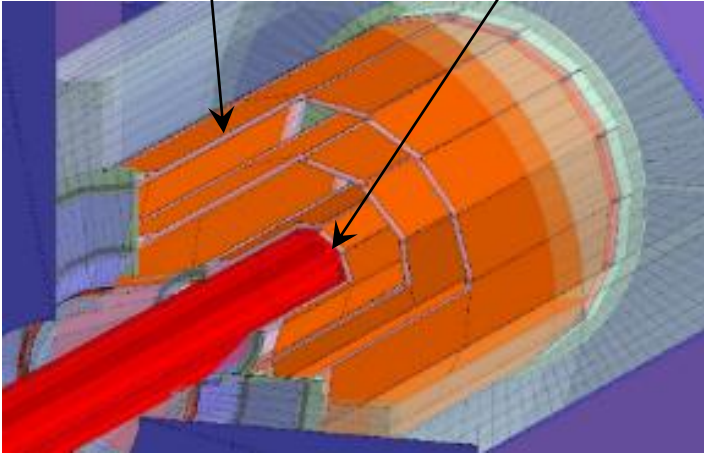
Sub-detector	Key technology	Key Specifications
Silicon vertex detector	Spatial resolution and materials	$\sigma_{r\phi} \sim 3 \mu\text{m}, X/X_0 < 0.15\%$ (per layer)
Silicon tracker	Large-area silicon detector	$\sigma\left(\frac{1}{p_T}\right) \sim 2 \times 10^{-5} \oplus \frac{1 \times 10^{-3}}{p \times \sin^{3/2} \theta} (\text{GeV}^{-1})$
TPC/Drift Chamber	Precise dE/dx (dN/dx) measurement	Relative uncertainty 2%
Time of Flight detector	Large-area silicon timing detector	$\sigma(t) \sim 30 \text{ ps}$
Electromagnetic Calorimeter	High granularity 4D crystal calorimeter	EM energy resolution $\sim 3\%/\sqrt{E(\text{GeV})}$ Granularity $\sim 2 \times 2 \times 2 \text{ cm}^3$
Magnet system	Ultra-thin High temperature Superconducting magnet	Magnet field 2 – 3 T Material budget $< 1.5X_0$ Thickness $< 150 \text{ mm}$
Hadron calorimeter	Scintillating glass Hadron calorimeter	Support PFA jet reconstruction Single hadron $\sigma_E^{had} \sim 40\%/\sqrt{E(\text{GeV})}$ Jet $\sigma_E^{jet} \sim 30\%/\sqrt{E(\text{GeV})}$

These specifications already include some of the 4th detector design





2 layers / ladder $R_{in} \sim 16$ mm



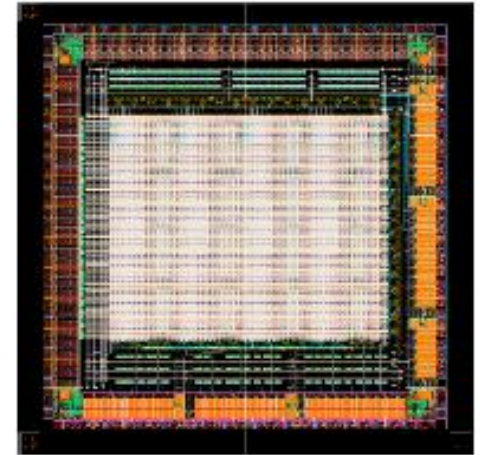
Goal: $\sigma(IP) \sim 5 \mu\text{m}$ for high P track.

CDR design spec:

- Single point resolution $\sim 3 \mu\text{m}$.
- Low material (0.15% X_0 / layer),
- Low power ($< 50 \text{ mW/cm}^2$)
- Radiation hard (1 Mrad/year)

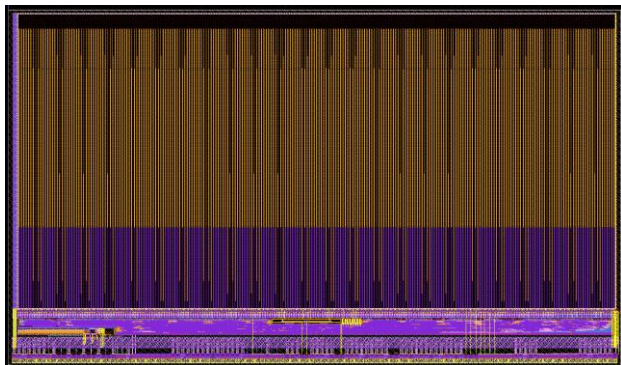
Silicon pixel sensor develops in 3 series:
JadePix / MIC, TaichuPix, CPV

CPV4 (SOI-3D), 64x64 array
 $\sim 21 \times 17 \mu\text{m}^2$ pixel size



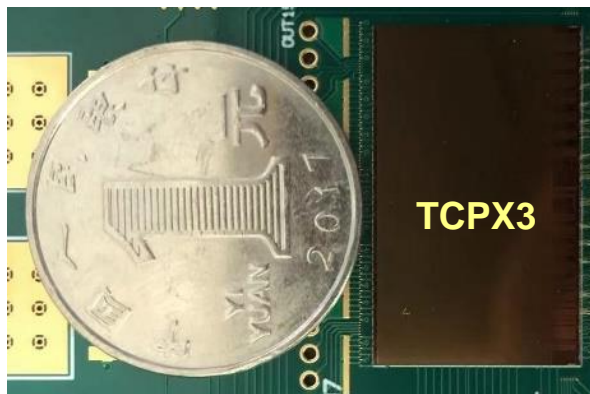
Upper chip

JadePix4 356x498 array of $20 \times 29 \mu\text{m}^2$



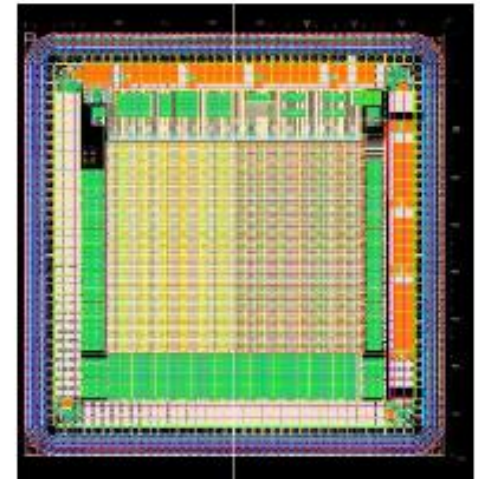
TowerJazz 180nm CIS process
 $\sigma_{x/y} \sim 3-4 \mu\text{m}$, $\sigma_t \sim 1 \mu\text{s}$, $\sim 100 \text{ mW/cm}^2$

TaichuPix3 1024x512 array of $25 \times 25 \mu\text{m}^2$



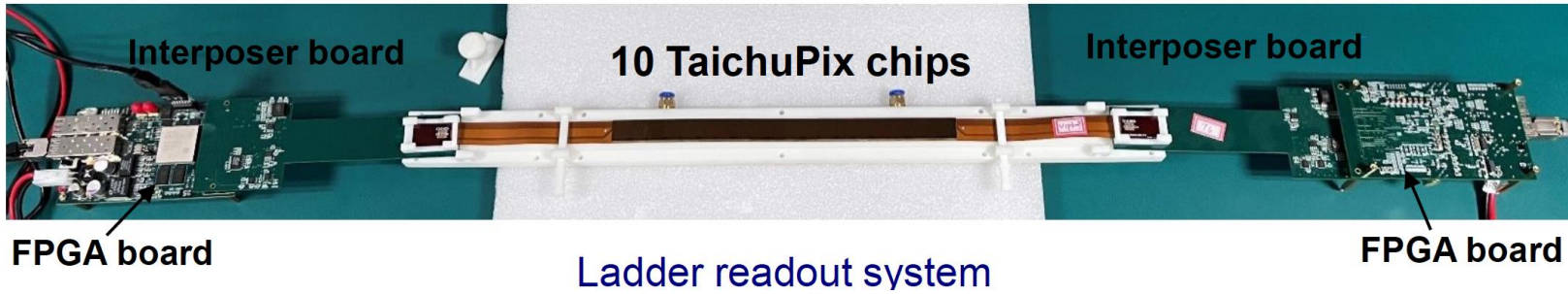
TCPX3

Lower chip



LAPIS 200nm SOI process

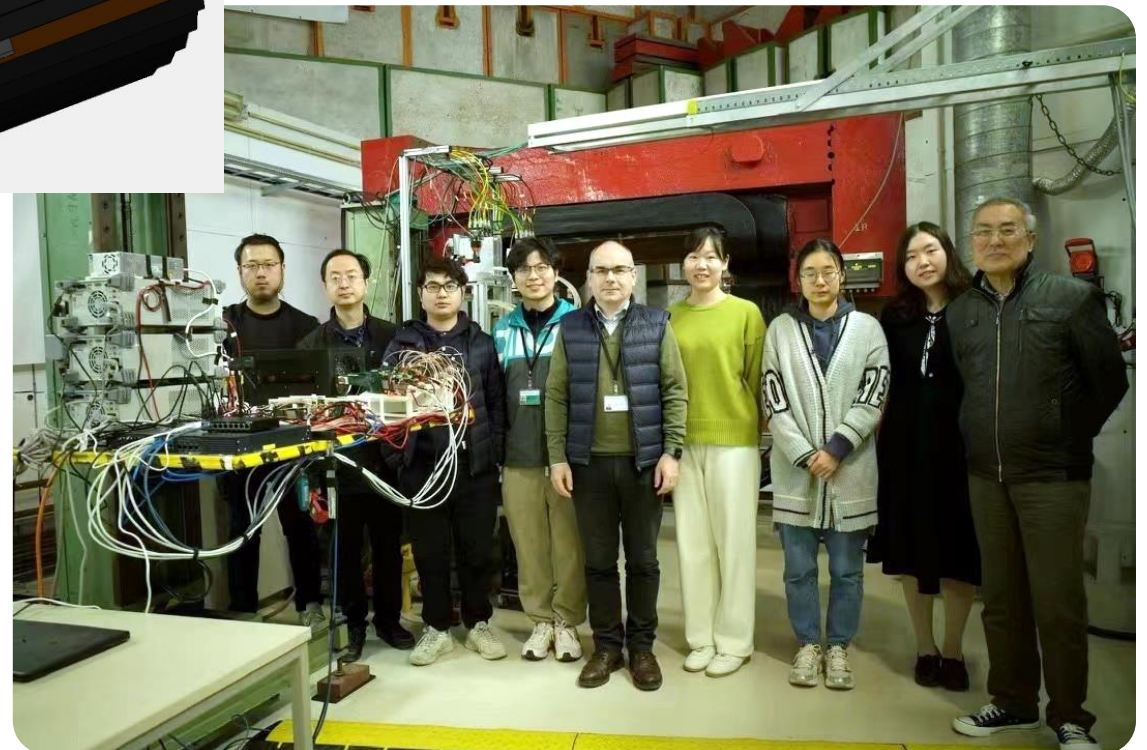
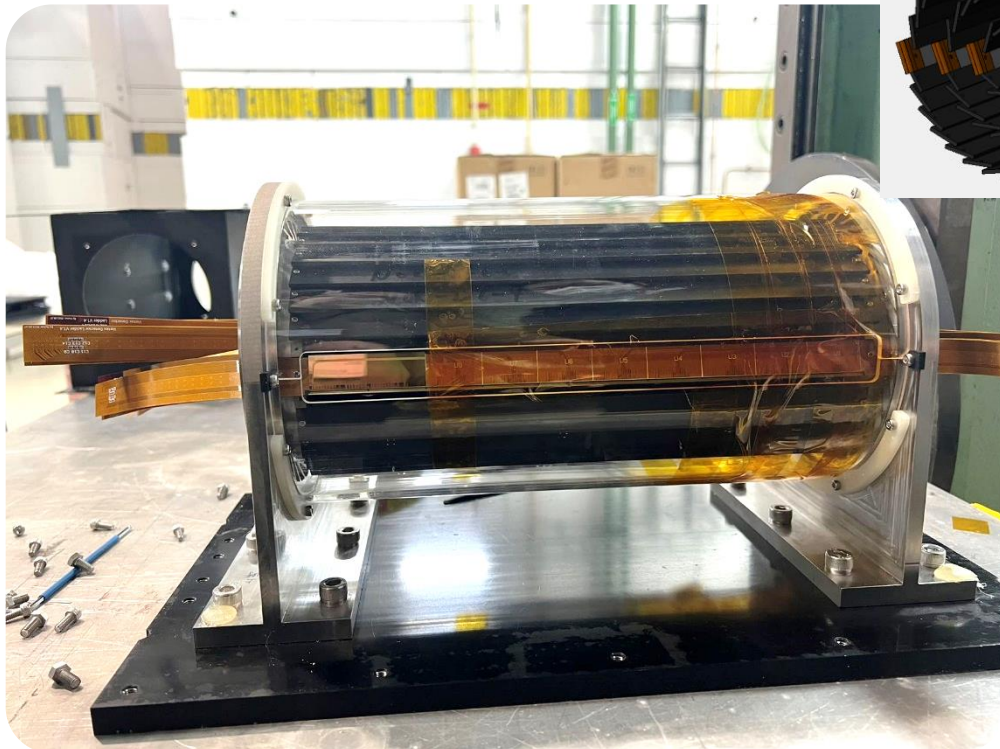
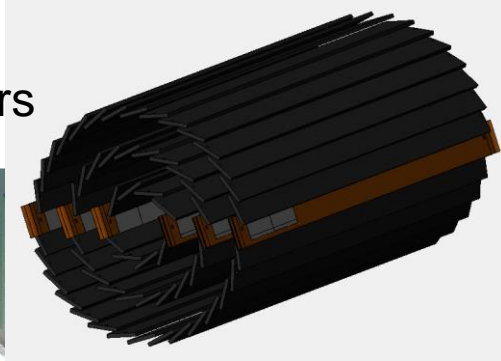
Prototyping Vertex Detector



TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ 4.9 μm

6 double-sided ladders





❖ Initial TPC design has difficulty @high luminosity Z mode due to IBF. Decide to use pixelated TPC

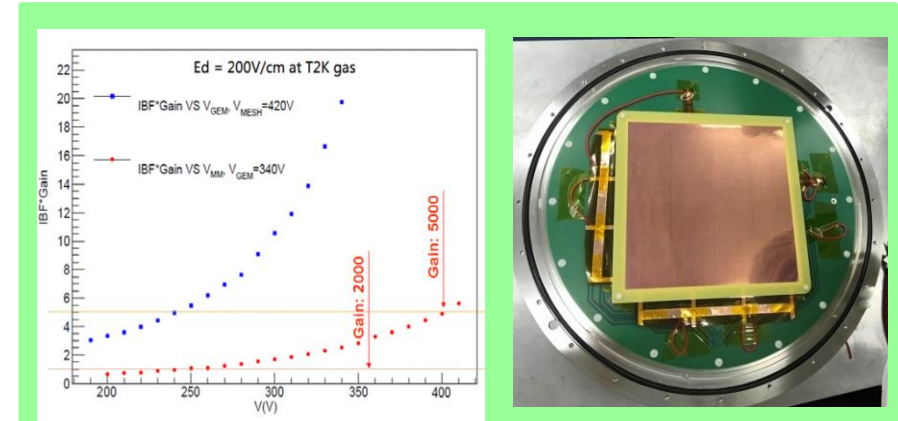
❖ R&D roadmap:

- From a module to a prototype
- Low power consumption FEE ASIC

Goal:
 $\sigma(r-\Phi) \sim 100 \mu\text{m}$

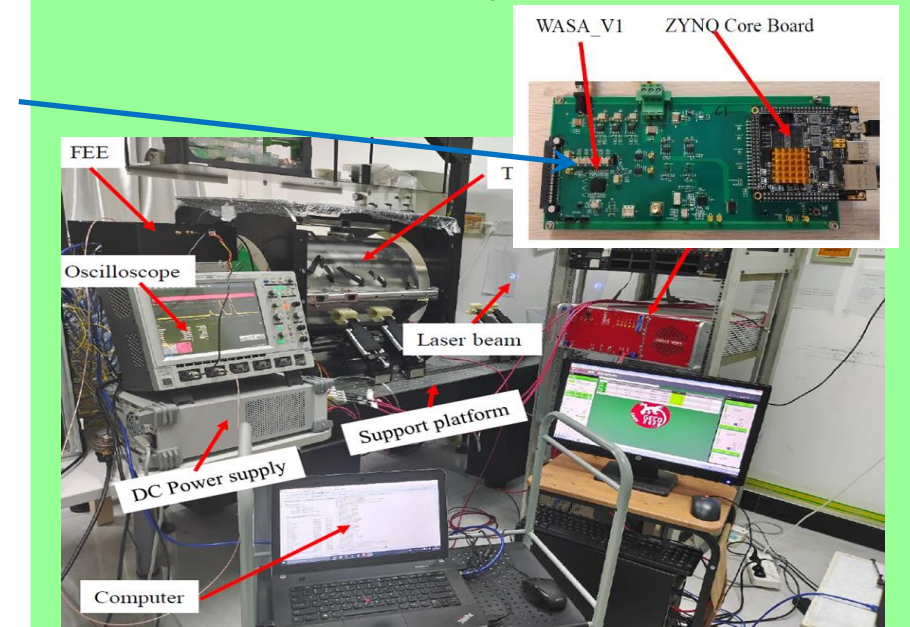
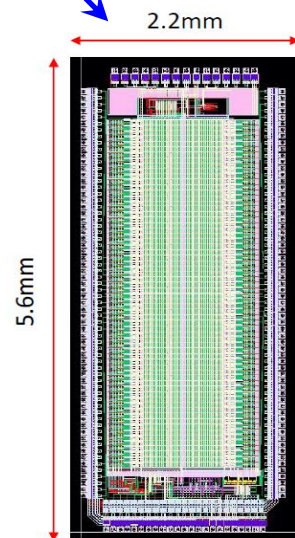
❖ Achievement so far:

- Hybrid GEM+Micromegas module: $\text{IBF} \times \text{Gain} \sim 1$ at $G=2000$
- Spatial resolution of $\sigma_{r\phi} \leq 100 \mu\text{m}$, dE/dx for PID: $<4\%$
- WASA chip: $\sim 3 \text{ mW/ch}$ with ADC, 32 channels/chip



GEM+Micromegas module R&D

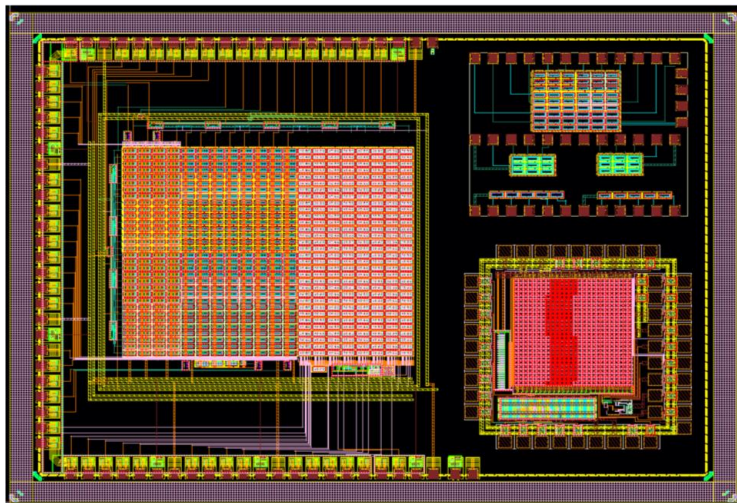
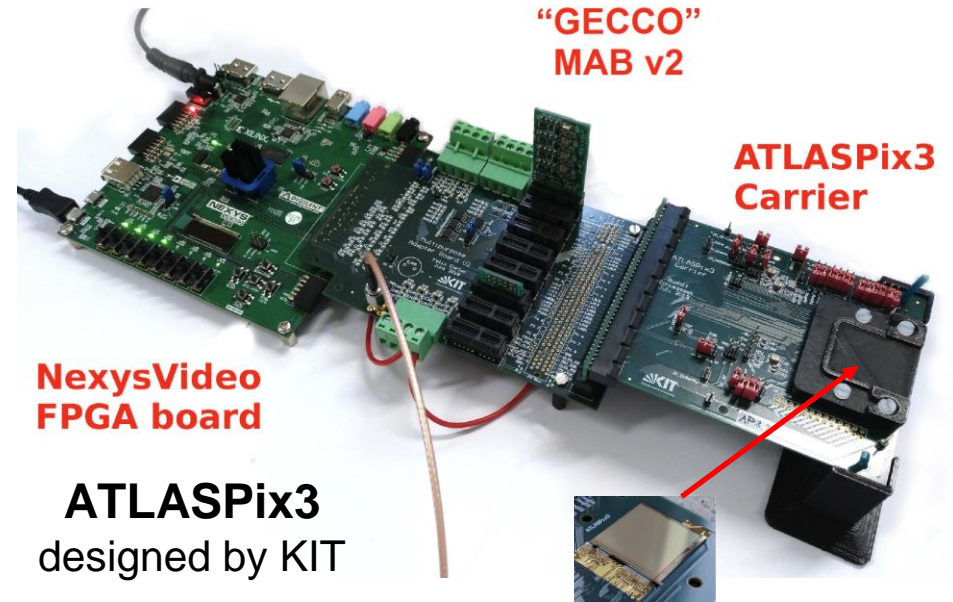
TPC prototype with integrated 266nm UV laser



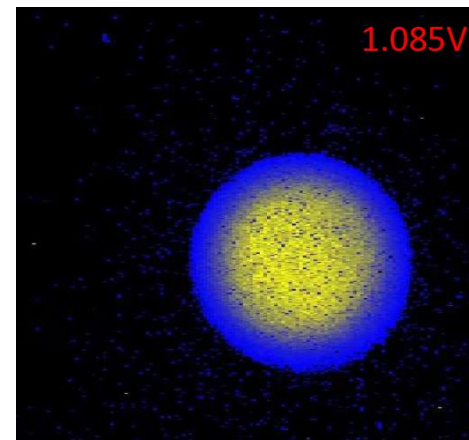
Low power consumption readout



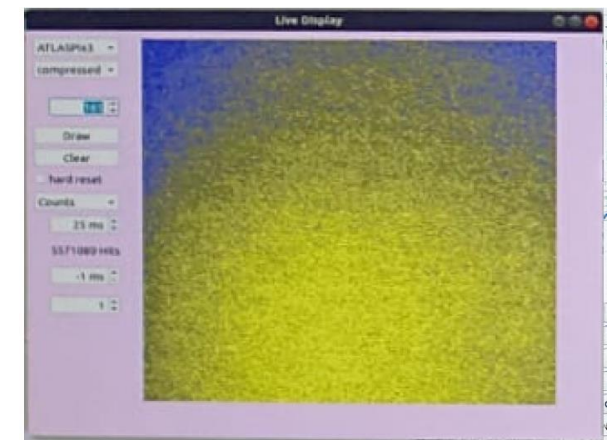
- ❑ Large area: $\sim 140 \text{ m}^2$ in Full SiTrk, or $\sim 70 \text{ m}^2$ in TPC+SiTrk
 - ➔ Cost effectiveness
- ❑ Focus on MAPS pixel tracker, also started SSD for outer layers
- ❑ Joint efforts on an ATLASPix3 based demonstrator
- ❑ ATLASPix & MightyPix use TSI 180nm HV process
 - ➔ Long term support (?)
- ❑ Exploring SMIC 55 nm HV HR process
 - ➔ Smaller feature size & alternative foundry
- ❑ Other possibilities, e.g. MALTA3, TPSCo-65nm



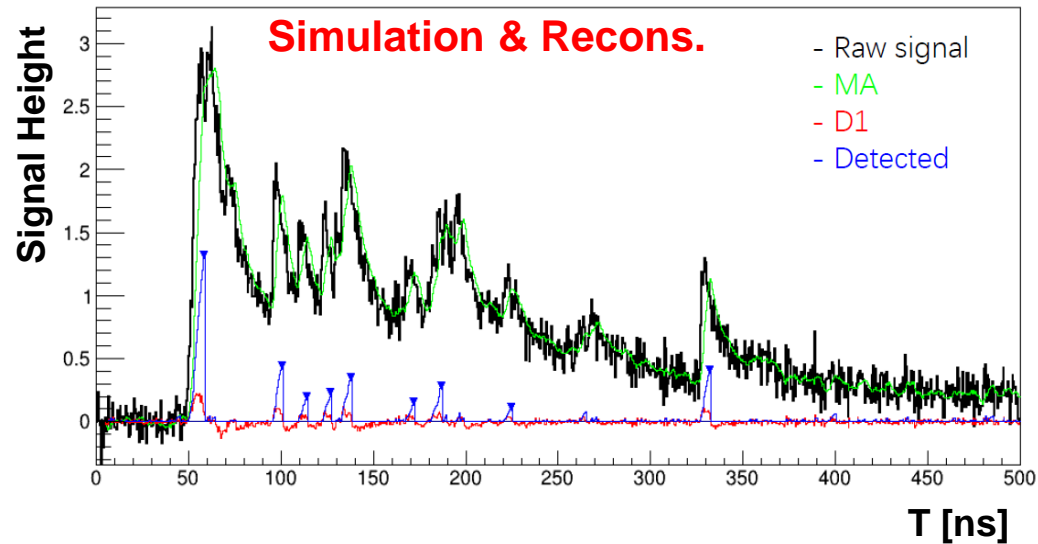
The 2nd design for SMIC 55nm HV HR process



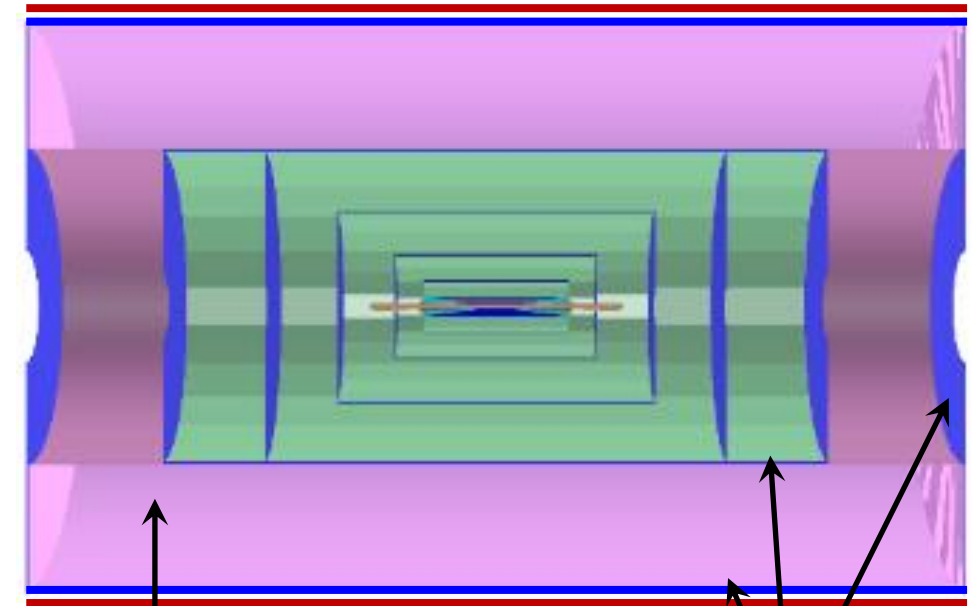
Hitmap with Fe55 source



Hitmap with electron beam



- ❑ A drift chamber optimized for PID: no stereo, larger cell, optimal gas mixture and HV
- ❑ Cluster counting algorithm (dN/dX) is more powerful than conventional dE/dx , but requires much more in the readout electronics.
- ❑ Studies: $dNdX$ reconstruction algorithm, readout electronics, prototype test in beam



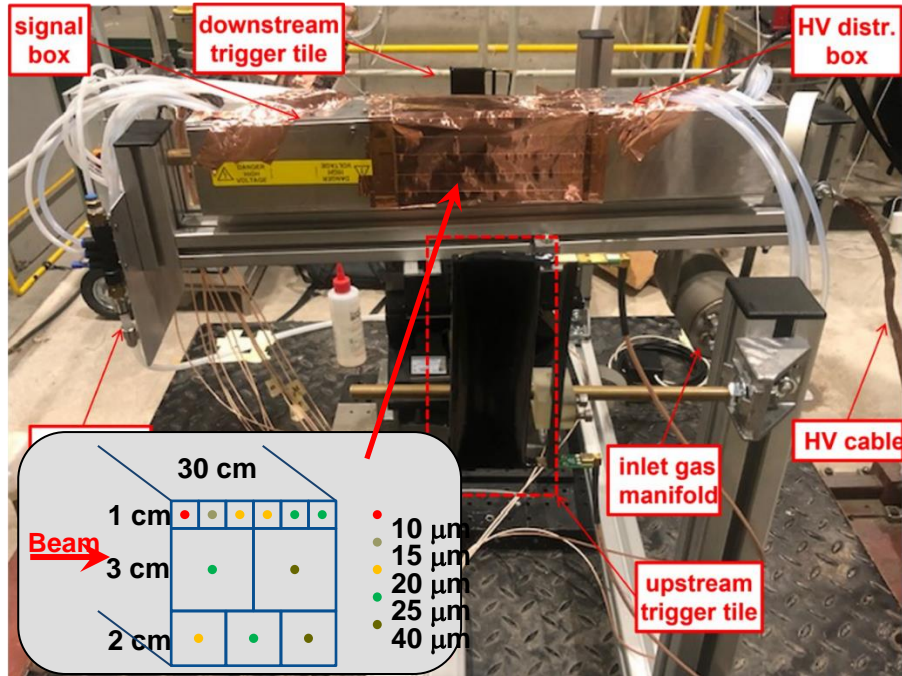
A Drift chamber between the 2 outer layers of FST, optimized for its PID power.

Full silicon trackers

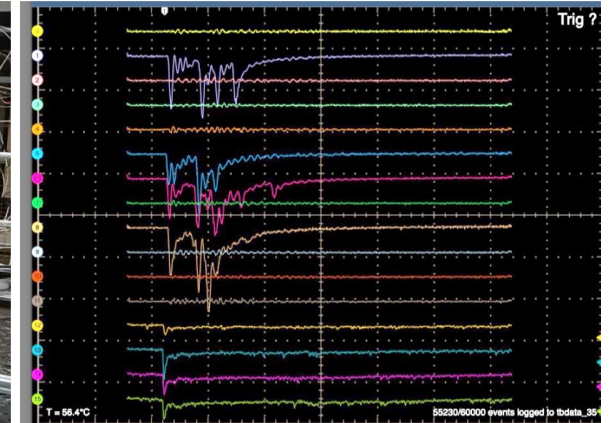
Supplementary Time of Flight, could be based on LGAD technology, even better if it acts as an outer SiTrk



Test Beam 2021.11



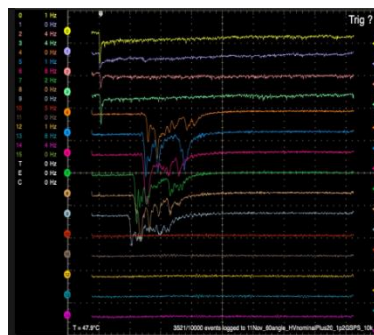
TB 2022.07



TB 2023.07

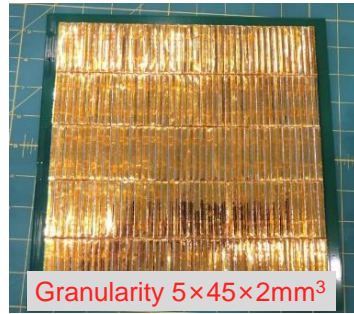
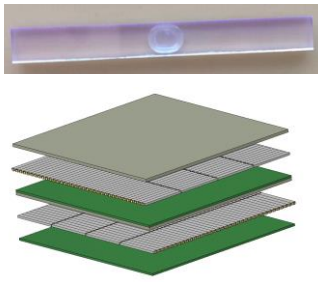


- ❑ Test beam and analysis led by the Italian group
- ❑ Measure number of clusters & efficiency, study effects of configuration
- ❑ Apply clustering algorithm in the real world, more realistic parameters to simulation

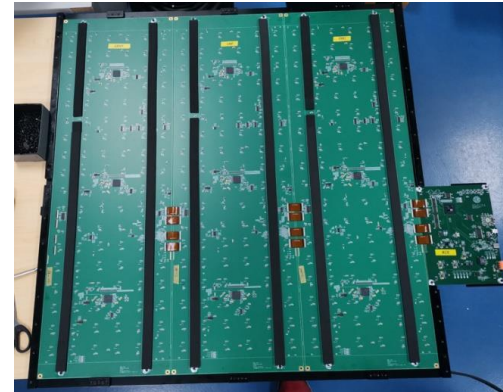
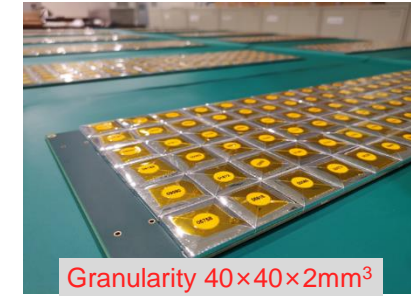
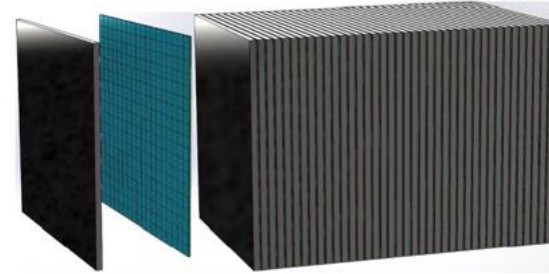




ECAL: scintillator(strip)+SiPM, CuW



HCAL: scintillator (tile)+SiPM, steel

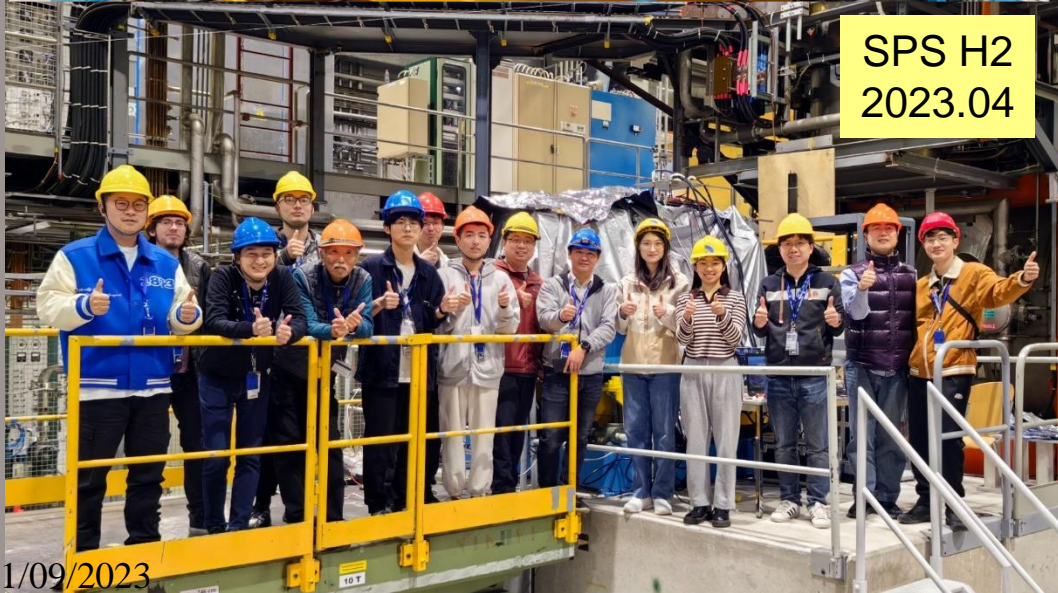


- ❑ ScW-ECAL: transverse $\sim 20 \times 20$ cm, 32 sampling layers
 - $\sim 6,700$ channels, SPIROC2E (192 chips)
- ❑ AHCAL: transverse 72×72 cm, 40 sampling layers
 - $\sim 13\text{k}$ channels, SPIROC2E (360 chips)

Prototypes developed within **CALICE**

- China: IHEP, SJTU, USTC
- Japan: U. Shinshu, U. Tokyo
- France: **CNRS Omega**
- Israel: Weizmann

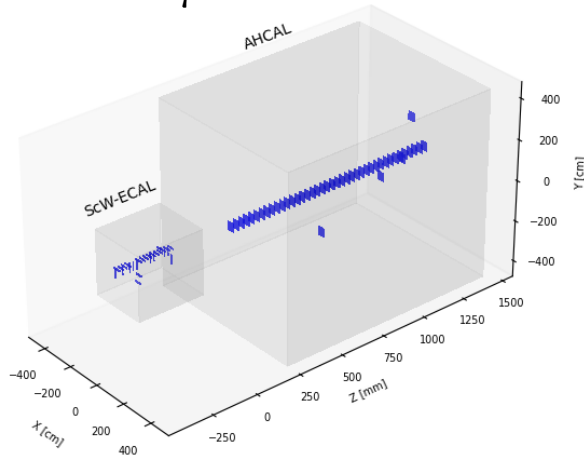
Testbeam of Prototype PFA Calorimeters



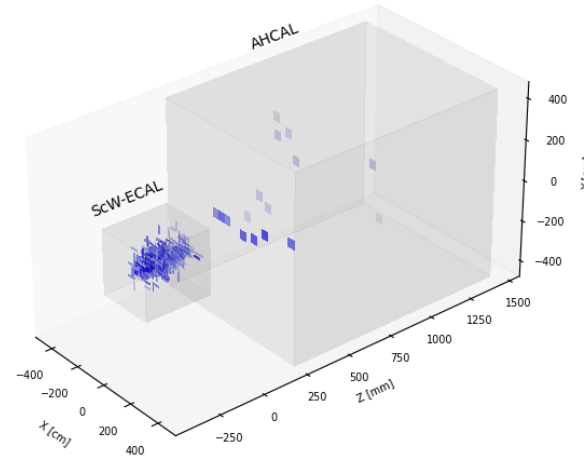


Within CALICE
collaboration

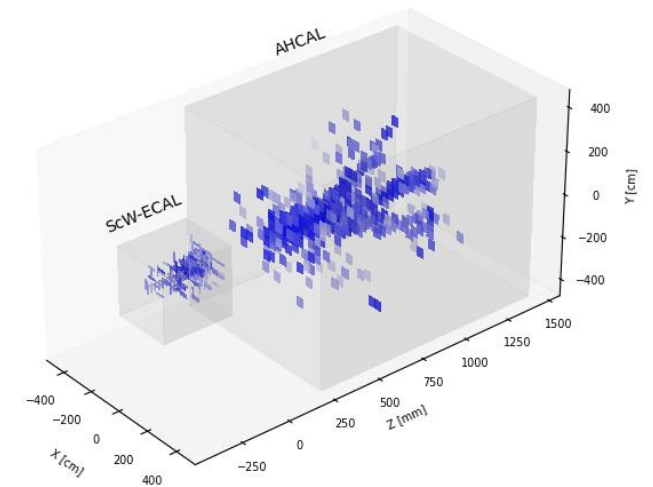
100 GeV μ^-



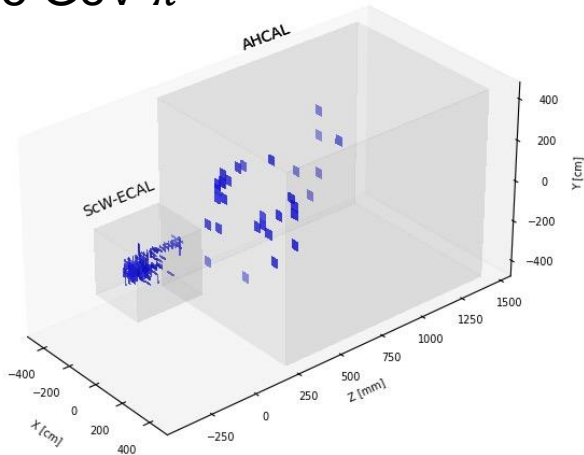
60 GeV e



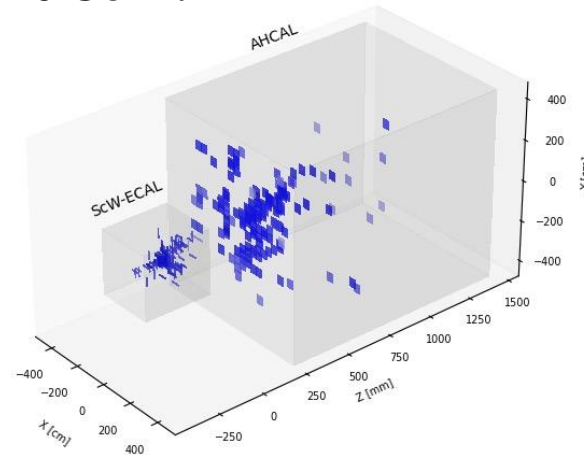
60 GeV π^-



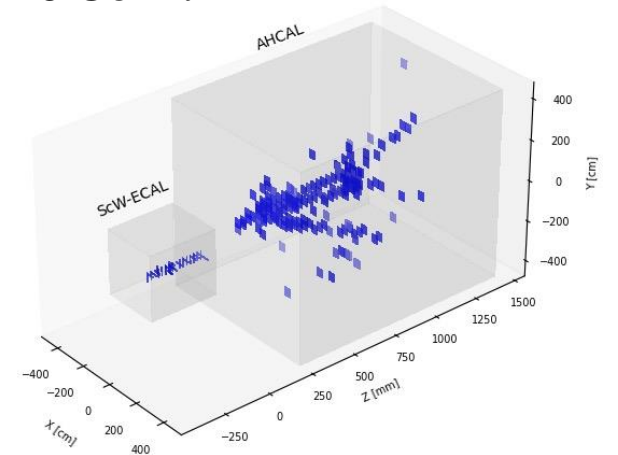
5 GeV π^-



10 GeV π^-

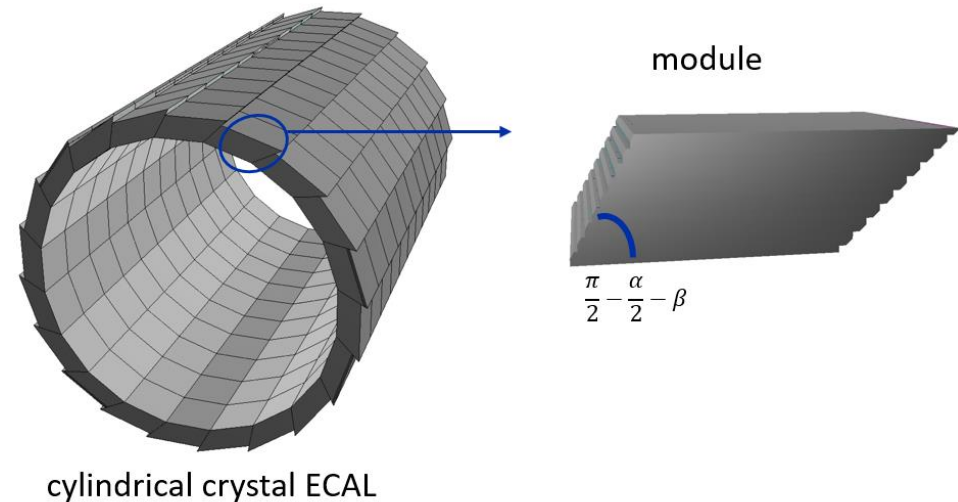
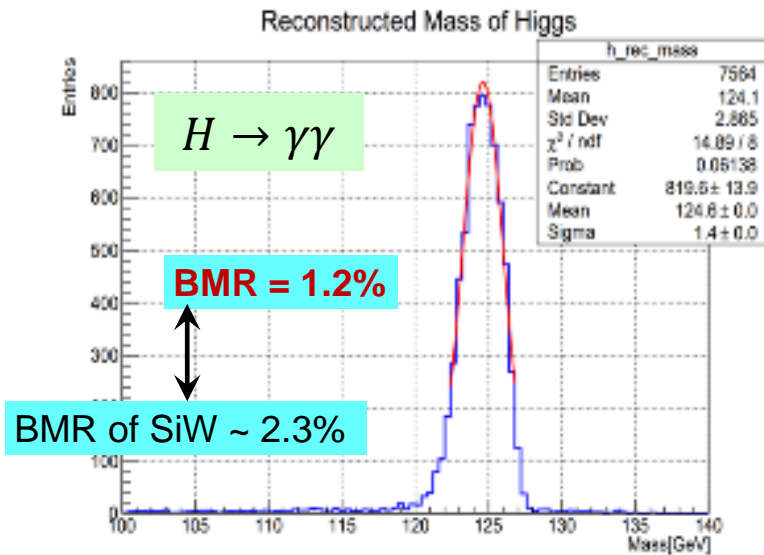
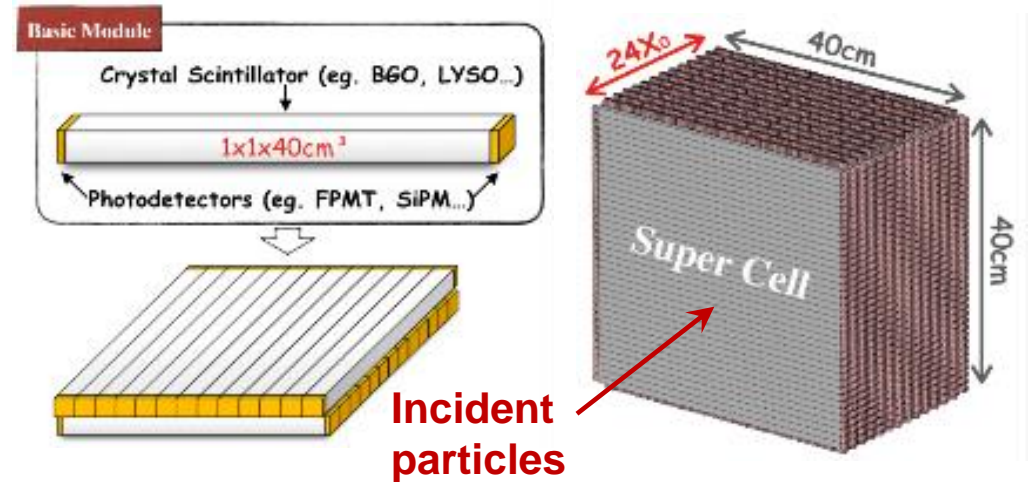


15 GeV π^-



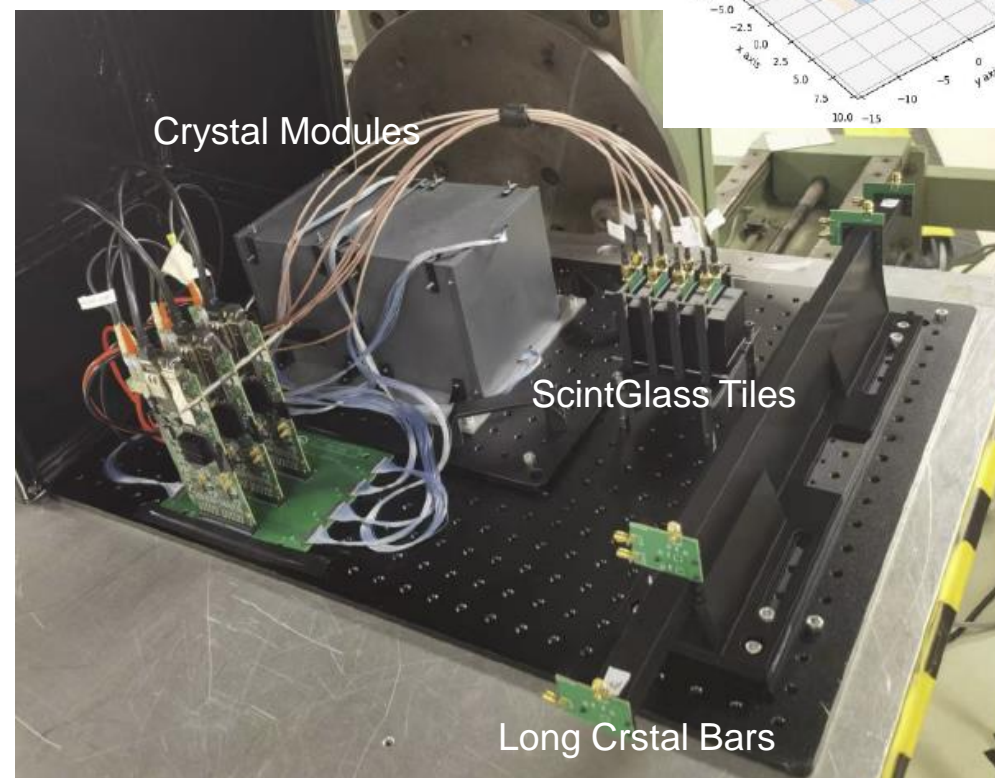
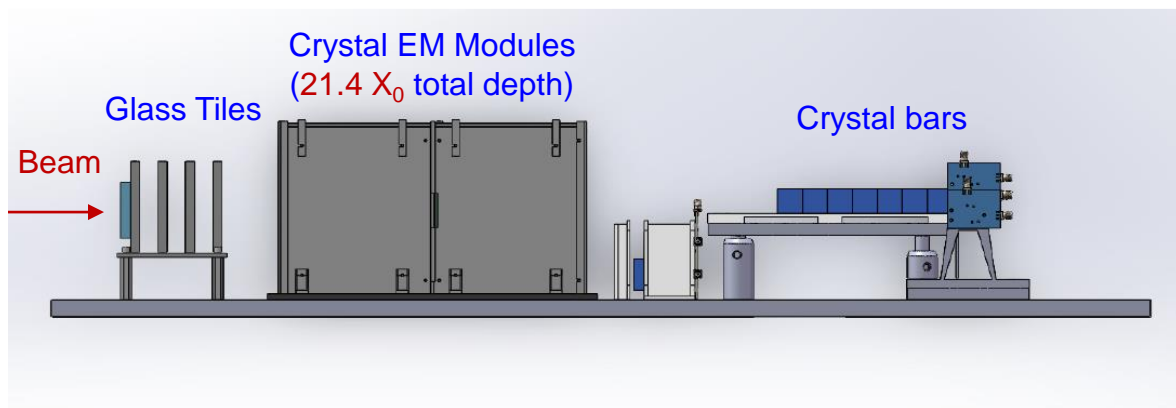
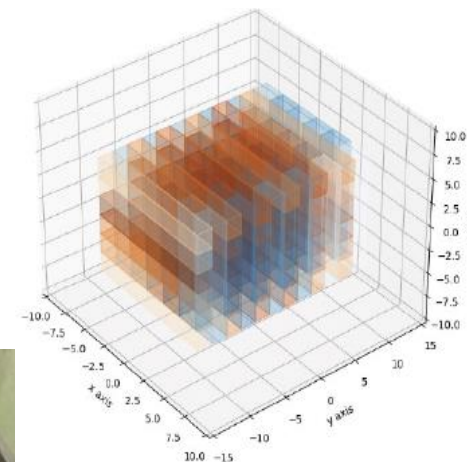
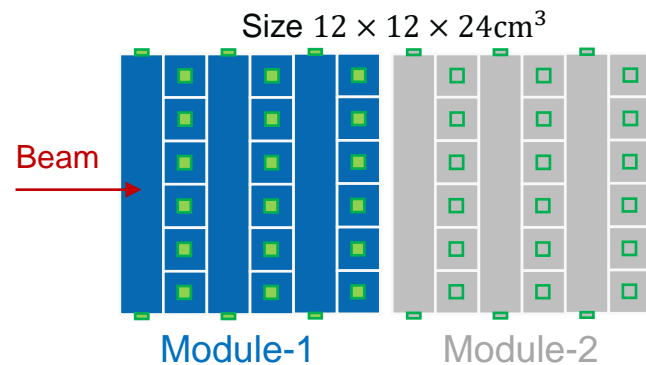


- ❖ Goal
 - Comparable BMR resolution as with the Si+W ECAL.
 - Much better sensitivity to γ/e , EM resolution $\leq 3\%/\sqrt{E(\text{GeV})}$
- ❖ Features:
 - Timing at two ends of the crystal bar
 - Crossed arrangement in adjacent layers.
 - High granularity with reduced readout channels
- ❖ Key issues:
 - Ambiguity caused by 2D measurements (**ghost hit**).
 - Identification of energy deposits from particles (**confusion**).



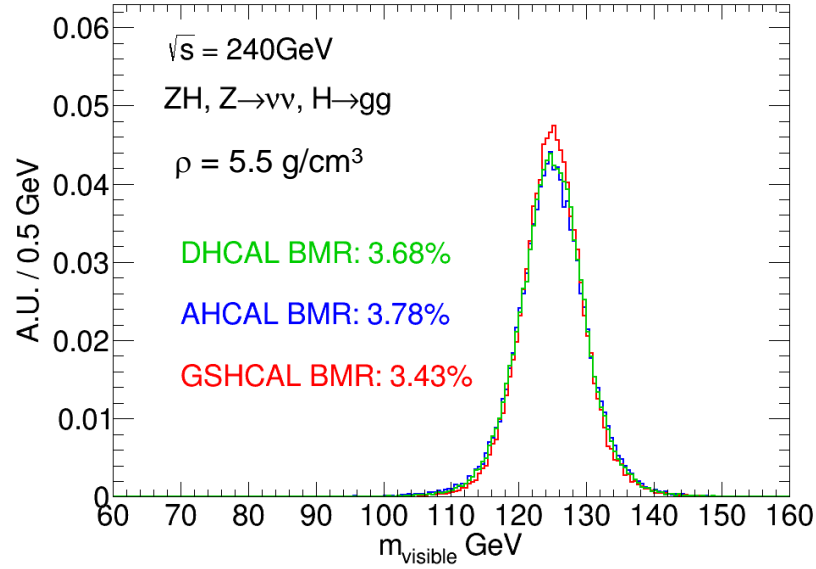


- ❖ A successful testbeam @ DESY, Oct 2023
- ❖ To address critical issues at system level
 - Validation: design of crystal-SiPM, light-weight mechanical structure
 - EM shower performance
- ❖ Module development
 - BGO crystal bars from SIC-CAS
 - SiPM: 3×3 mm² sensitive area, 10μm pixel pitch
 - Front-end electronics with CITIROC, by **CNRS OMEGA**. An ASIC with a large dynamic range would be more desirable

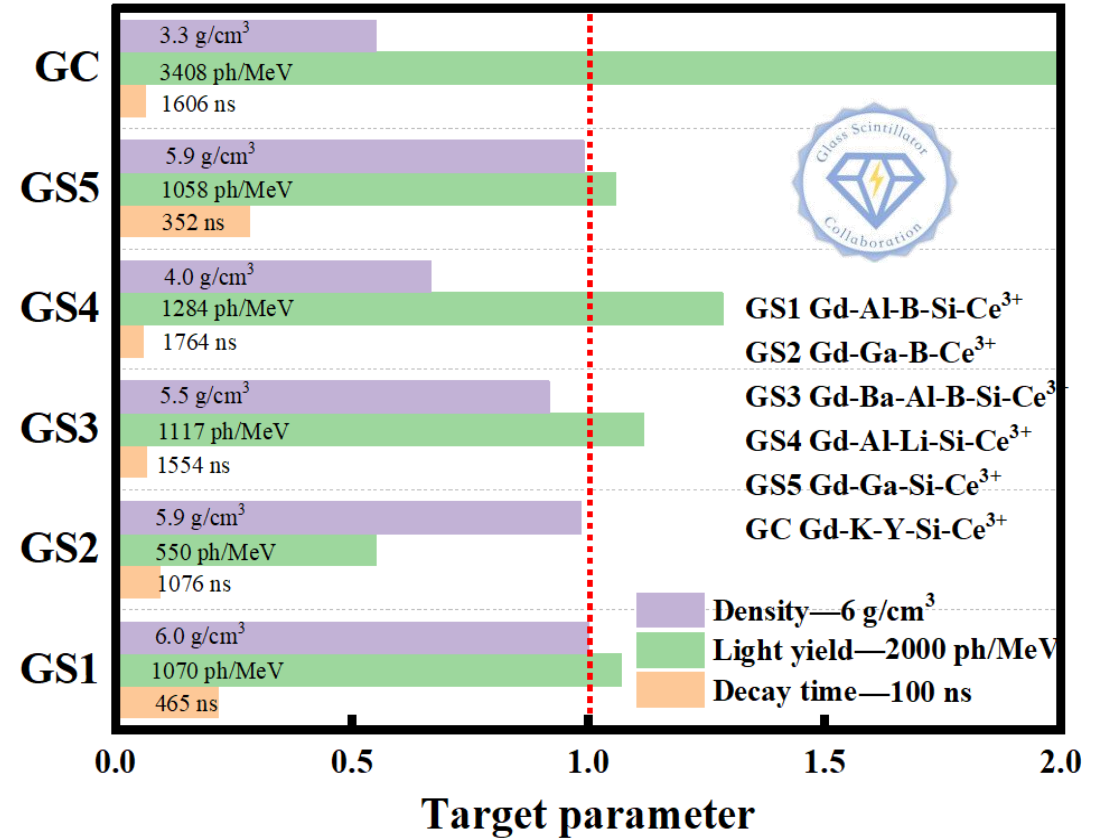
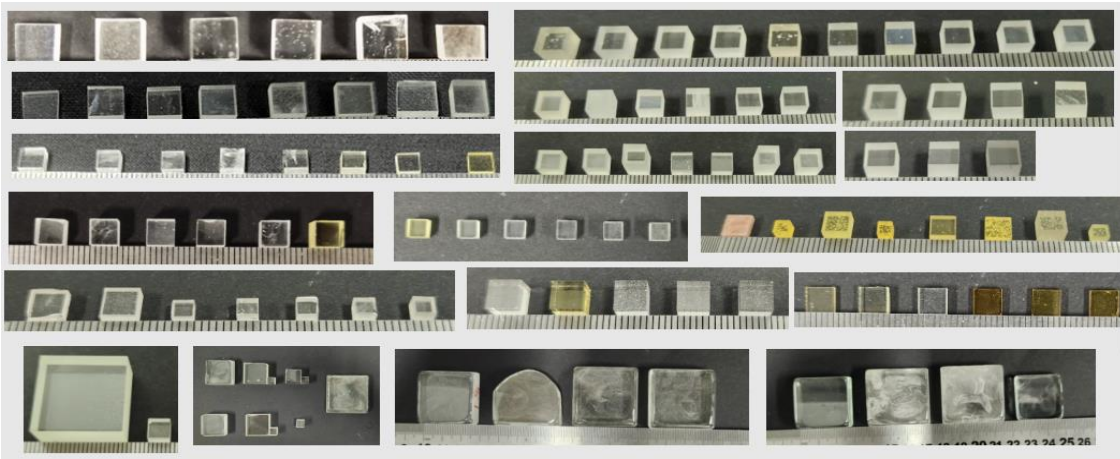


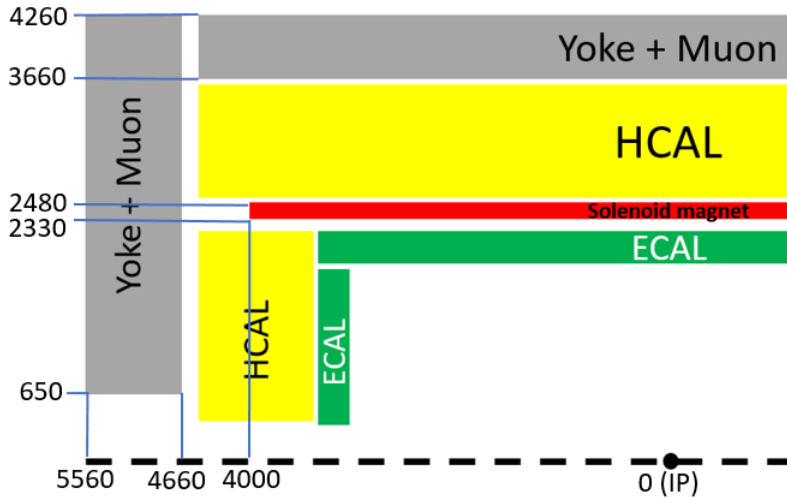


Replacing plastic scintillator with high density glass scintillator



- Light yield: 1000~2000 ph / MeV
- Density: 5~7 g/cm³
- Scintillation time: ~100 ns
- Low cost
- Tiles in cm scale for PFA HCAL

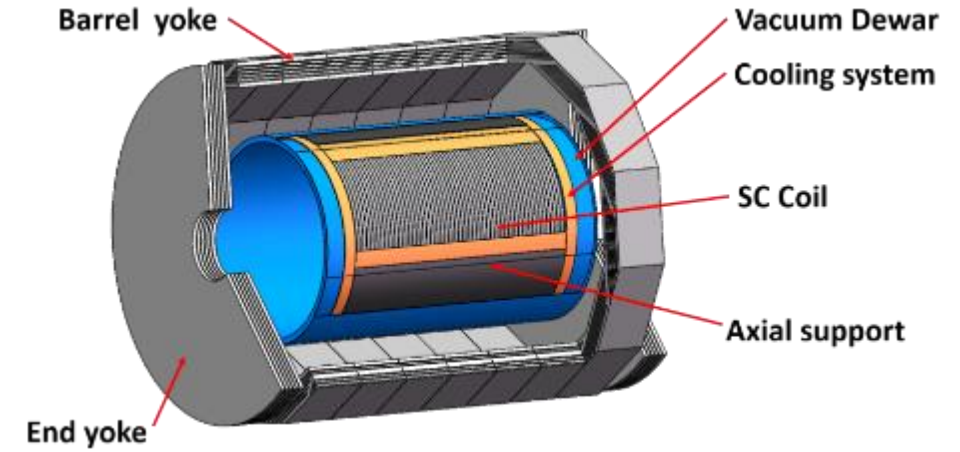




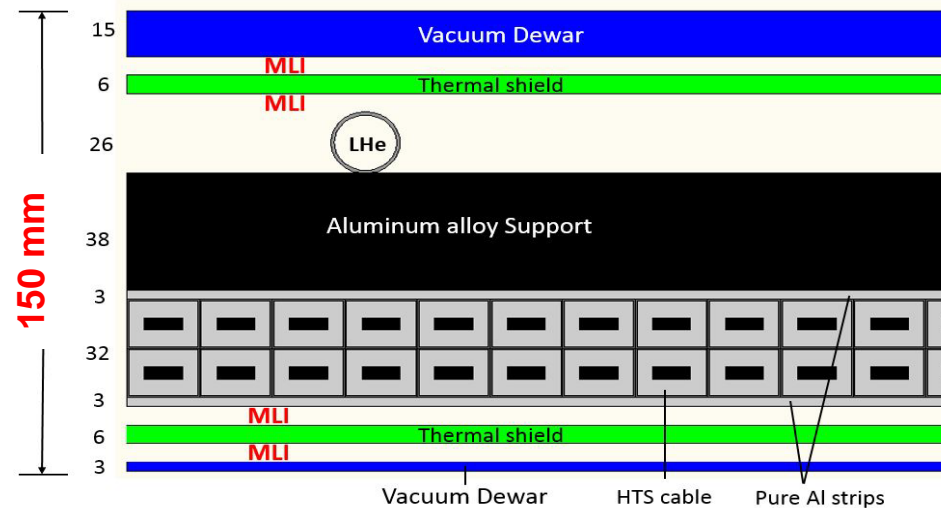
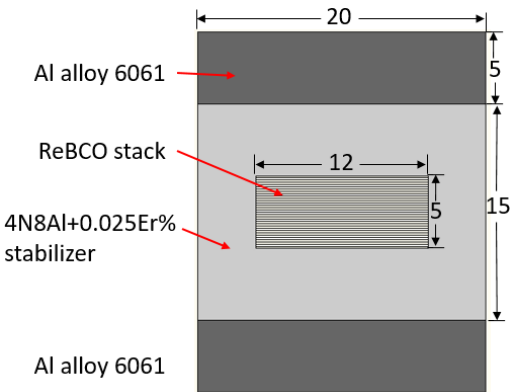
Challenges

Low mass $< 1.5X_0$
 ultra-thin < 150 mm
 high strength cable

R&D: high strength HTS cable,
 ultra-thin cryostat.



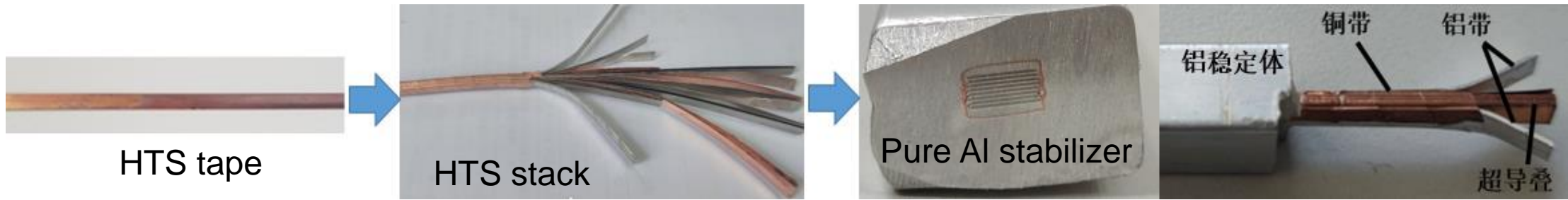
Al stabilized ReBCO stacked tape conductor (ASTC) cable



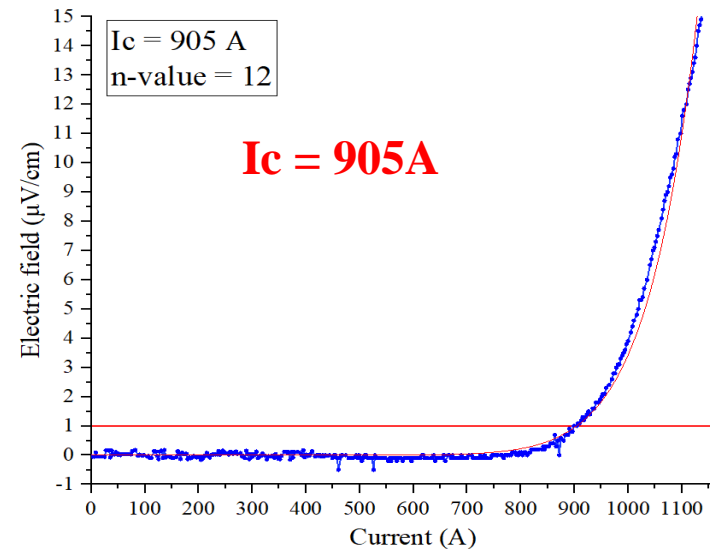
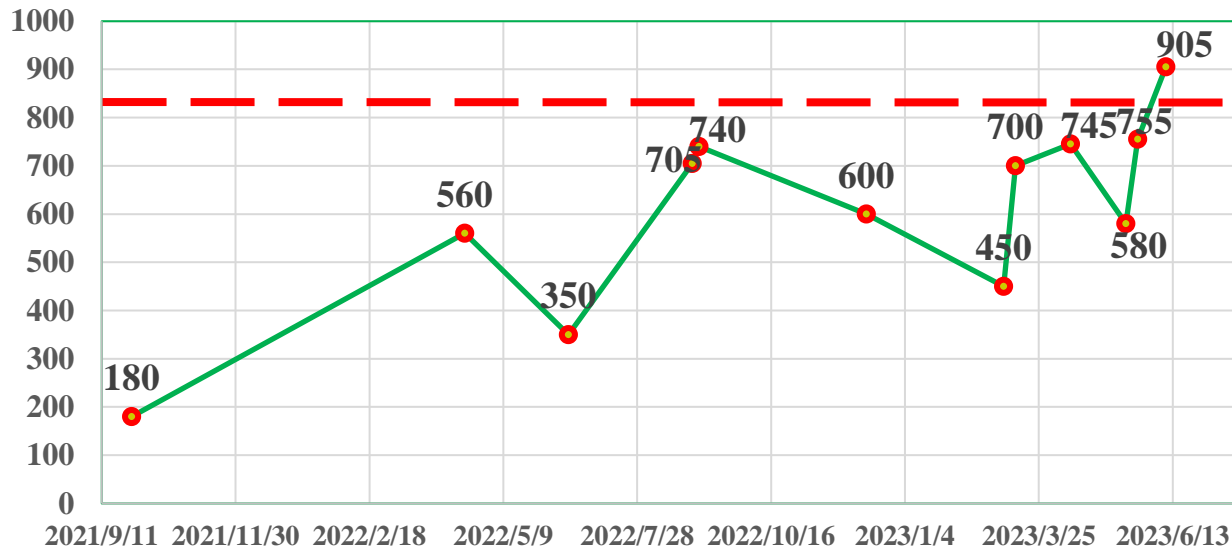
Magnetic field	3 T	Current	28000 A
Inner diameter	4660 mm	Inductance	1.27 H
Outer diameter	4960 mm	Stored energy	500 MJ
Magnet thickness	150 mm	Cold mass	27 ton
Length	8000 mm	HTS cable length	10.7 km
Total weight	48 ton	ASTC weight	16.6 ton



Significant progress !



Object: single tape core $I_c > 100 \text{ A}@77\text{K}$; 14-core cable $I_c > 830 \text{ A}@77\text{K}$, self-field.



Many Other Detector R&Ds



Stereo Crystal ECAL

$\alpha = 30^\circ$
14 layers

FE readout

adjacent layers
 $\alpha' = -\alpha$

LGAD ToF

Drift Chamber

AD9689 – 2000 EBZ Xilinx KCU105

Scintillator Bar Muon

TPC Prototype

Dual Readout CAL

SCEPCAL

GRPC SDHCAL

RWell SDHCAL

μRWELL for PS & Muon

Beampipe Design



Det	Technology	Det	Technology
Pixel Vertex	JadePix	Calorimeter	Crystal ECAL
	TaichuPix		Stereo Crystal ECAL
	CPV(SOI)		Scint+W ECAL
	Stitching		Si+W ECAL
	Arcadia		Scint+Fe AHCAL
Tracker & PID	CEPCPix		ScintGlass AHCAL
	Silicon Strip		RPC SDHCAL
	TPC		MPGD SDHCAL
	Drift chamber		DR Calorimeter
	PID DC		Muon
	AC-LGAD ToF	RPC	
Lumi	SiTrk+Crystal ECAL	μ -Rwell	
	SiTrk+SiW ECAL	Misc	HTS / LTS Magnet
	Fast LumMoni		MDI & Integration
CEPC SW	TDAQ scheme		

- ❖ Some R&D efforts are already associated with international collaborations: CALICE, LCTPC, & RD*
- ❖ The ECFA DRDs cover much broader scopes, with more general supports, e.g. testbeam facilities
- ❖ We will never stop seeking for better technologies.
- ❖ However, we need to converge for TDR of a reference detector
 - Start preparation in **January of 2024**
 - A draft version by **December of 2024**
 - Official release by **June 30, 2025**



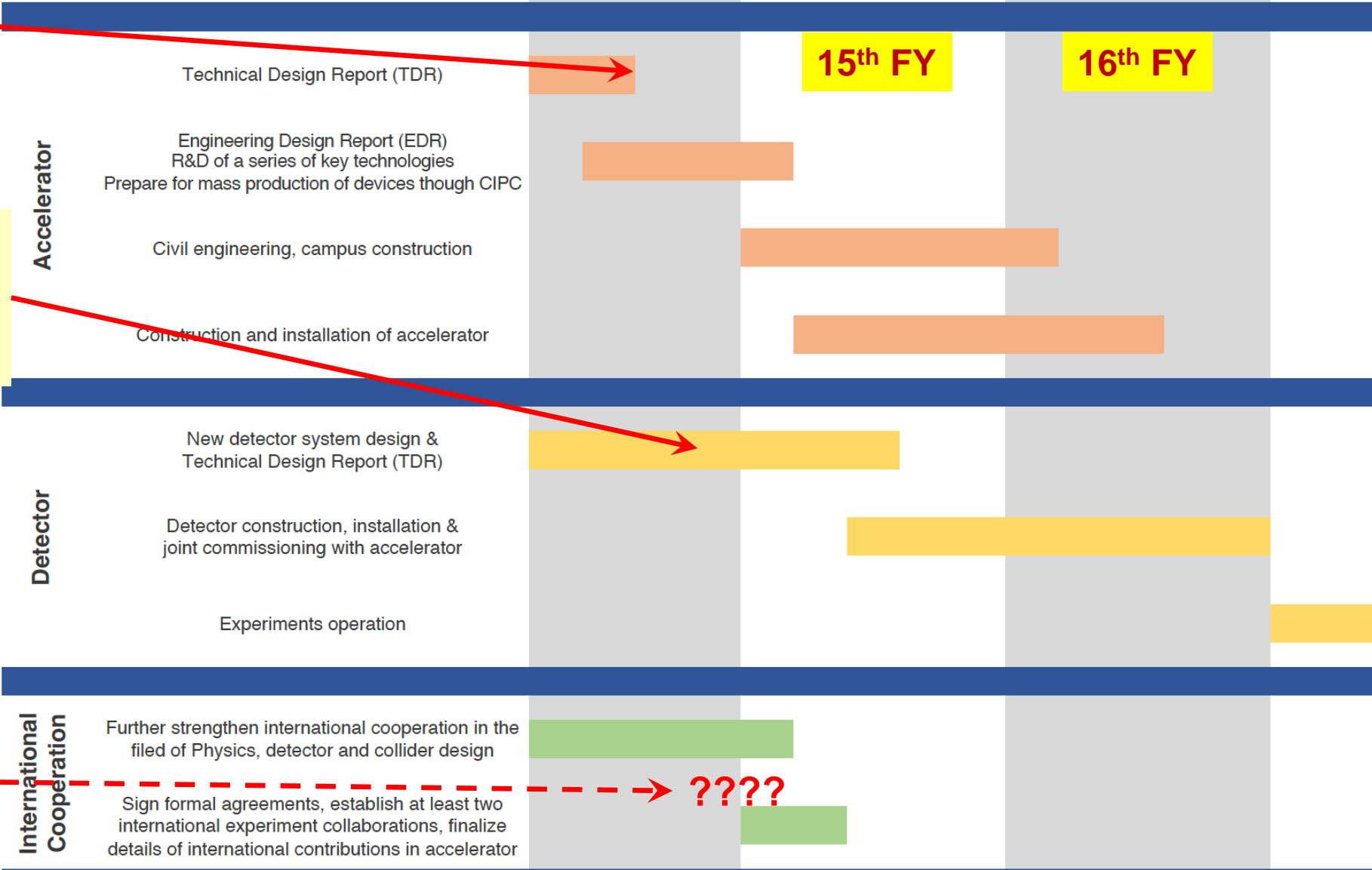
CEPC Project Timeline

2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037

Completion of Accelerator TDR

Goal
TDR of a Reference Detector @ June 30, 2025

International Collaborations



15th FY

16th FY

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