MAPS-based Upstream Tracker for LHCb Upgrade II

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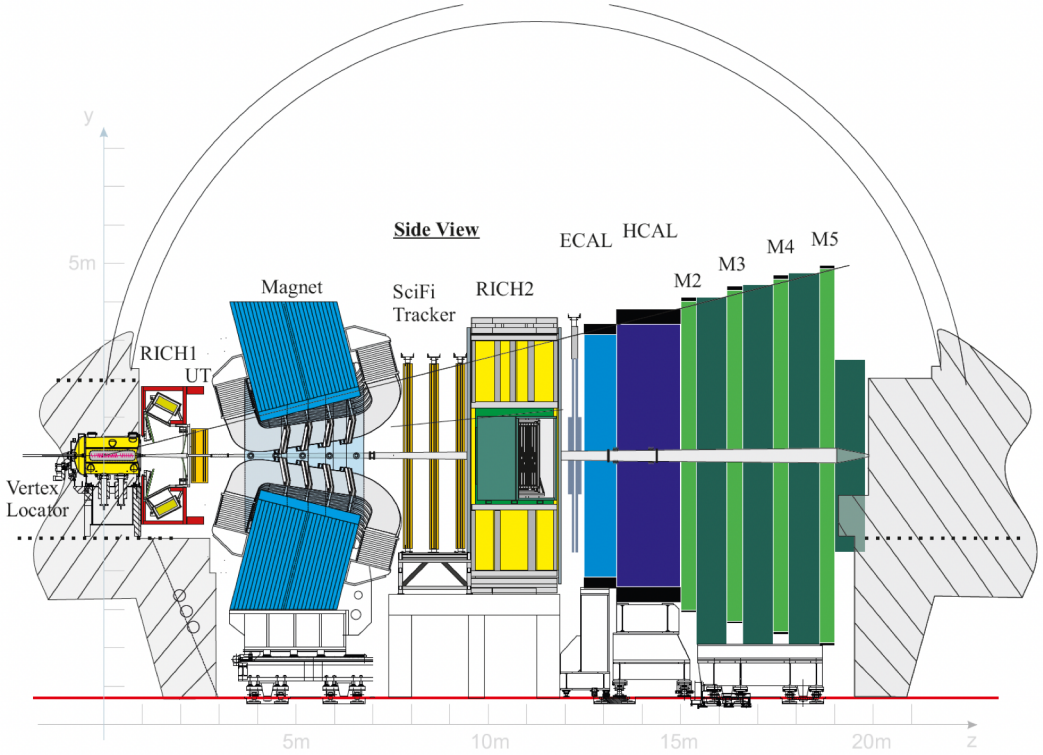
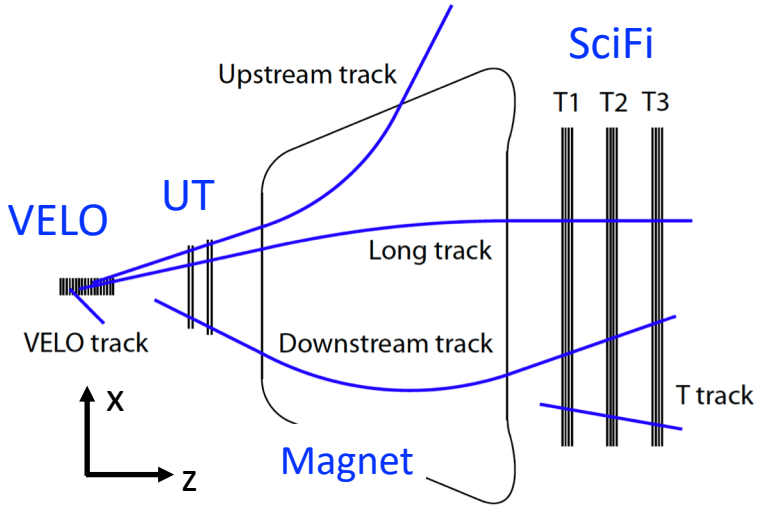
Content

- Introduction to Upstream Tracker
- LHCb Upgrade II challenges for UT
- MAPS-based UT for Upgrade II
  - System design
  - Sensor options: HVCMOS vs. Small-electrode CMOS
  - Simulation and optimization
- Summary

Tracking in LHCb Upgrade I

- LHCb: single-armed spectrometer dedicated to heavy flavour study at LHC
- Upgrade I completed in March 2023
  - Luminosity increase ×5 → $2\times10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - Removal of Hardware trigger

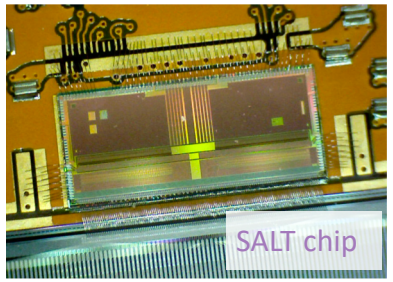




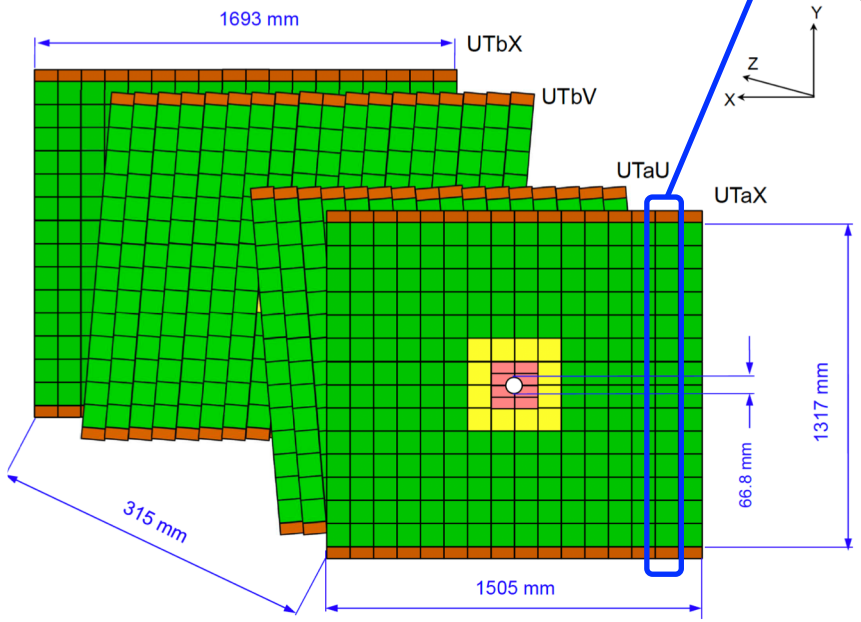
- New sub-detectors for the tracking system
- Upstream Tracker (UT) is essential:
  - Speed-up of VELO-SciFi matching
  - Reduction of ghost rate
  - Reconstruction of long-lived particles

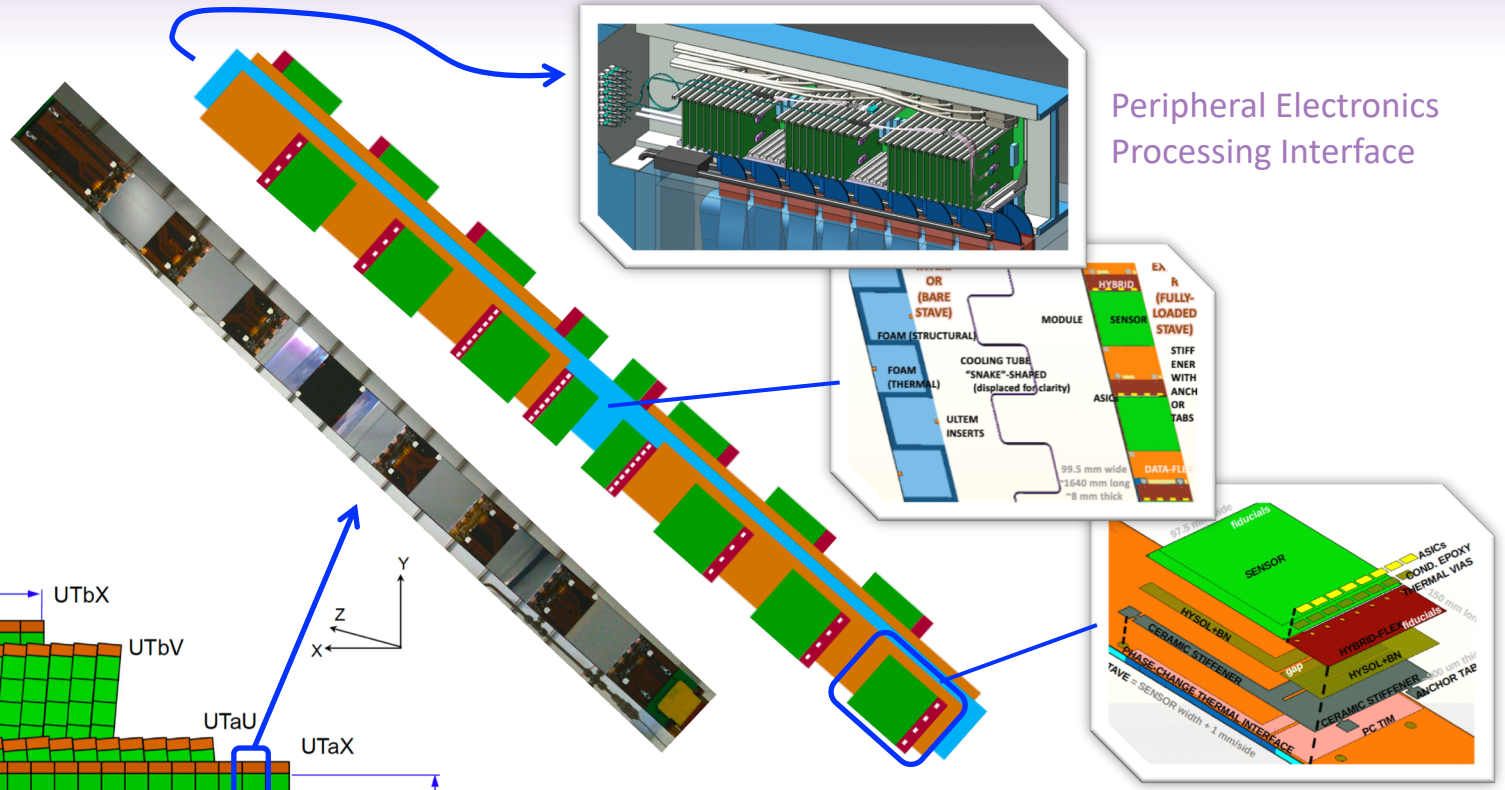
Upstream Tracker (UT)

- Four planes of silicon strip detectors
  - Strips along y-axis (or $\pm$ 5°)
- Higher segmentation near the center
- Readout ASICs: SALT at sensor proximity



Sensor	A	B	C	D
Type	p-in-n	n-in-p	n-in-p	n-in-p
Thickness(μm)	320	250	250	250
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16

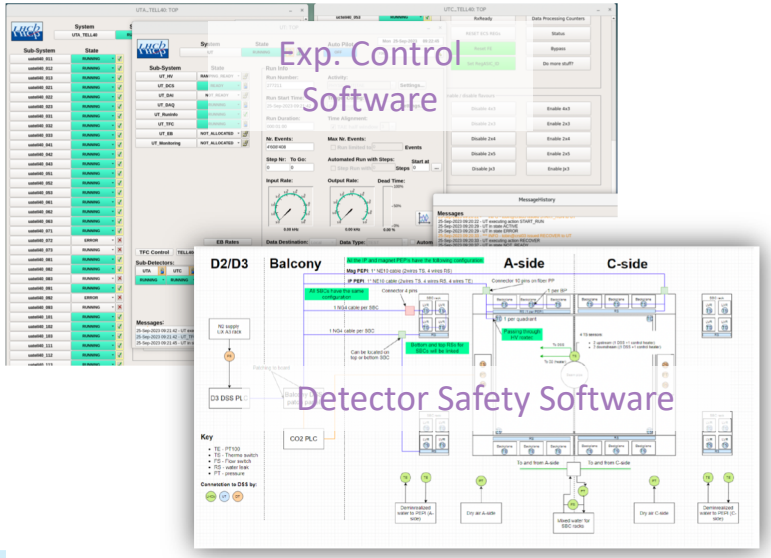


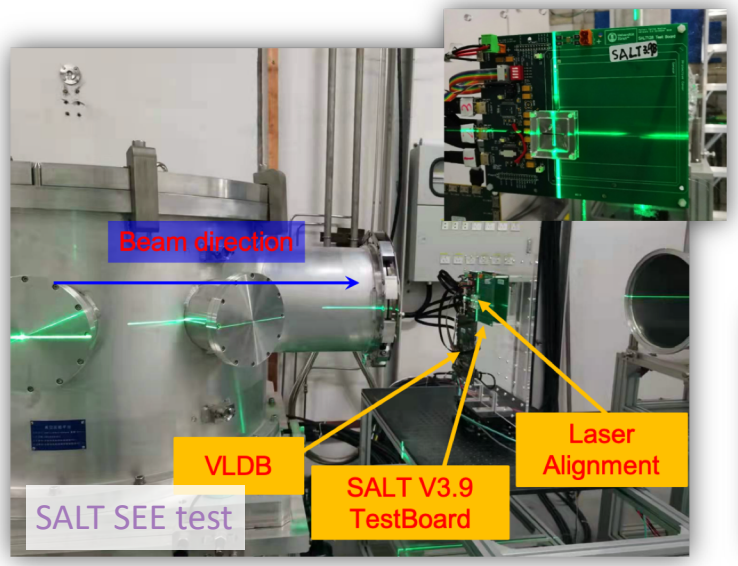


- Modules mounted on both sides of staves to allow overlapping
- Stave: Cooling tube (CO_2) embedded in foam core + CFRP face sheets
- Stave readout at both ends:
  - data formatting, timing distribution, control and optical conversion

Chinese contribution

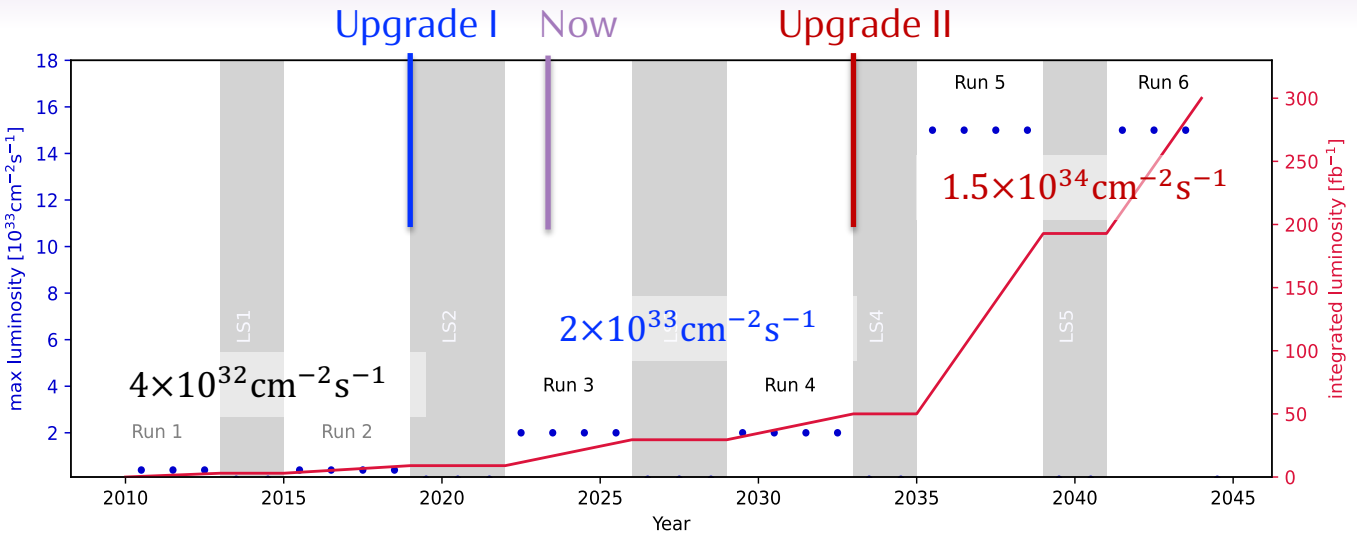
- Chinese groups play a key role
  - Integration and installation at CERN, ensuring Upgrade I completion in time
  - Study of SEE effects in SALT chips using domestic and oversea facilities
  - Developing control & monitoring software





LHCb Upgrade II

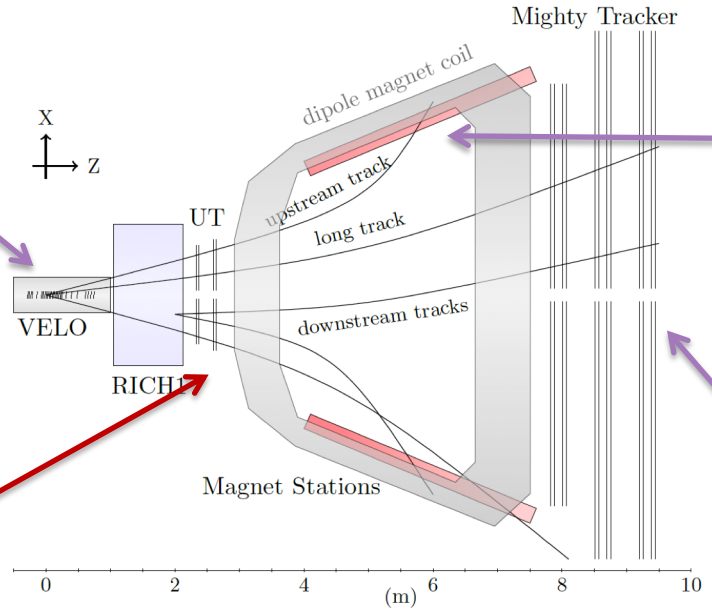
- Upgrade II planned at LS4 to fully exploit the HL-LHC potential in flavor physics & beyond
- Aim for an luminosity of $1.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}}$ and $\mathcal{L}_{\mathrm{int}} \sim 300\ \mathrm{fb^{-1}}$ in the lifetime of LHC



- High-lumi operation challenges:
  - Large pile-up: $\mu \sim 1 \rightarrow 5$ (UI) $\rightarrow$ 40 (UII)
  - High multiplicity ($\rightarrow$ occupancy)
  - Severe radiation damage

- Efficient tracking in real-time is crucial!

New technology Adding timing info



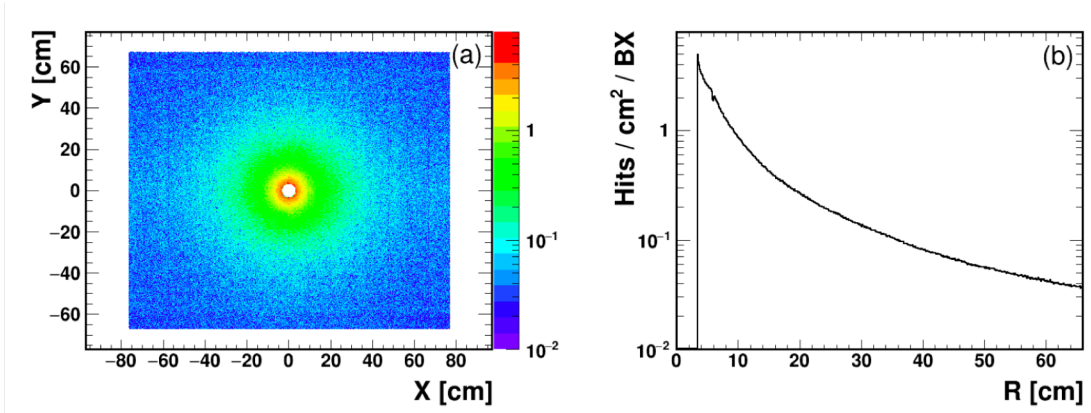
New detector inside magnet to improve low momentum tracking

Will the current UT work under UII condition?

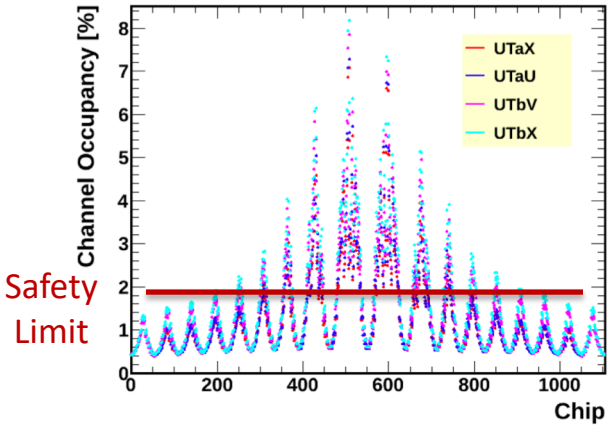
Inner part of SciFi replaced with CMOS

Challenges for UT in Upgrade II

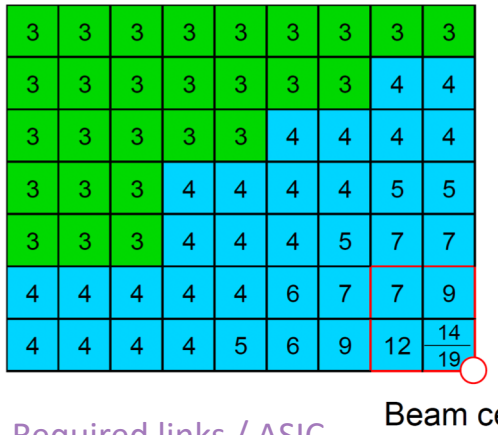
- Simulation performed with UT in UII condition
  - Max hit density ~ 6 hits/cm^2/BX for beam-beam crossings in pp
  - For Pb-Pb ~ 3 hits/cm^2/BX, but multiplicity is higher
- Current UT cannot work safely after × 7.5 increase in luminosity!
  - Max occupancy ~10%
  - Data rate much more than current UT can handle
  - Max fluence of ~ 3×10^{15} n_{eq}/cm^2 may be too high for current sensor



Hit density in a layer under UII condition



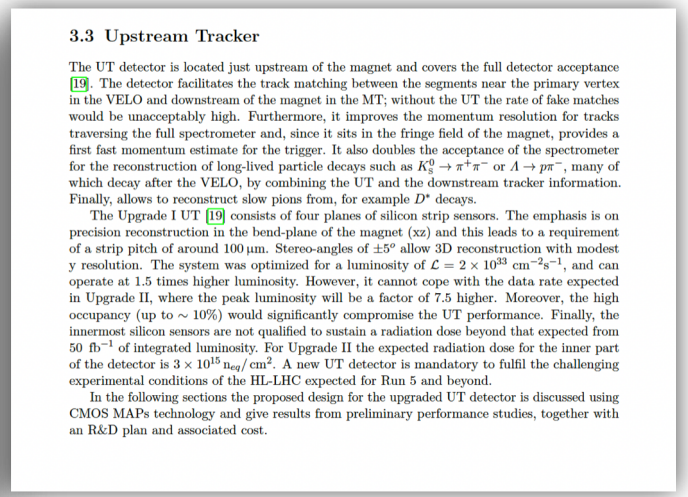
Channel occupancy



Required links / ASIC
Max 5 available!

MAPS-based UT upgrade

- Proposal for a new UT using CMOS MAPS technology
  - Higher granularity for high multiplicity
  - Better radiation tolerance
- R&D collaboration (U2UT) formed mainly by Chinese and French institutes



3.3 Upstream Tracker

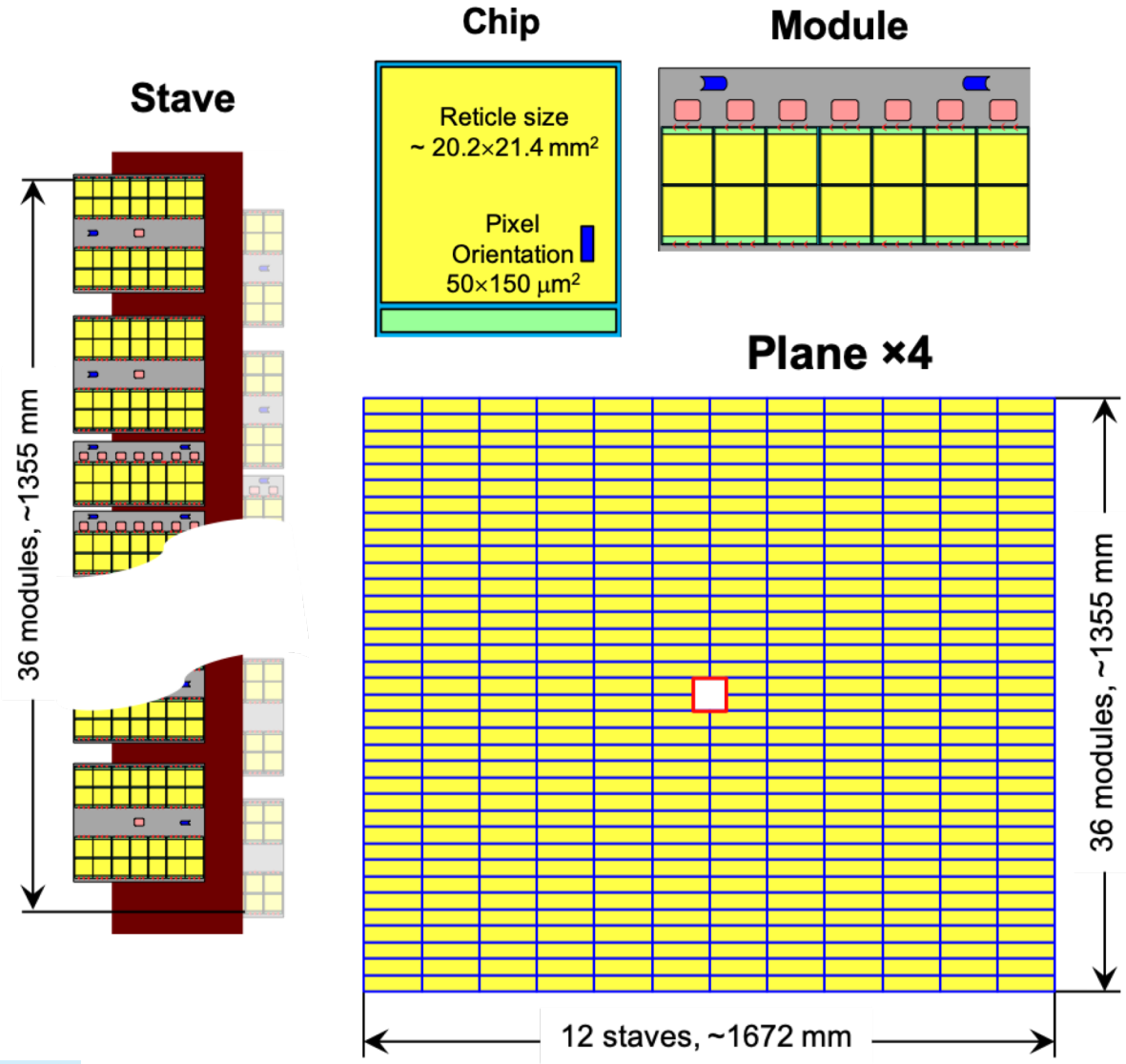
The UT detector is located just upstream of the magnet and covers the full detector acceptance [19]. The detector facilitates the track matching between the segments near the primary vertex in the VELO and downstream of the magnet in the MT; without the UT the rate of fake matches would be unacceptably high. Furthermore, it improves the momentum resolution for tracks traversing the full spectrometer and, since it sits in the fringe field of the magnet, provides a first fast momentum estimate for the trigger. It also doubles the acceptance of the spectrometer for the reconstruction of long-lived particle decays such as $K^0_S \to \pi^+\pi^-$ or $\Lambda \to p\pi^-$, many of which decay after the VELO, by combining the UT and the downstream tracker information. Finally, allows to reconstruct slow pions from, for example D^* decays.

The Upgrade I UT [19] consists of four planes of silicon strip sensors. The emphasis is on precision reconstruction in the bend-plane of the magnet (xz) and this leads to a requirement of a strip pitch of around 100 µm. Stereo-angles of $\pm 5°$ allow 3D reconstruction with modest y resolution. The system was optimized for a luminosity of $\mathcal{L} = 2 \times 10^{33}$ cm^{-2}s^{-1}, and can operate at 1.5 times higher luminosity. However, it cannot cope with the data rate expected in Upgrade II, where the peak luminosity will be a factor of 7.5 higher. Moreover, the high occupancy (up to $\sim 10\%$) would significantly compromise the UT performance. Finally, the innermost silicon sensors are not qualified to sustain a radiation dose beyond that expected from 50 fb^{-1} of integrated luminosity. For Upgrade II the expected radiation dose for the inner part of the detector is 3×10^{15} n$_{eq}$/cm^2. A new UT detector is mandatory to fulfil the challenging experimental conditions of the HL-LHC expected for Run 5 and beyond.

In the following sections the proposed design for the upgraded UT detector is discussed using CMOS MAPs technology and give results from preliminary performance studies, together with an R&D plan and associated cost.

LHCb Upgrade II TDR, CERN-LHCC-2021-012;
Y. Li, Nucl. Inst. Meth. A 1032 (2022) 166629

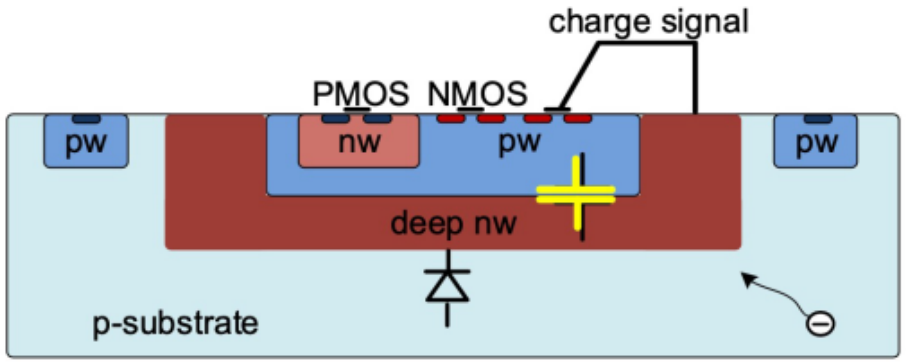
System design



- Preliminary system design proposed
- Certain features of current UT kept
  - Stave structure
  - Strip/ long-pixel orientation
- Shown for HVCMOS technology, similar for small-electrode CMOS

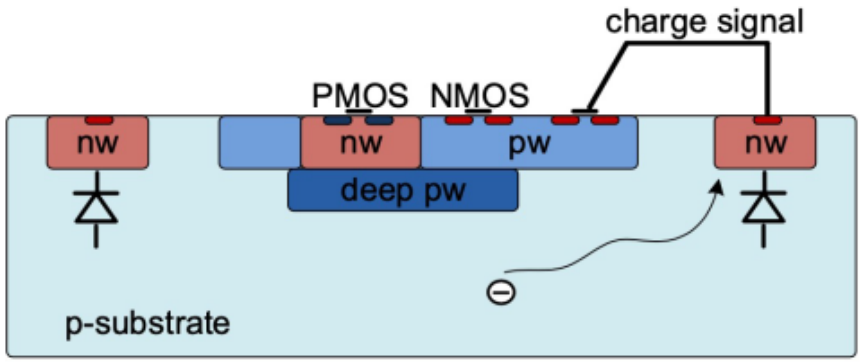
Ring	5	4	3	2	1
e-links / chip	1	1	1	1-3	2-7
Gbps / e-link	0.32	0.64	1.28	1.28	1.28
lpGBT / module	0.5	1	2	7	14/10
Num of modules	1312	240	80	64	32
Num of lpGPTs	656	240	160	448	384

Main sensor options



High Voltage CMOS

- Circuitry inside the charge collection well
- Large uniform electric field
- On average shorter drift path
- Better radiation hardness (less trapping)
- HV-CMOS process commercially available
- Large sensor capacitance (pw and dnw)
- Foundries: TSI-180, Lfoundry-150, …



CMOS with small electrode

- Circuitry outside the charge collection well
- Optimization of little low-field regions
- On average longer drift path
- Radiation hardness needs process modifications
- Very small sensor capacitance
- Foundries: Towerjazz-180, TPSCo-65…

Sensor specifications

Characteristics	LV-CMOS	HV-CMOS
Chip size	3.5 × 3.5 cm^2	2.0 × 2.0 cm^2
Pixel size	30 × 30 um^2	50 × 150 um^2
Chip thickness	~ 100 um	
Position resolution	5-10 um	15, 40 um
Time resolution	O (1) ns	
Power consumption	100 – 300 mW/cm^2	
Radiation dose	3×10^{15} n_{eq}/cm^2, or 240 MRad TID	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s

Capable of distinguishing 25ns bunch crossing

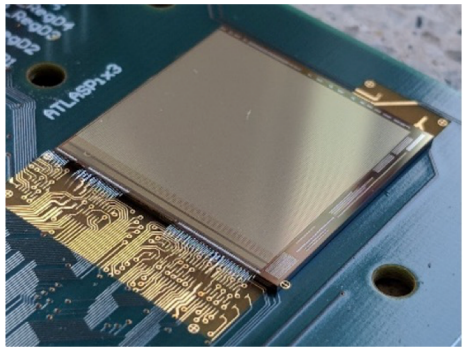
Depends on timing resolution

Affects cooling requirements

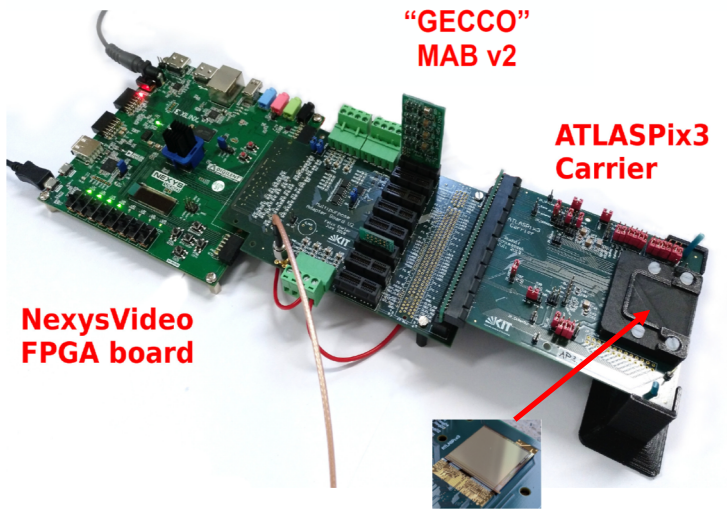
Achievable by HV-CMOS

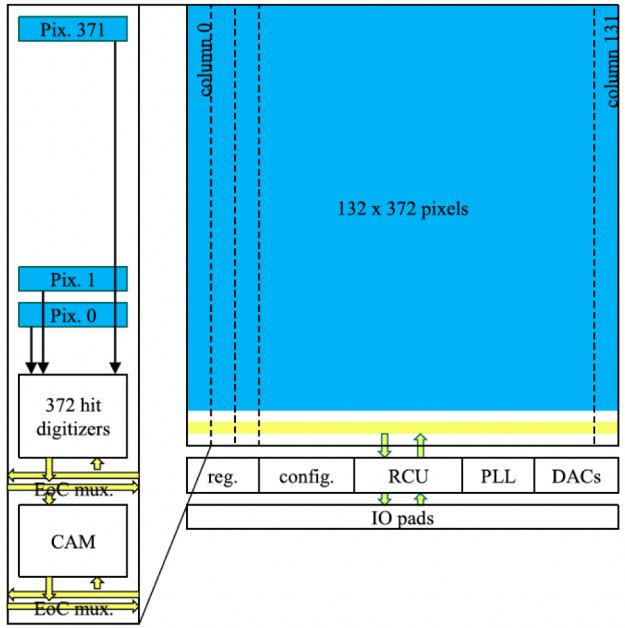
HVCMOS option: ATLASPix3

- ATLASPix3 chip developed for HL-LHC
  - TSI 180nm HV process on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 132 columns × 372 rows (20.2 × 21 mm^2 chip)
  - Time resolution: ~7 (4) ns w/o (with) ToT correction
  - Functioning after ~10^{15} n_{eq}/cm^2
  - Power consumption ~160 mW/cm^2
- Also serves as potential candidate for CEPC tracker



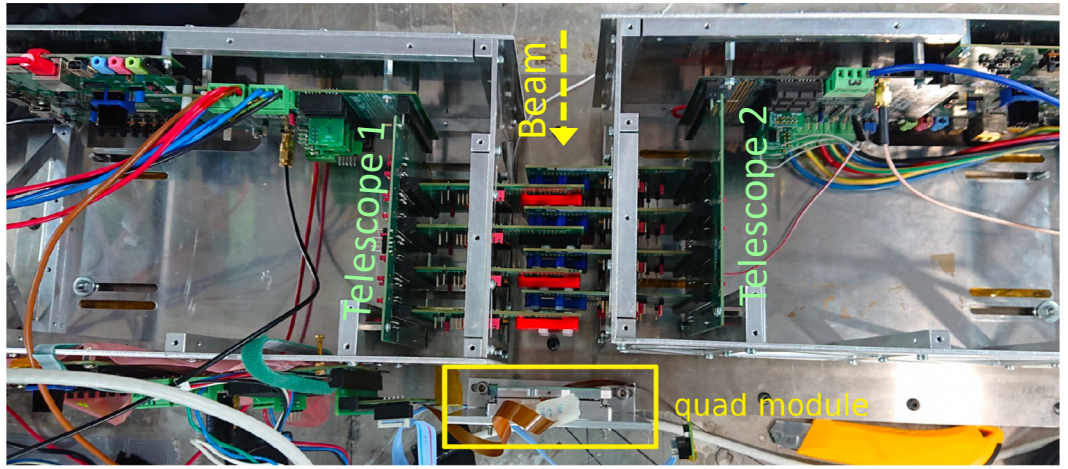
I. Peric et al., IEEE JSSC, Vol 56, No.8, Aug. 2021



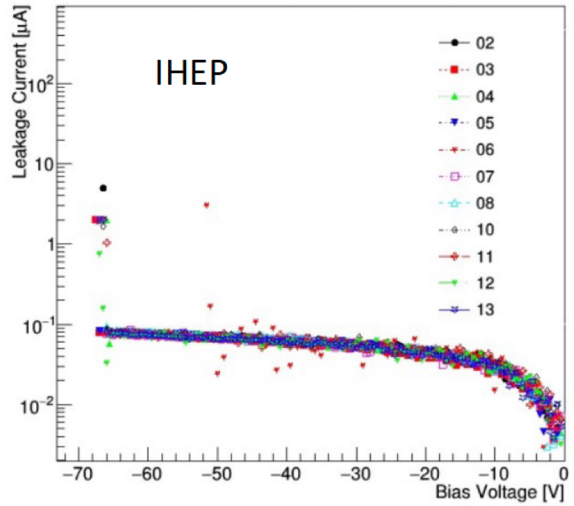


Test with ATLASPix3

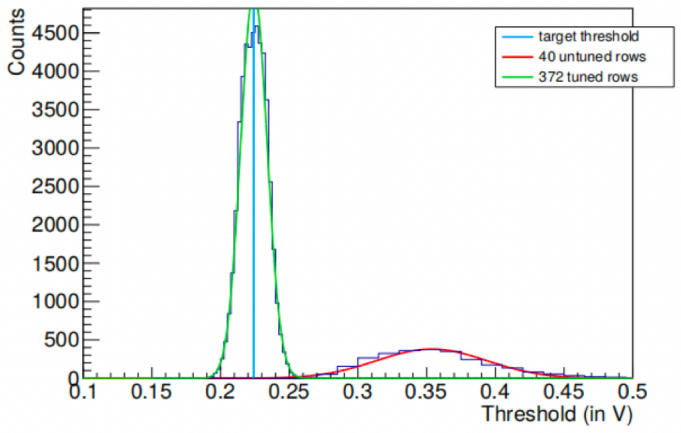
- The ATLASPix3.1 chips had been extensively tested at IHEP, readout using a GECCO system.
- Threshold trimming and noise performance, noise ~60 e for threshold ~1700 e.
- Tested in cosmic ray, various radioactive sources and electron beams



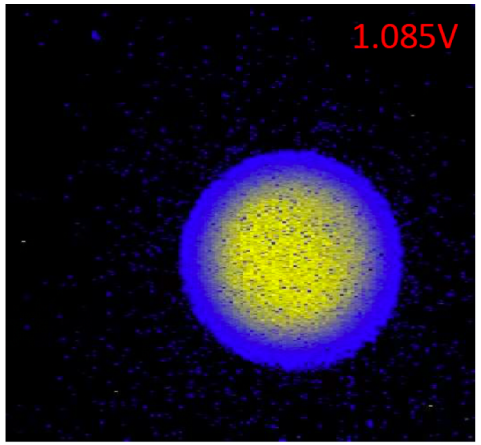
Beamtest at DESY 2022



IV measurement

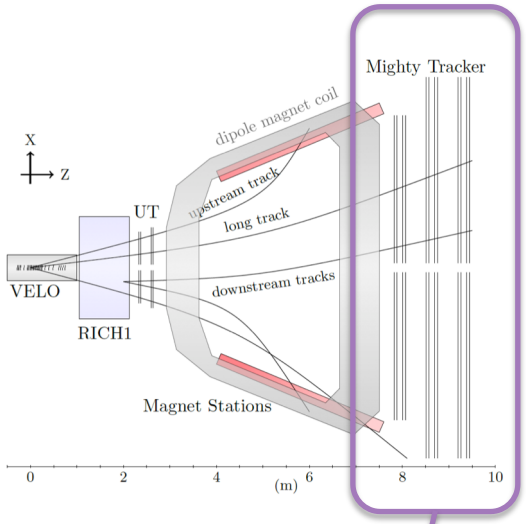


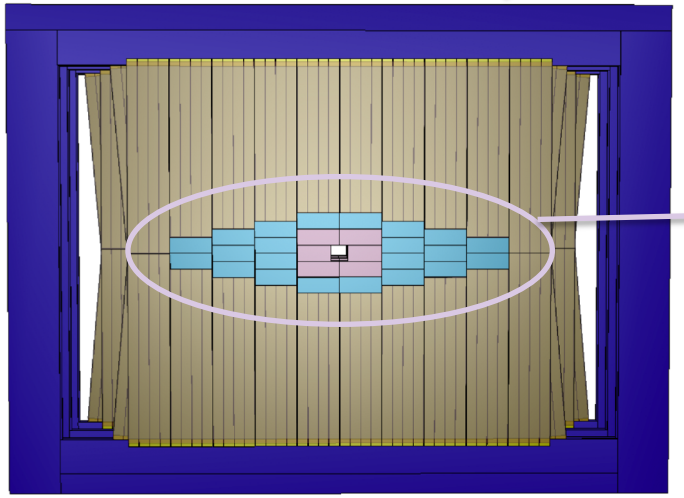
Threshold trimming



Hitmap with Fe55 source

Synergy with Mighty Tracker





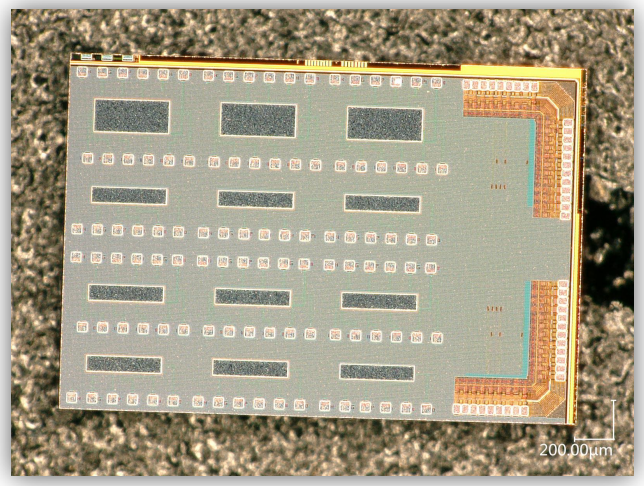
- Innermost region of SciFi will be replace by CMOS tracker
- Less radiation, more complex integration
  - Partial installation expected in LS3!
- R&D based on HV-CMOS
  - Initial tests with ATLASPix3
- MightyPix series under development
  - Implemented in TSI 180nm process
  - MightyPix1 submitted in May 2022, test ongoing

Pixel size	< 100 µm x 300 µm
In-time efficiency	> 99% within 25 ns window
Timing resolution	~ 3 ns within 25 ns window
Radiation tolerance	6 x 10^{14} 1 MeV n_{eq}/cm^2
Power consumption	< 150 mW/cm^2
Data transmission	4 links of 1.28 Gb/s each
Compatibility with the LHCb readout system	

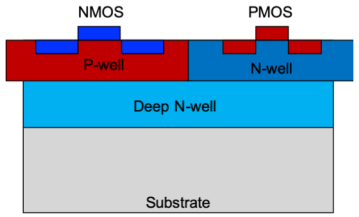
MightyPix1 floorplan
¼ of a full matrix size

Validation of 55nm HVCMOS process

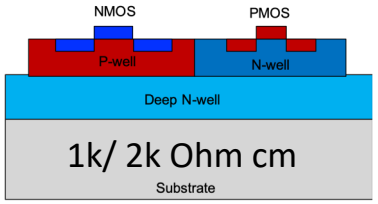
- Smaller node = higher circuit density + lower power consumption!
- Design and test team: IHEP, KIT, Hunan U., …
- Oct 2022: First MPW submitted in 55nm LL process in low resistance wafer
  - Similar deep N well structure under transistors -> the major validation target
- Aug 2023: Second MPW submitted in 55nm HV process with high-resistance wafer
  - Validation of HV diode + small pixel array + limited digital design
- Future development expected if results from Aug MPW look promising



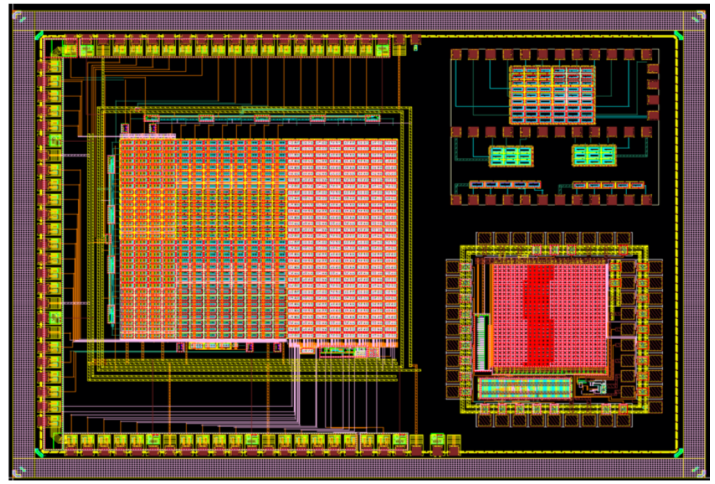
Chip from 2022 MPW



LL process



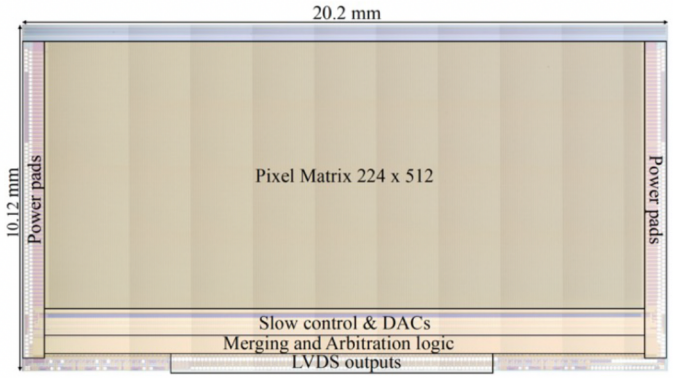
HV process

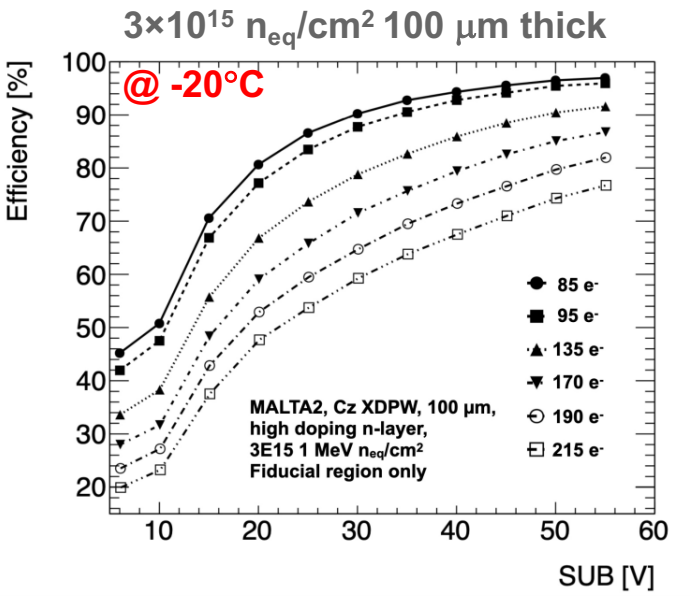


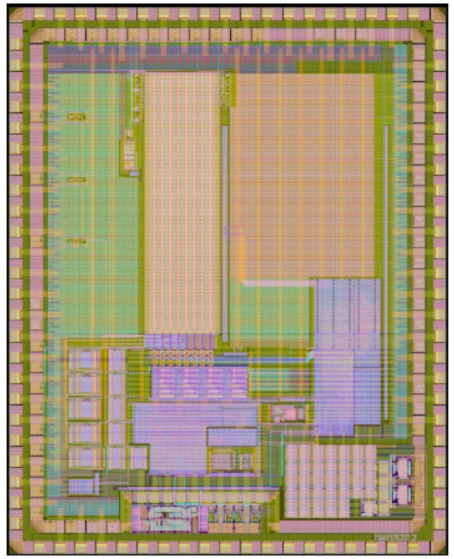
Design for 2023 MPW

Small electrode CMOS: TowerJazz MALTA

- TJ 180 nm CMOS modified process
  - Pixel size: $36.4 \times 33\ \mu m^2$
  - Proven $3{\times}10^{15}\ n_{eq}cm^{-2}$, 100 MRad @ $-20°C$
- MALTA2 tested at CEA-IRFU
  - Average noise ~12 e as expected, homogenous over the matrix
- MALTA3 submitted in Q2 2023
  - Triggerless readout, serialized output
- UT specific verification to be investigated



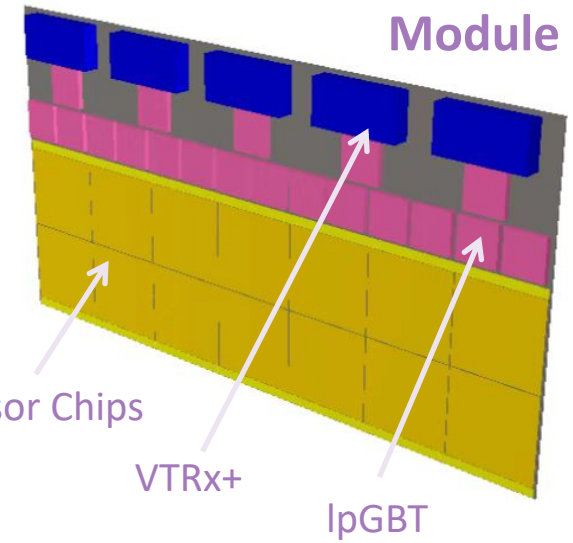


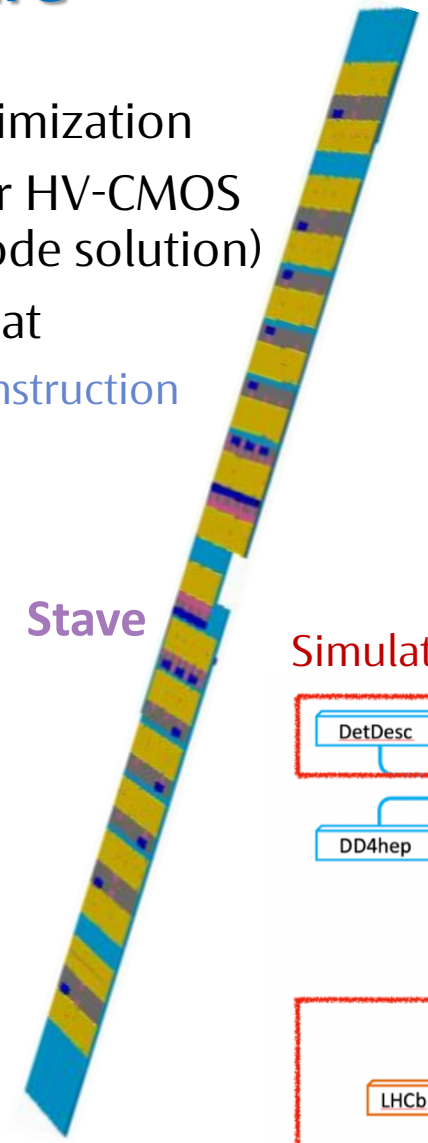


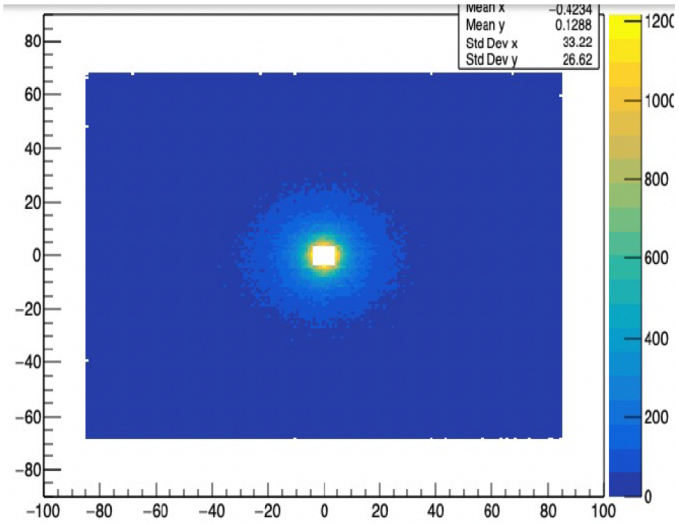
MALTA 3 layout

Detector modelling in software

- Full simulation mandatory for design optimization
- Detector description has been created for HV-CMOS solution (easily adaptable to small electrode solution)
- Created in both DDDB and DD4HEP format
  - Integration into LHCb simulation and reconstruction software framework ongoing



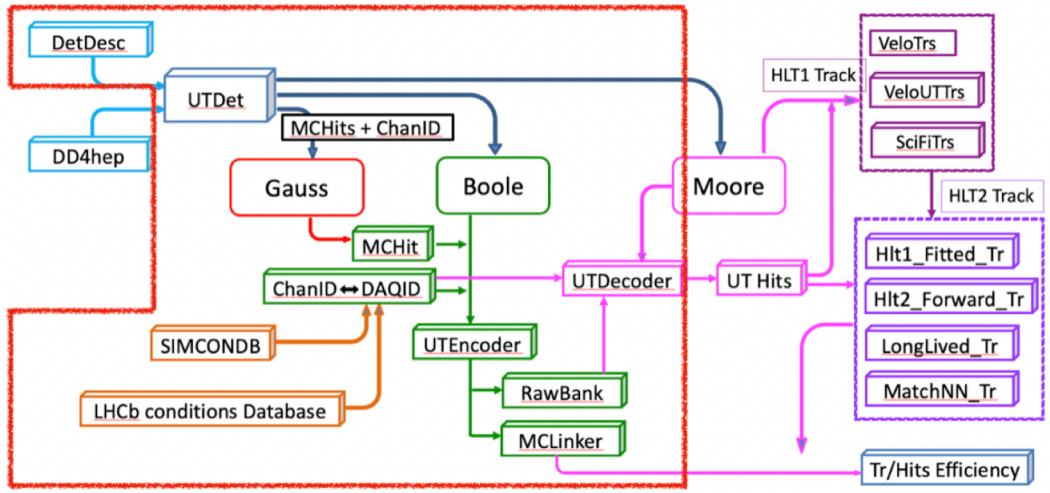




Hitmap in Run 5/6 condition

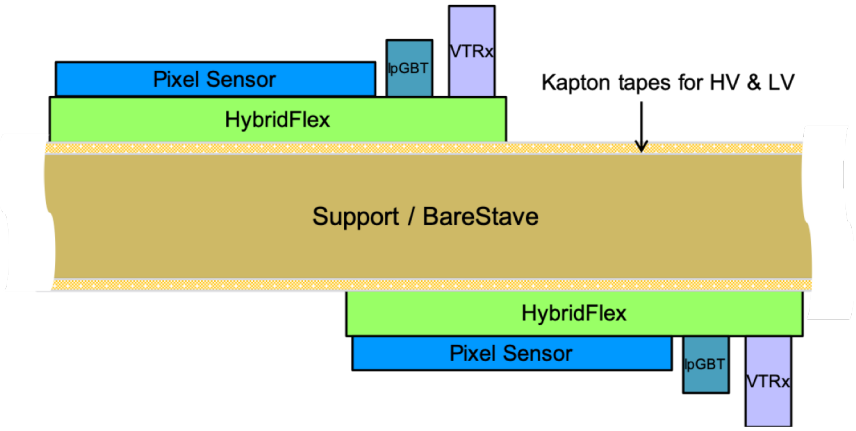
Simulation & digitization finished

Tracking under work

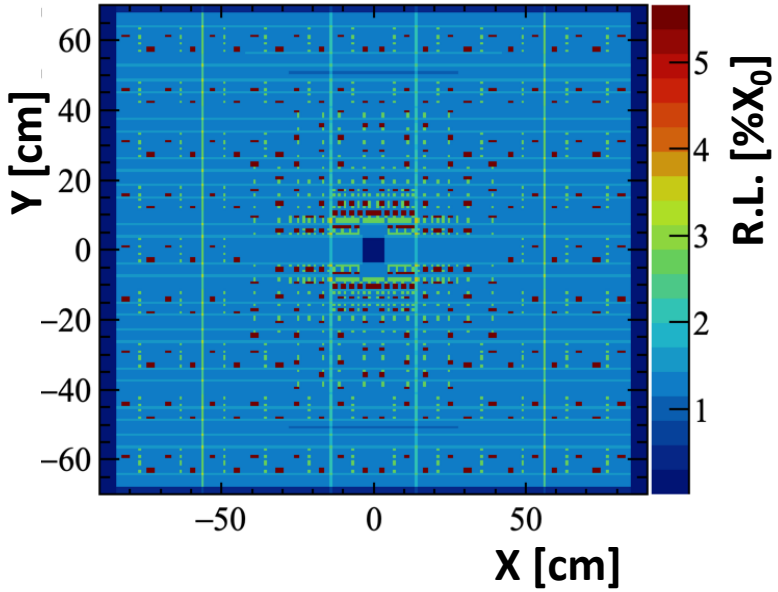


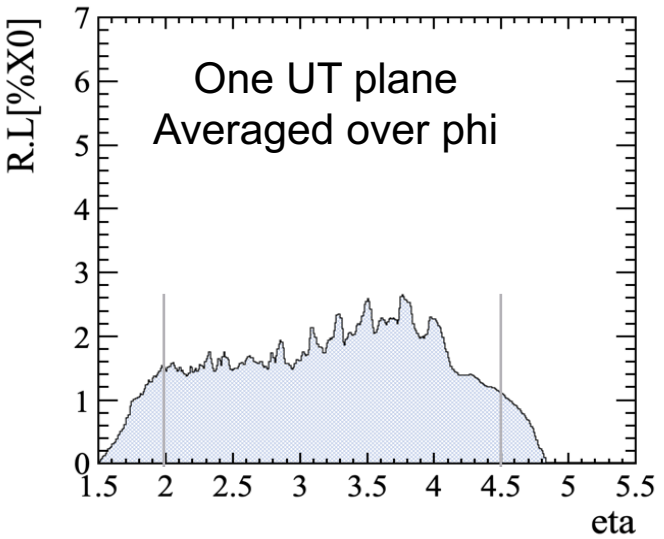
Material scan

- Material scan performed with a simplified stave structure
  - Detailed composite of VTRx+ and lpGBT not known
  - Not all electronics components included
  - Yet a good starting point for material budget study



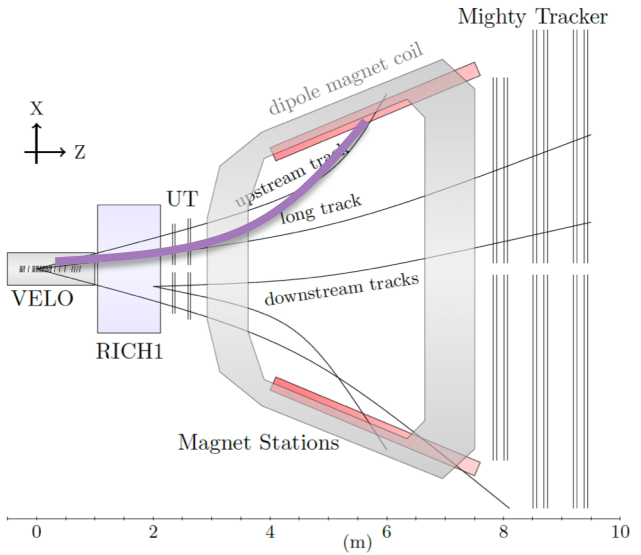
(Preliminary)	Thickness [mm]	RL (2<h<4.5) [% X_0]
Pixel Sensor	0.200	0.24
lpGBT	1.250	0.25
VTRx+	4.000	0.27
HybridFlex	0.300	0.42
Kapton Tape	0.100	0.14
BareStave	4.000	0.21
One plane	**-**	**1.54**





Detector Optimisation

- Detailed studies foreseen to define / to optimise the UT design
  - Impact on tracking performance of VELO-UT(-MS)
  - Detector acceptance optimization associated with magnet station
  - Optimisation on number and layout of layers (3 vs. 4)
  - Estimation of material budget and cooling options
  - Effect of a possible additional timing layer with different technology
  - …



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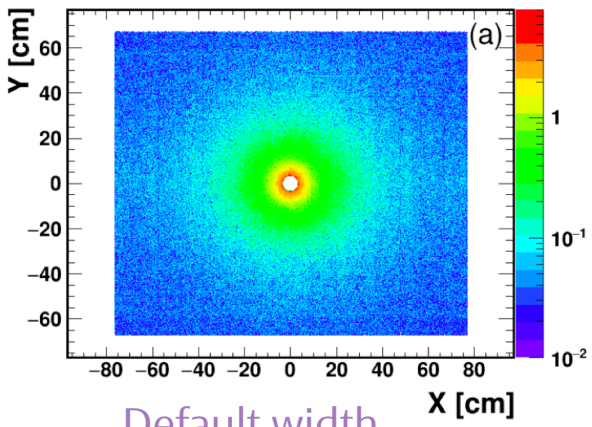

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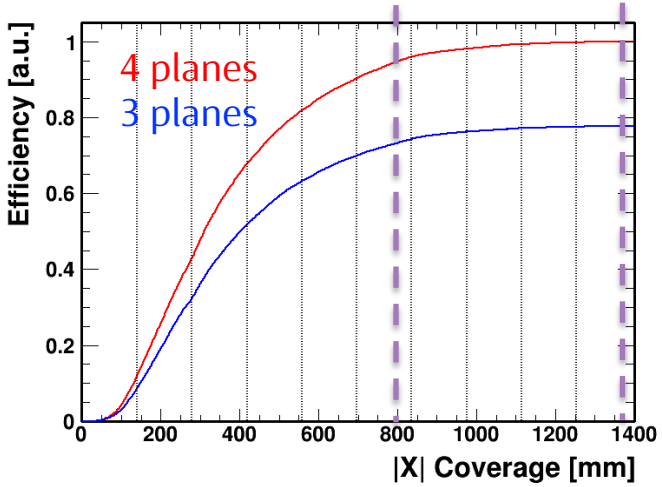

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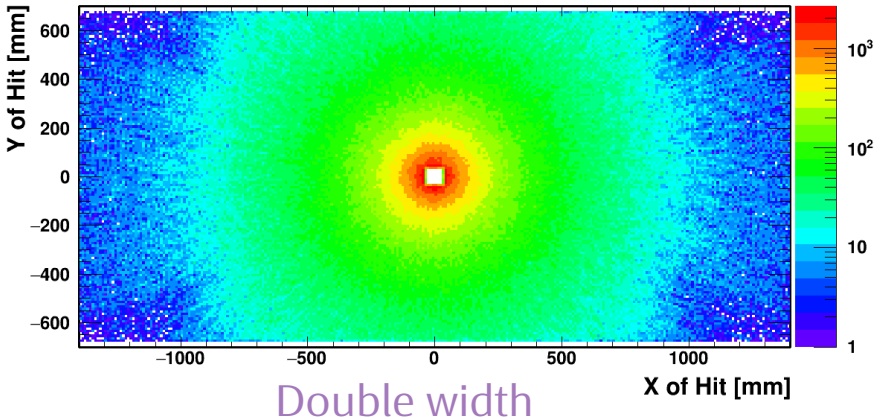

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Summary

- LHCb UT has been successfully installed and being commissioned
- For Upgrade II a new UT is compulsory, R&D for a MAPS-based U2UT is ongoing aiming for TDR ~2027
  - HV-CMOS and small-electrode CMOS options
  - Full simulation and optimization studies kicked off
- Chinese and French groups are backbones of the the MAPS-based UT development
- Your participation and interests are welcome