9-12月考核汇报

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CONTENT

1. MMC固件开发

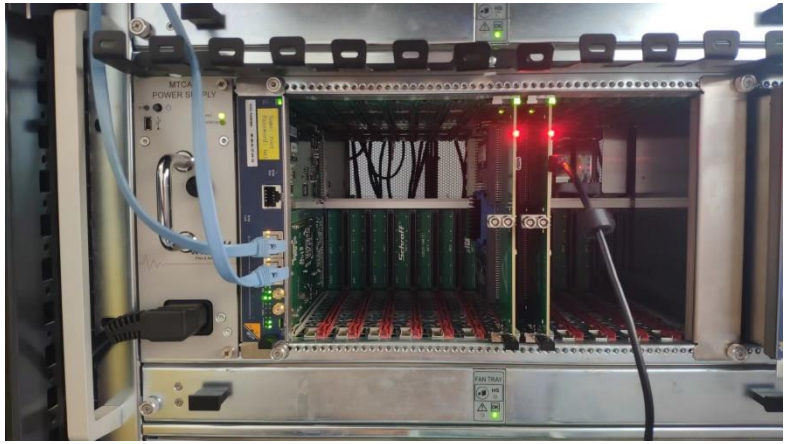
- 在基于RISC-V架构的MCU GD32VF103上实现了MicroTCA机箱AMC板卡的模块管理控制固件

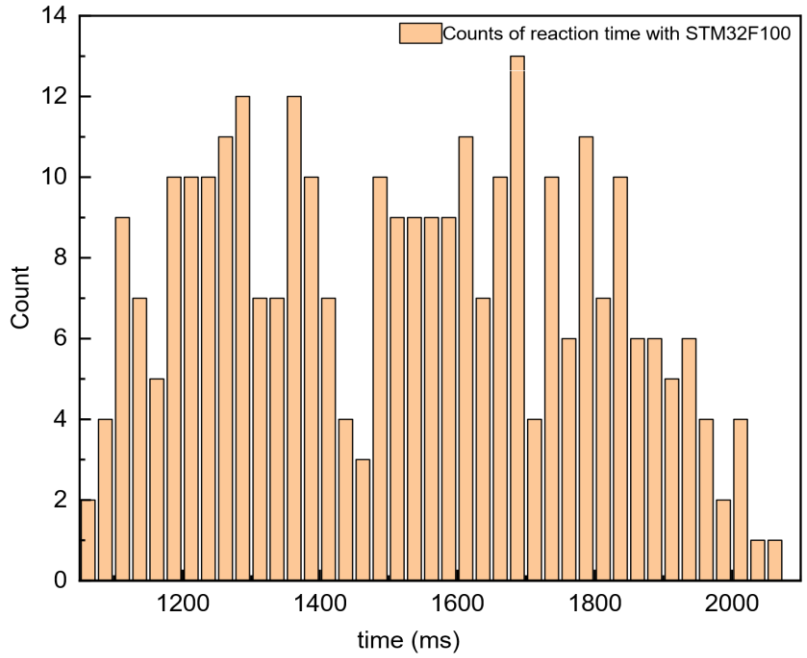
1. MMC固件开发

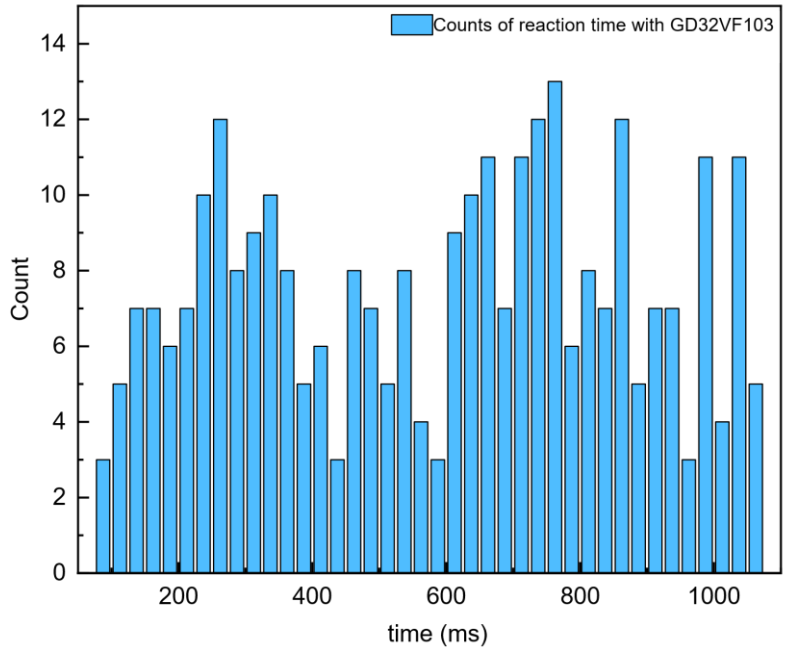
- **对比MMC固件在STM32F100和GD32VF103上运行热插拔功能的时间**

响应时间：从插拔产生中断开始计时，板卡上电稳定结束计时，300次测试

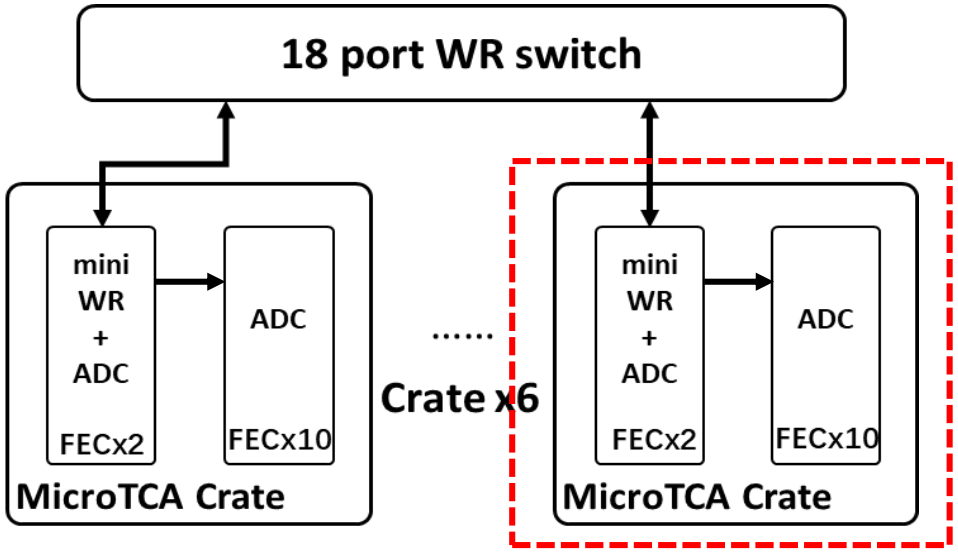
reaction time	STM32F100	GD32VF103
Mean (ms)	1519.66447	586.7133333
minimum (ms)	1072	84
maximum (ms)	2067	1072





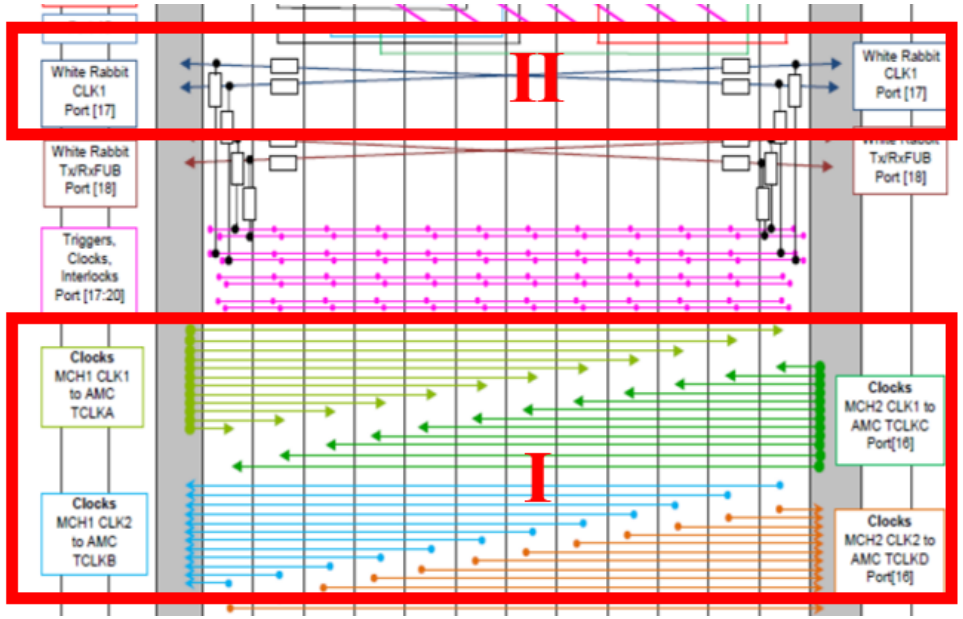


2. WR时钟测试



Clock synchronization system structure

- 方案一：通过MCH控制器进行点对点扇出(CLK1 CLK2)
- 方案二：基于背板M - LVDS总线进行广播扇出(port 17)

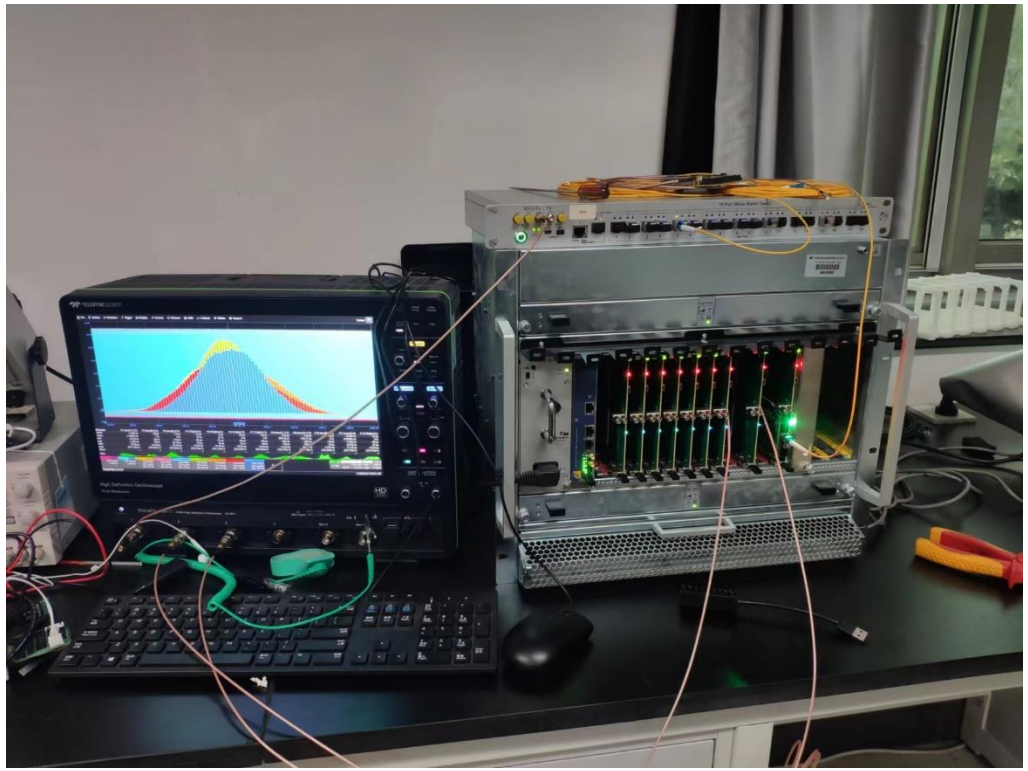


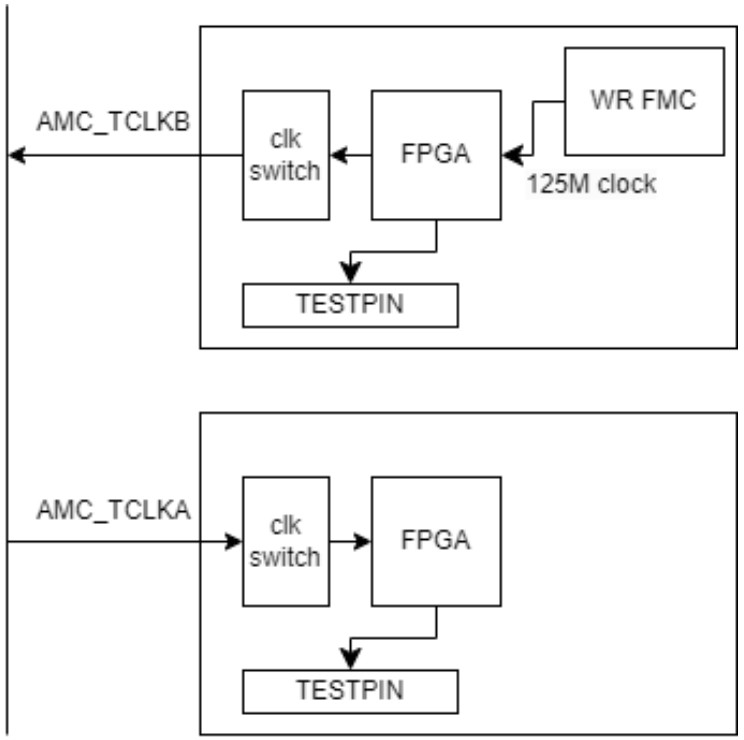
对于方案一，需要修改MCH配置文件时钟配置部分，实现：

- MCH1 CLK1 to AMC TCLKA
- AMC TCLKB to MCH1 CLK2

2. WR时钟测试

- 确定时钟测试方案





工作：

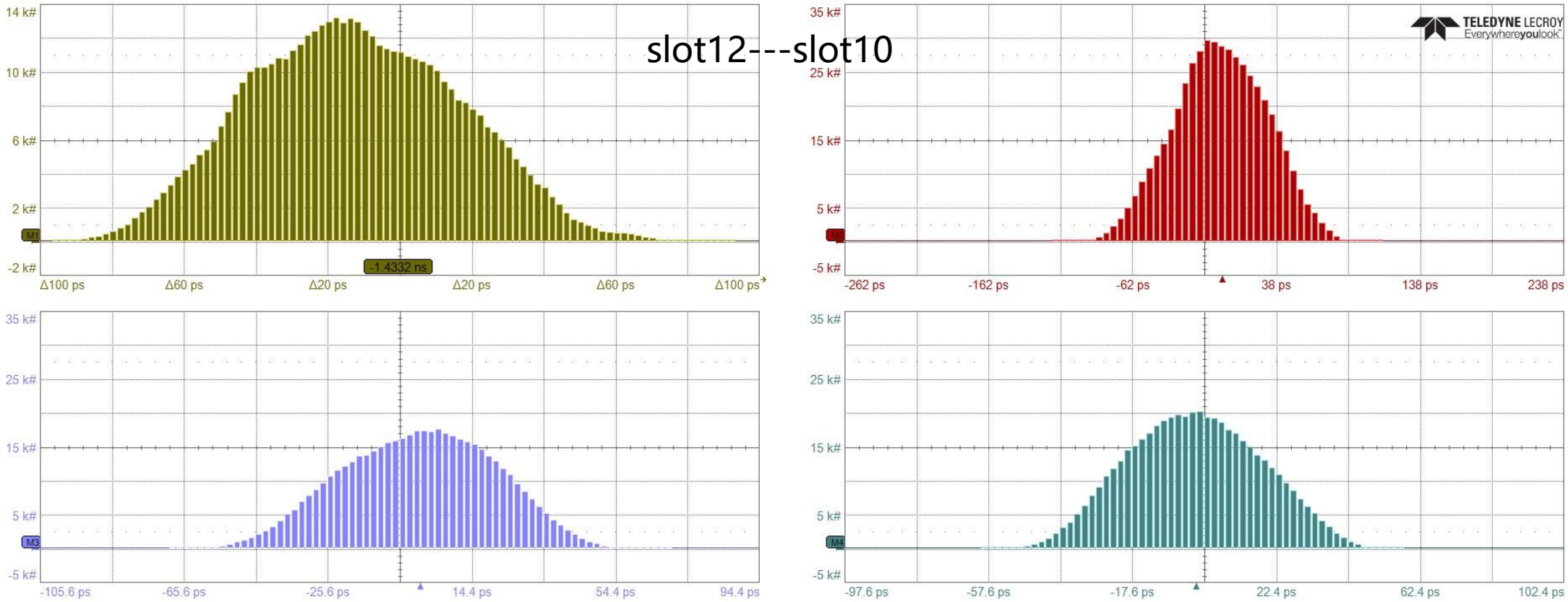
a) FPGA测试配置

b) MCU时钟配置；

c) python测试脚本编写

d) 数据处理

2. WR时钟测试



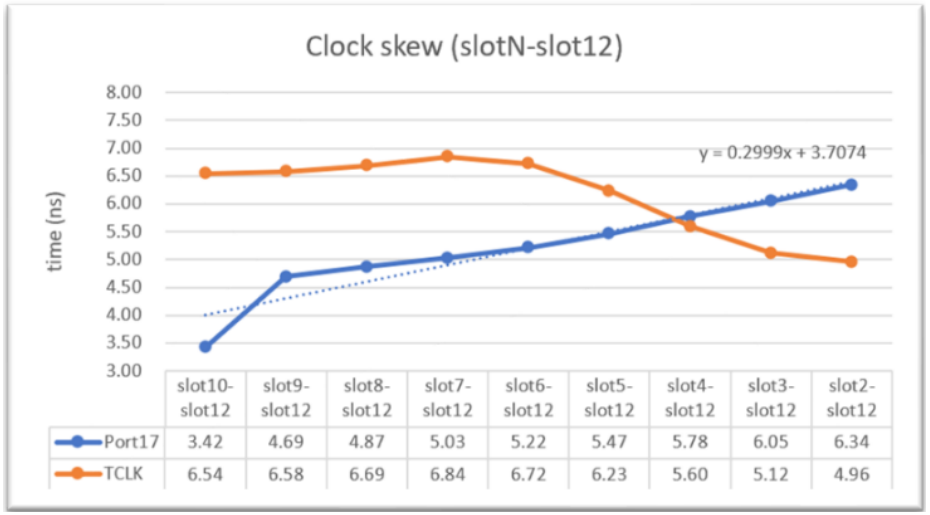
Measure	P1:skew(C2,C3)	P2:dper@lv(C2)	P3:dper@lv(C3)	P4:TIE@lv(C2)	P5:TIE@lv(C3)	P6:TIE@lv(C2)	P7:TIE@lv(C3)	P8:---	P9:---	P10:---	P11:---	P12:---
value	-1.489 ns	20 ps	41 ps	2 ps	14 ps	8 ps	12 ps					
mean	-1.44583 ns	0 fs	0 fs	27 fs	28 fs	0 fs	0 fs					
min	-1.531 ns	-61 ps	-108 ps	-38 ps	-69 ps	-40 ps	-65 ps					
max	-1.341 ns	76 ps	121 ps	41 ps	70 ps	37 ps	61 ps					
sdev	29.16 ps	25.56 ps	32.23 ps	14.06 ps	21.06 ps	12.73 ps	18.35 ps					
num	527.078e+3	526.234e+3	526.656e+3	526.656e+3	527.078e+3	527.078e+3	527.500e+3					
status	✔	✔	✔	✔	✔	✔	✔					
histo												

M1	M2	M3	M4
2.00 k#/div	5.00 k#/div	5.00 k#/div	5.00 k#/div
20.0 ps/div	50.0 ps/div	20.0 ps/div	20.0 ps/div
500.000 k#	500.000 k#	500.000 k#	500.000 k#

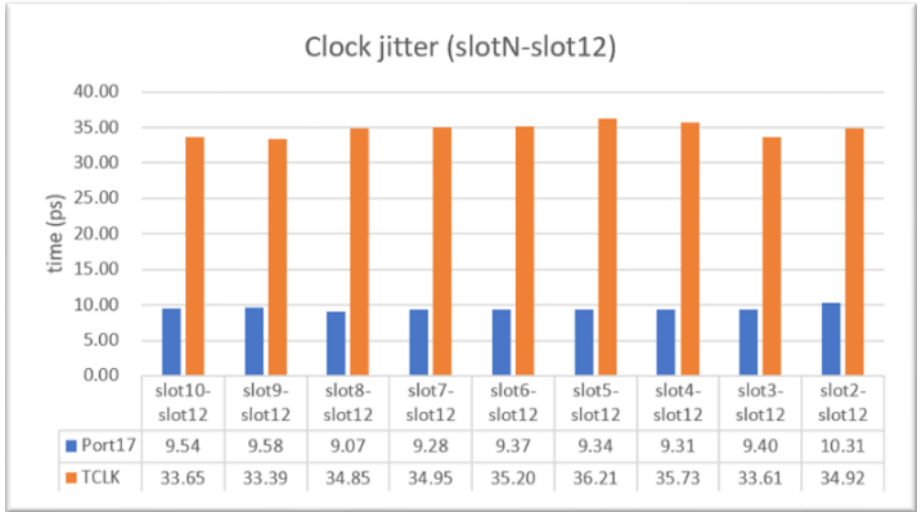
HD	Tbase	0.00 µs	Trigger	C2 DC
12 Bits	1.00 µs/div		Stop	1.670 V
	100 kS	10 GS/s	Edge	Positive

2. WR时钟测试

带有Mini-WR的AMC在 slot12 ,移动AMC接收板槽位



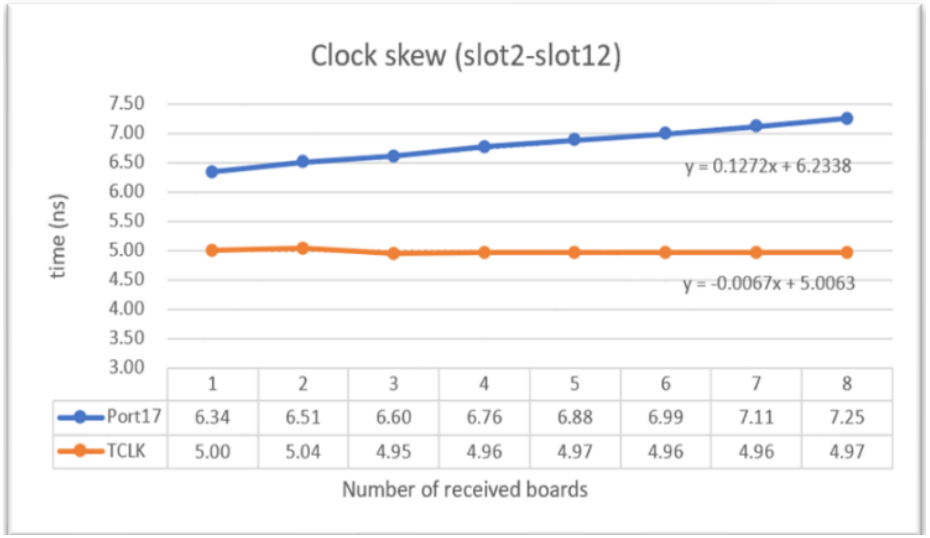
	slot10-slot12	slot9-slot12	slot8-slot12	slot7-slot12	slot6-slot12	slot5-slot12	slot4-slot12	slot3-slot12	slot2-slot12
Port17	3.42	4.69	4.87	5.03	5.22	5.47	5.78	6.05	6.34
TCLK	6.54	6.58	6.69	6.84	6.72	6.23	5.60	5.12	4.96



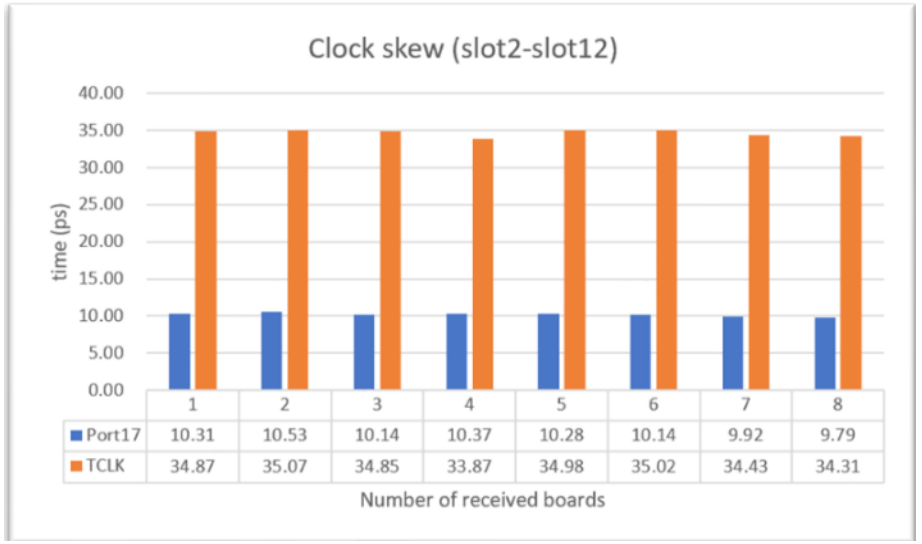
	slot10-slot12	slot9-slot12	slot8-slot12	slot7-slot12	slot6-slot12	slot5-slot12	slot4-slot12	slot3-slot12	slot2-slot12
Port17	9.54	9.58	9.07	9.28	9.37	9.34	9.31	9.40	10.31
TCLK	33.65	33.39	34.85	34.95	35.20	36.21	35.73	33.61	34.92

- TCLK方案具有确定性的偏斜，但抖动更大

带有Mini-WR的AMC在 slot12 ,测试的AMC接收板在slot2, 增加板卡数量



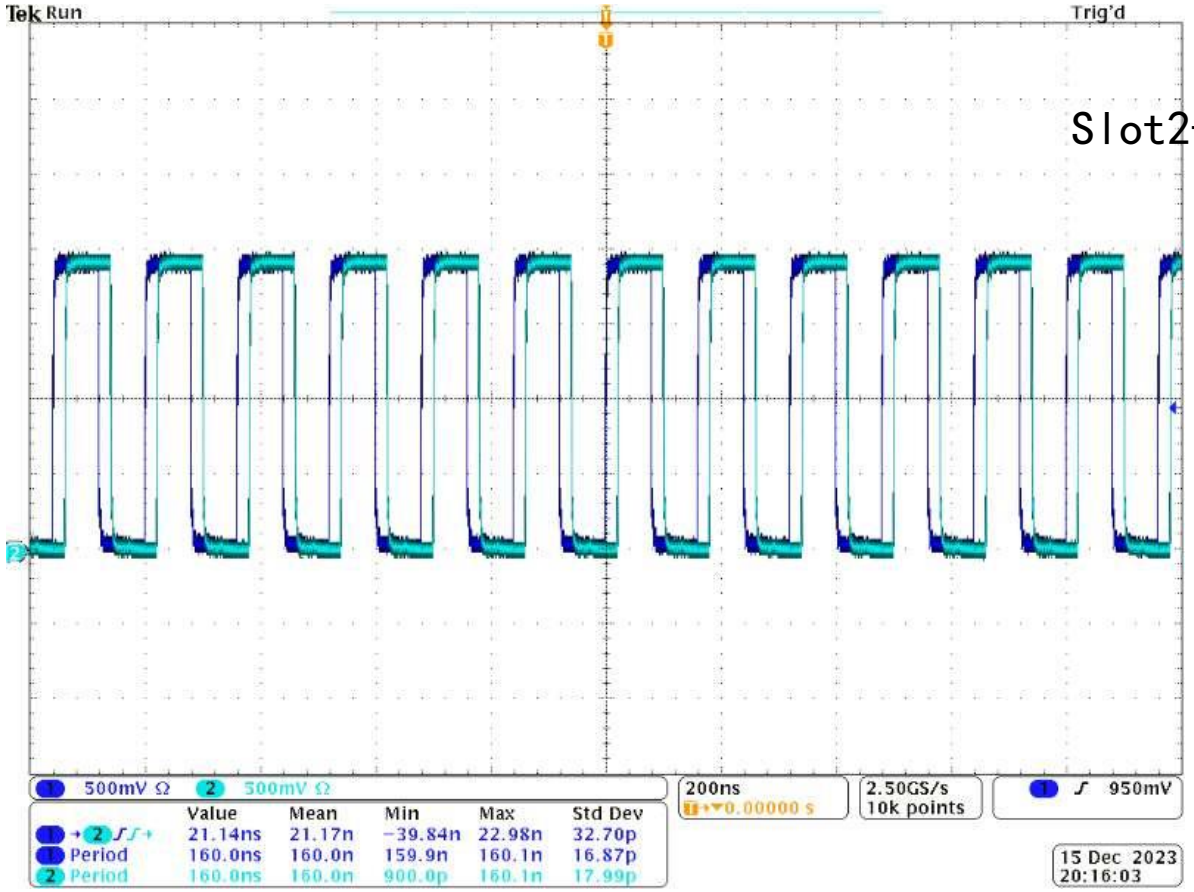
	1	2	3	4	5	6	7	8
Port17	6.34	6.51	6.60	6.76	6.88	6.99	7.11	7.25
TCLK	5.00	5.04	4.95	4.96	4.97	4.96	4.96	4.97



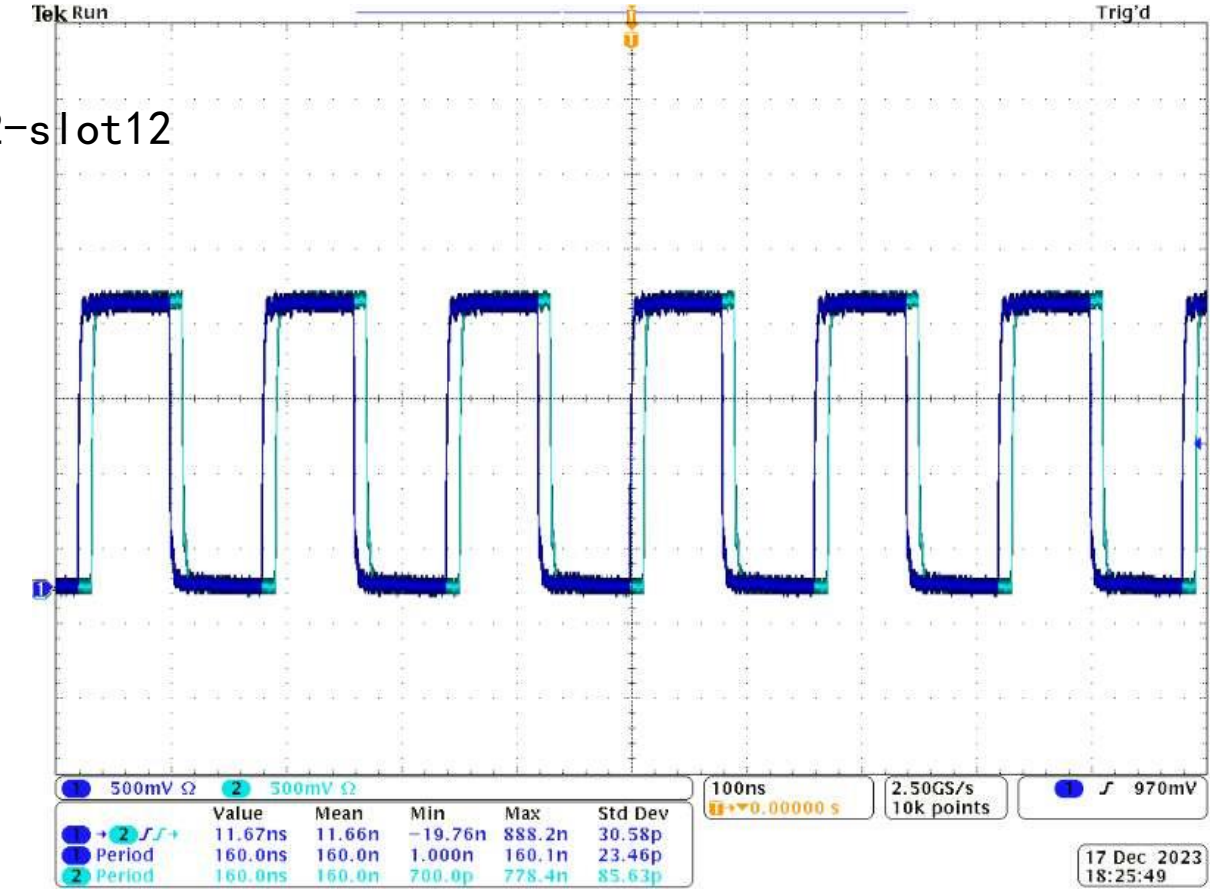
	1	2	3	4	5	6	7	8
Port17	10.31	10.53	10.14	10.37	10.28	10.14	9.92	9.79
TCLK	34.87	35.07	34.85	33.87	34.98	35.02	34.43	34.31

- Port17方案具有较小的抖动，但偏斜与位置和接收器数量有关

2. WR时钟测试



Slot2-slot12

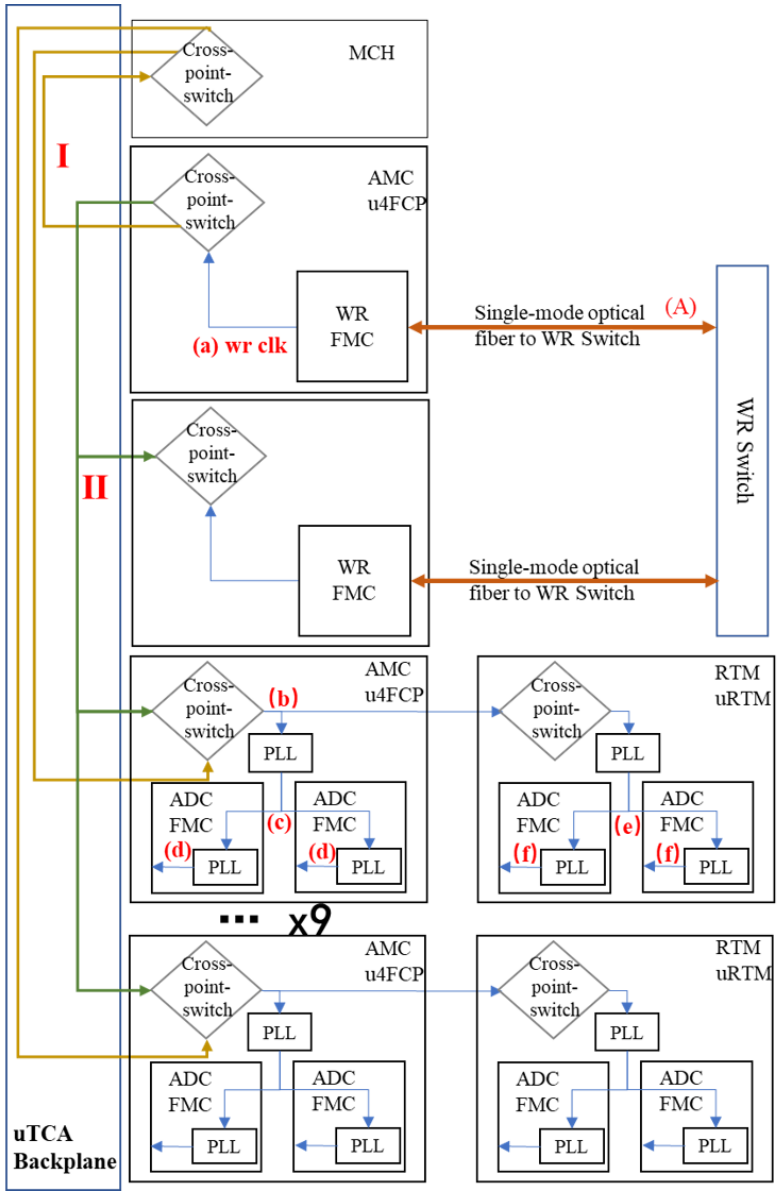


TCLK: 21.14 ns

Port17: 11.67 ns

3. 下一步计划

- 继续时钟测试



THANKS