课题三：ALICE探测器升级

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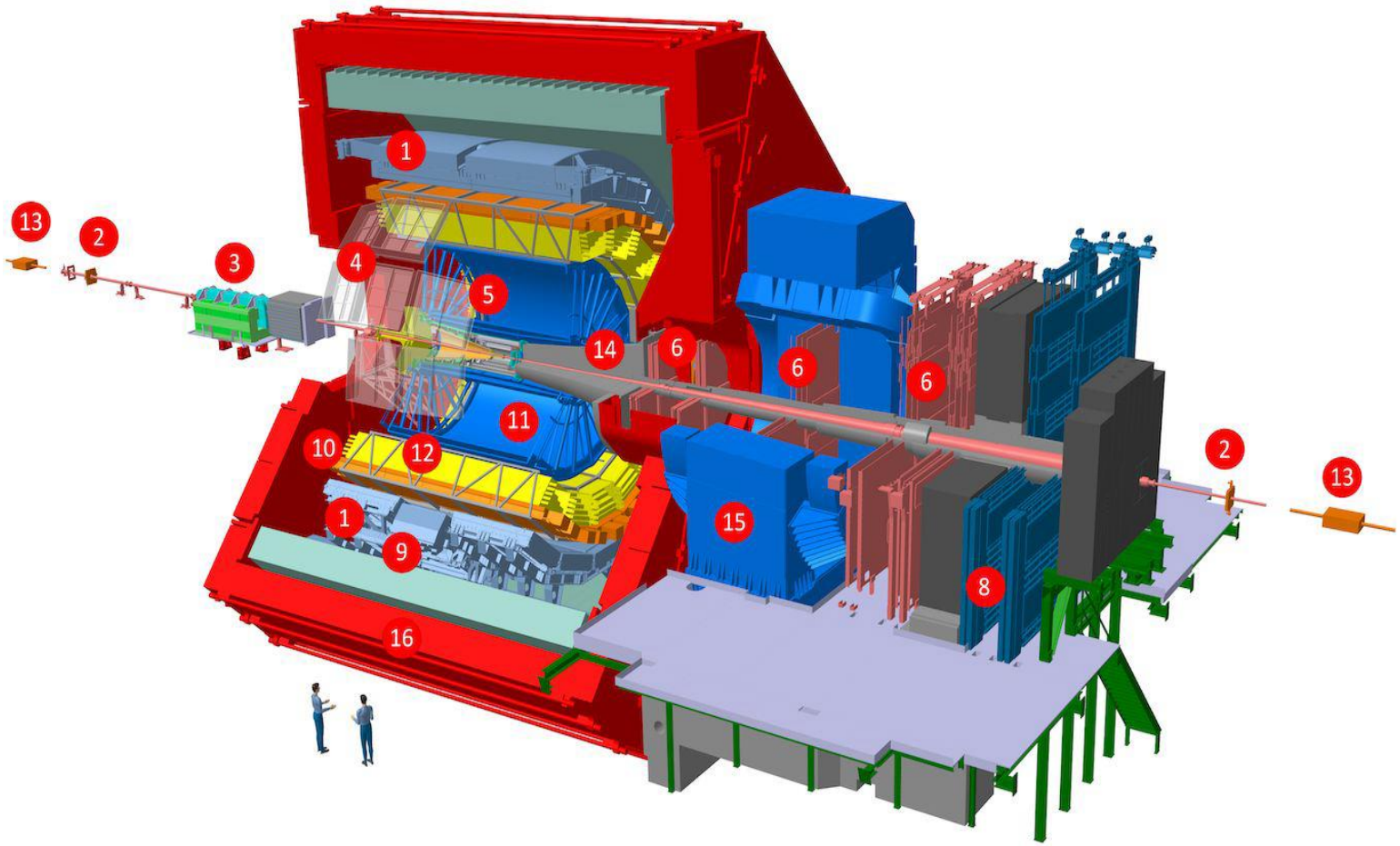
报告内容

- 研究内容
- 考核指标
- 进度安排
- **课题研究进展**

升级后的ALICE探测器（2029年）

LS3 （2026-2028）期间



1 **EMCAL** | Electromagnetic Calorimeter

2 **FIT** | Fast Interaction Trigger

3 **FoCal** | Forward Calorimeter — 新增

4 **HMPID**| High Momentum Particle Identification Detector

5 **ITS**| Inner Tracking System — 更新

6 **MCH**| Muon Tracking Chambers

7 **MFT**| Muon Forward Tracker

8 **MID**| Muon Identifier

9 **PHOS/CPV**| Photon Spectrometer

10 **TOF**| Time Of Flight

11 **TPC**| Time Projection Chamber

12 **TRD**| Transition Radiation Detector

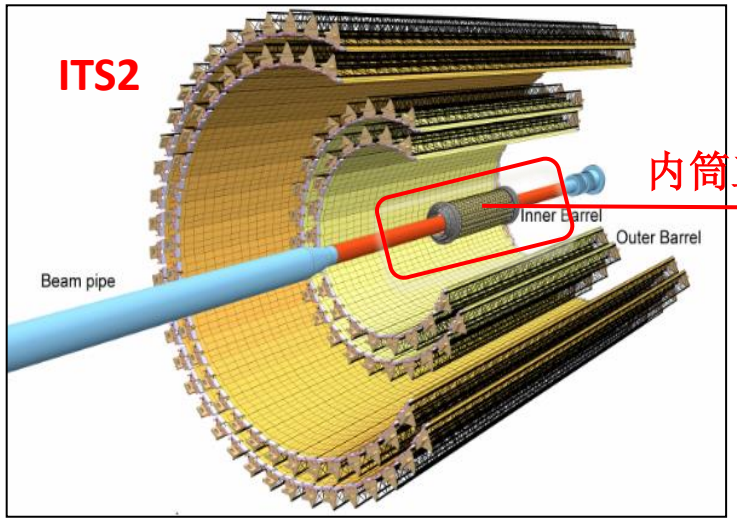
13 **ZDC**| Zero Degree Calorimeter

14 **Absorber**

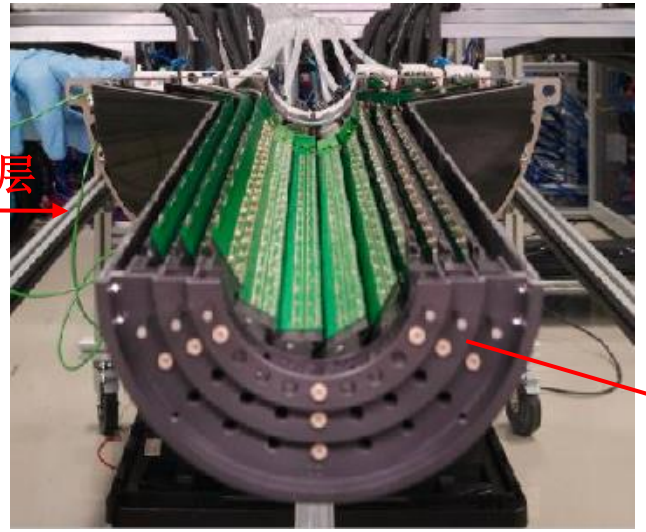
15 **Dipole Magnet**

16 **L3 Magnet**

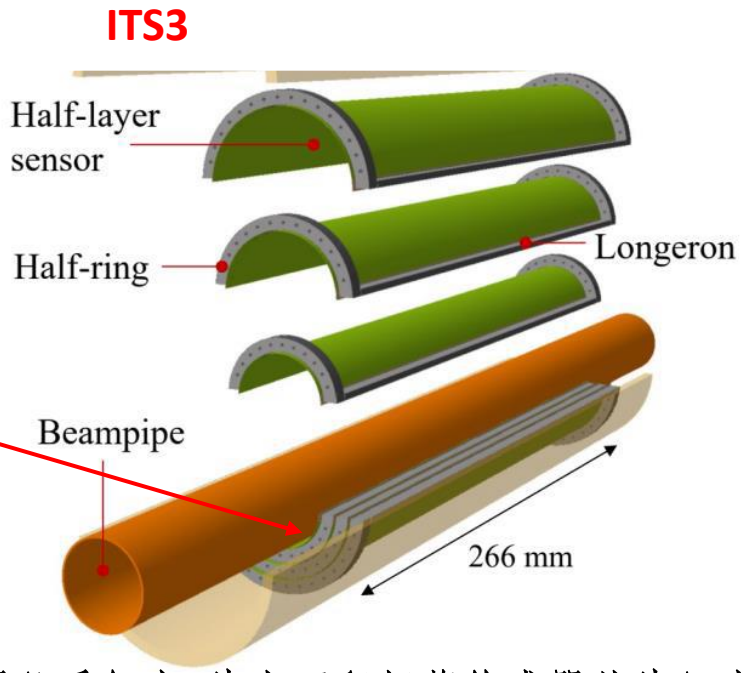
ITS3



内筒三层



替换为



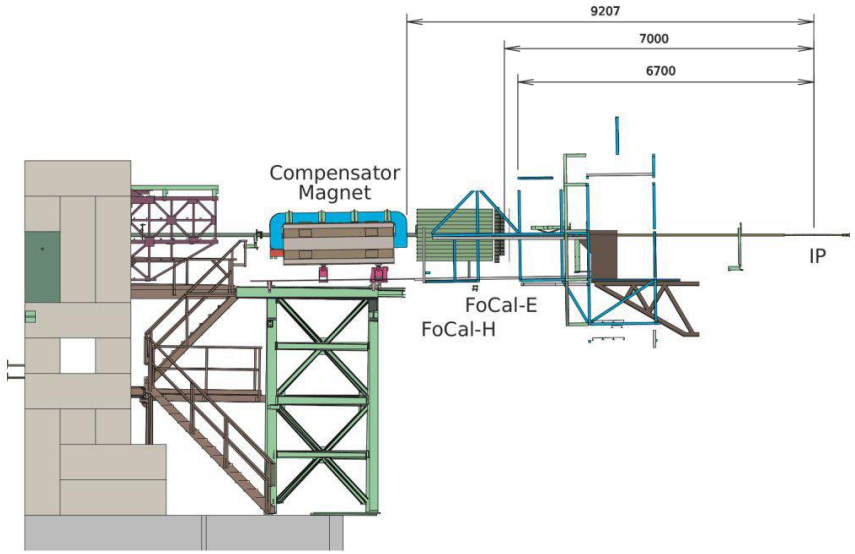
	ITS2	ITS3
到碰撞点的径向距离 （mm）	22	18
最内层辐射长度（%X_0）	~0.35	~0.05
像素大小 （μm²）	30×30	*O*(15×15)
芯片大小 （cm²）	1.5×3.0	O(90×280)
芯片厚度 （μm）	50	20-40

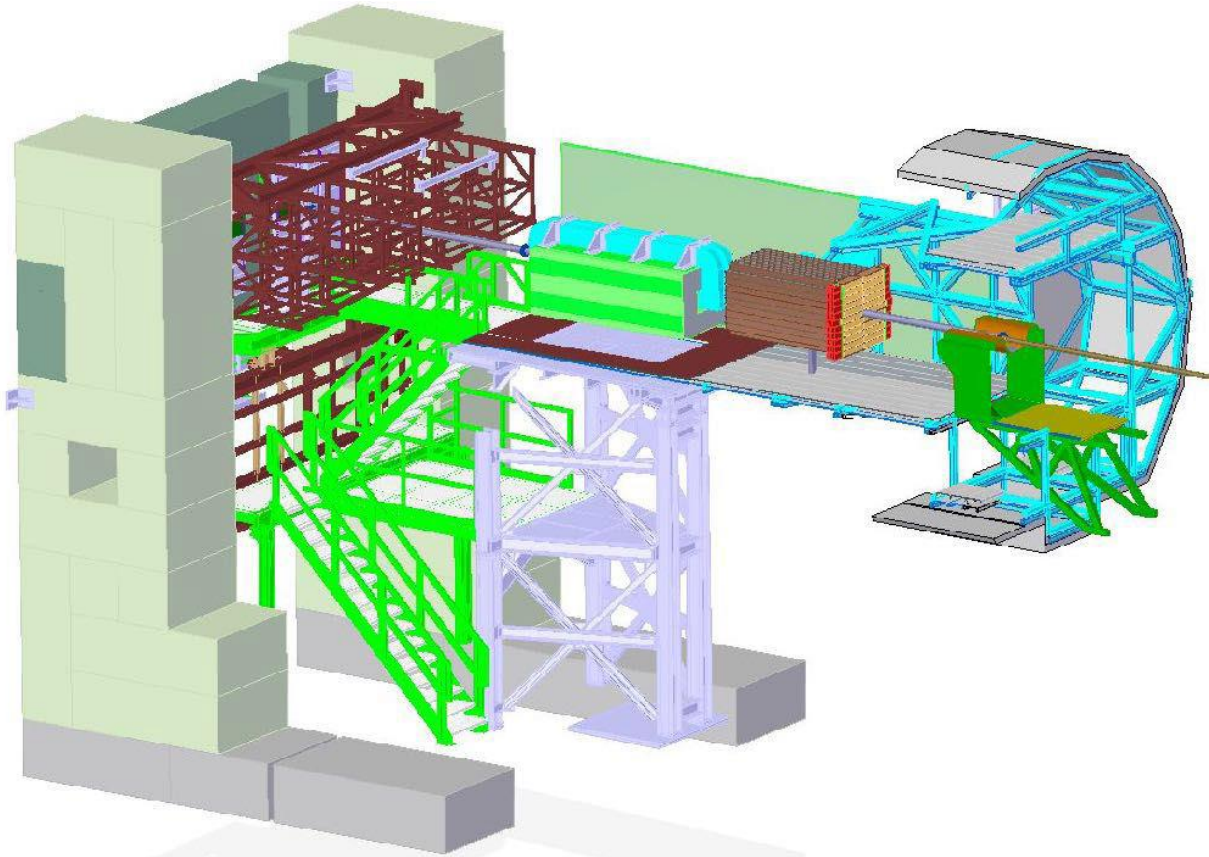
整个探测器几乎仅由6片大面积超薄传感器芯片组成

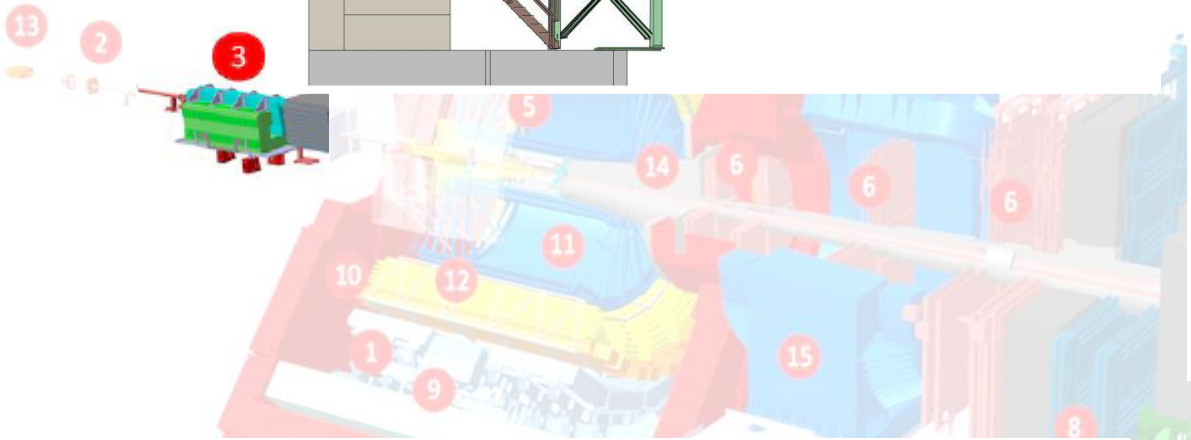
- 非常小的探测器材料辐射长度
- 非常均匀的材料分布，减小系统误差
- 更细的束流管，探测器最内层半径更小

- 会极大地提升在重离子碰撞中测量低横动量粲强子和底强子以及低质量双电子的能力

Forward Calorimeter (FoCal)



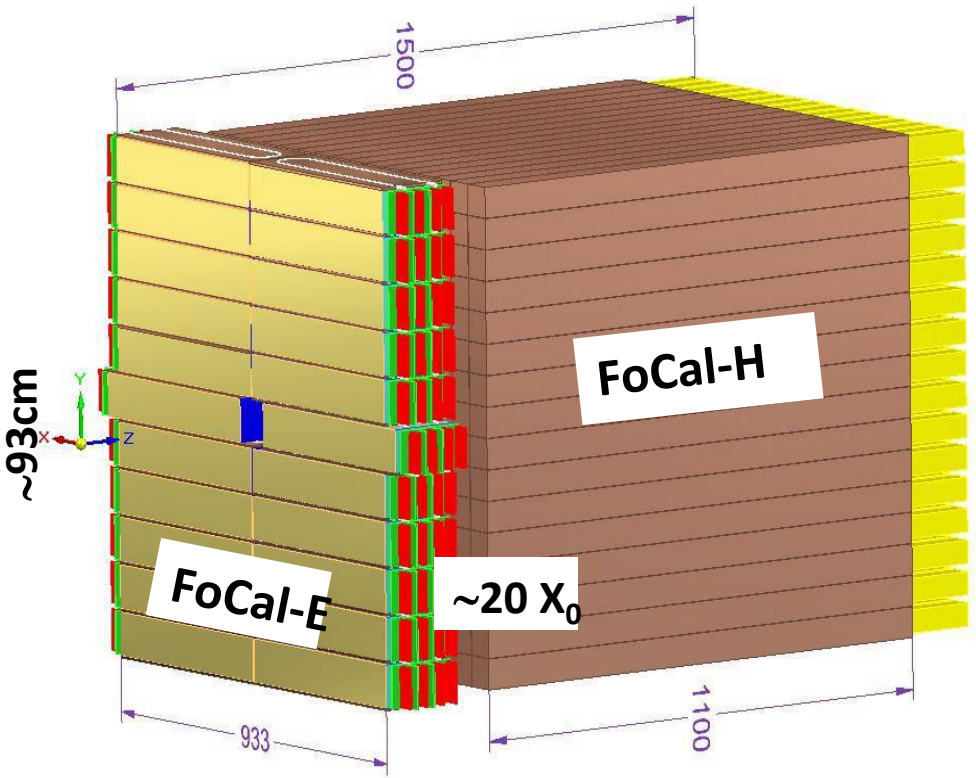




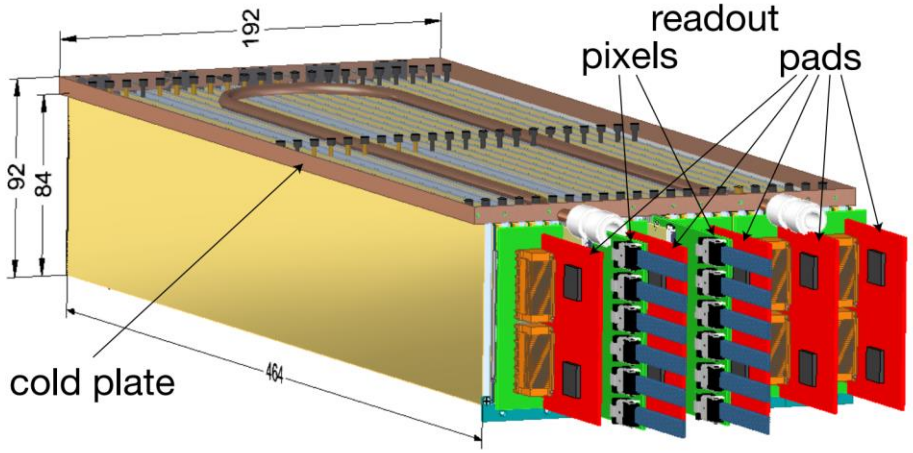
- 离碰撞点的距离为7米
- 覆盖赝快度：3.4 - 5.8

- 小x物理

FoCal探测器的构造

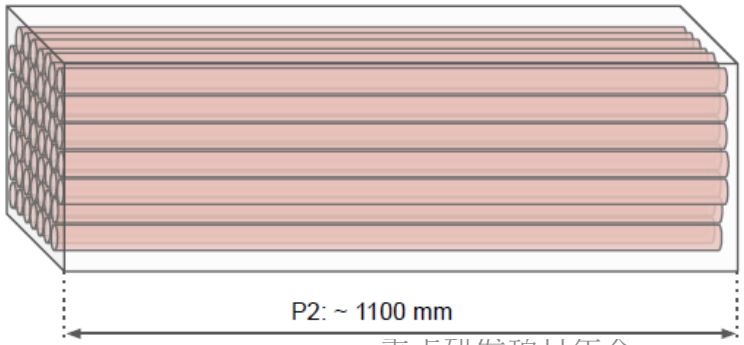


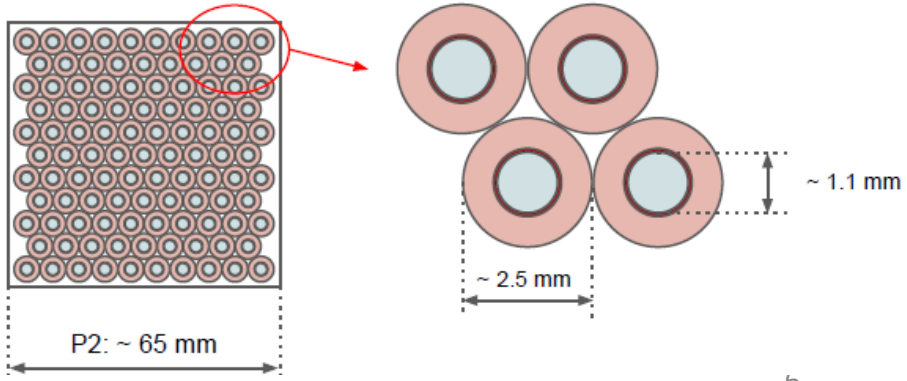
- FoCal-E: 18层粒度为1×1 cm^2硅片+2层硅像素层取样型电磁量能器



共含22个FoCal-E模块

- FoCal-H: 毛细铜管+闪烁光纤意大利面型强子量能器





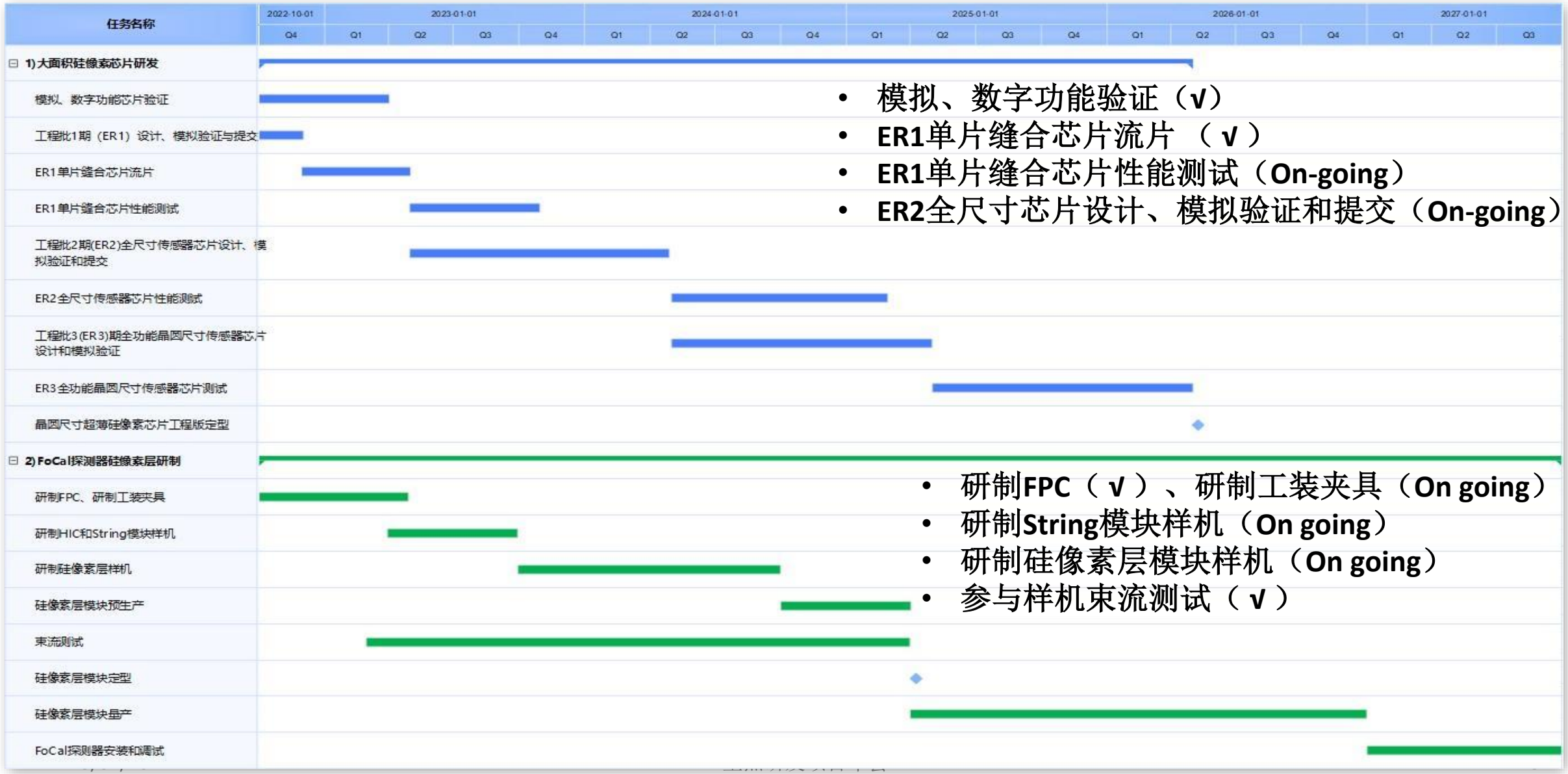
研究内容

- 合作研发晶圆尺寸的超薄硅像素芯片
  - 与CERN合作，利用缝合技术，研发晶圆尺寸的超薄硅像素芯片
  - 参与芯片设计、模拟验证和测试等工作
- FoCal探测器的硅像素层研制
  - 与挪威卑尔根大学等单位合作，研制出FoCal探测器的硅像素层及其读出电子学系统
  - 参与束流测试，研究硅像素层模块的性能
  - 通过探测器模拟，优化FoCal的构造和像素层的位置
  - 设计开发探测器读出单元，结合系统模拟，优化固件架构设计，提高探测器性能
  - 基于束流测试结果，优化MC模拟参数，研究探测器物理性能，建立分析框架

考核指标

课题目标[1]	预期成果				考核指标[2]				考核方式（方法）及评价手段[4]
	预期成果名称			预期成果类型	指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	
（限500字以内。）参与研发用于ALICE第三代硅像素探测器的晶圆尺寸硅像素芯片，掌握其研发关键技术；完成FoCal探测器的硅像素层的研制任务，掌握研制基于硅像素芯片的高粒度量能器及其读出电子学的关键技术。发表论文1-2篇；培养研究生2-3名。	主要成果	1	合作研发出大面积硅像素芯片	□新理论 □新原理 □新产品 □新技术 □新方法 ■关键部件 □数据库 □软件 □应用解决方案 □实验装置/系统 □临床指南/规范 □工程工艺 □标准 □论文 □发明专利 □其他_____	指标1.1 芯片技术指标-面积、功耗等	无	芯片面积达90 mm x 140 mm	芯片面积达90 mm×140 mm，像素大小约15 um×15 um，功耗低至20 mW/cm^2	合作组安排测试，提供测试结果
		2	合作研制出FoCal硅像素层模块及其读出电路板	□新理论 □新原理 □新产品 □新技术 □新方法 ■关键部件 □数据库 □软件 □应用解决方案 ■实验装置/系统 □临床指南/规范 □工程工艺 □标准 □论文 □发明专利 □其他_____	指标2.1 FoCal技术指标-位置分辨本领	～10 mm	样机位置分辨率～5 mm	～5 mm	合作组安排测试，提供测试结果
	其他成果								

进度安排

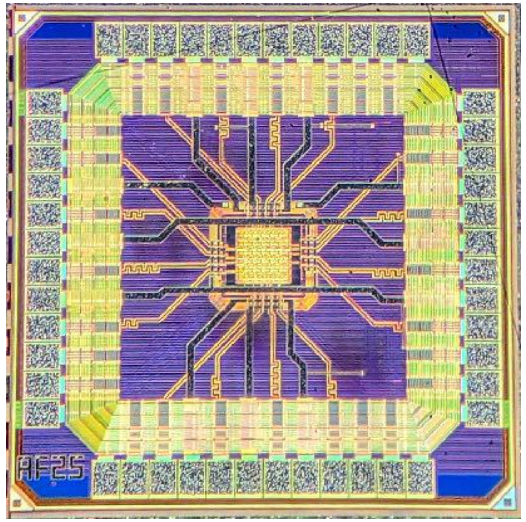


- 模拟、数字功能验证（√）
- ER1单片缝合芯片流片 （ √ ）
- ER1单片缝合芯片性能测试（On-going）
- ER2全尺寸芯片设计、模拟验证和提交（On-going）

- 研制FPC（ √ ）、研制工装夹具（On going）
- 研制String模块样机（On going）
- 研制硅像素层模块样机（On going）
- 参与样机束流测试（ √ ）

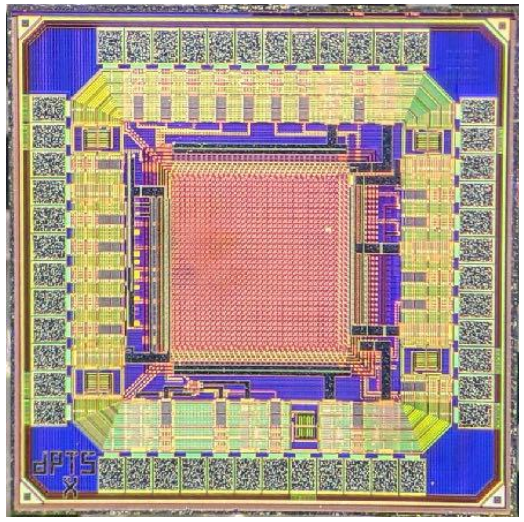
ITS3芯片研发进展：模拟、数字功能验证

APTS



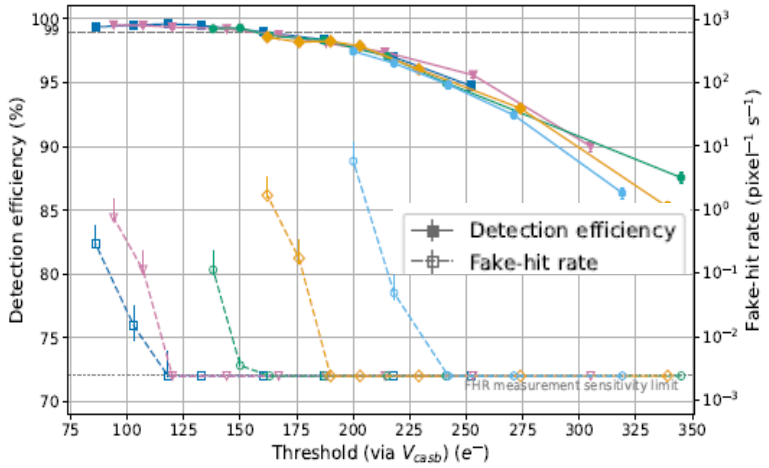
Matrix: 6x6 pixels
Readout: direct analog readout of central 4x4
Pitch: 10, 15, 20, 25 µm
Total: 34 dies

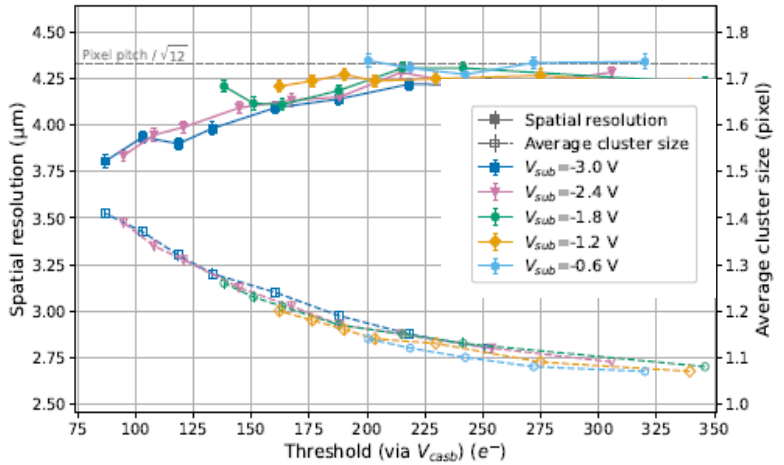
DPTS



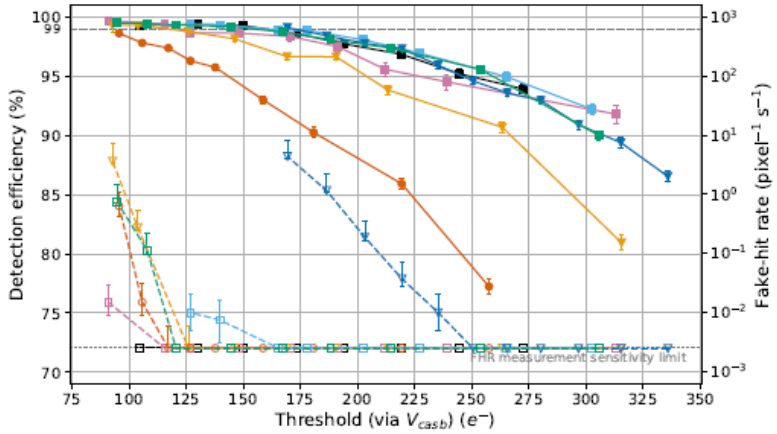
Matrix: 32x32 pixels
Readout: async. digital with ToT
Pitch: 15 µm
Total: 3 dies

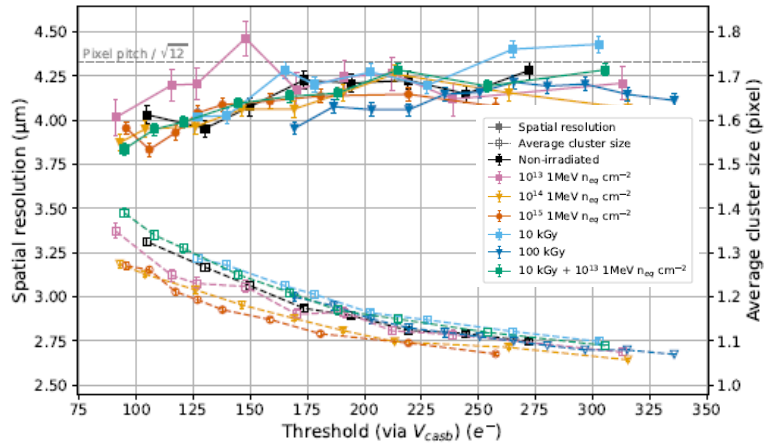
NIMA 1056 (2023) 168589 (arXiv:2212.08621)





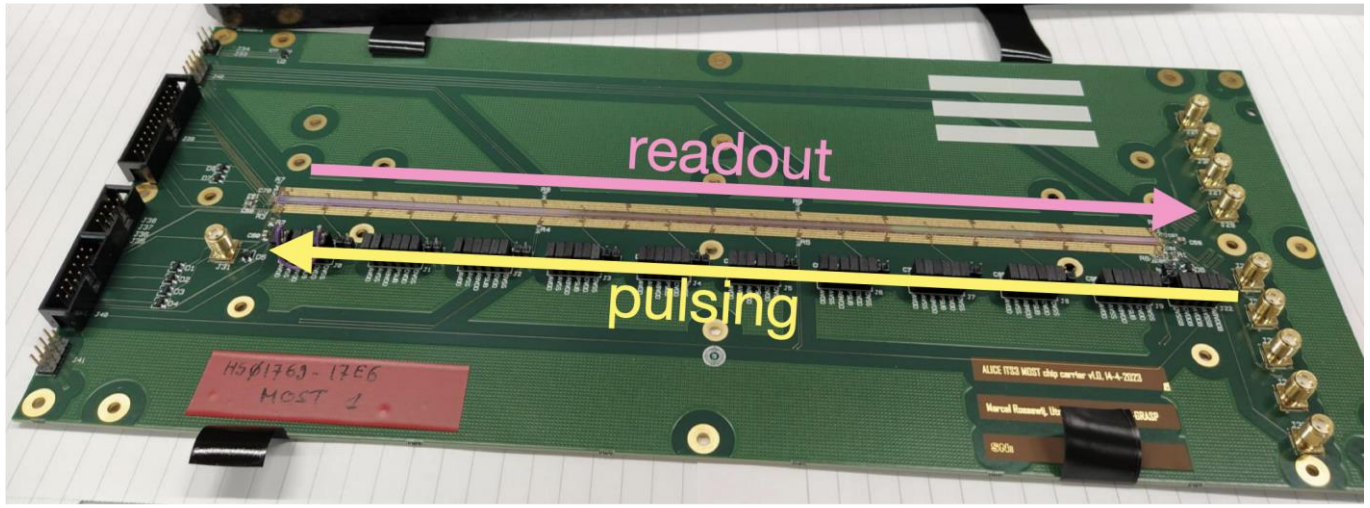
Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{sub} = V_{pwell}$.

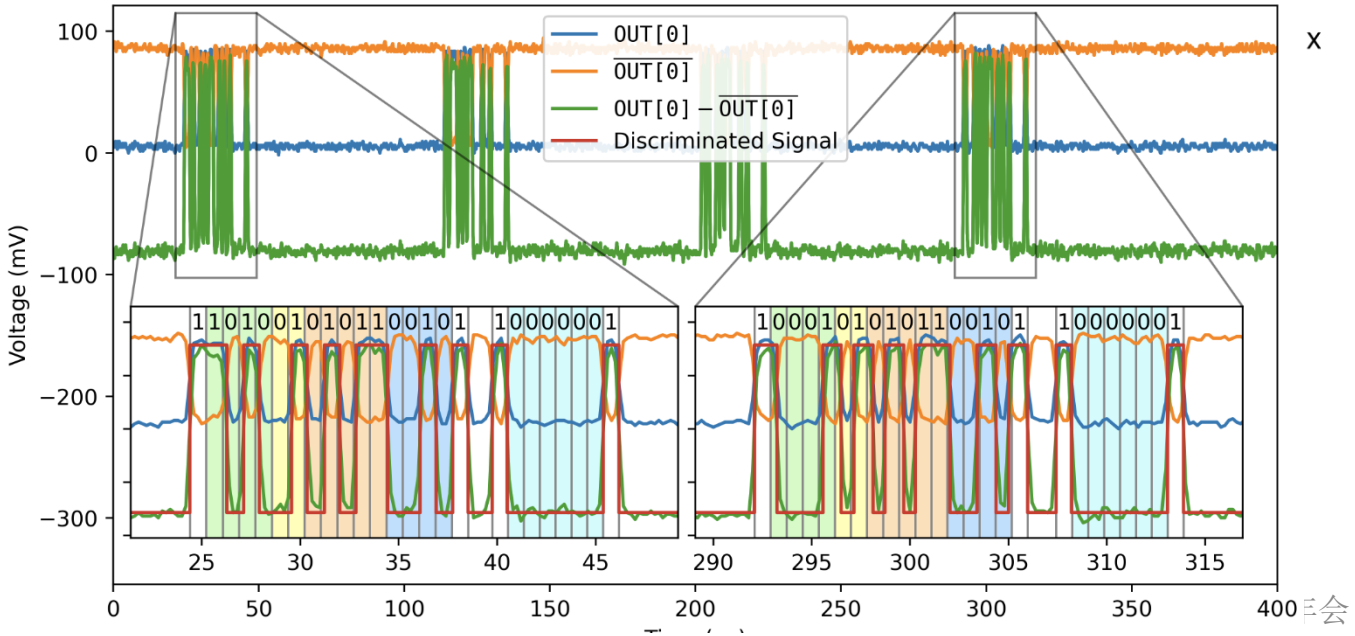




Sensors irradiated to different levels.

ER1单片缝合芯片性能测试：数据传输





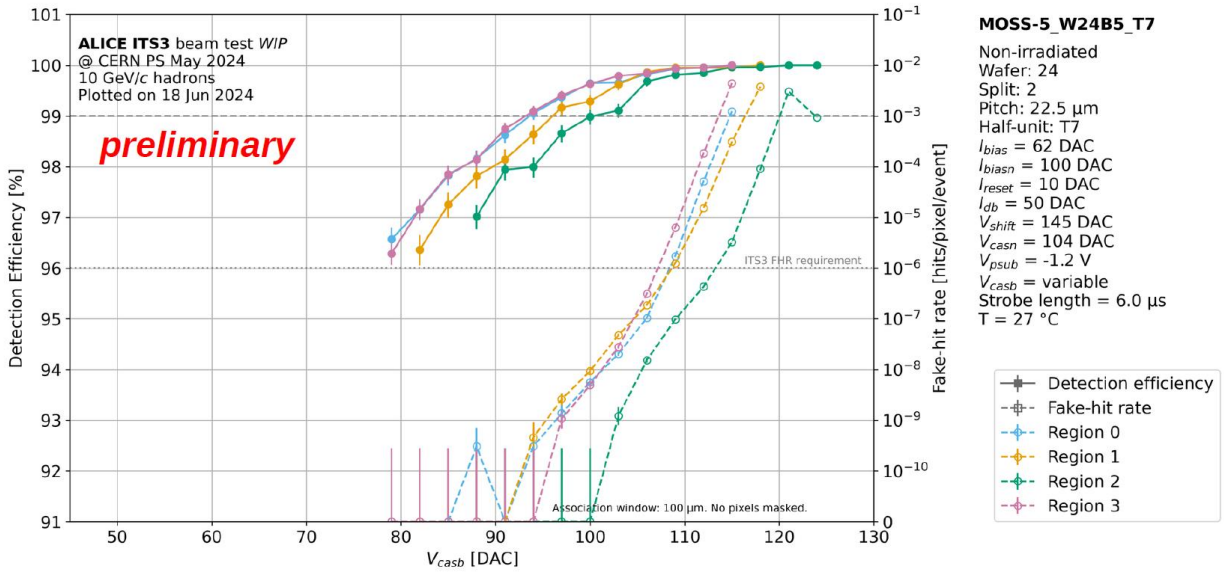
- Slow control backbone works across all stitches
  - Digital readout done by 256 lines (4 per column)
  - serial data at 1 Gb/s
  - across full chip (26cm) towards bottom (right) end
  - all lines work
  - responses to digital pulsing according to specs
- MOSS design fully functional

  Design concepts and methodology validated

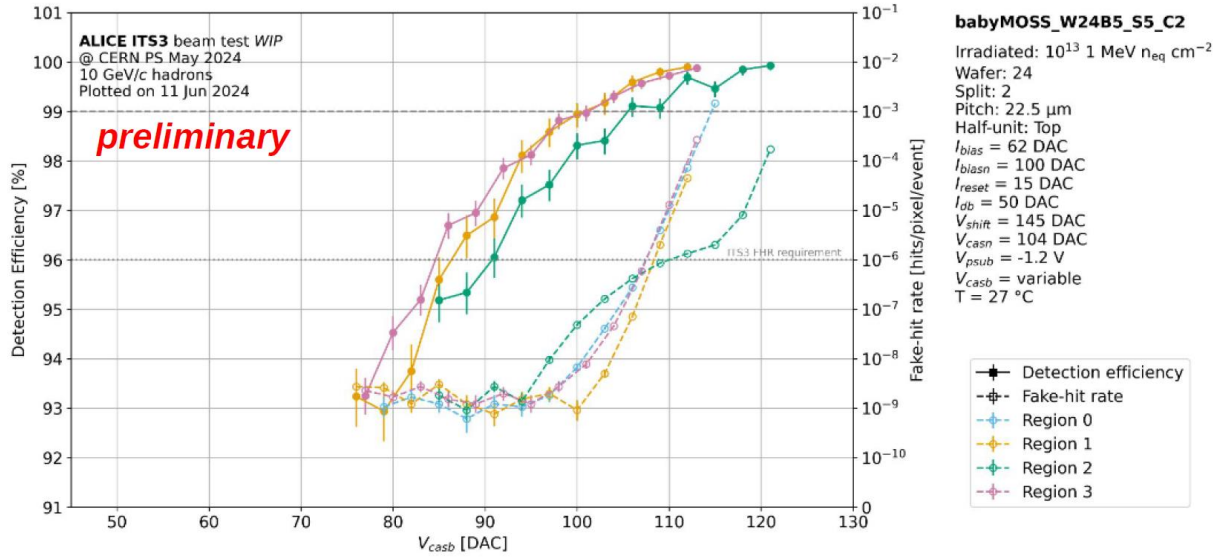
  Much learning on yield, handling and performance of a full-scale device

ER1单片缝合芯片性能测试：探测效率和分辨率

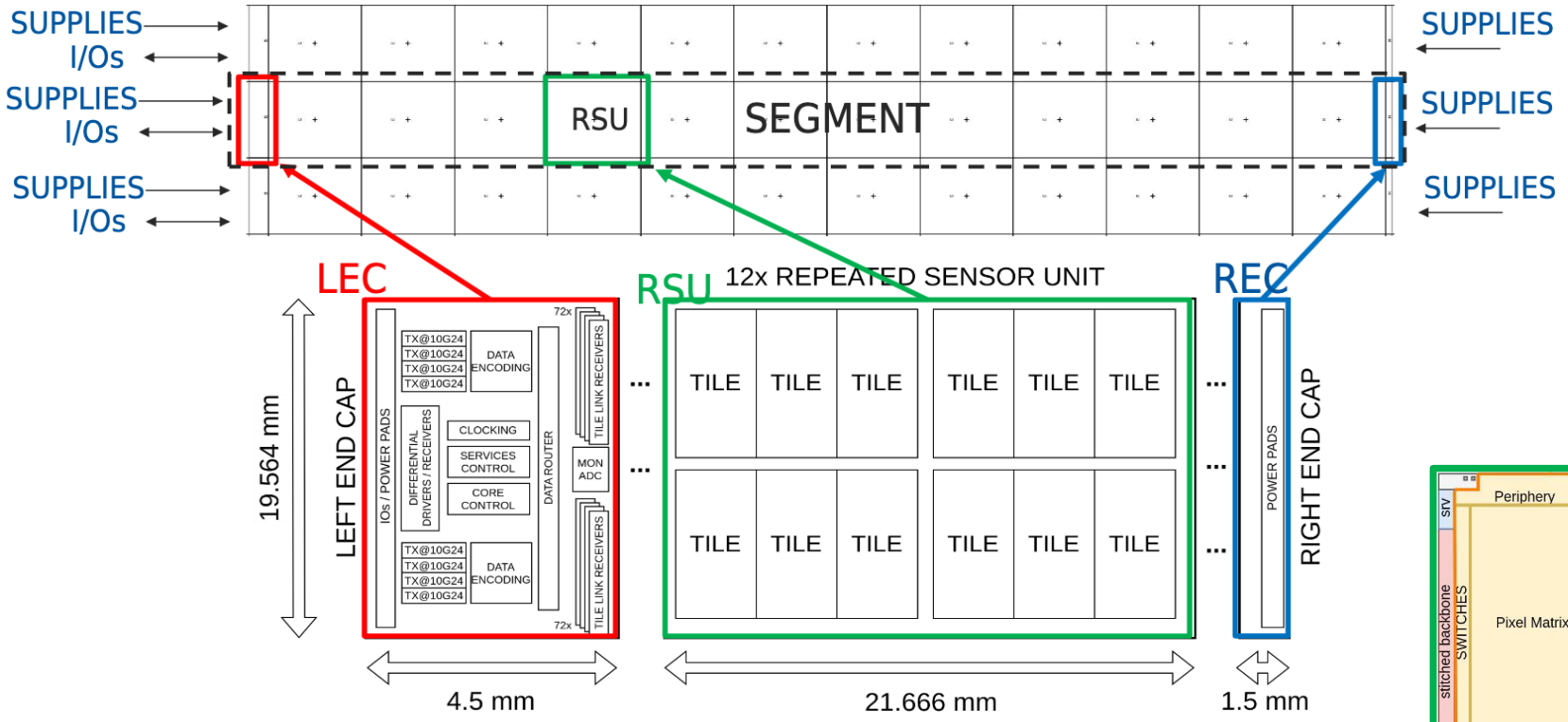
Non-irradiated MOSS,PSUB = -1.2 V



Irradiated babyMOSS, PSUB = -1.2 V

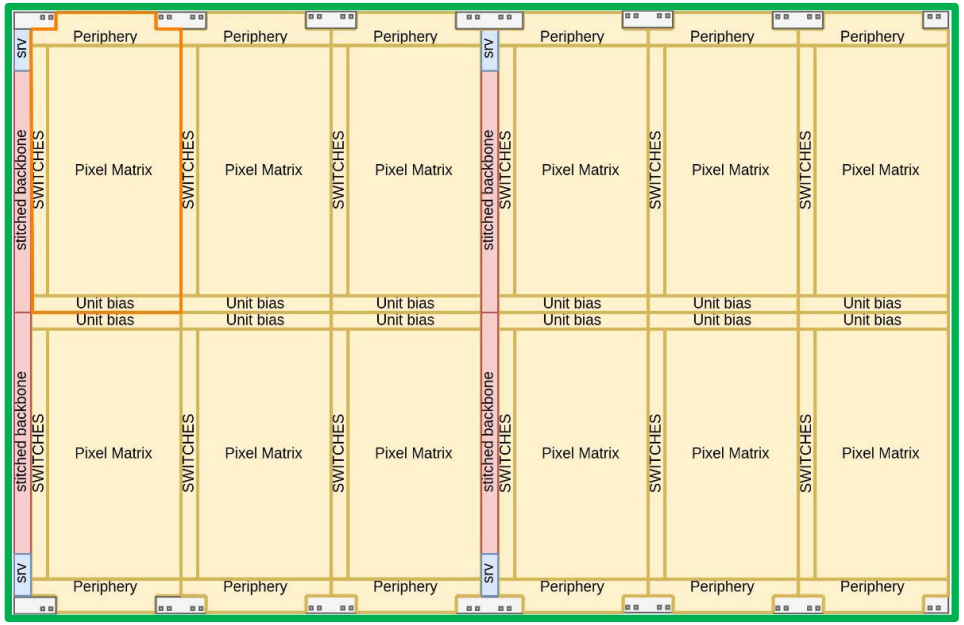


ER2芯片： MOSAIX总体结构



- Design ongoing
  submission target October 2024

RSU



12 RSU per segment, 12 TILEs per RSU
144 TILEs can be switched on, biased and read out independently

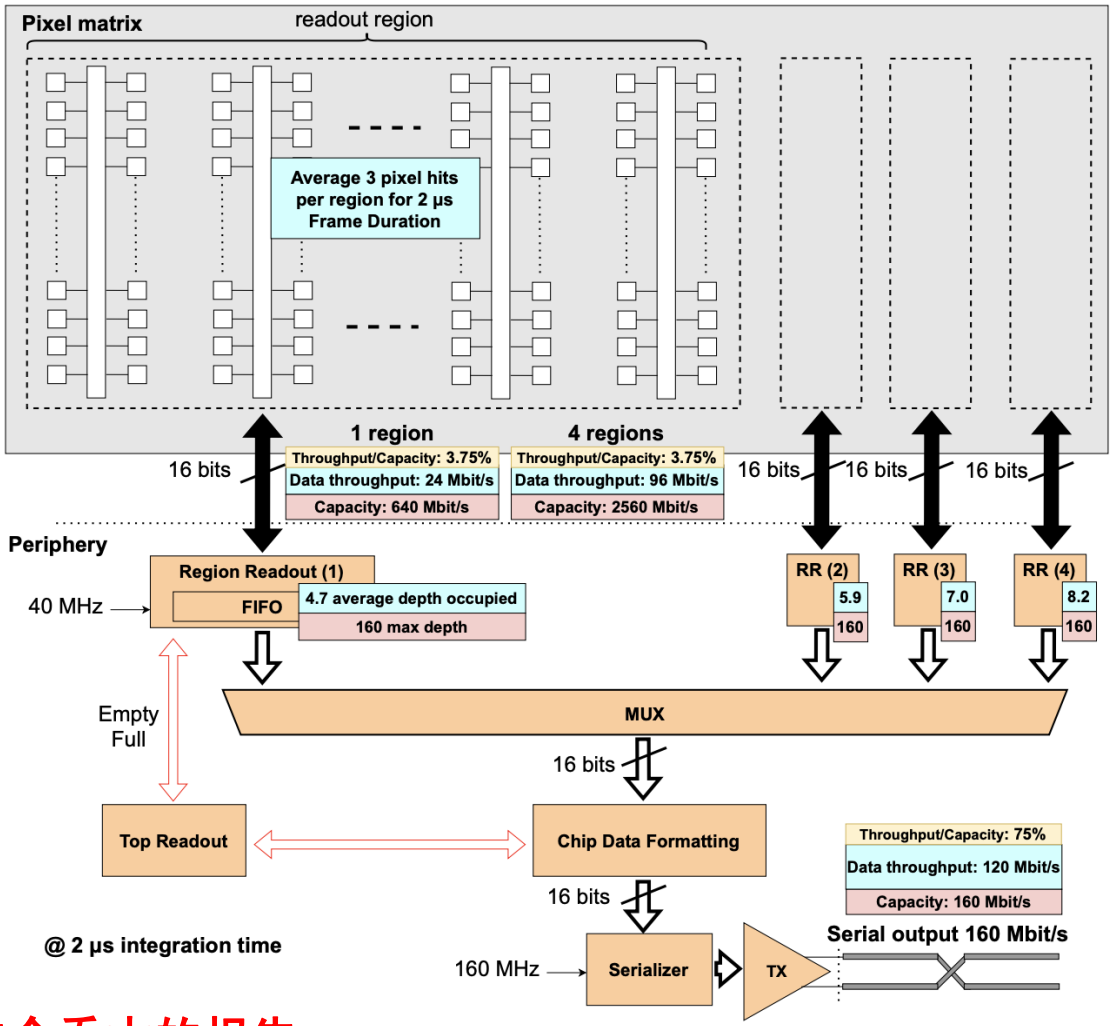
Programmable Switches
One TILE is 1/864=0.116% of L0 acceptance

ER2芯片设计：ASIC框图

设计指标

Simulation parameters	Value	Unit	Conditions
Particle Rates			
Pb-Pb Interaction Rate	164	kHz	Safety factor 2
Particle flux (Hadronic)	2.55	MHz cm^{-2}	z=0 cm, all centralities.
Particle flux (QED)	3.20	MHz cm^{-2}	z=0 cm.
Total particle flux	5.75	MHz cm^{-2}	z=0 cm, all centralities.
Geometry, timing, encoding, data transfer capacity			
Pixel dimensions	20.8 × 22.8	µm × µm	
Tile pixel array size	442 × 156		
Pixels per Tile	68952		
Sensitive Area of the tile	0.328	cm^2	
Tiles per segment	144		
Readout regions per tile	3 or 4		
Frame Interval Duration (FD)	2 or 5	µs	
Minimum average cluster size	2.1		$\Delta z = 0$ cm, Fig. 3.43.
Pixel hit encoding time	25	ns	
Bits per pixel hit	16	bit	
Capacity of tile link	160	Mbit s^{-1}	
Aggregated capacity (Segment)	23.04	Gbit s^{-1}	
Simulation results			
Average pixel occupancy	$< 2.0 \times 10^{-4}$		z=0 cm.
Average pixel occupancy	$< 5.0 \times 10^{-4}$		z=0 cm, FD=5 µs.
Data throughput	120	Mbit s^{-1} Tile^{-1}	z=0 cm.
Data throughput	15.55	Gbit s^{-1} Segment^{-1}	
Data throughput per unit area	365	Mbit s^{-1} cm^{-2}	z=0 cm.
Data throughput per unit area	329	Mbit s^{-1} cm^{-2}	Average over z.
Data throughput per link	2.58	Gbit s^{-1}	
Incomplete event probability	$< 6 \times 10^{-5}$		Layer 0 segment.
Incomplete event probability	$< 2 \times 10^{-4}$		Full layer 0.

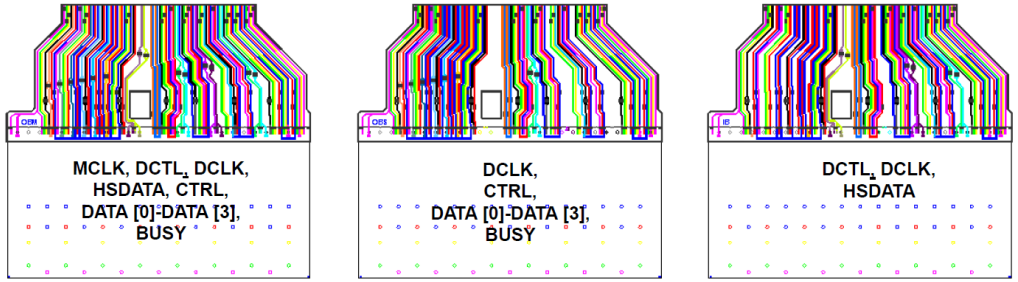
One tile (total 6) of the half of one repeated sensor unit (total 12)

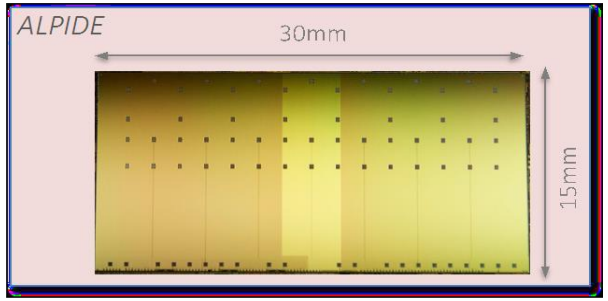


更多细节见下午仝乔木的报告

FoCal探测器硅像素层制作流程

3 type of chip-cables





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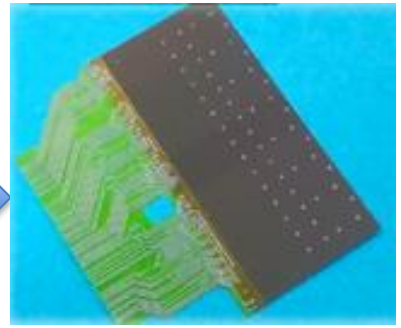
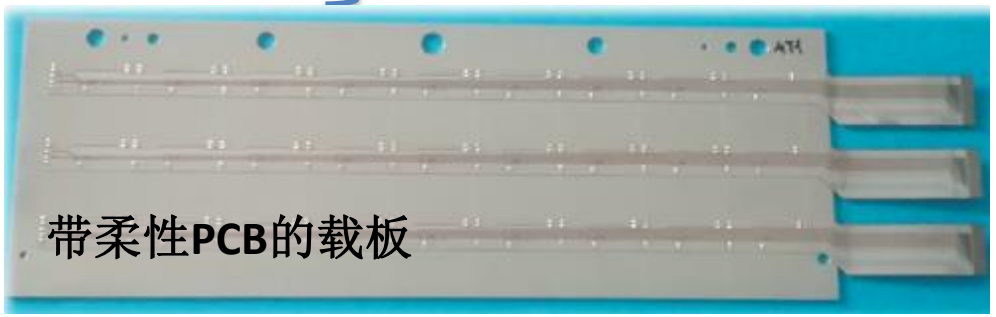
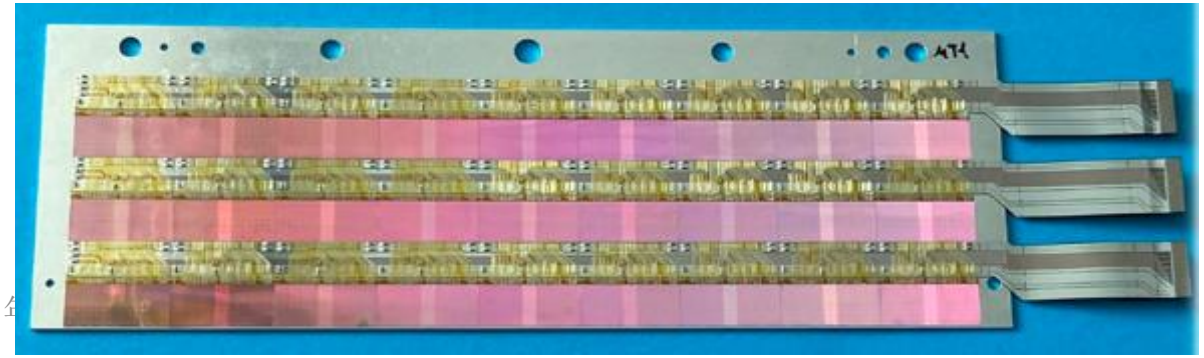




SpTAB

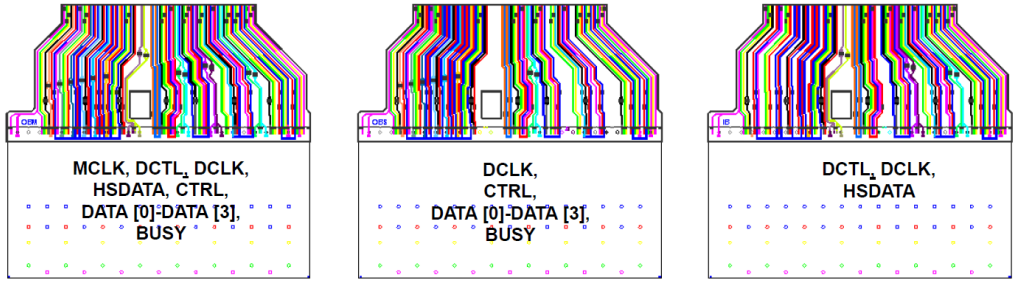


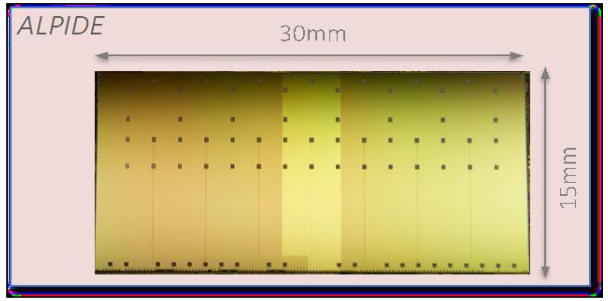
更多细节见下午刘军的报告

- 研制各种夹具
- 承担部分组装任务

FoCal硅像素层研制进展: 单芯片组装夹具研制

3 type of chip-cables





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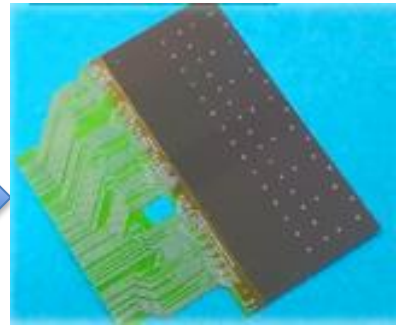
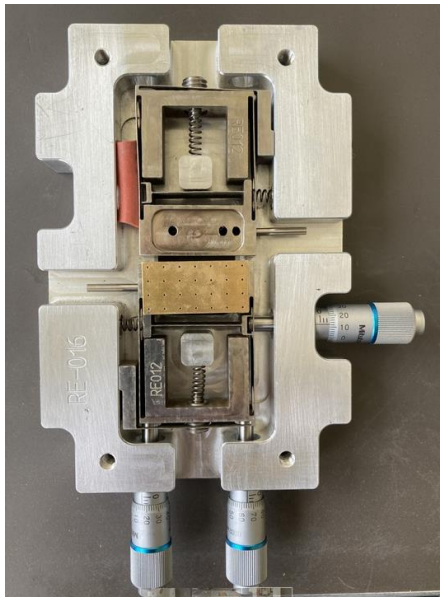
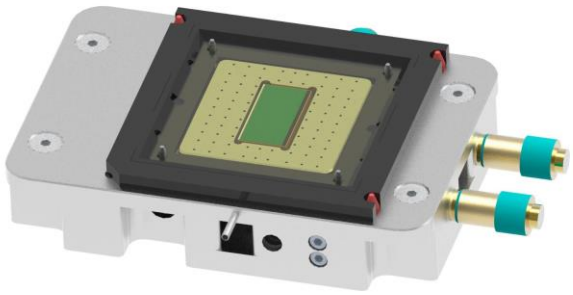
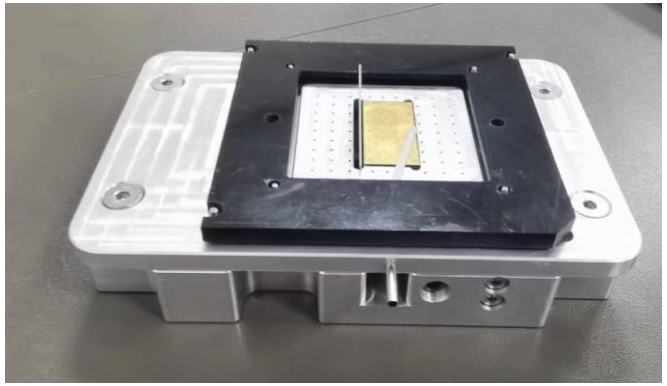






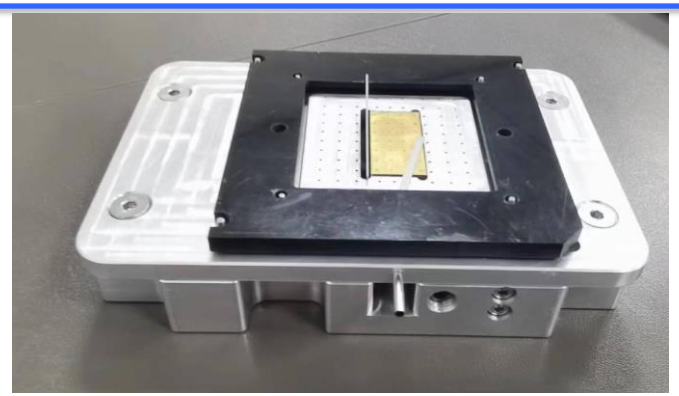
Single ALPIDE mounting jig

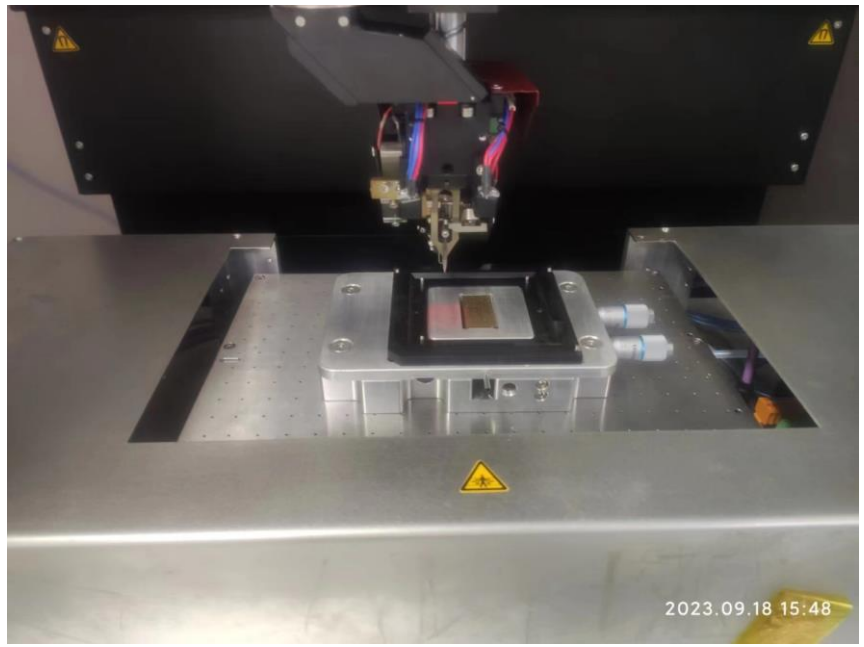
First try failed with one component
Solved by heat treatment



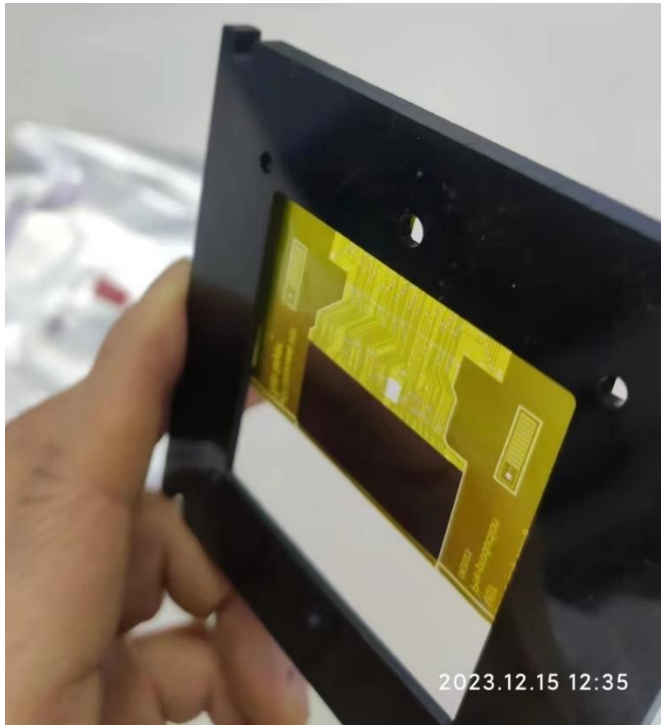
- Brought to CERN for validation in May,2023
- Three more jigs produced and sent to labs in 2023
- Vacuum tightness validated
- Functioning tested with micrometer heads

FoCal硅像素层研制进展: ALPIDE2Chipcable



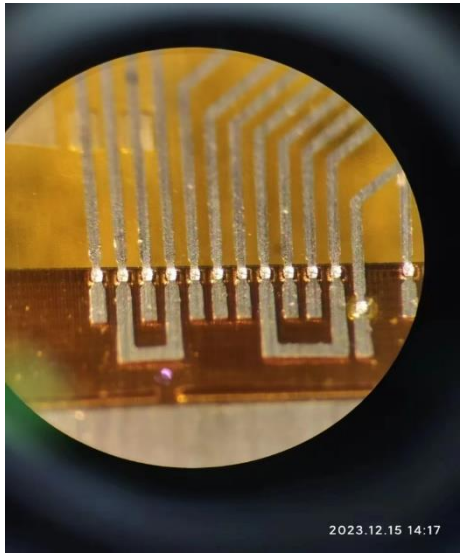


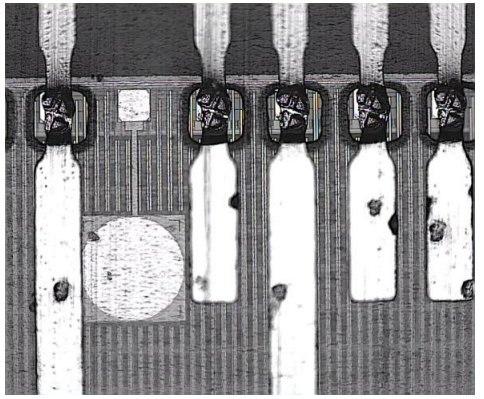
To hold the single ALPIDE mounting jig, the bonder table is lowered by 2 cm

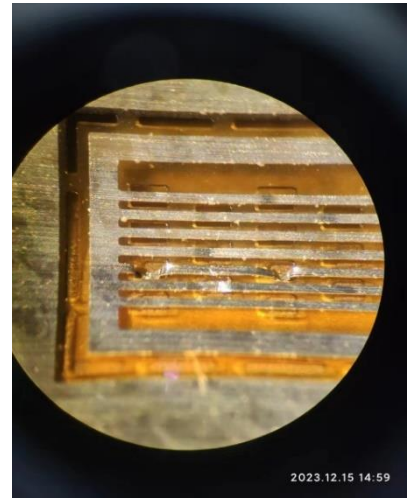


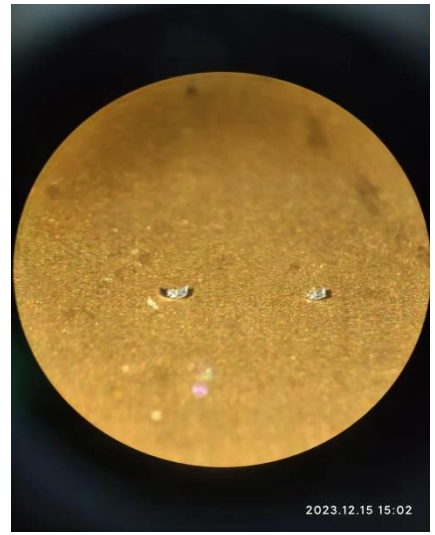
ALPIDE is bonded to chipcable

View under microscope





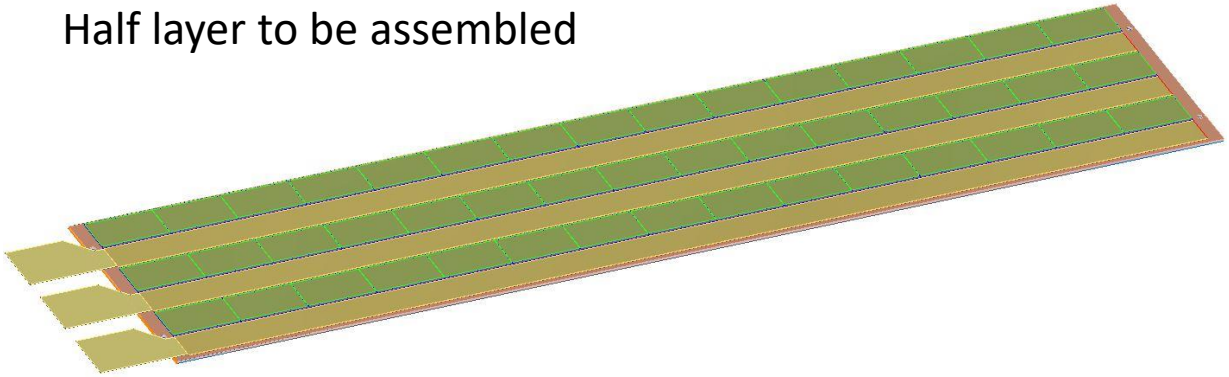




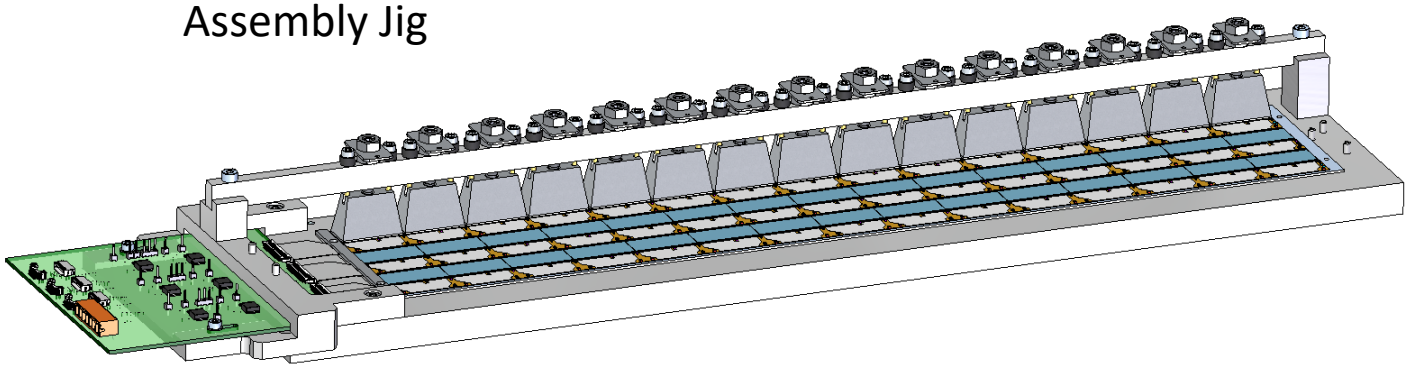
Peel test

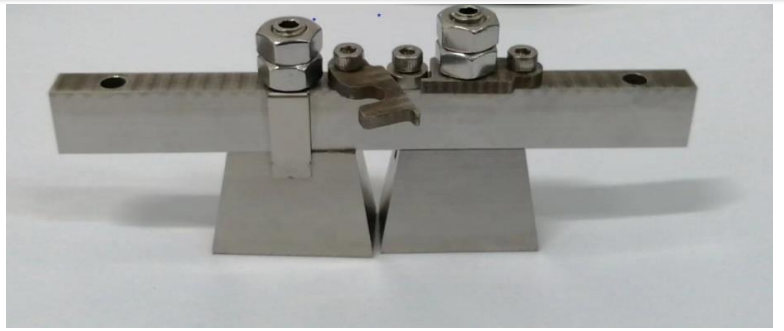
FoCal硅像素层研制进展: 组装夹具研制

Half layer to be assembled

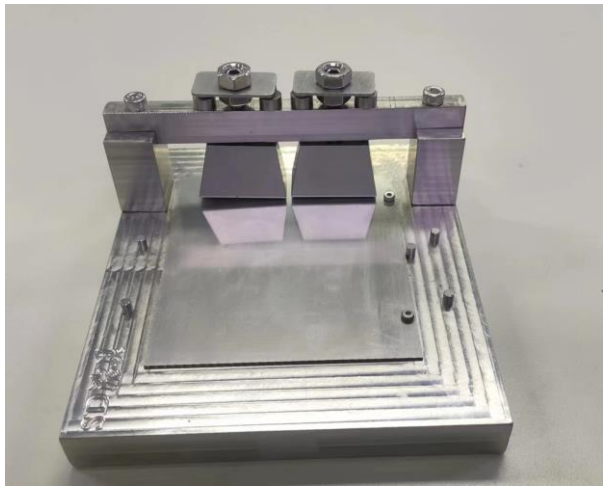


Assembly Jig





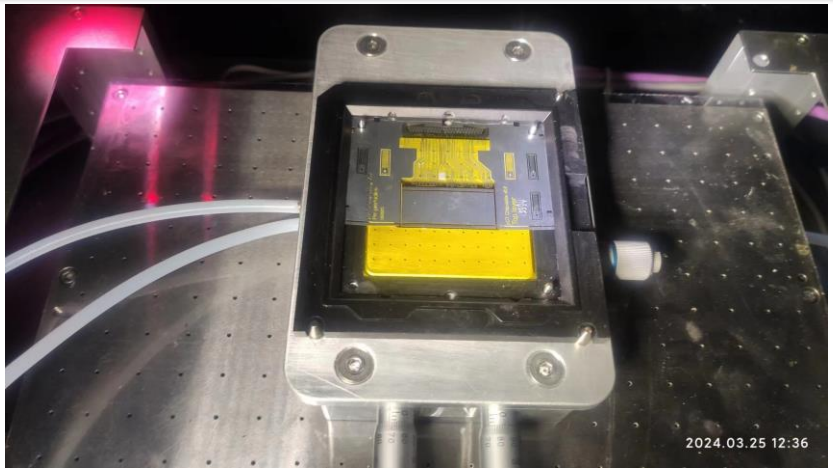
1st test sample with two structures produced and sent to Europe before Christmas, 2023



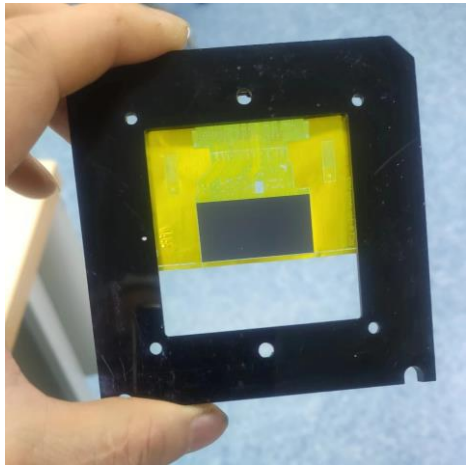
2nd version of test sample produced and sent to Oslo in April, 2024

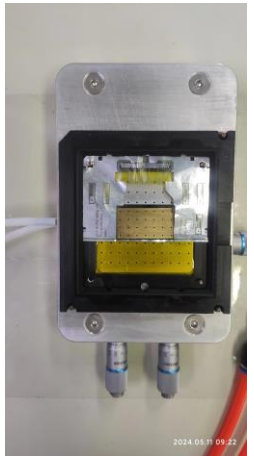
Production of assembly jigs on-going

FoCal硅像素层研制进展: 组装流程测试

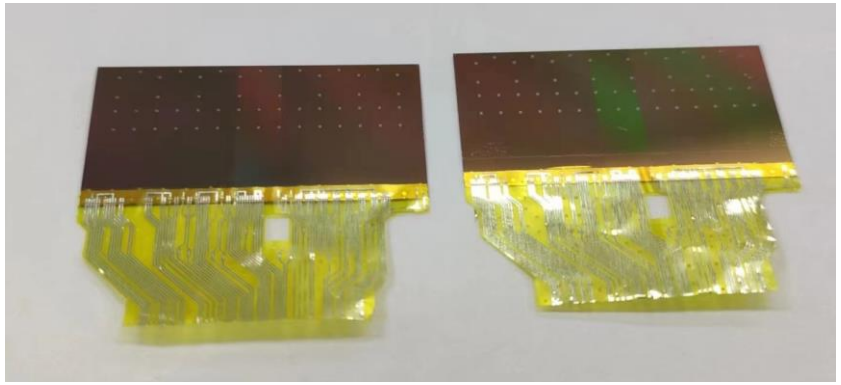


SpTab Bonding using F&K Delvotec G5 64000 bonder

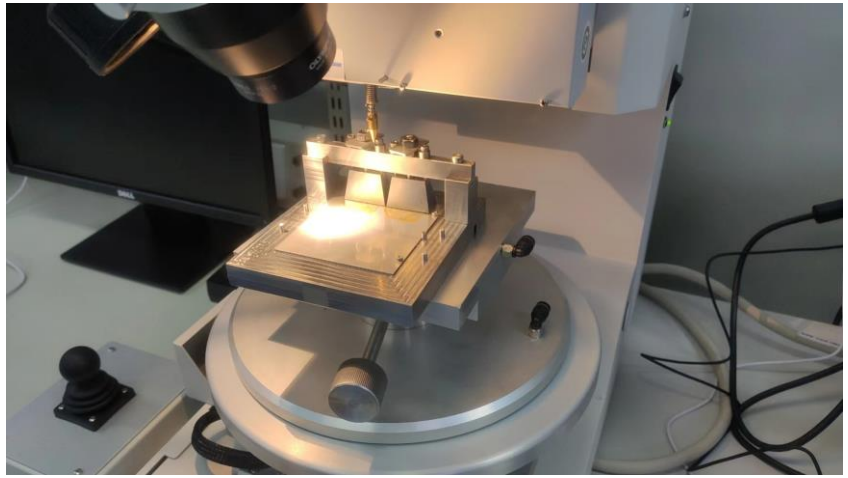


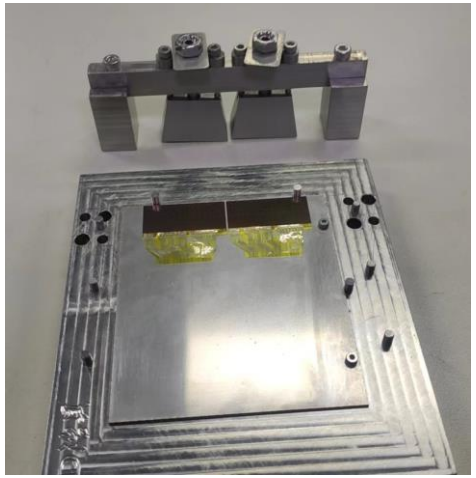


Cut off the part for assembly



The parts for assembly



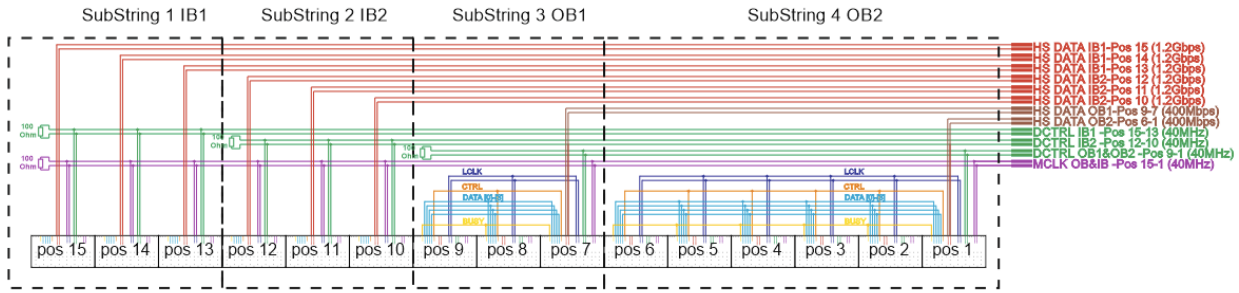


Place the parts using the assembly tool prototype under a microscope

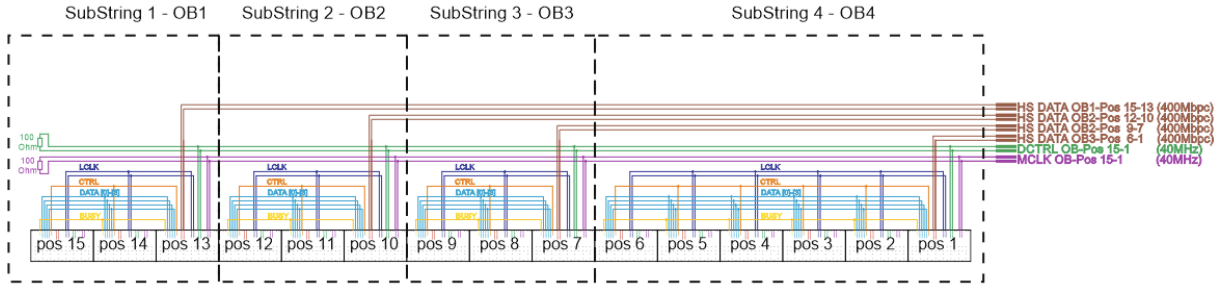
- **The full procedure with a checklist to be established**

FoCal硅像素层研制进展: String研制

Schematic diagram



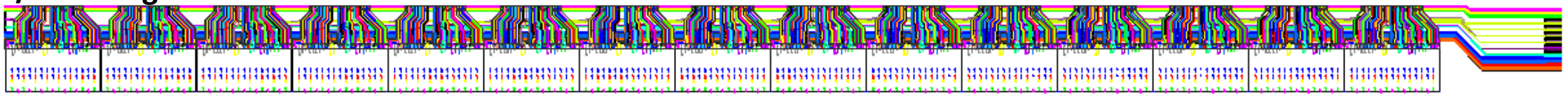
IB/OB



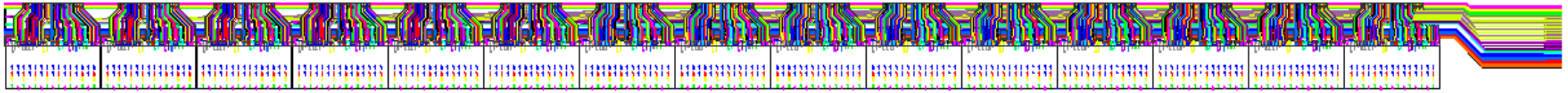
OB

Layout

IB/OB string



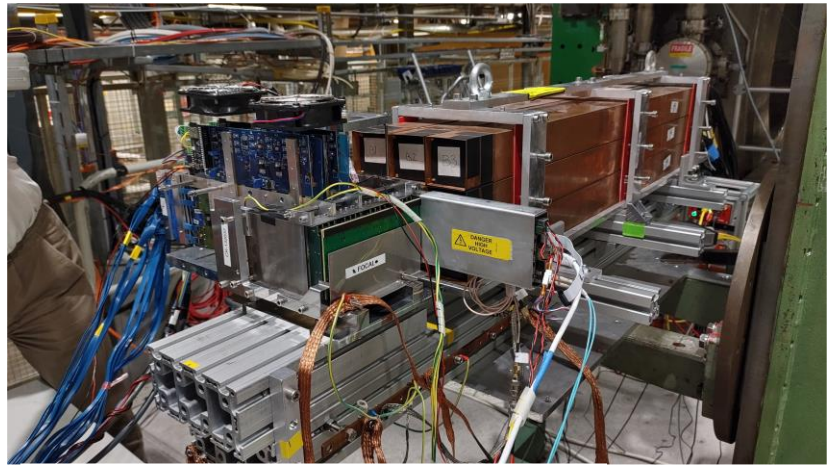
OB string

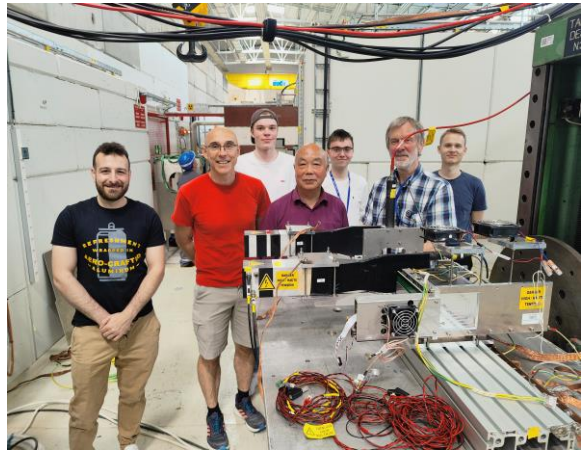


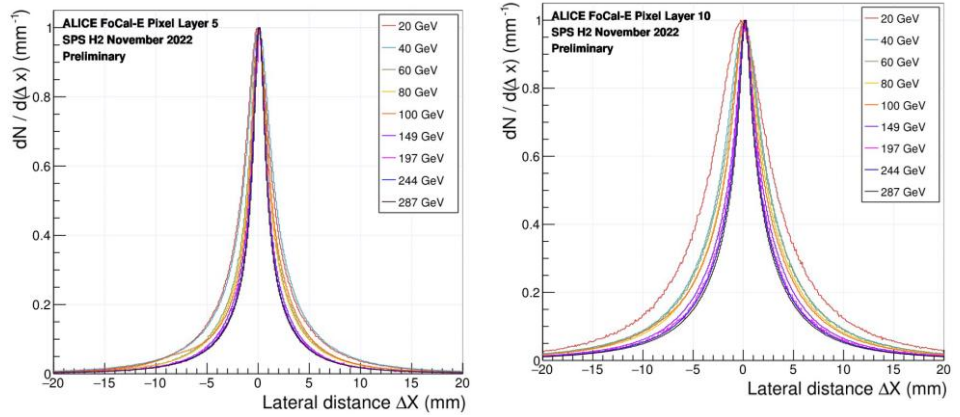
Production is expected to start in July in Ukraine

关于读出电子学的更多细节
见吝守龙的报告

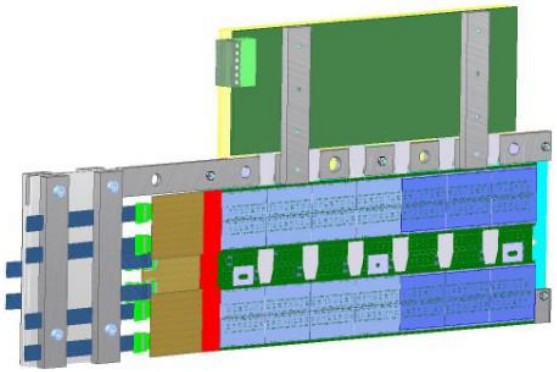
FoCal硅像素层研制进展: 束流测试及其数据分析



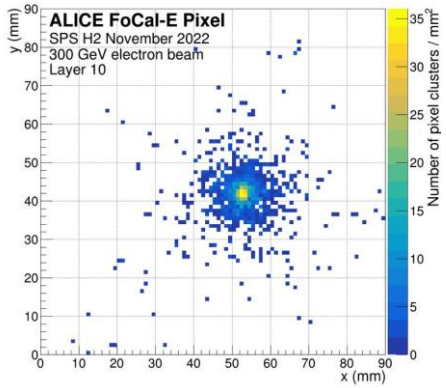


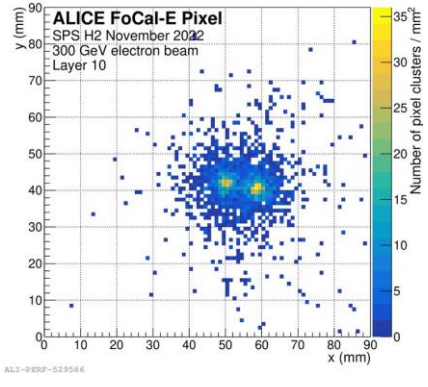


arXiv:2311.07413



基于HIC的硅像素层样机





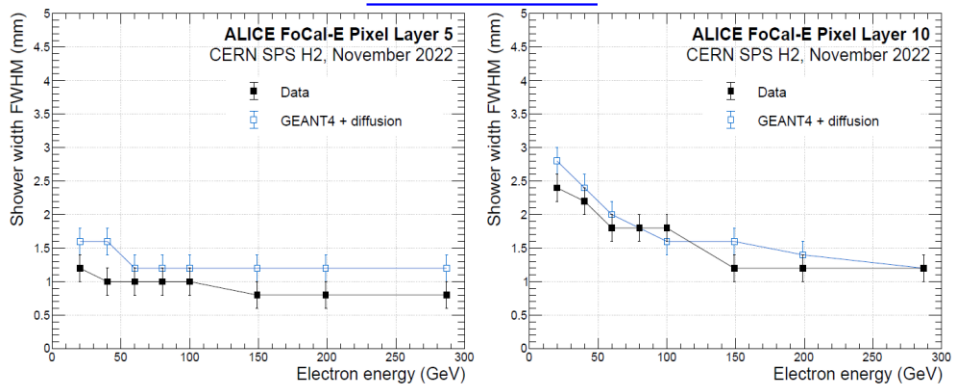


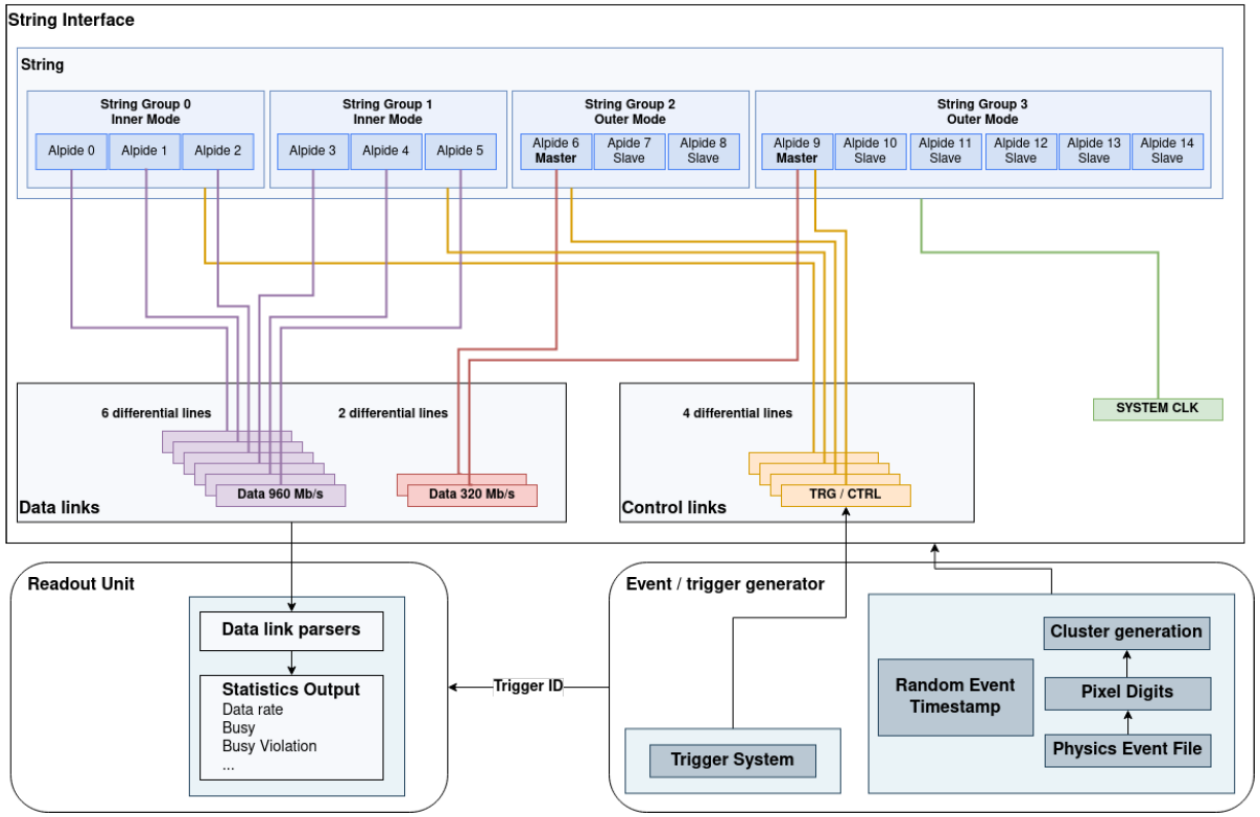
Figure 33. Measured and simulated FWHM for layer 5 (left panel) and 10 (right panel) versus electron energy. The error bars represent an uncertainty of 0.2 mm.

- Liu He participated the Nov. beam test in 2022
- Jie Yi and Prof. Zhou participated the May and June beam test in 2023

- **Shower width of 1 mm achieved.**
- **Analysis has been summarized in a paper accepted for publication in JINST and also documented in Liu He's master thesis**

SystemC 模拟

SystemC 模拟框架



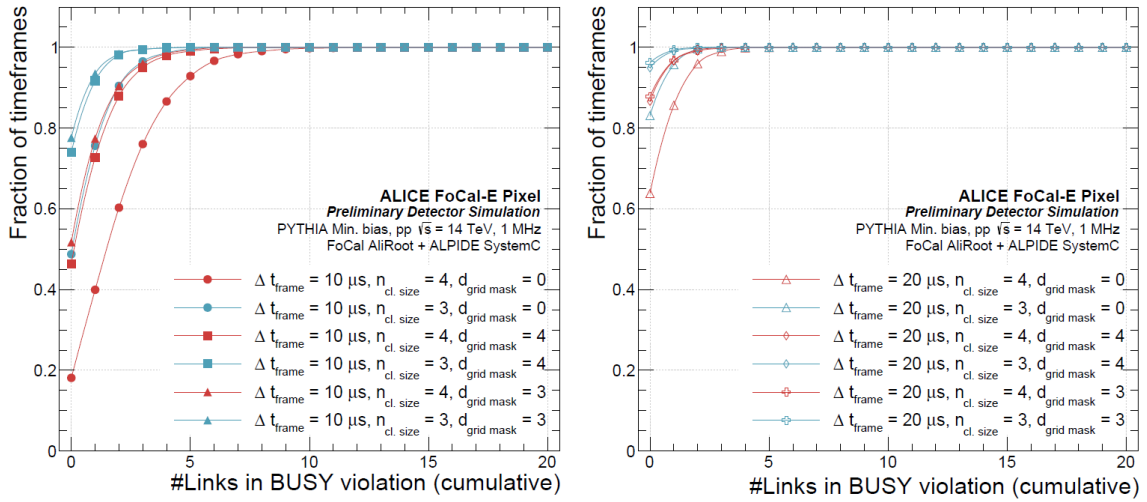
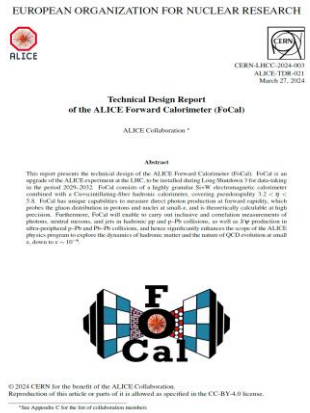


Fig. A.19: Fraction of frames with the cumulative number of links in BUSY violation for pp collisions, i. e. #Links with grid mask of $d_{\text{grid mask}} = 4$ and $d_{\text{grid mask}} = 3$, with two different timeframe lengths $\Delta t_{\text{frame}} = 10\,\mu\text{s}$ (left) and $\Delta t_{\text{frame}} = 20\,\mu\text{s}$ (right). The cumulative curves show the probability to encounter a timeframe with a maximum of #Links in BUSY violations.


EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

Technical Design Report of the ALICE Forward Calorimeter (FoCal)

- **Results from SystemC simulation have been documented in TDR, which have been approved in March 2024.**
- **It has also been fully documented in Jie Yi's master thesis**

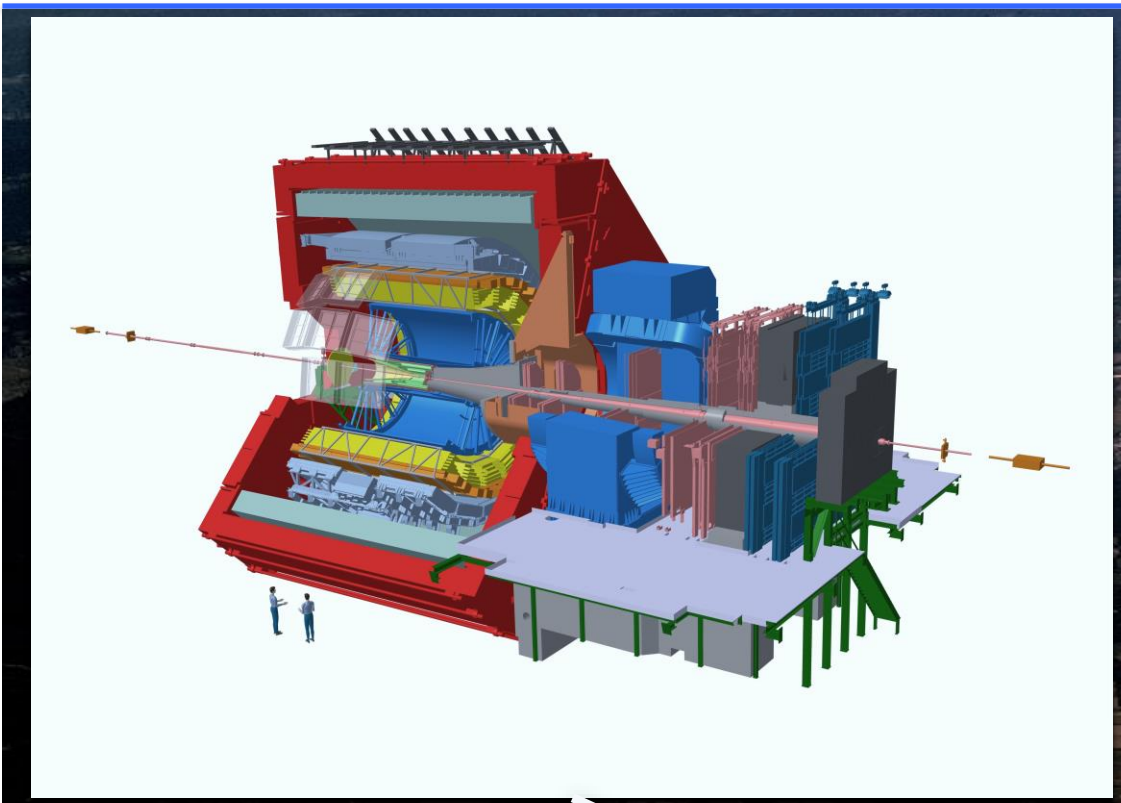
更多细节见下午易杰的报告

总结

- 课题将完成ALICE中国组承担的ALICE在LS3期间的升级任务
  - 参与用于ITS3的大面积超薄柔性硅像素芯片的研发
  - 参与FoCal探测器硅像素层及其读出电子学系统的研制
- 课题组开展的相关工作
  - ITS3 ER1芯片测试和ER2芯片设计和模拟验证正在有序推进
  - 已研制出单ALPIDE芯片工装夹具
  - 硅像素层的工装夹具正在制作之中
  - 正在建立硅像素层模块组装流程
  - 正在开发读出电子学系统的固件
  - 基于束流测试结果的文章已经被JINST接受发表
  - 系统模拟的结果被包含在TDR之中

谢谢各位专家的指导!

课题简介



- ALICE是LHC上唯一致力于重离子碰撞物理的大科学装置。
- 研究夸克-胶子等离子体（QGP）的性质及其演化规律，以深入理解由量子色动力学（QCD）主导的多粒子系统的特性，认识早期宇宙及其演化规律。

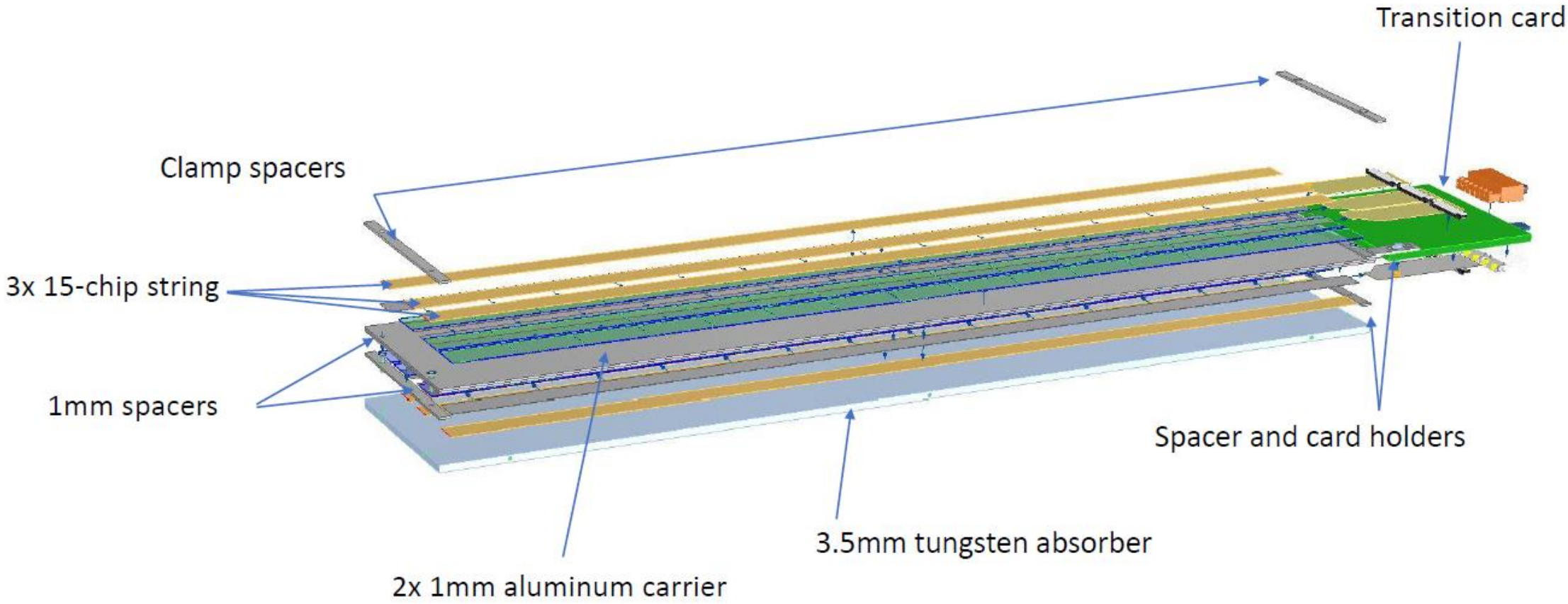
~40个国家，~172个大学和研究机构，~2000名科学家和工程技术人员

探测器建造费用： 200 M 瑞郎

本次升级总经费：18 M 瑞郎

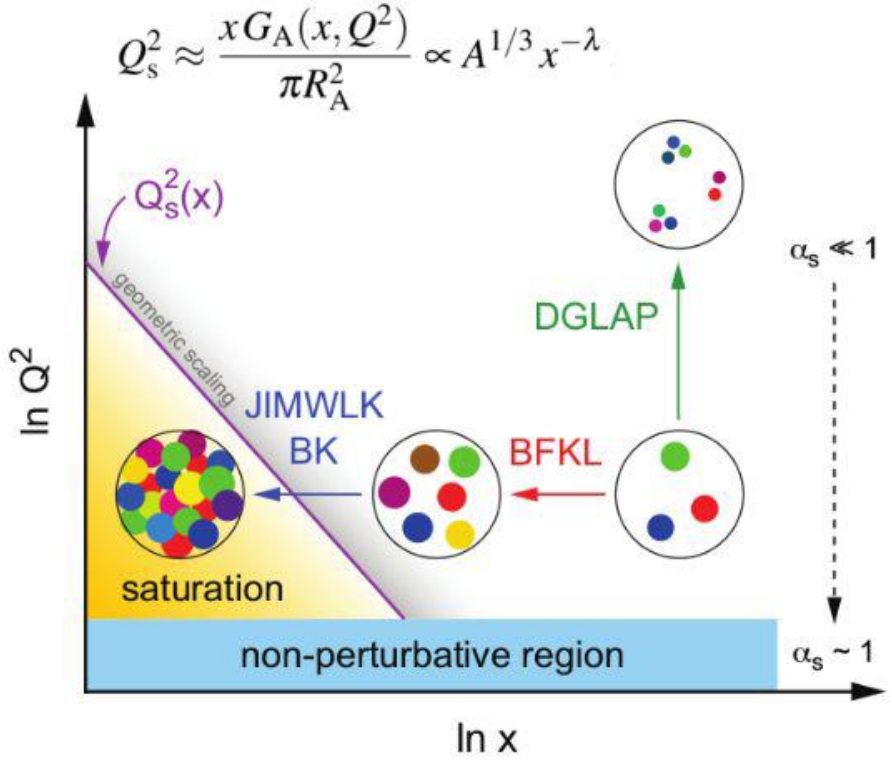
→ 中国组预期贡献：~2.8 %

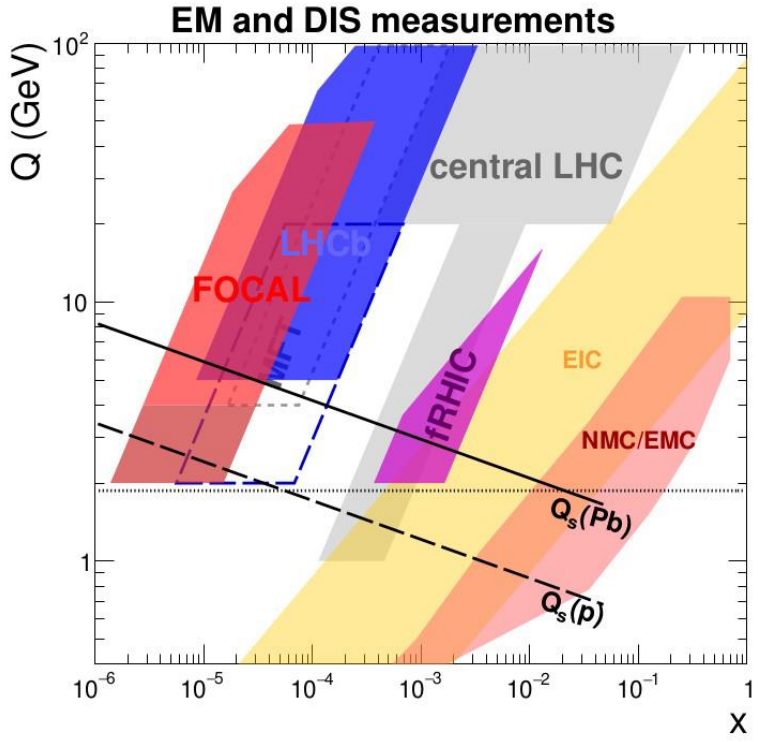
FoCal硅像素层的结构

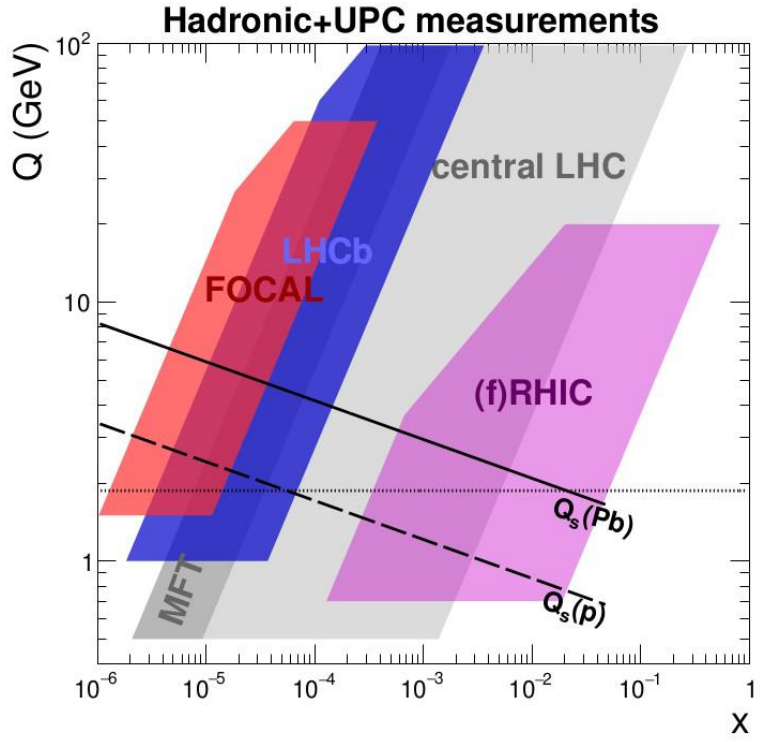


Total thickness = 3.5 (absorber) + 1.0 (spacer) + 1.0 (carrier) + 1.0 (carrier) + 1.0 (spacer) + 1.0 (spacer) = **8.5mm**

FoCal的物理目标

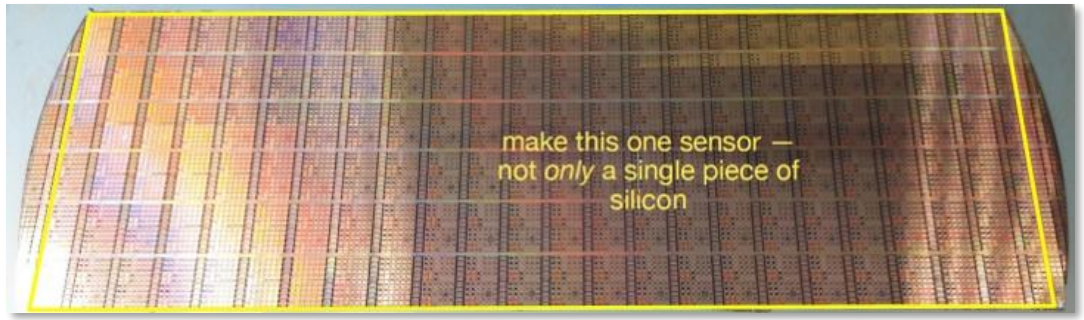


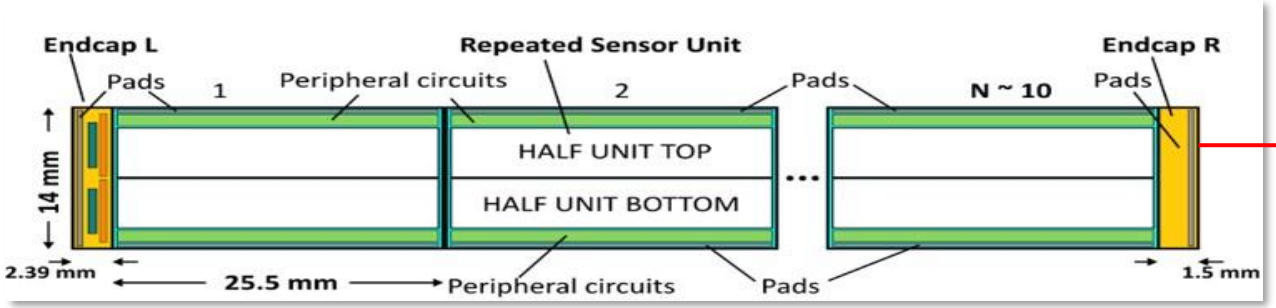


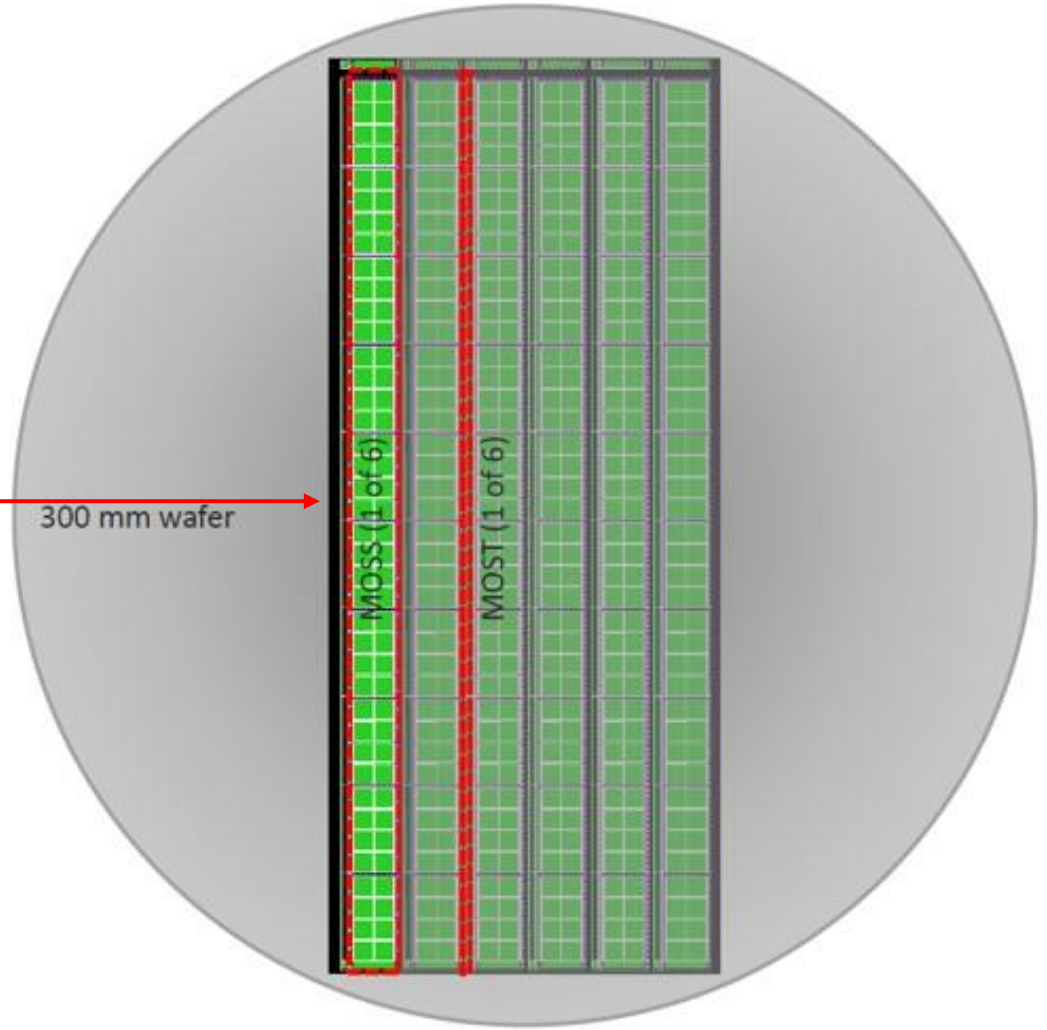


- FoCal将拓展*Q*-*x*探测区域，x低至10^{-6}，*Q*达4 GeV→测量质子-质子碰撞中前向快度区直接光子的横动量谱
- 研究小*x*物理及QCD非线性动力学→测量π^0-π^0和γ-π^0方位角关联

合作研发晶圆尺寸的超薄硅像素芯片





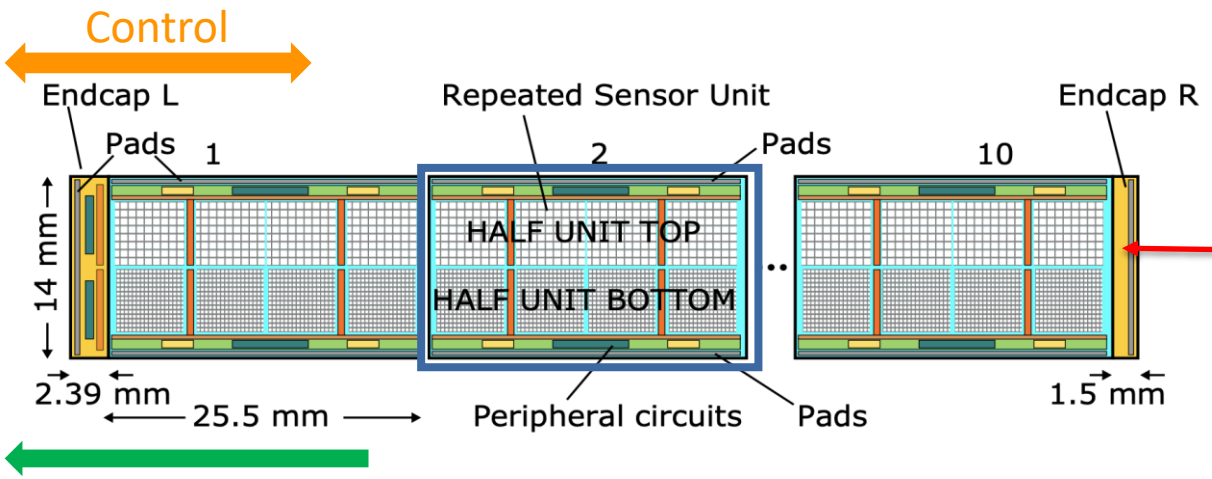


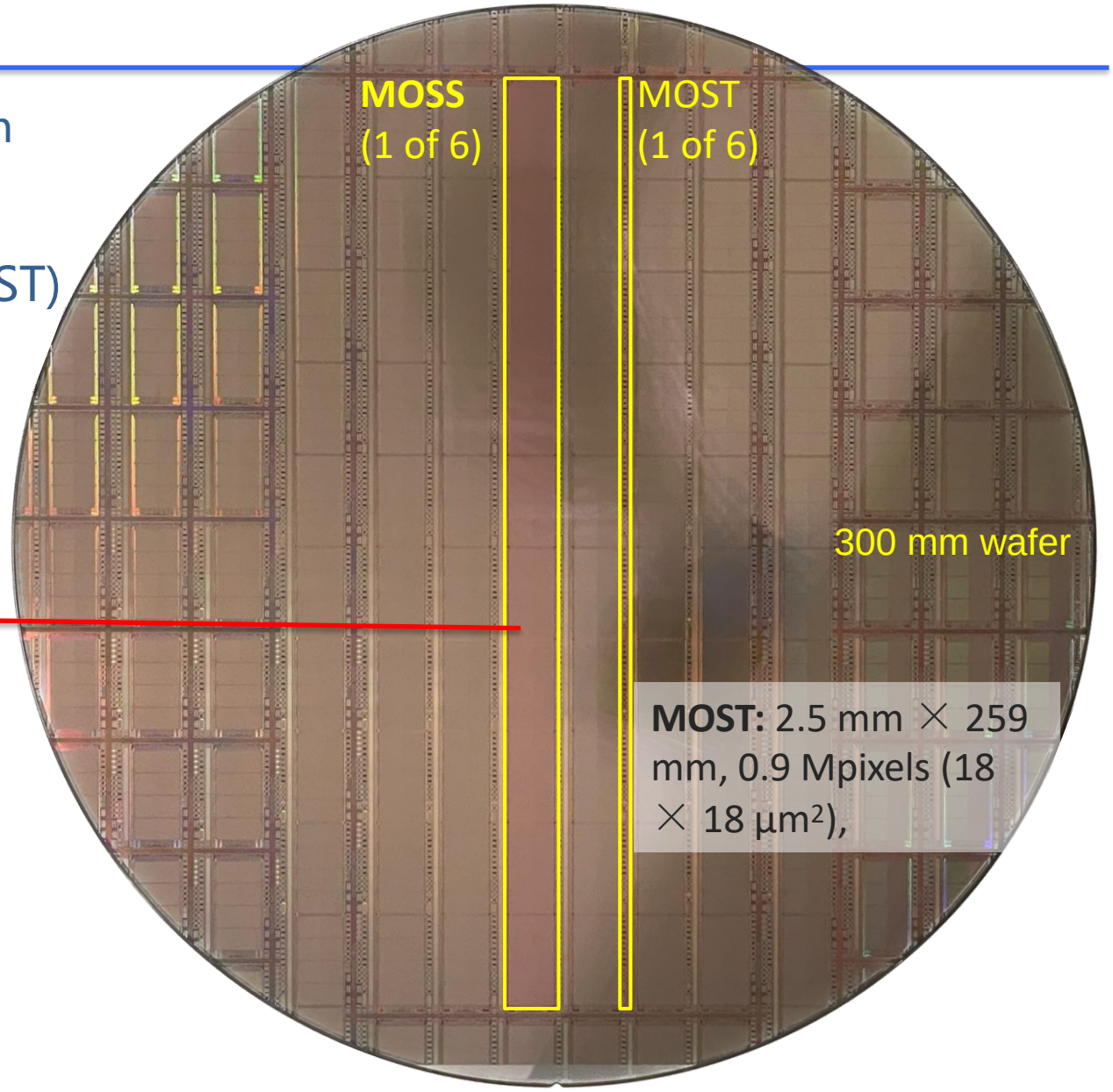
- 基于缝合技术合作研发晶圆尺寸的硅像素芯片
- 优化像素传感器读出架构，采用全局选通、优先编码、击中驱动异步读出方法，降低功耗
- 研究降低芯片对故障的敏感度的方案，以提高良品率
  - 各重复单元是独立的芯片，有独立的电源域和使能信号等
  - 缝合传输主干是唯一所有重复传感器单元共用的模块，负责控制信号和数据的传输，也有其独立的电源域

ER1 MAPS Chip

Aim at learning and proving **stitching**, submitted in December 2022

Two wafer scale stitched sensor chips (MOSS, MOST)

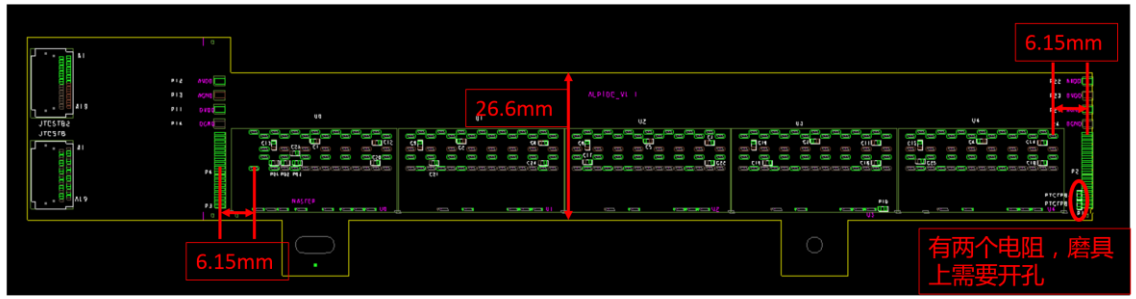


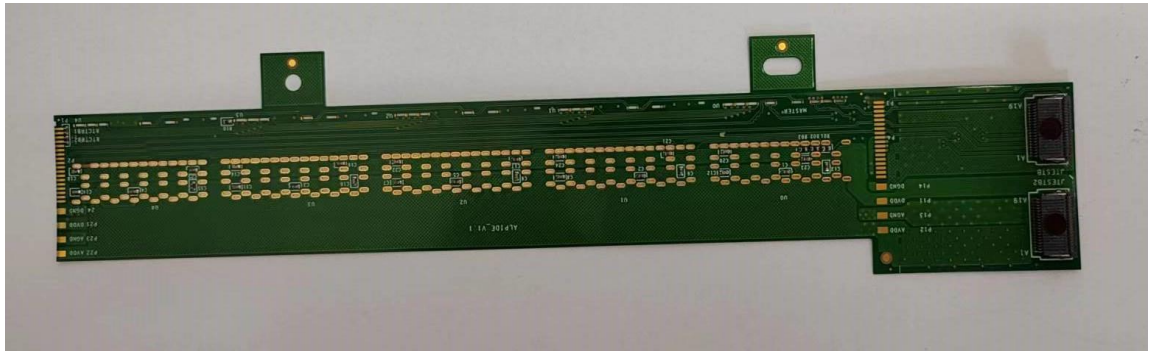


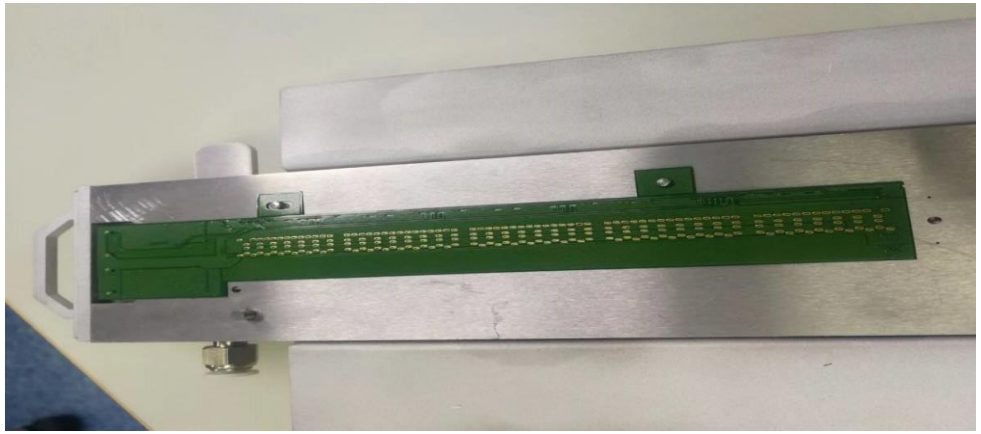
	Pixel matrix	Pixel size
Matrices on the top	256 × 256	22.5 μm
Matrices on the bottom	320 × 320	18 μm

The MOSS chip contains 20 half units and 6.72 million pixels.

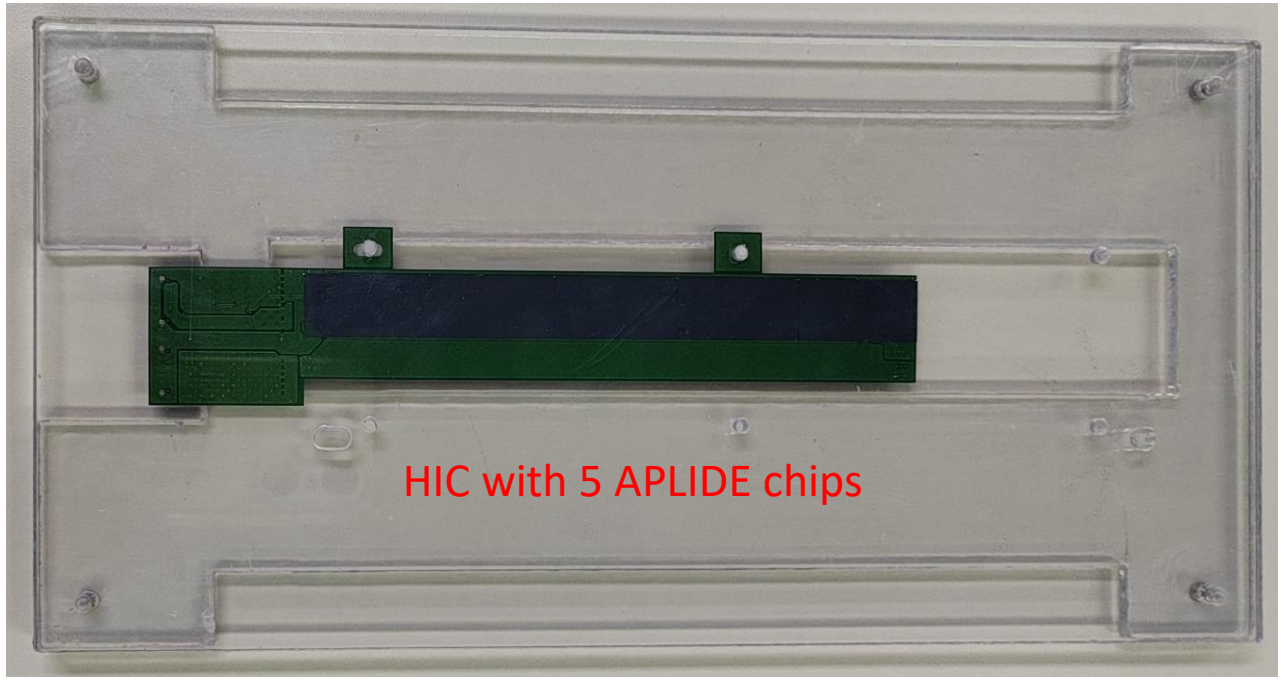
FoCal硅像素层研制进展: FPC、 夹具研制





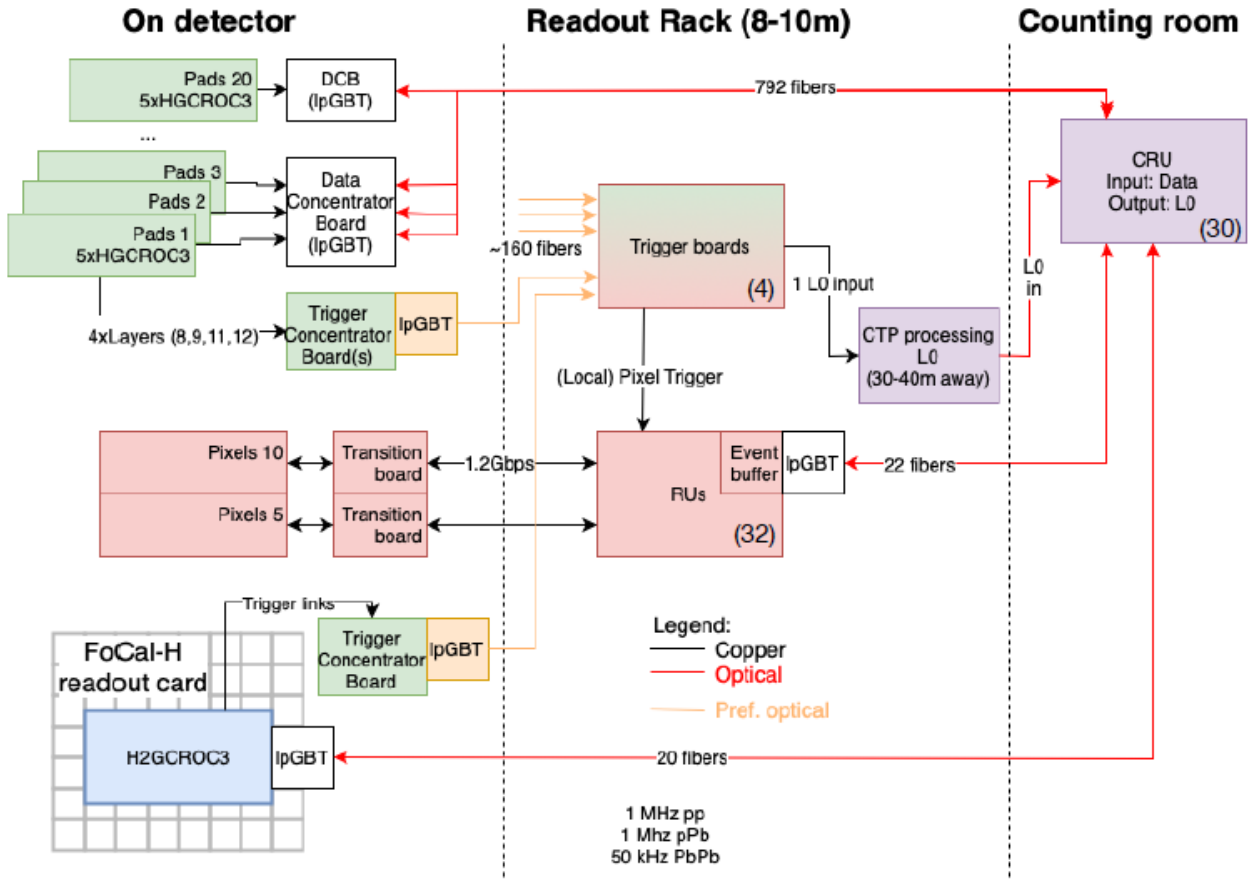


FPC gripper

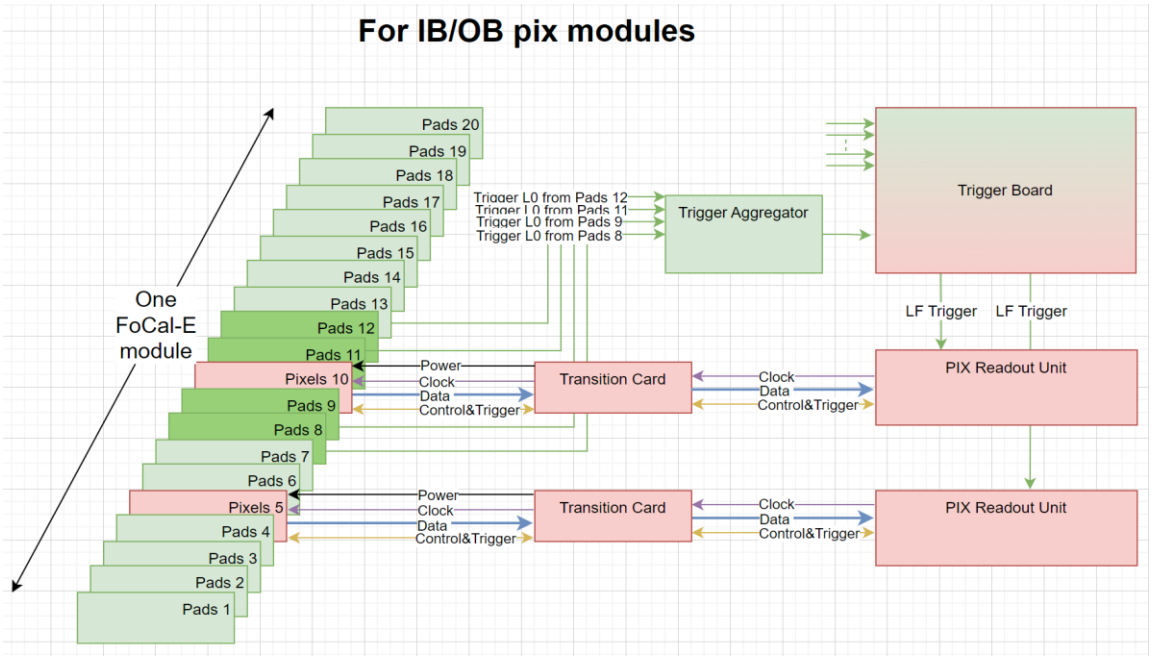


- R&D on HIC as backup solution is ended as chips have to be returned to CERN by the end of March,2023
- We are suggested to join the effort on string-based pixel layer R&D and production.

FoCal探测器硅像素层读出电子学系统



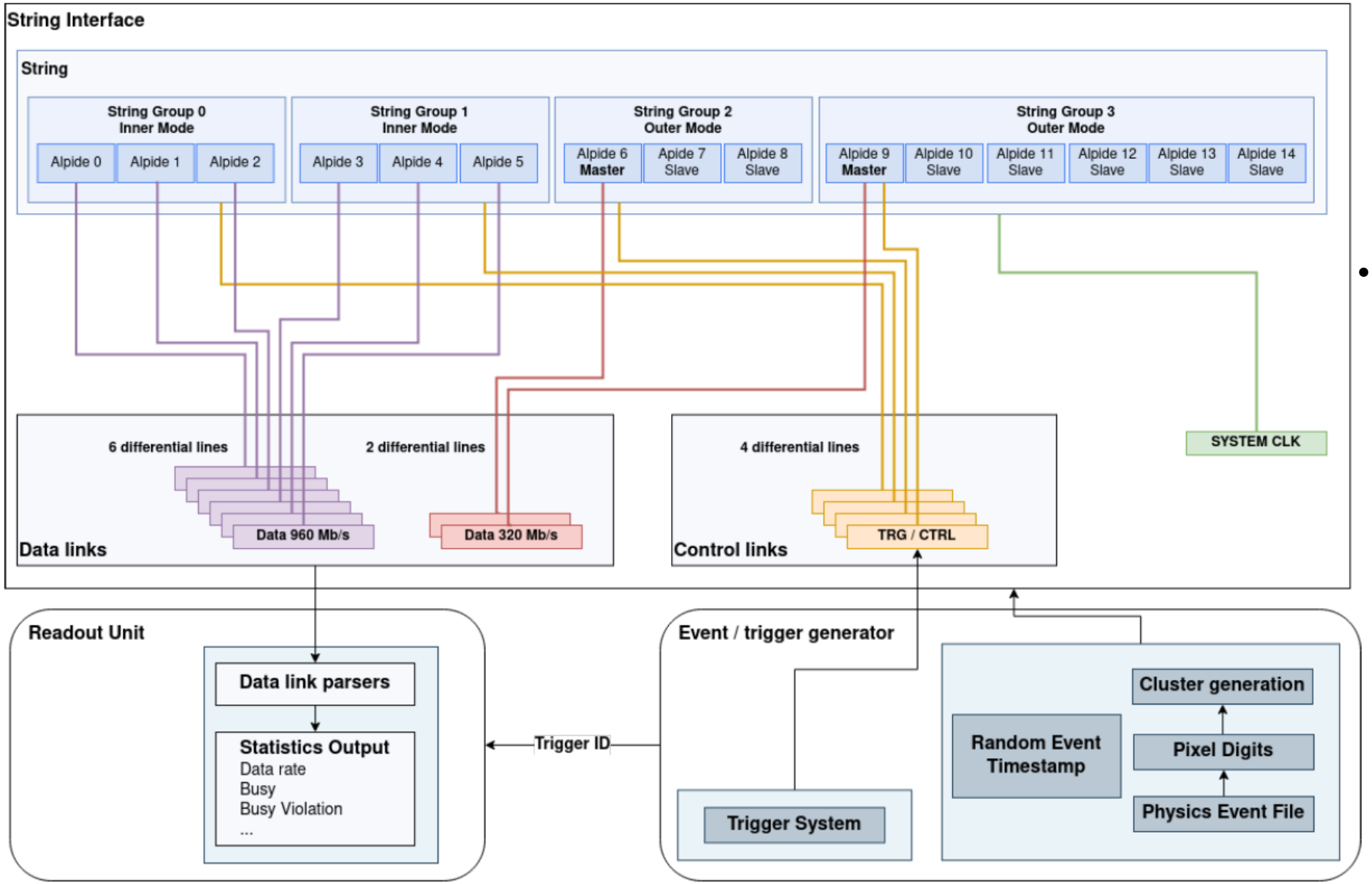
FoCal读出系统



硅像素层读出系统

- 将合作研制硅像素层读出单元

SystemC模拟框架

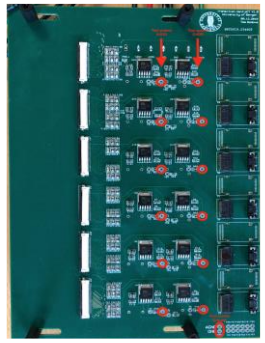


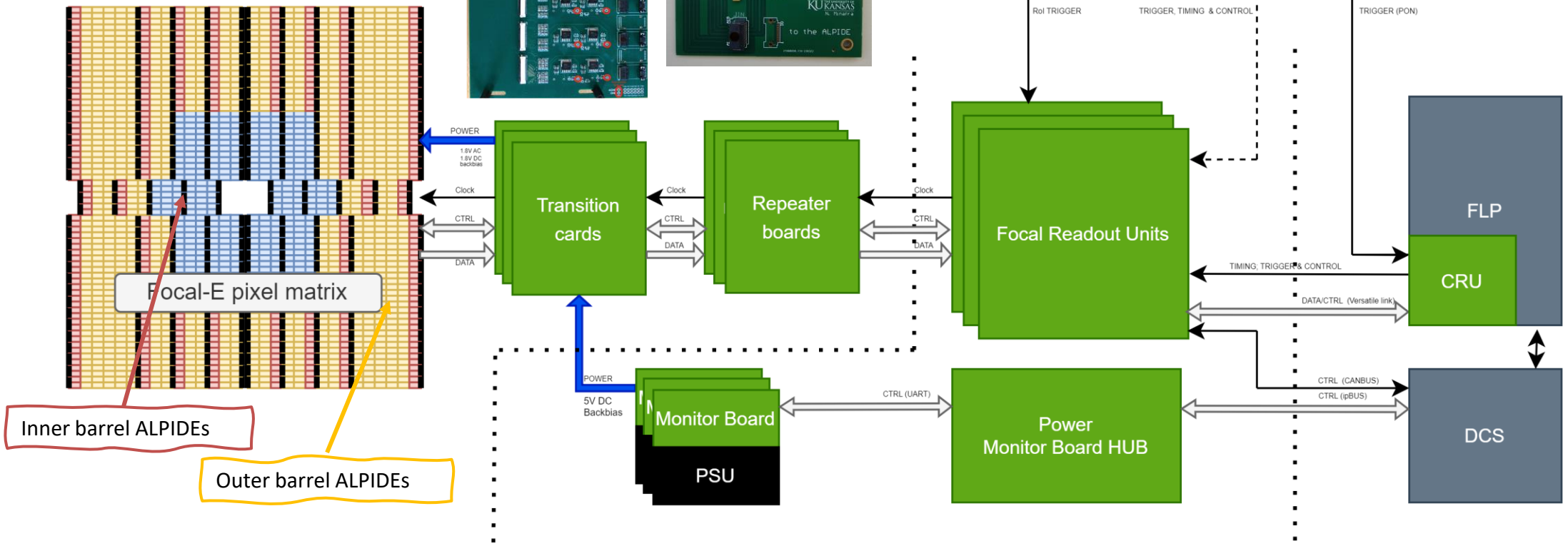
- 通过系统模拟，优化FoCal的构造和像素层的位置，在实现有效分离高能π^0衰变光子的同时，减小读出带宽和读出死（忙）时间。

FoCal硅像素层读出电子学进展

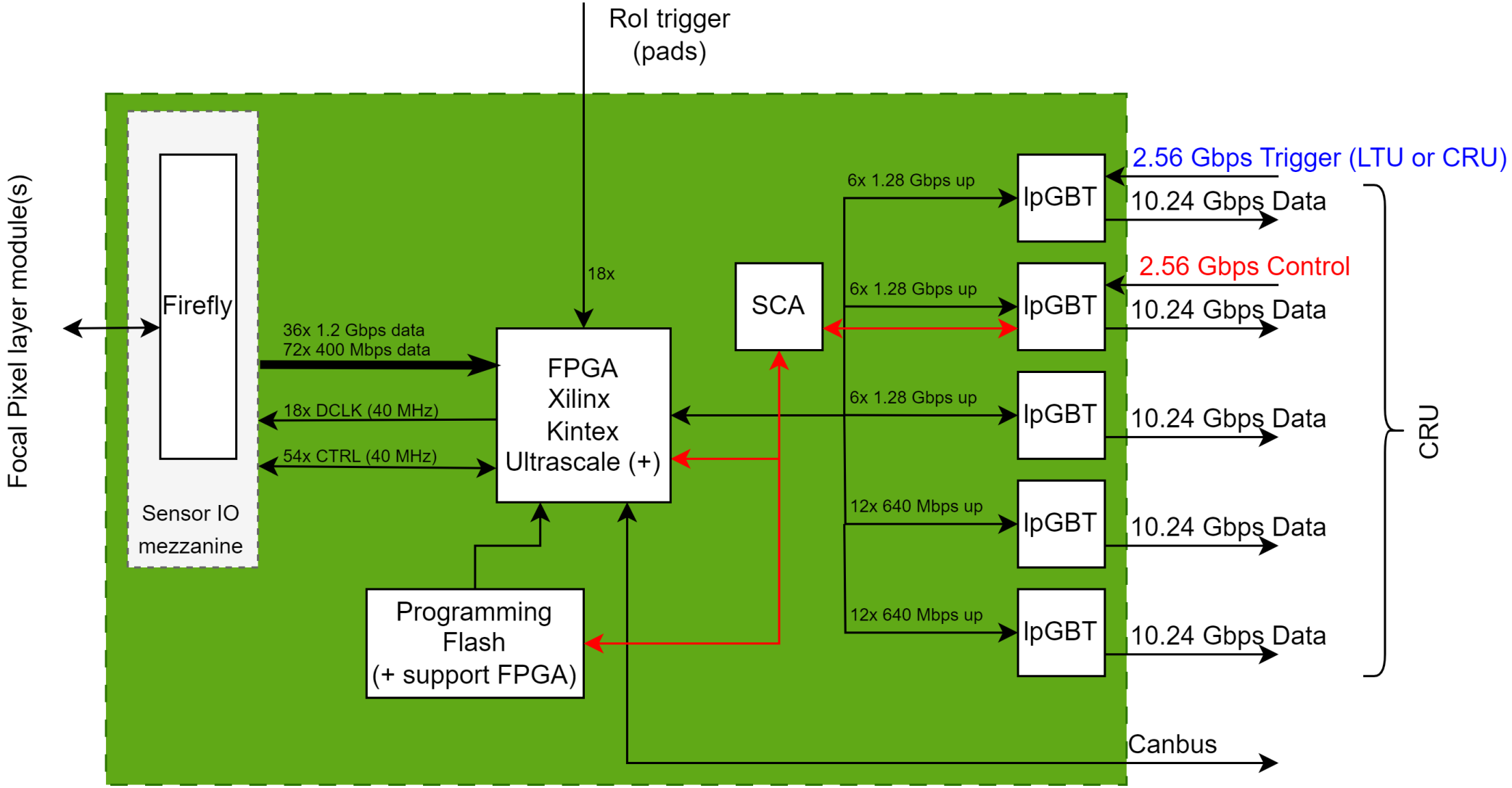
Readout chain similar to ITS2

2 detector layers
3940 ITS2 ALPIDEs



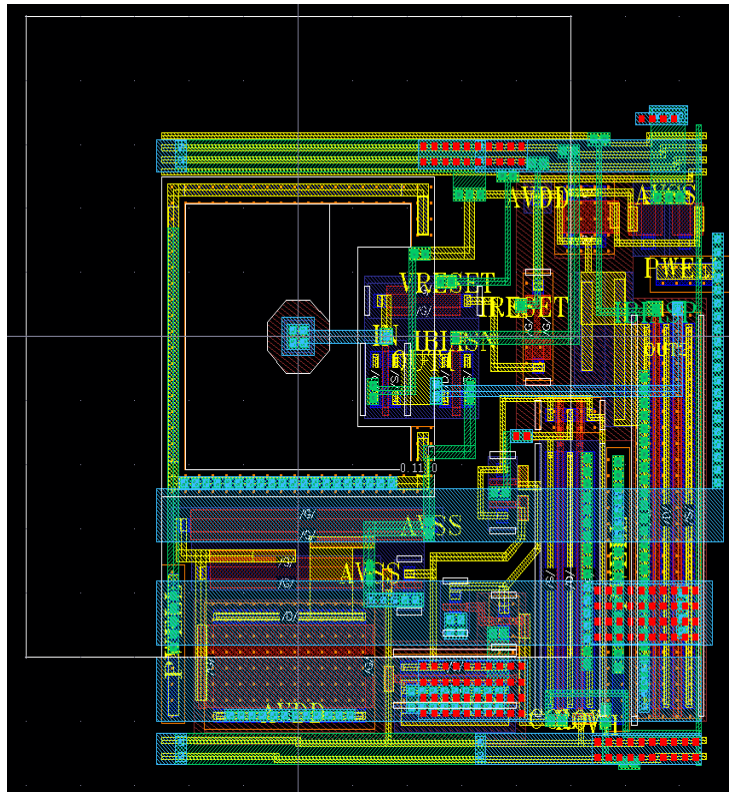


FoCal硅像素层读出电子学进展：RU

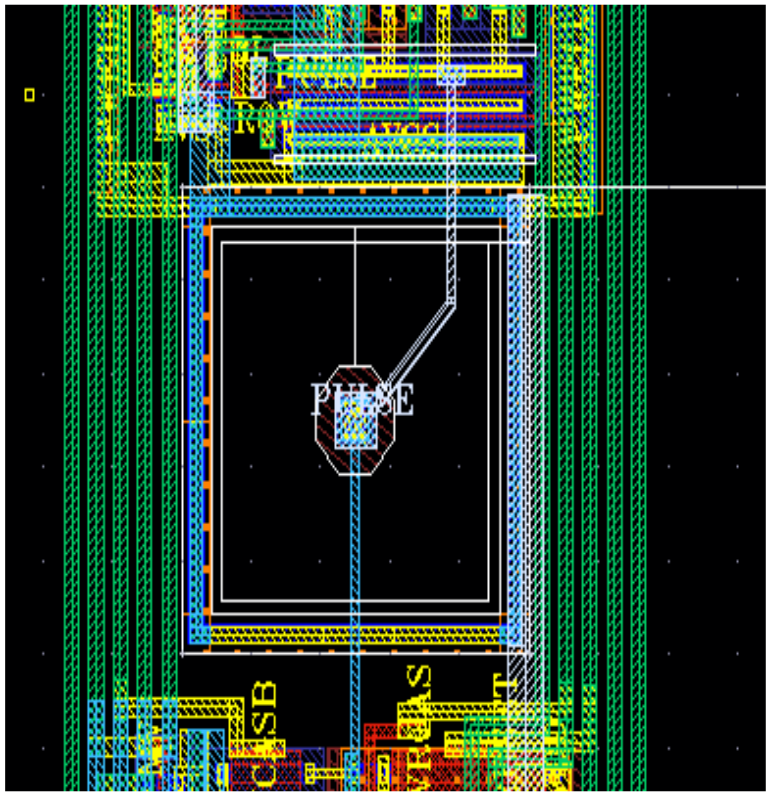


ER2芯片设计：功能优化

- Reduce the input capacitance while balance current leakage



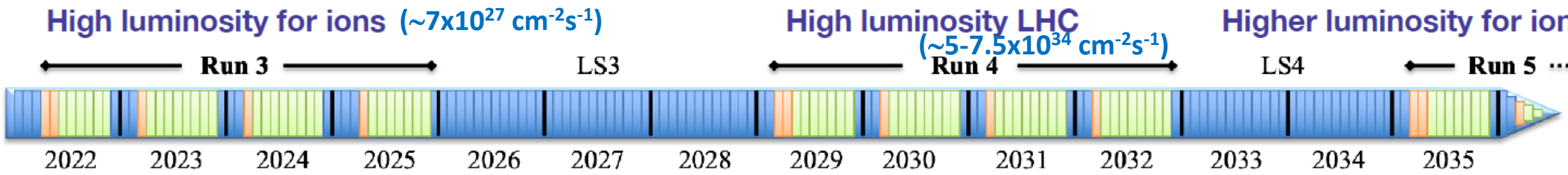
APTS



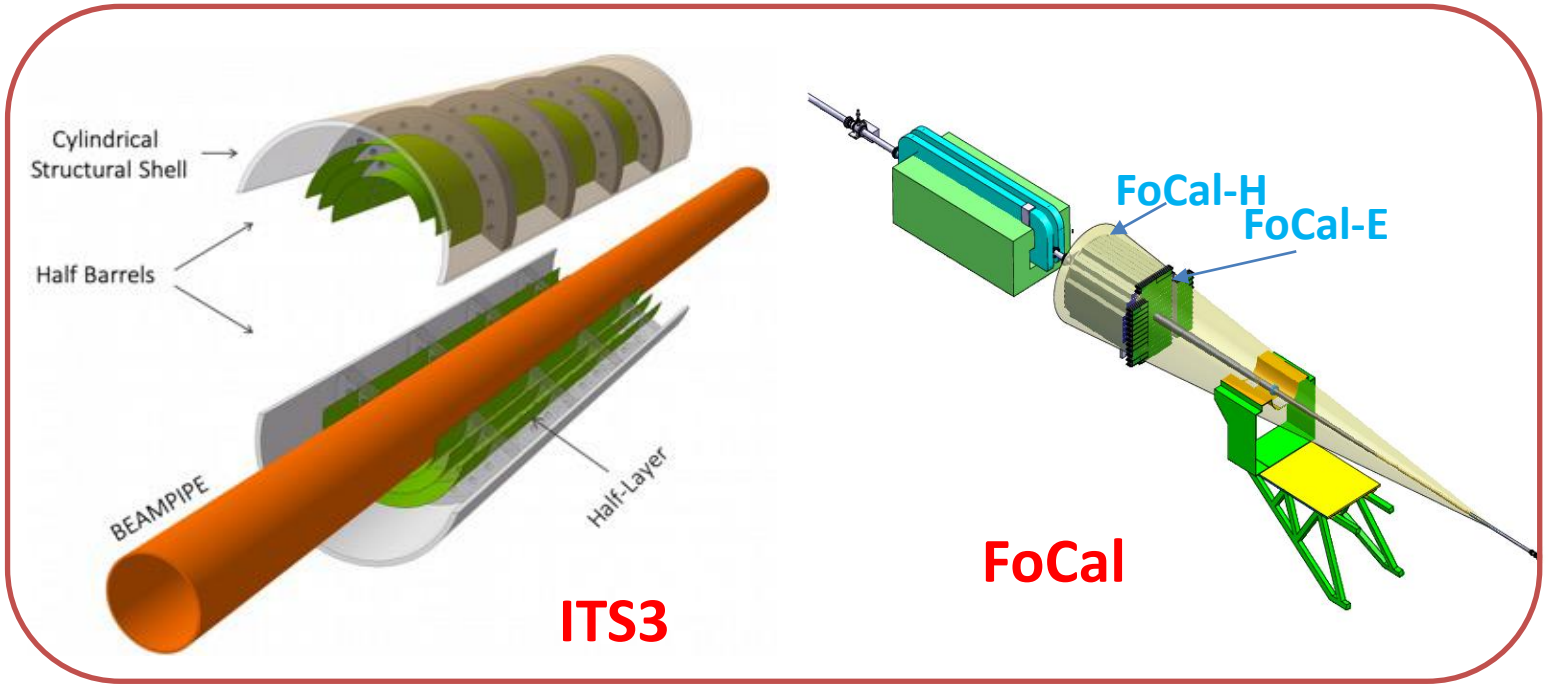
DPTS

- The length of the metal lines at the input terminal has a negligible impact on its own capacitance, approximately from 0.01 to 0.05fF.
- Concerning coupling capacitance, shortening the metal lines significantly reduces the coupling capacitance between the input terminal and the substrate PWELL, while changes in other areas are minor.
- Optimizing the layout of power lines and isolation rings can reduce some coupling capacitance.
- Additionally, removing the PULSE covering the M4 metal portion on the input terminal can decrease the coupling capacitance by approximately 0.1fF.

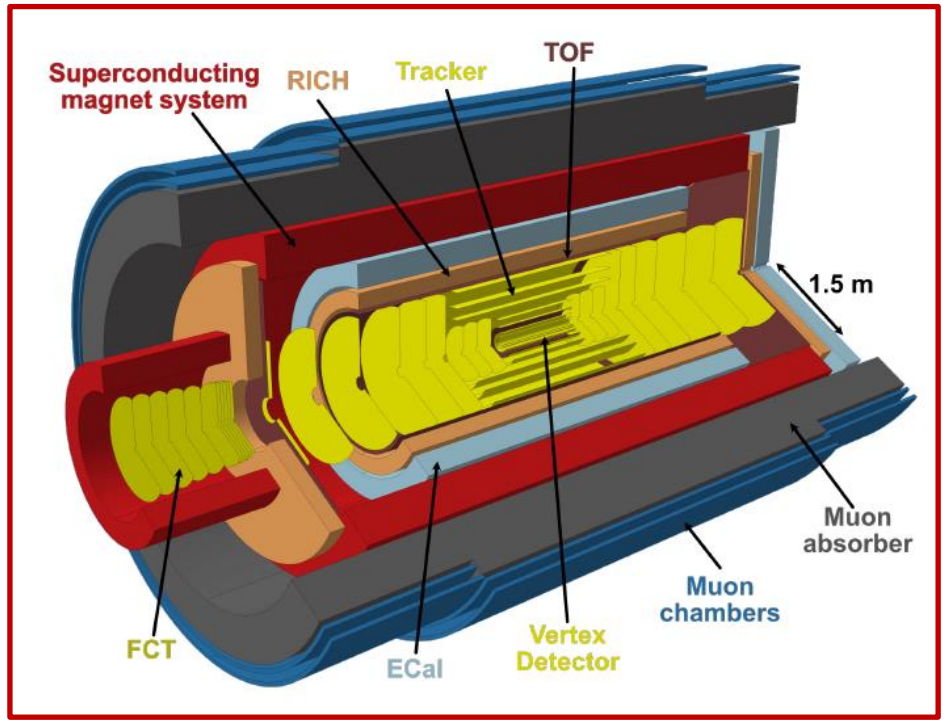
LHC运行和ALICE升级计划



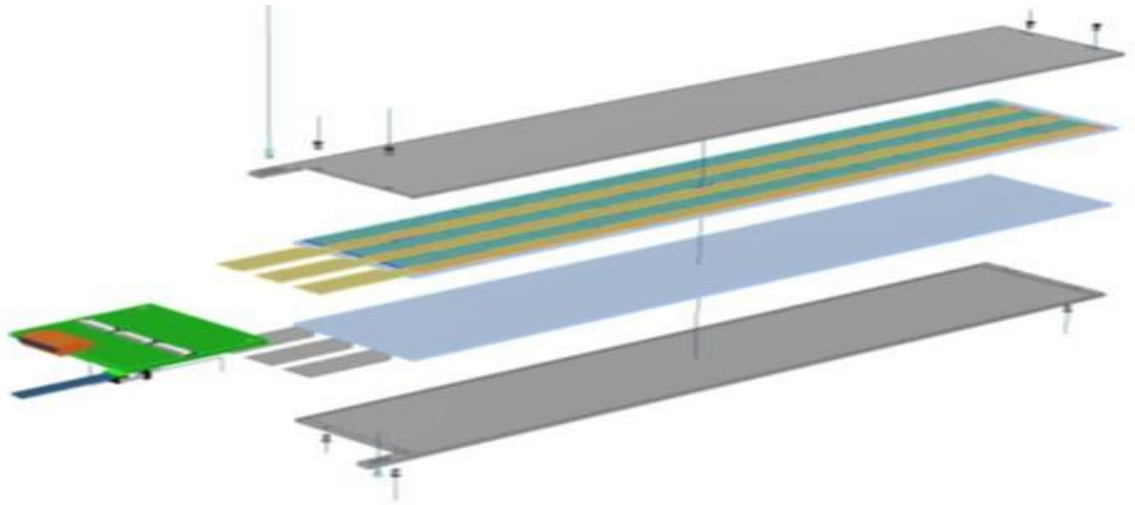
Intermediate upgrade



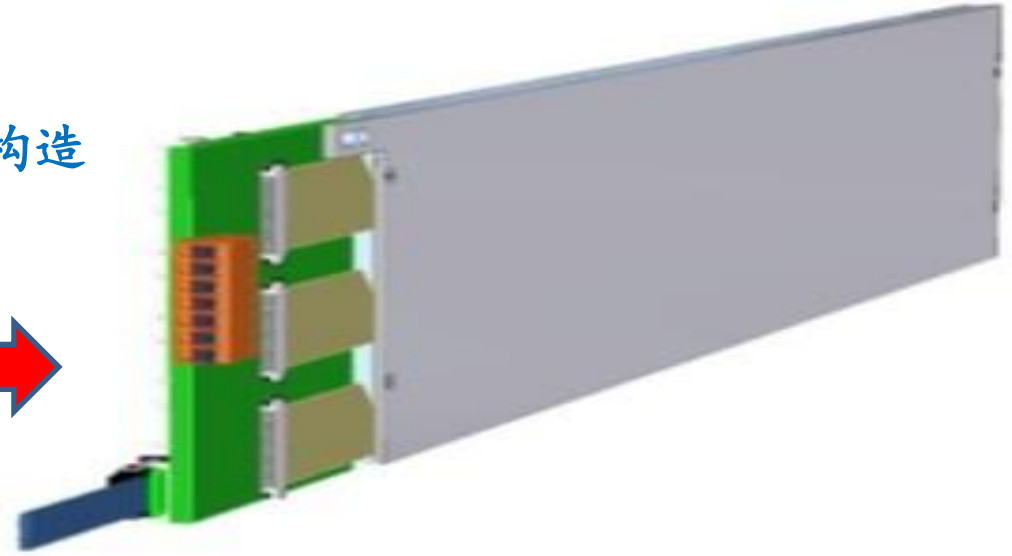
Major upgrade

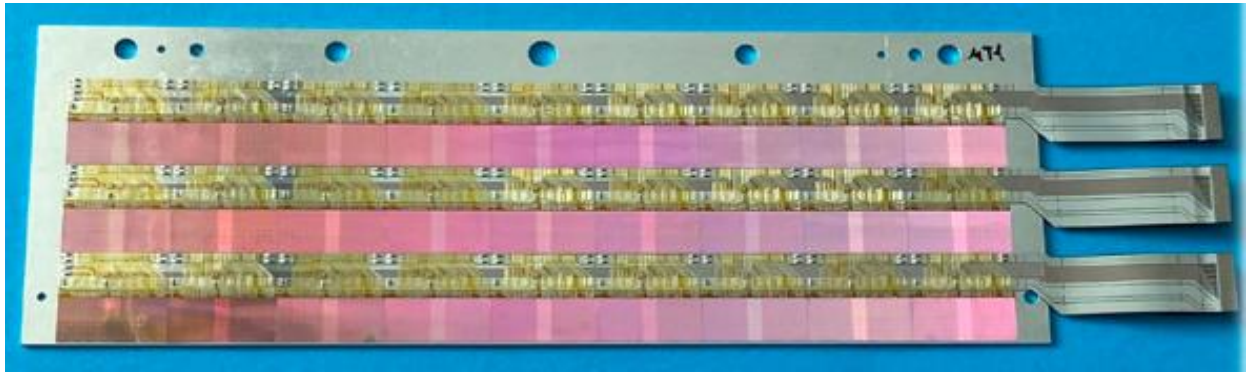


FoCal探测器硅像素层的研制

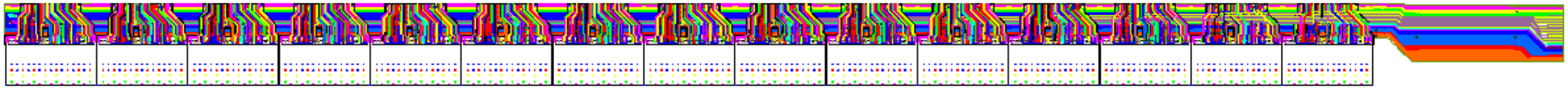


硅像素层构造





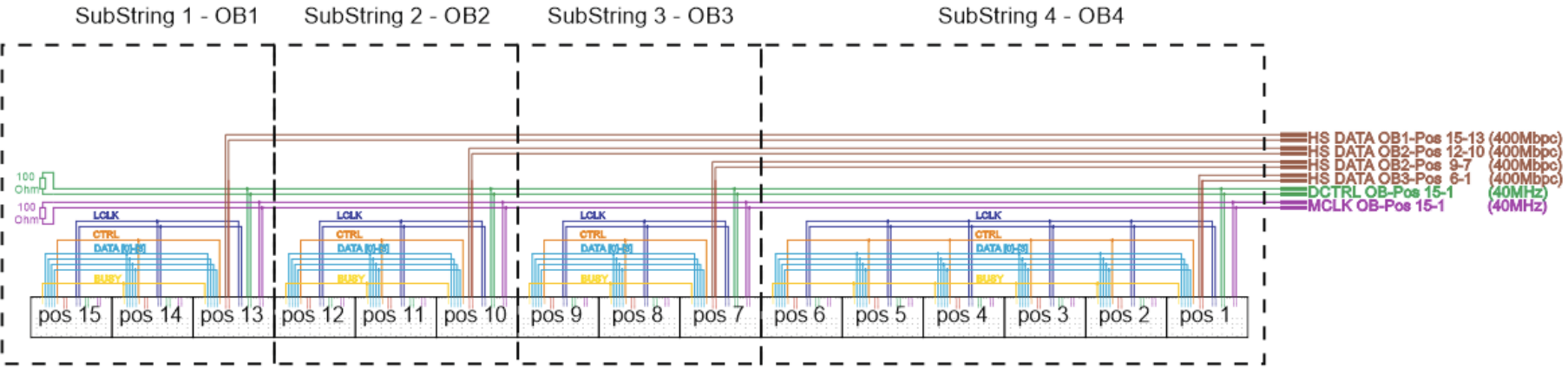
- 每个模块含 2 × 3 个长条，每个长条由15 个ALPIDE芯片及其读出柔性电路组成
- 每个模块含90个 ALPIDE芯片
- FoCal共44 个像素层模块, 需要3960个ALPIDE芯片



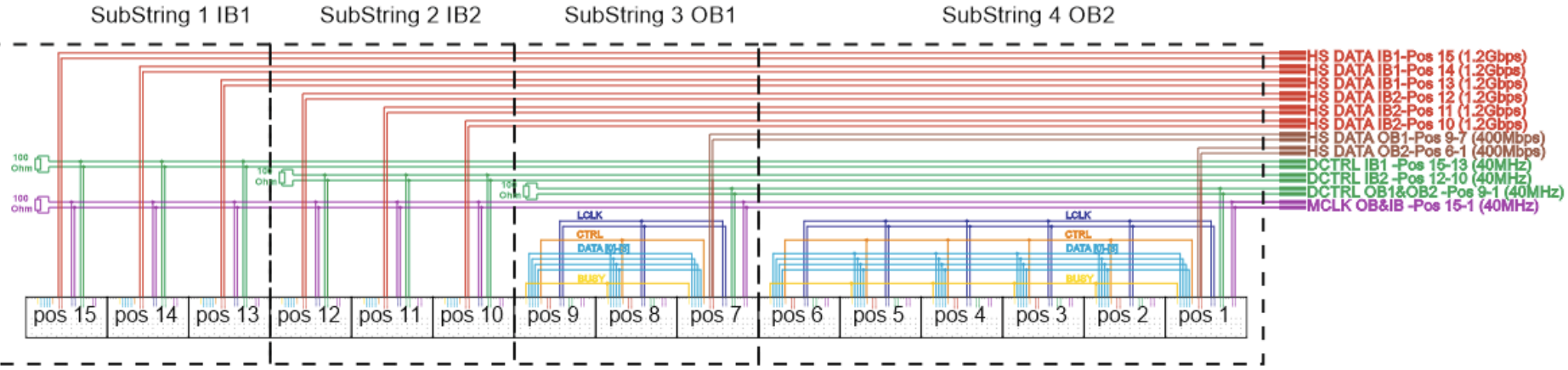
由15个ALPIDE组成的长条

FoCal硅像素层研制进展: String研制

Schematic diagram of strings



OB string



IB/OB string

- 1个由IB/OB ALPIDE芯片构成的模块 含6个长条 → 1个RU:
  - 36 IB chips @ 960 Mbps
  - 12 OB 主芯片 @ 320 Mbps

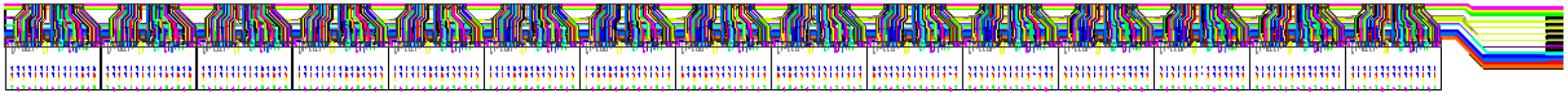
  带宽: 38.4 Gbps
- 3 个由OB ALPIDE 芯片构成的模块 → 1个RU:
  - 每个模块含24个OB主芯片
  - → 72 个OB 主芯片 @ 320 Mbps

  带宽: 23.4 Gbps

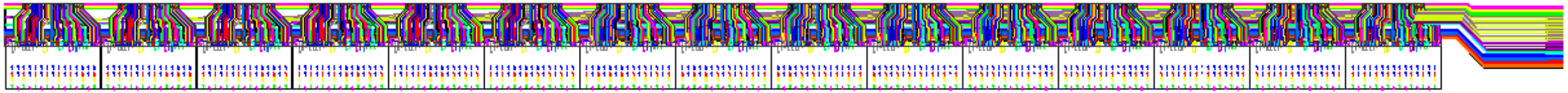
FoCal硅像素层研制进展: String研制

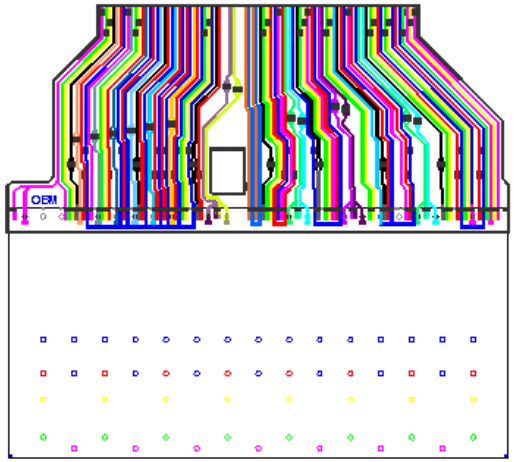
Layout of the strings

IB/OB string

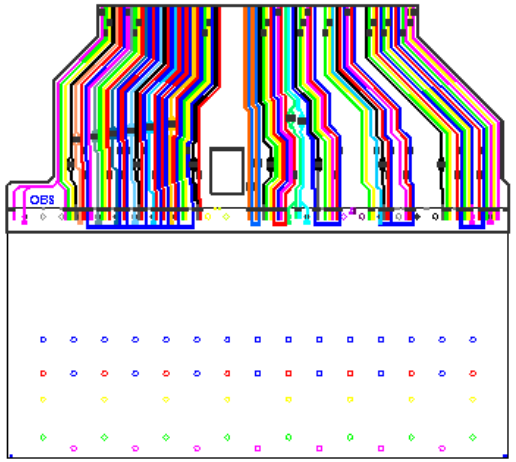


OB string

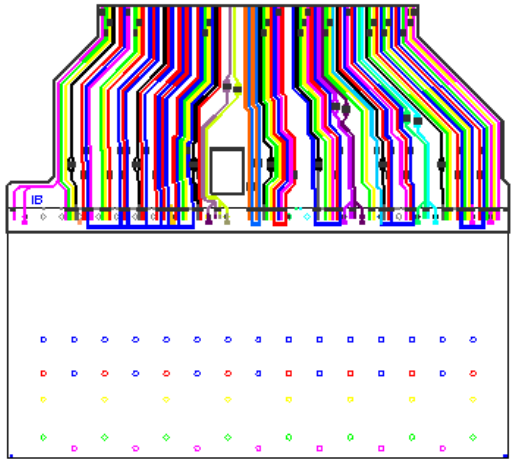




OB-M



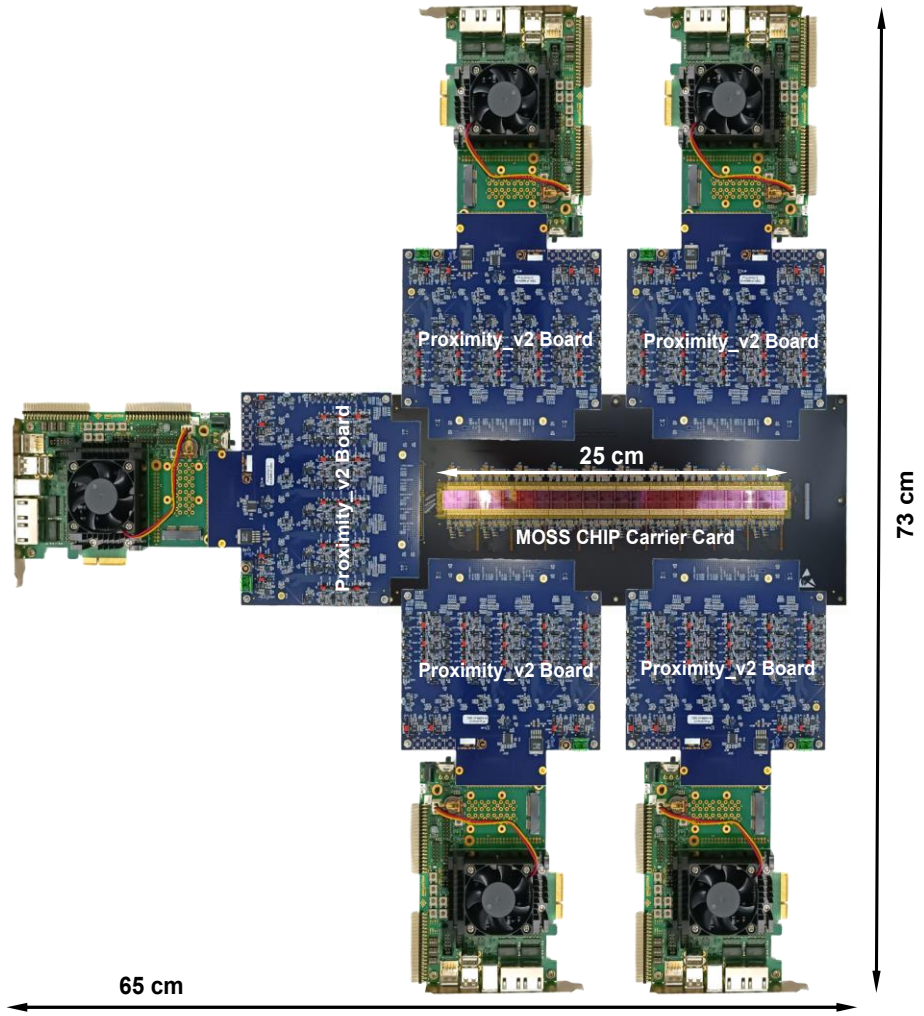
OB-S



IB

Three different types of chip-cables are designed as similar as possible

ER1单片缝合芯片性能测试: 产率



ER1 test system

Yields

		RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10
Wafer 20	1-TOP	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - II	OK - II	OK - I	OK - II
	1-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - II	OK - I
	2-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	2-BOT	OK - II	OK - I	OK - I	LIMIT	OK - II	OK - I	OK - I	OK - I	OK - I	OK - II
	3-TOP	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I
	3-BOT	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - II	OK - I	LIMIT	OK - I	OK - II
	4-TOP	OK - I	OK - I	LIMIT	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - II	OK - I
	5-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I
	5-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	6-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - II	OK - II
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
Wafer 21	1-TOP	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - II	OK - II
	1-BOT	OK - II	OK - II	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I
	2-TOP	OK - I	OK - II	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I
	2-BOT	LIMIT	OK - II	OK - I	OK - II	OK - I	LIMIT	LIMIT	OK - I	OK - I	OK - II
	3-TOP	OK - II	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	3-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	4-TOP	OK - I	OK - II	OK - I	OK - I	OK - II	LIMIT	OK - I	OK - II	OK - I	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - II	OK - II	LIMIT	LIMIT
	5-TOP	LIMIT	OK - I	OK - I	OK - II	OK - I	OK - I	OK - II	OK - II	OK - I	OK - II
	5-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - II
	6-TOP	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	LIMIT	OK - II	OK - I	OK - II
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	LIMIT	OK - I
Wafer 22	1-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	1-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	2-TOP	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II
	2-BOT	LIMIT	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I
	3-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	3-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	4-TOP	OK - I	OK - I	OK - I	OK - II	OK - II	OK - I	OK - II	OK - II	OK - II	OK - I
	4-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I
	5-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I
	5-BOT	OK - I	OK - I	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
	6-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I
	6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - II	OK - I	OK - I

115/120 'OK' (95.8%)
19 HUs 'OK-II'
5 HUs 'LIMIT'

109/120 'OK' (90.8%)
29 HUs 'OK-II'
11 HUs 'LIMIT'

116/120 'OK' (96.7%)
11 HUs 'OK-II'
4 HUs 'LIMIT'