ALICE内径迹探测器硅像素芯片的设计

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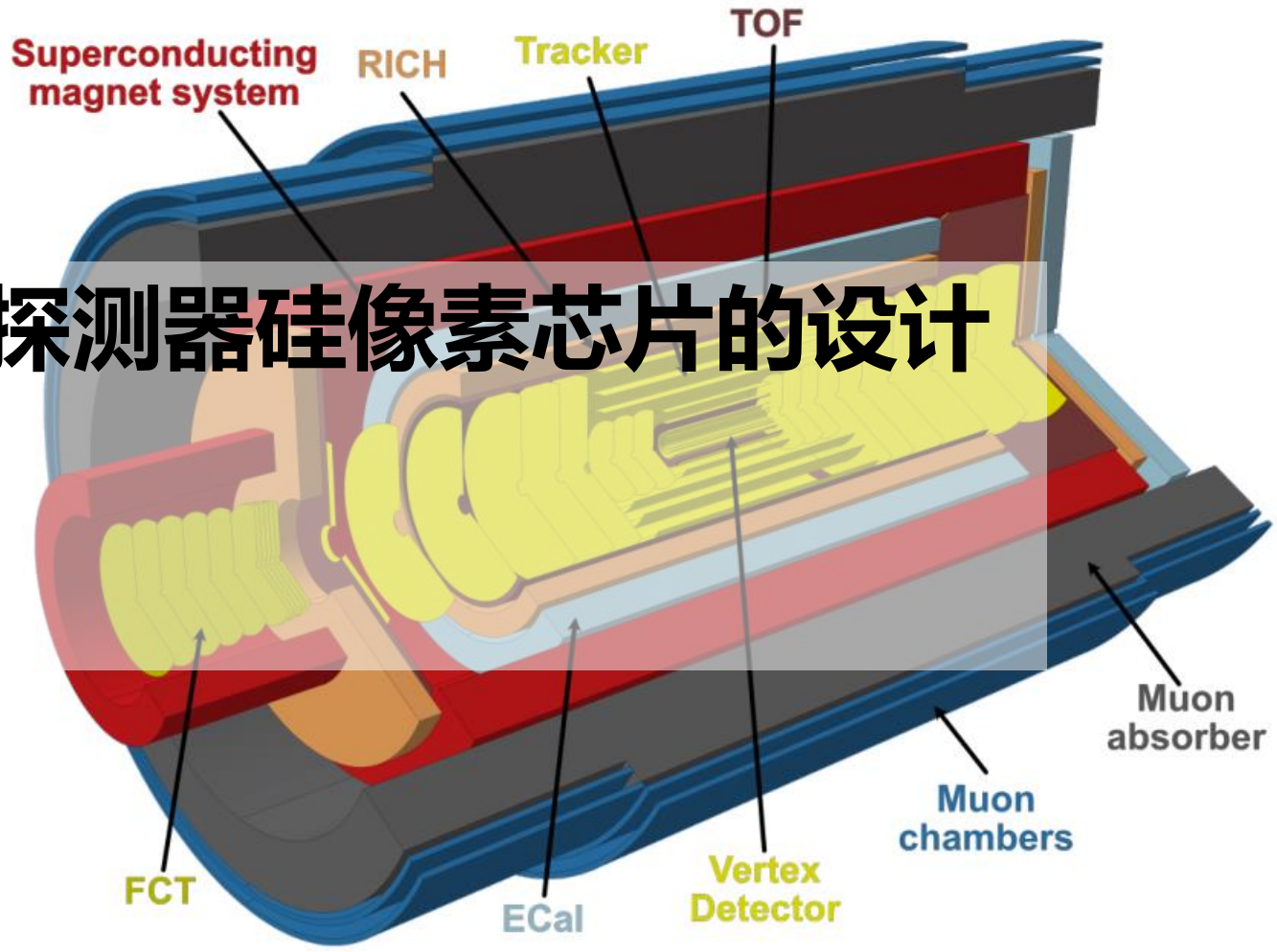
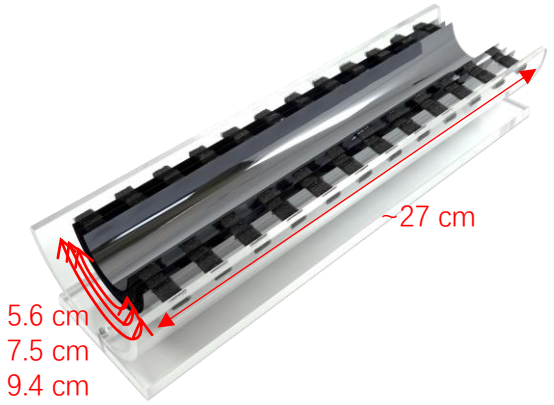
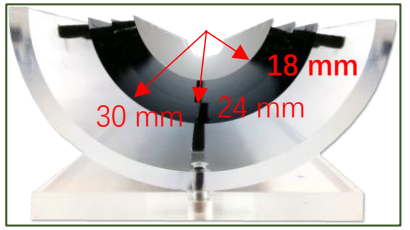


ITS3 ENGINEERING MODEL

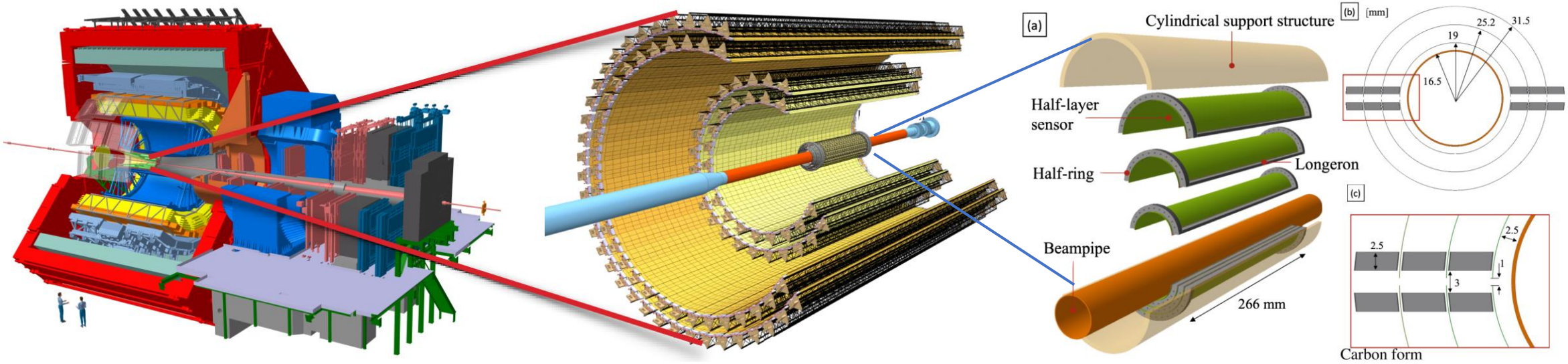




ALICE

2024年7月13日

Review: ITS2 & ITS3



ITS2

7 Layers:
➞3 inner barrel (IB) and 4 outer barrel (OB)
Large active area and granularity
➞10m^2 active silicon area, 12.5 x 1E9 pixels
Built with ALPIDE chips
➞180nm CMOS MAPS, 15 x 30 mm^2, 512 x 1024 pixels

* M. Mager, for ALICE Collab, NIM-A 824, 434 (2016)

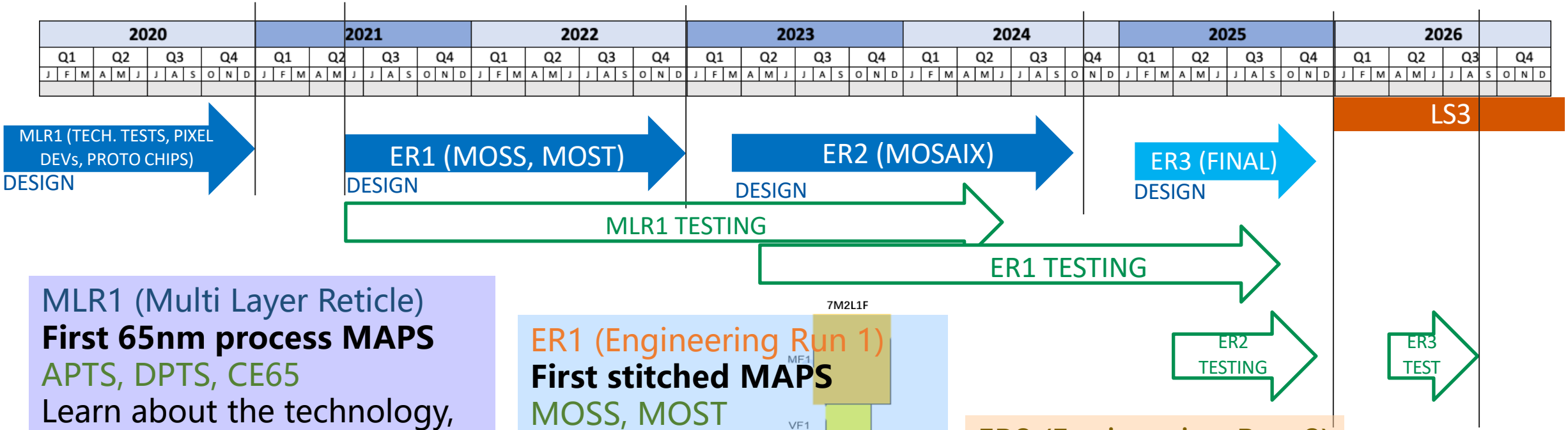
ITS3 TDR: CERN-LHCC-2024-003

ITS3: replacement of ITS2 inner barrel

Bent wafer-scale sensor ASIC
➞65 nm CMOS MAPS
➞Fabricated with stitching
➞Power density < 40 mW/cm^2
3 layers with 6 sensors
Air cooling between layers

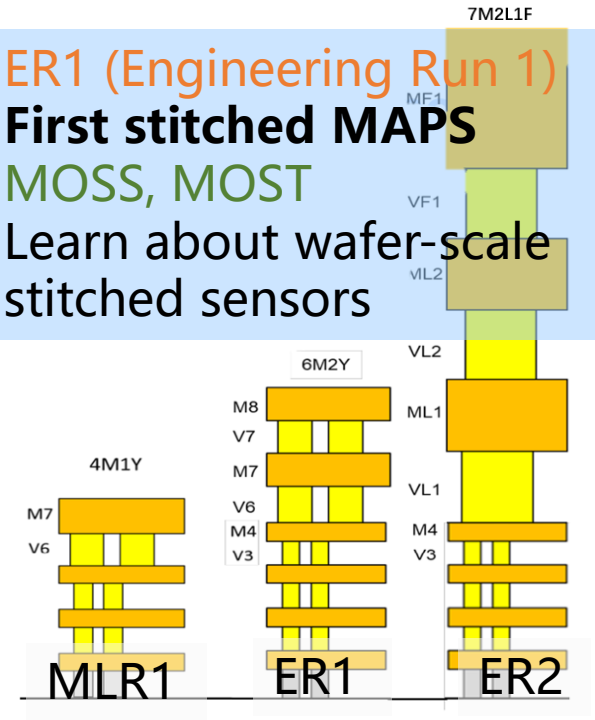
Closer to interaction point
➞Beampipe: 18.2 mm → 16.0 mm
➞Layer 0 position: ~24 mm → 19.0 mm

ITS3 Chip development roadmap



MLR1 (Multi Layer Reticle)
First 65nm process MAPS
APTS, DPTS, CE65
Learn about the technology, characterize pixels, transistors and building blocks

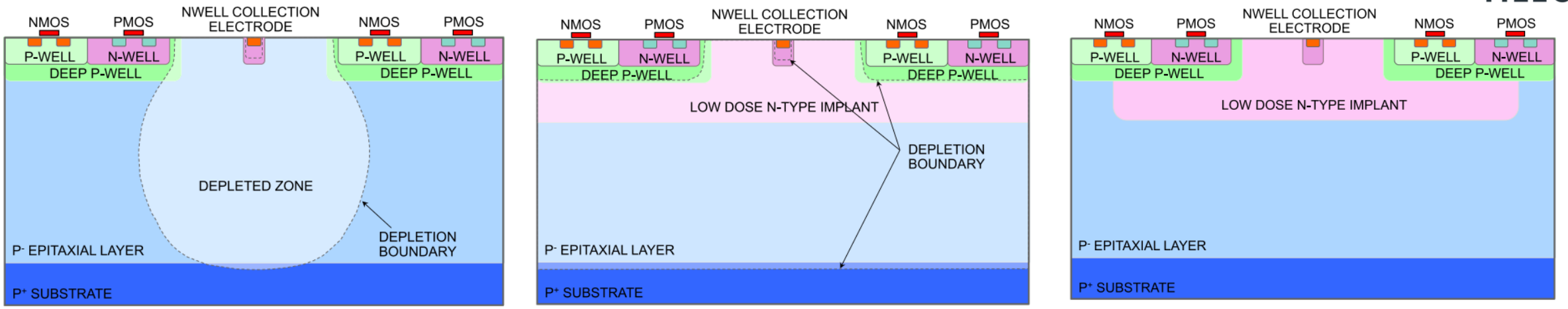
ER1 (Engineering Run 1)
First stitched MAPS
MOSS, MOST
Learn about wafer-scale stitched sensors



ER2 (Engineering Run 2)
ITS3 sensor prototype
MOSAIX
Design ongoing

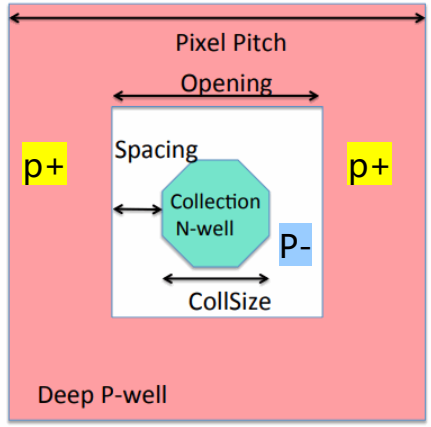
ER3 ITS3 sensor production

Sensor design

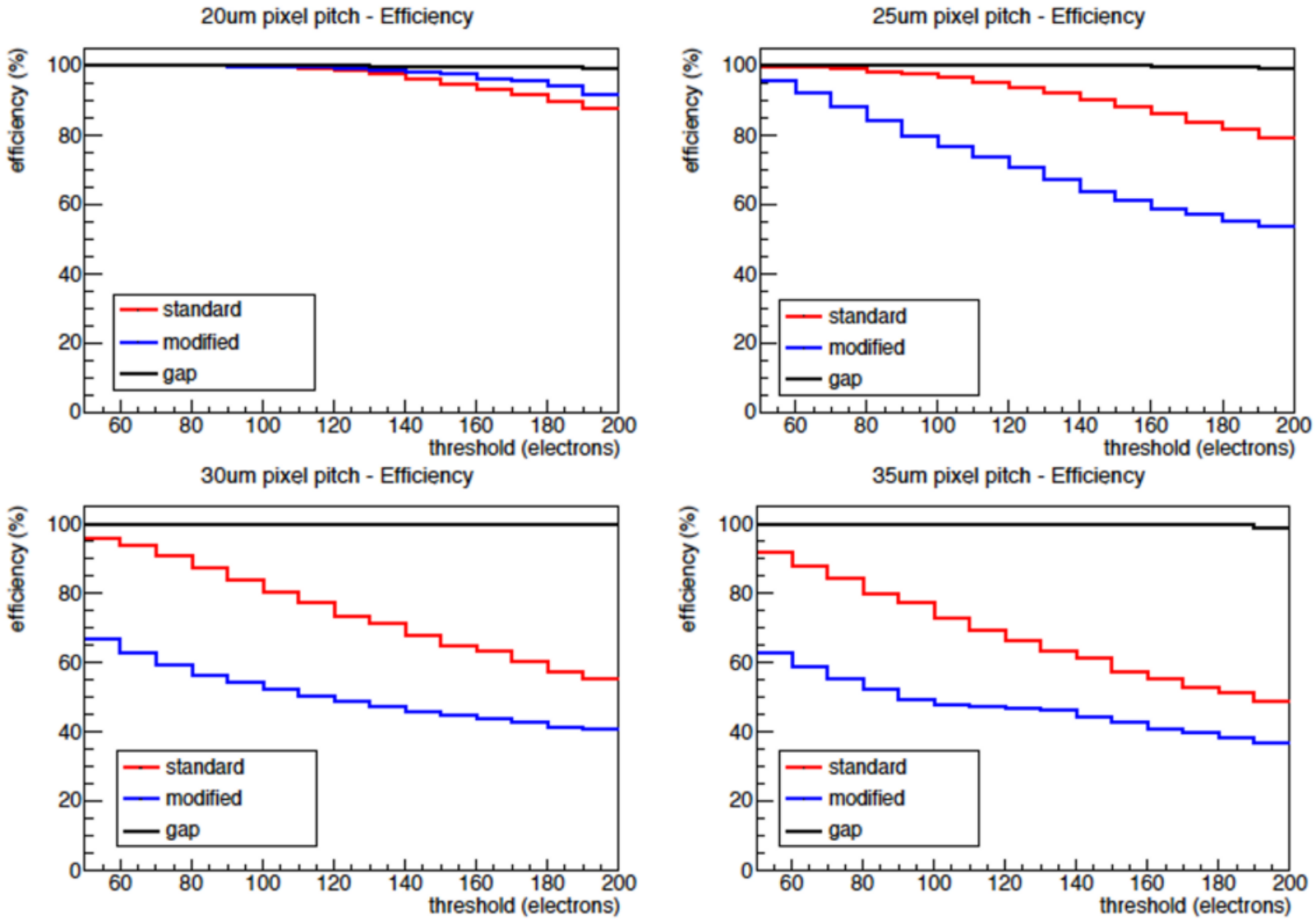


(a) standard (b) low-dose n− implant (c) with gap in the implant

Cross-sections of three different pixel designs implemented



layout(top view)

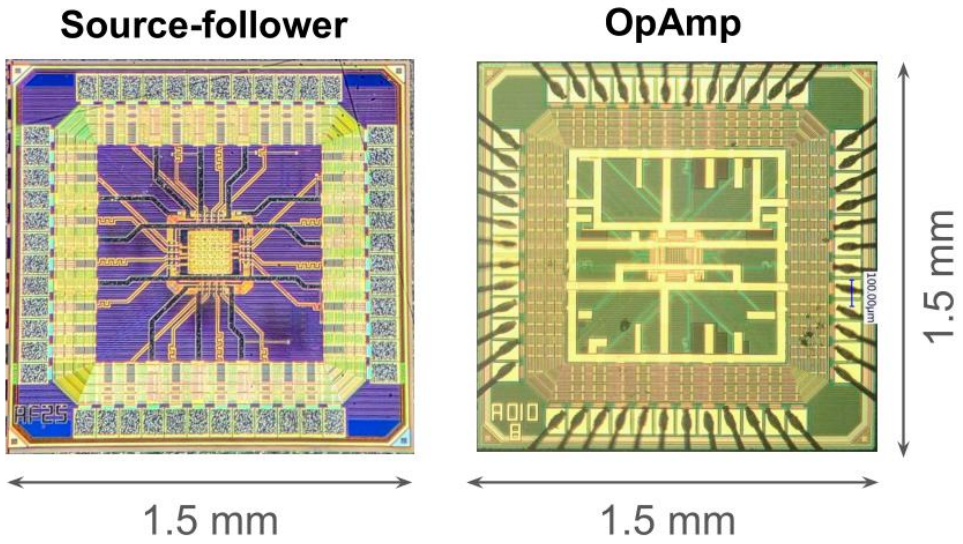


CERN-LHCC-2024-003 ; ALICE-TDR-021

MLR1 Chips

APTS

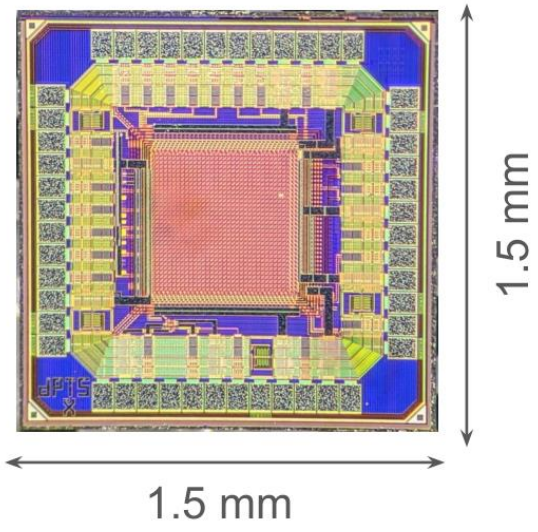
Analogue Pixel Test Structure



Matrix: 6×6 pixels
Pitch: 10, 15, 20, 25 µm
Direct analogue readout of central 4×4 submatrix
AC/DC coupling
3 process modifications
Purpose: testing pixel cell

DPTS

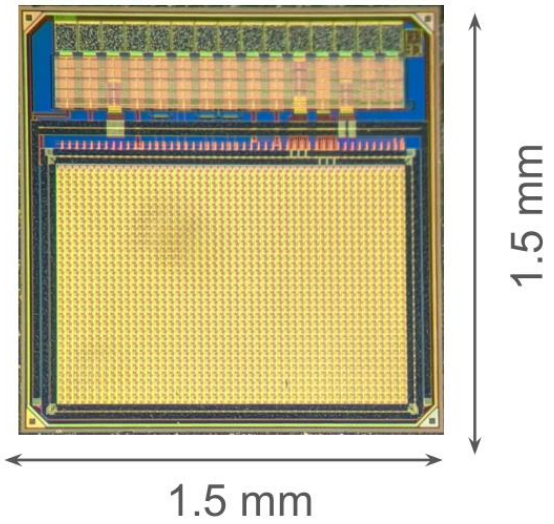
Digital Pixel Test Structure



Matrix: 32×32 pixels
Pitch: 15 µm
Asynchronous digital readout
Time-over-Threshold information
Only modified with gap process modification
Purpose: testing pixel front-end

CE-65

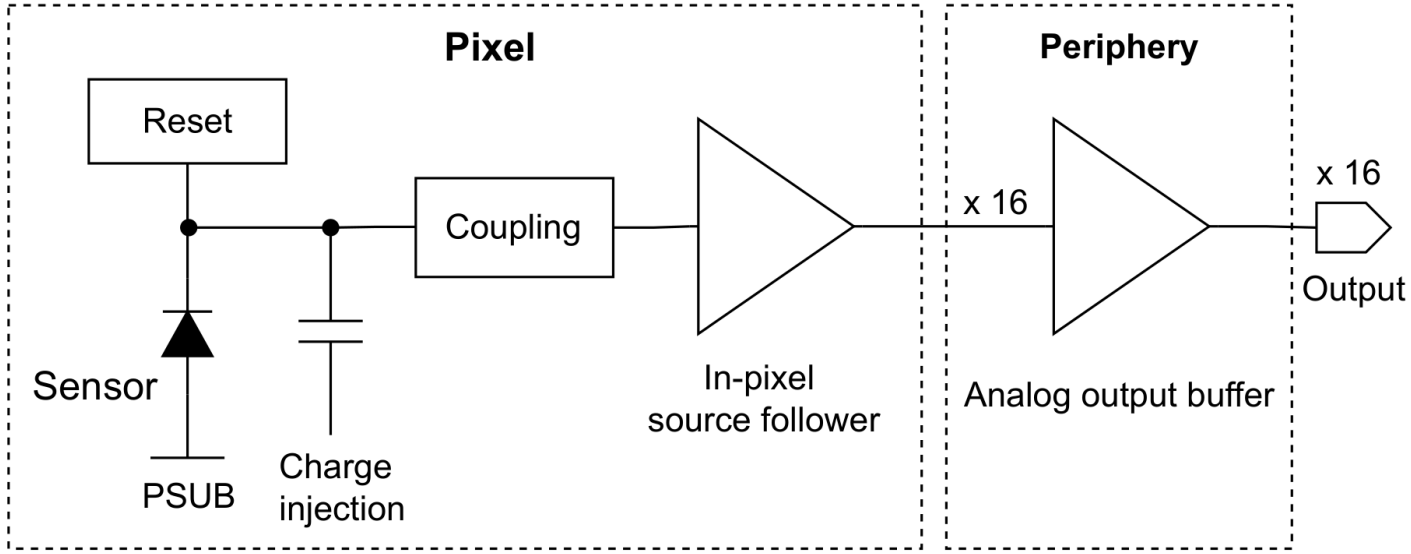
Circuit Exploratoire 65

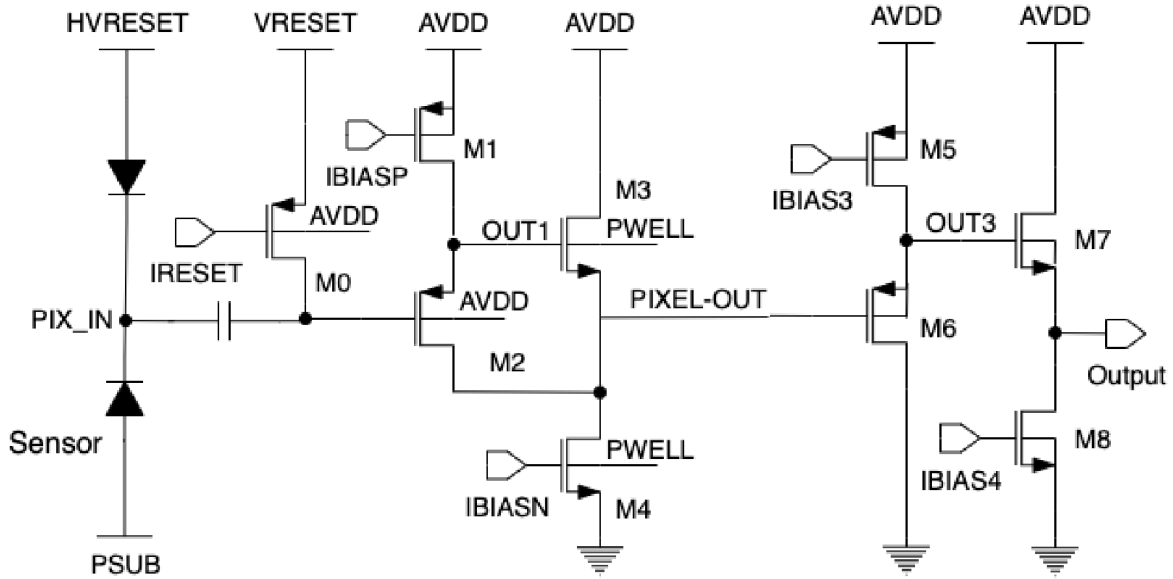


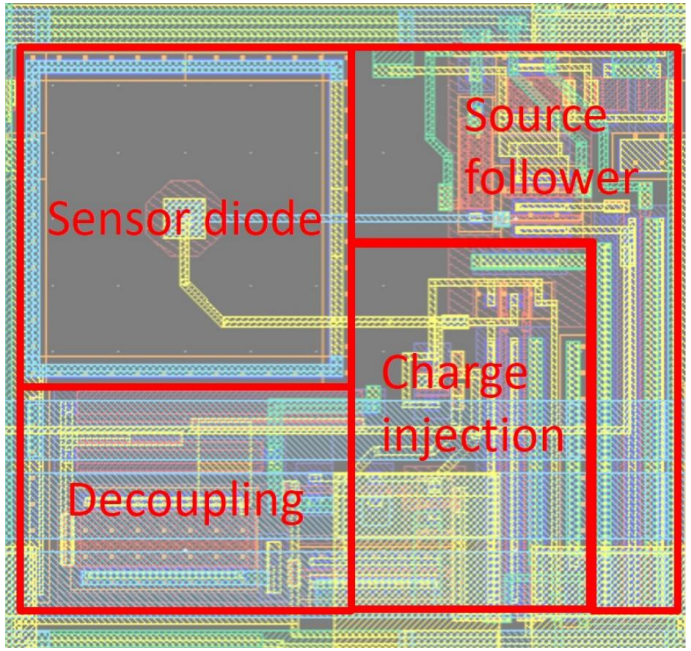
Matrix: 64x32, 48x32 pixels
Pitch: 15, 25 µm
Readout: rolling shutter analog
Purpose: testing pixel with rolling shutter

APTS-SF Design

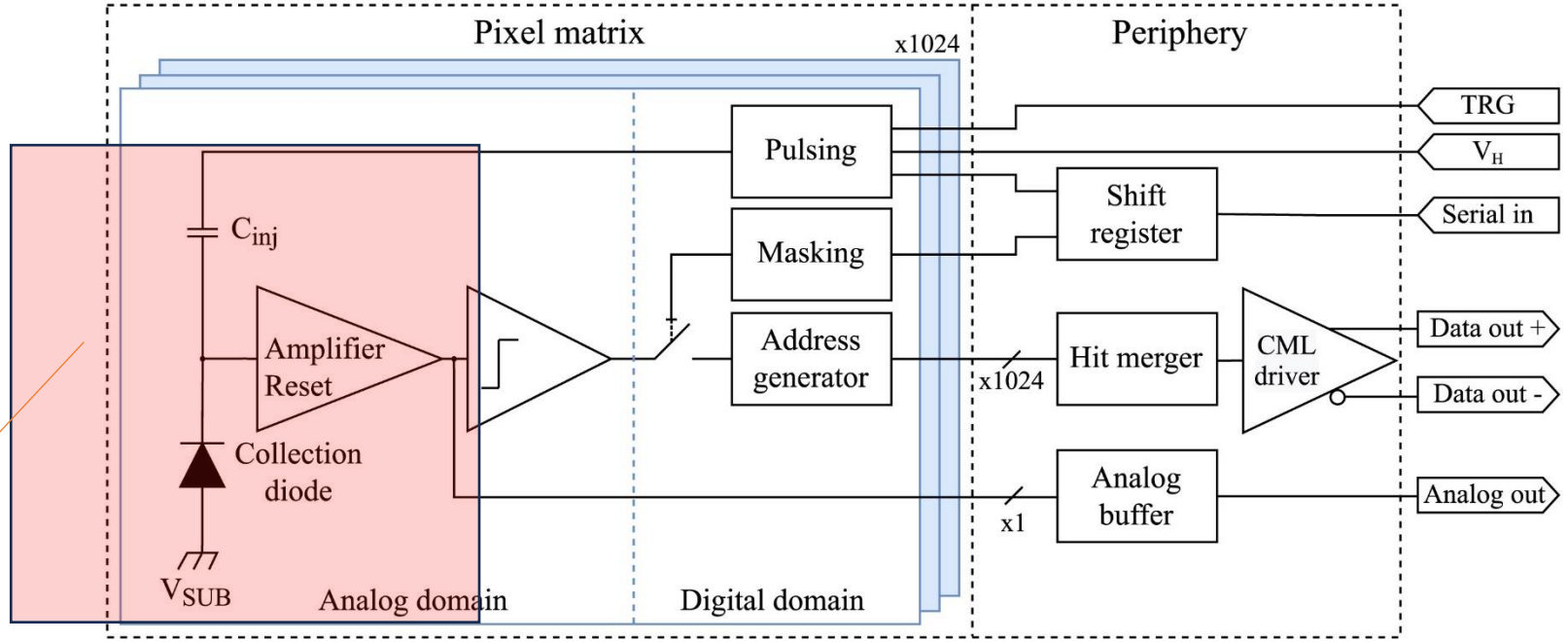
Readout with Source Follower

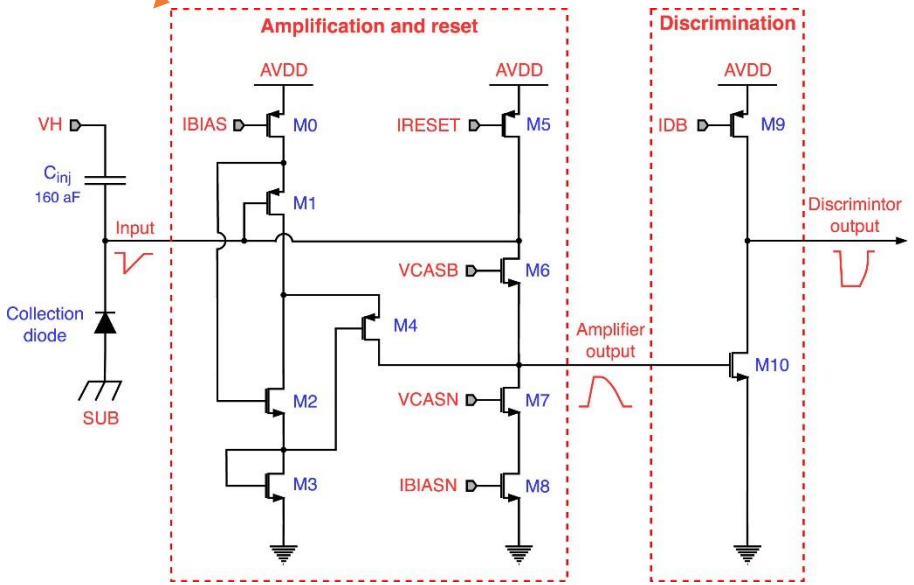


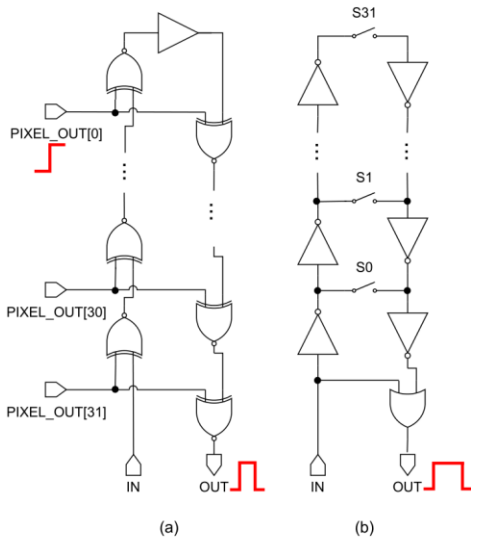


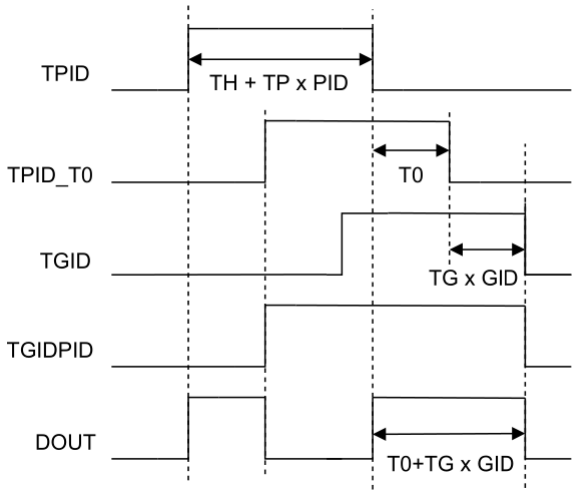


DPTS Design


Pixel matrix
x1024
Periphery
Pulsing
Masking
Address generator
Shift register
Hit merger
CML driver
Analog buffer
x1024
x1
TRG
V_H
Serial in
Data out +
Data out -
Analog out
C_{inj}
Amplifier Reset
Collection diode
V_{SUB}
Analog domain
Digital domain

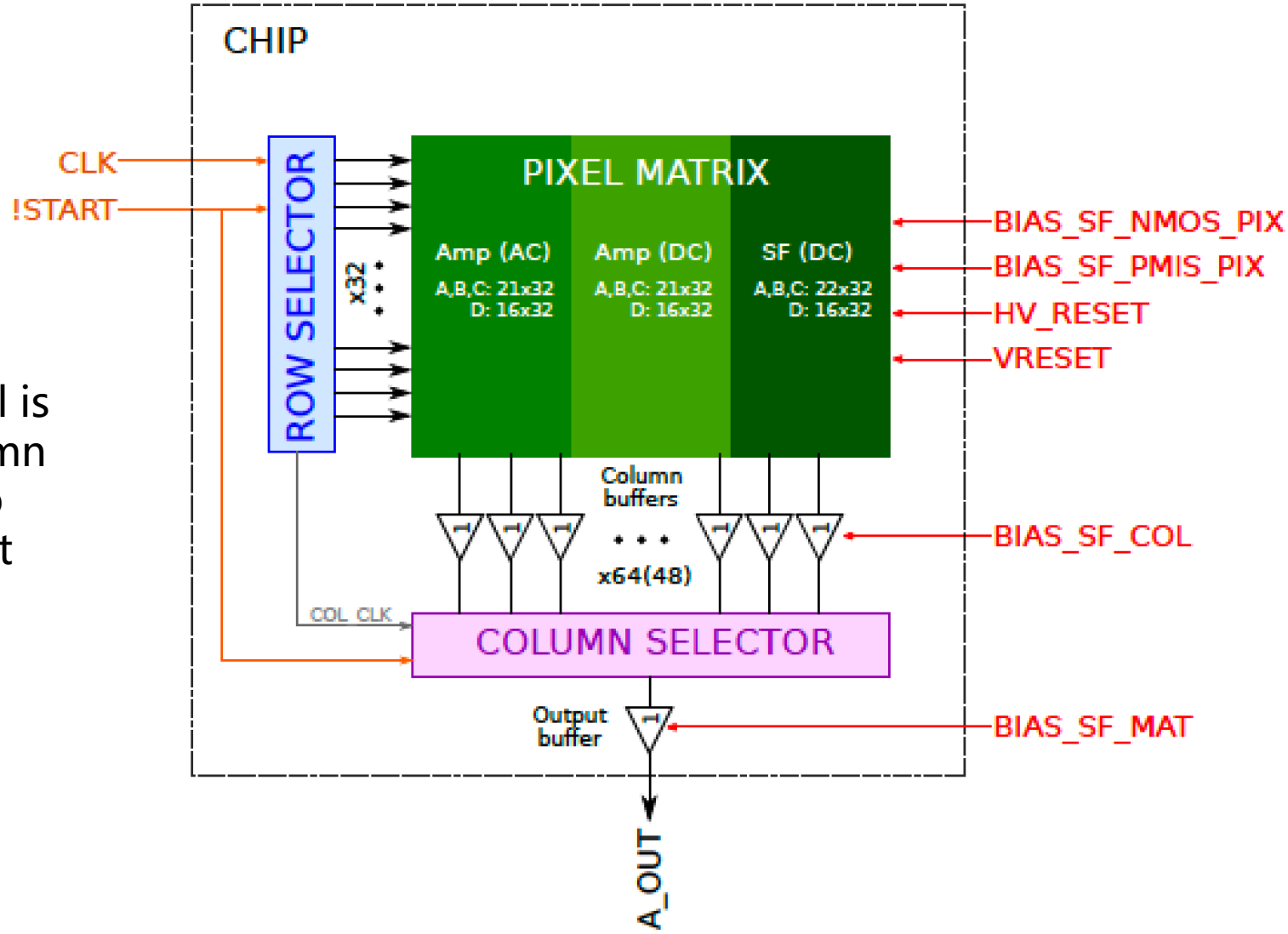

Amplification and reset
Discrimination
AVDD
AVDD
AVDD
VH
IBIAS
M0
IRESET
M5
IDB
M9
C_{inj}
160 aF
Input
M1
Discrimintor output
VCASB
M6
M4
Collection diode
Amplifier output
M10
M2
VCASN
M7
SUB
M3
IBIASN
M8


PIXEL_OUT[0]
PIXEL_OUT[30]
PIXEL_OUT[31]
IN
OUT
(a)
S31
S1
S0
IN
OUT
(b)


TPID
TH + TP x PID
TPID_T0
T0
TGID
TG x GID
TGIDPID
DOUT
T0+TG x GID

CE-65 rolling shutter readout

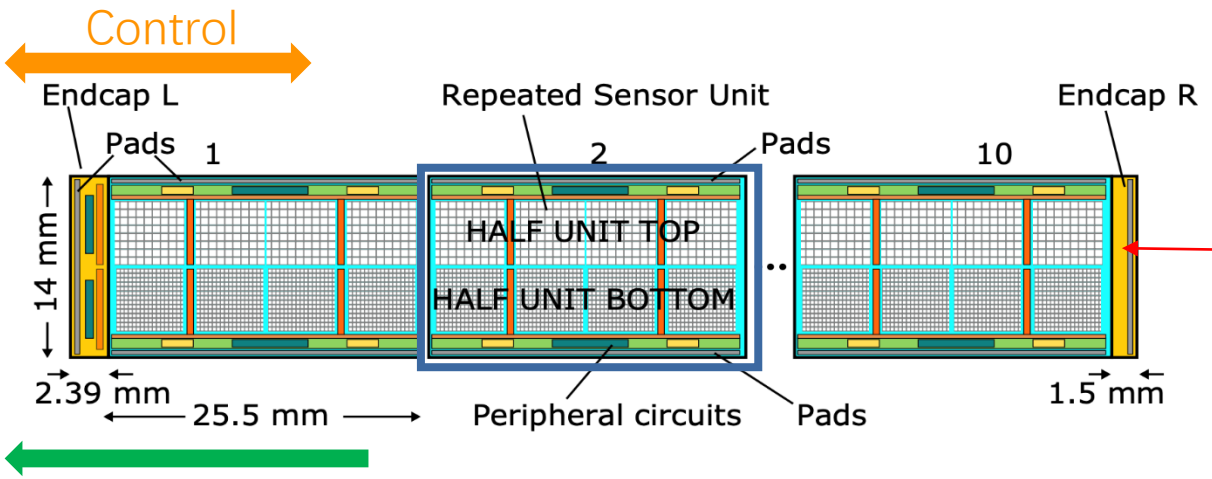
The output of a particular pixel is selected using a row and column selector block, and buffered to make it available on the output pad.



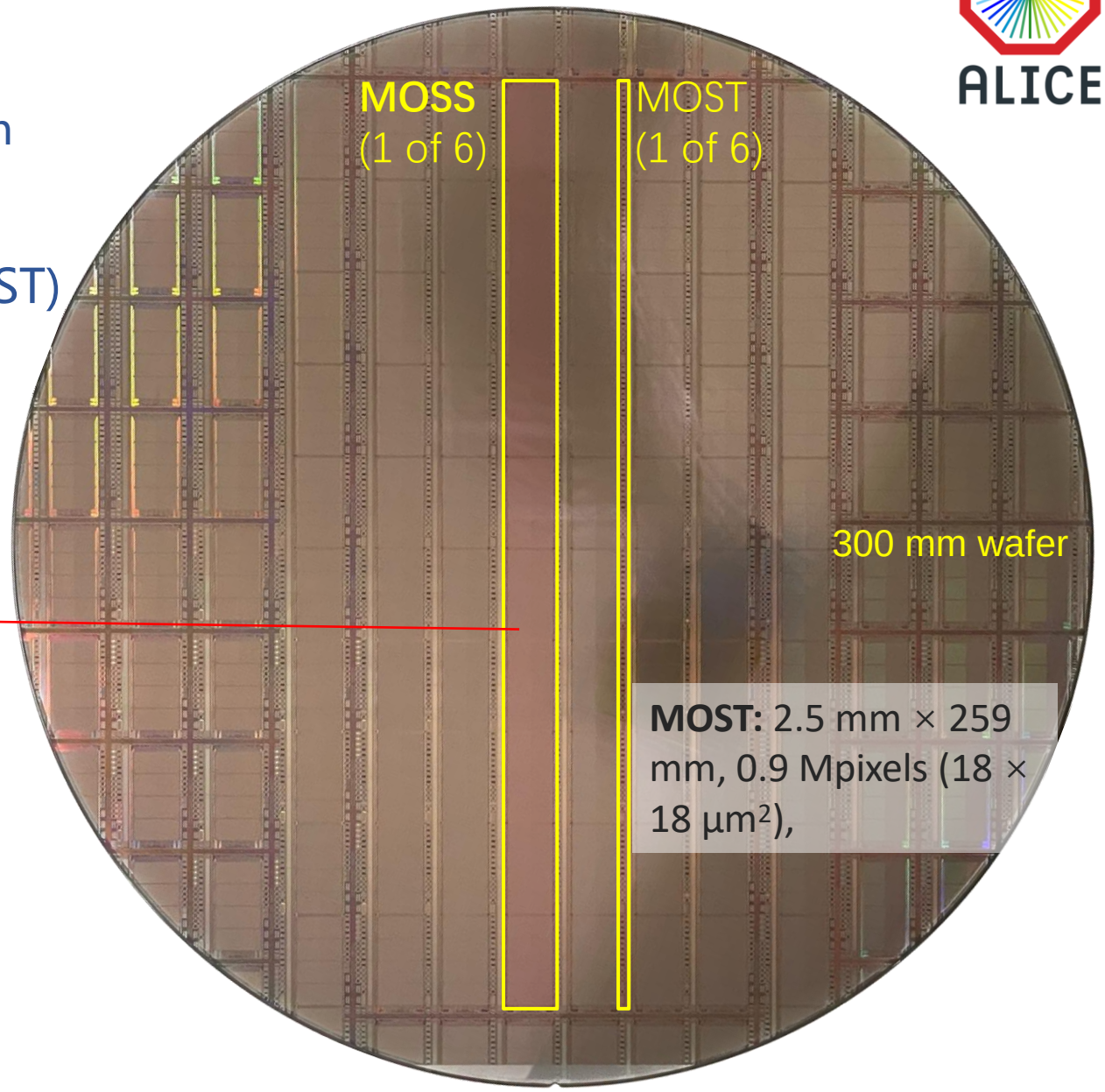
ER1 MAPS Chip

Aim at learning and proving **stitching**, submitted in December 2022

Two wafer scale stitched sensor chips (MOSS, MOST)



	Pixel matrix	Pixel size
Matrices on the top	256 × 256	22.5 μm
Matrices on the bottom	320 × 320	18 μm

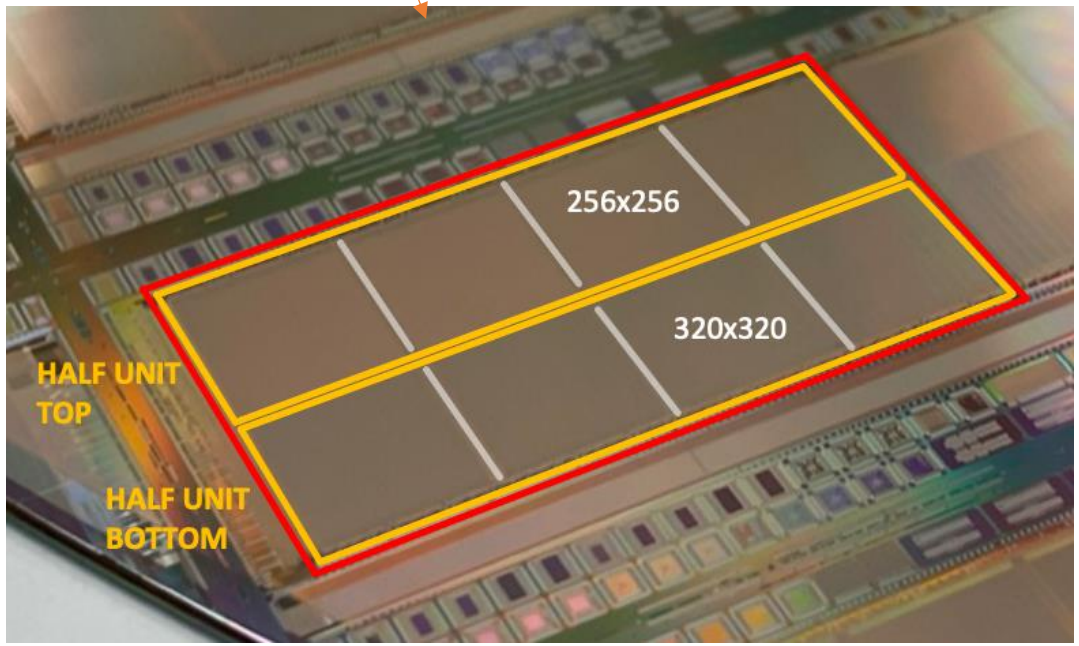


The MOSS chip contains 20 half units and 6.72 million pixels.

MOSS – Architecture

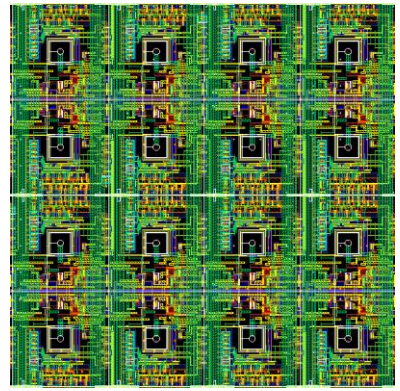
Module integration on wafer scale die for the first time

Repeated (Stitched) Sensing Unit

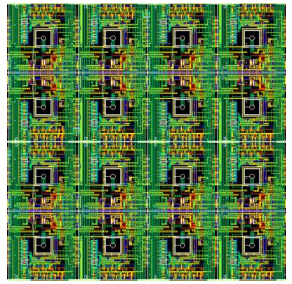


1 of 10 REPEATED UNITS

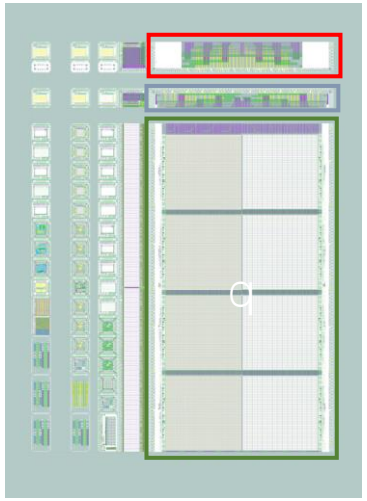
Large Pixel Pitch
22.5 µm



Fine Pixel Pitch
18 µm



Investigate effects
of layout density



Reticle

MOSS power distribution and IOs

Monolithic Stitched Sensor Prototype

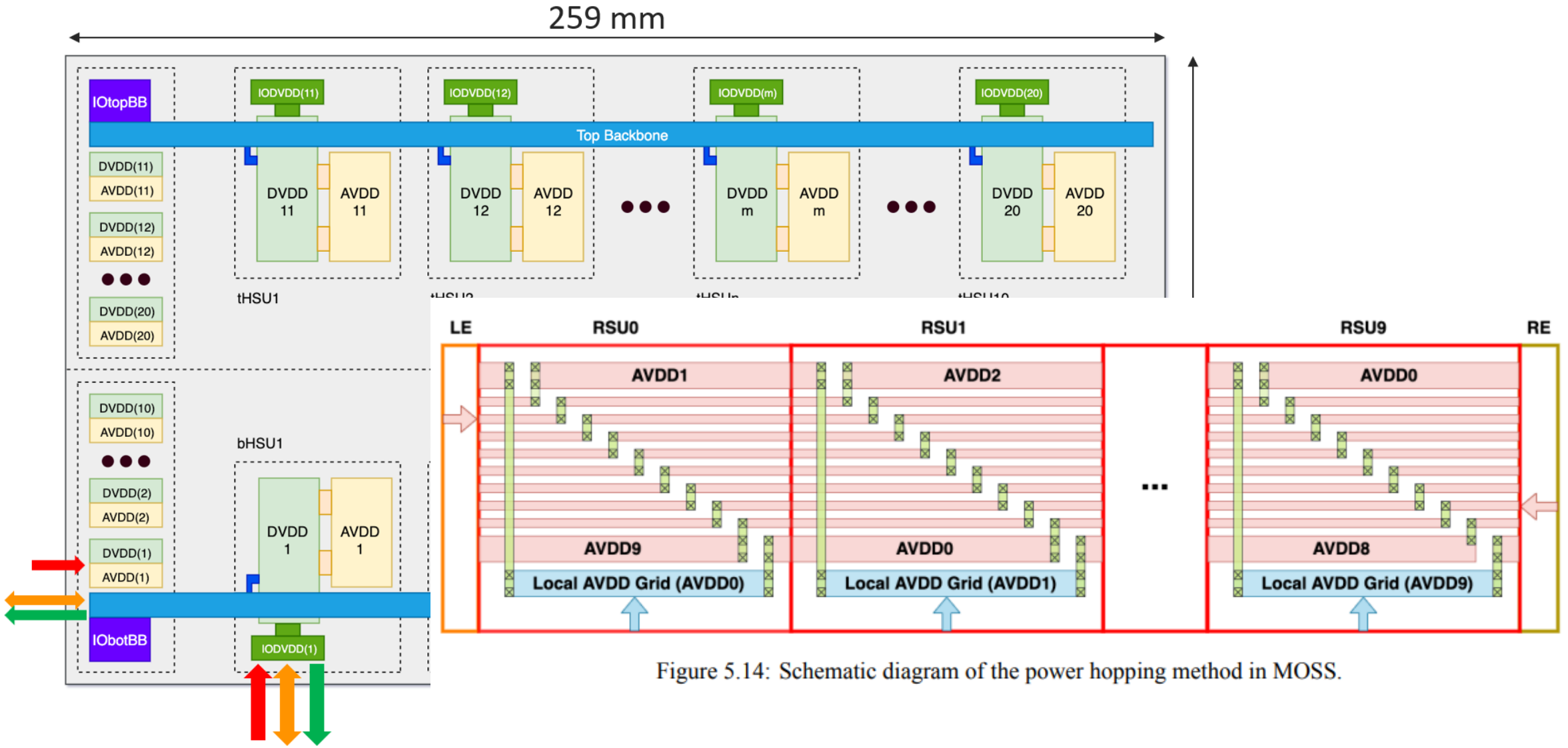
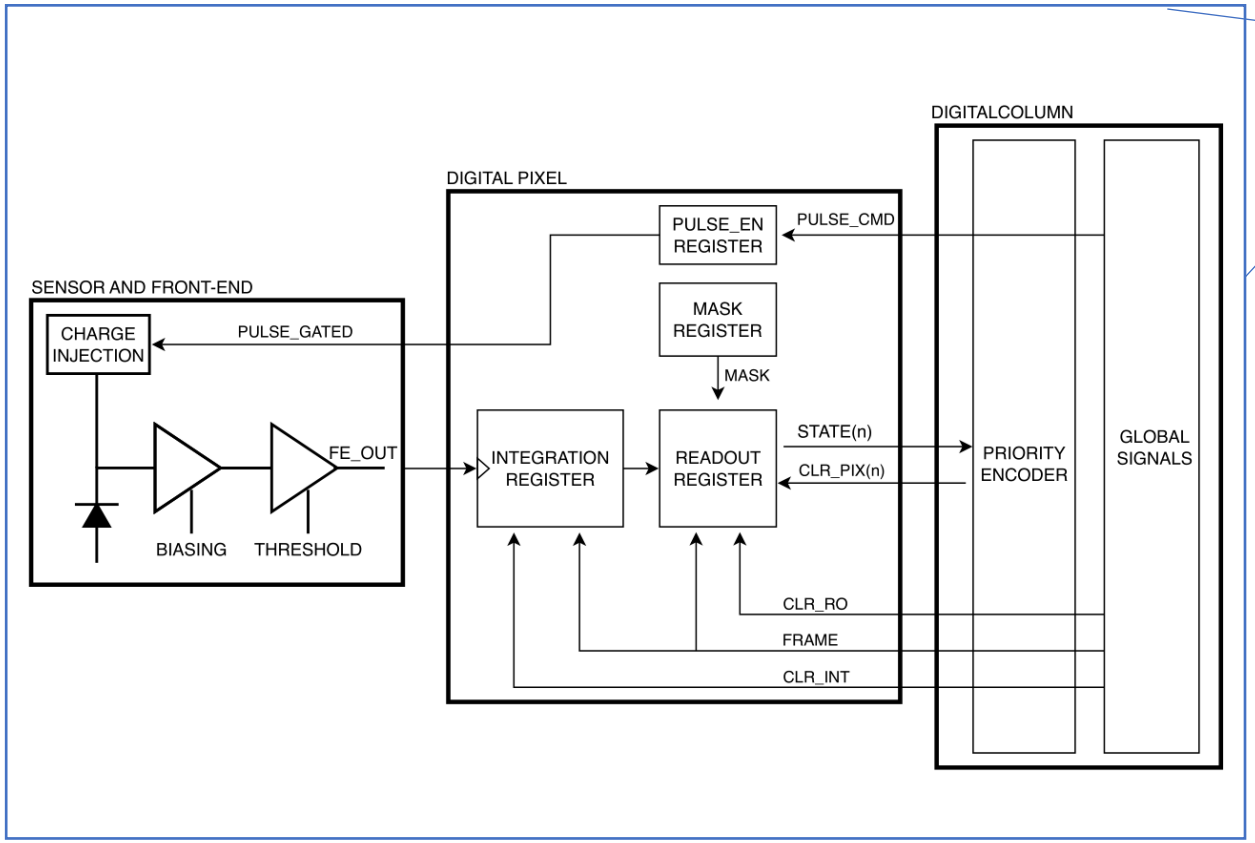
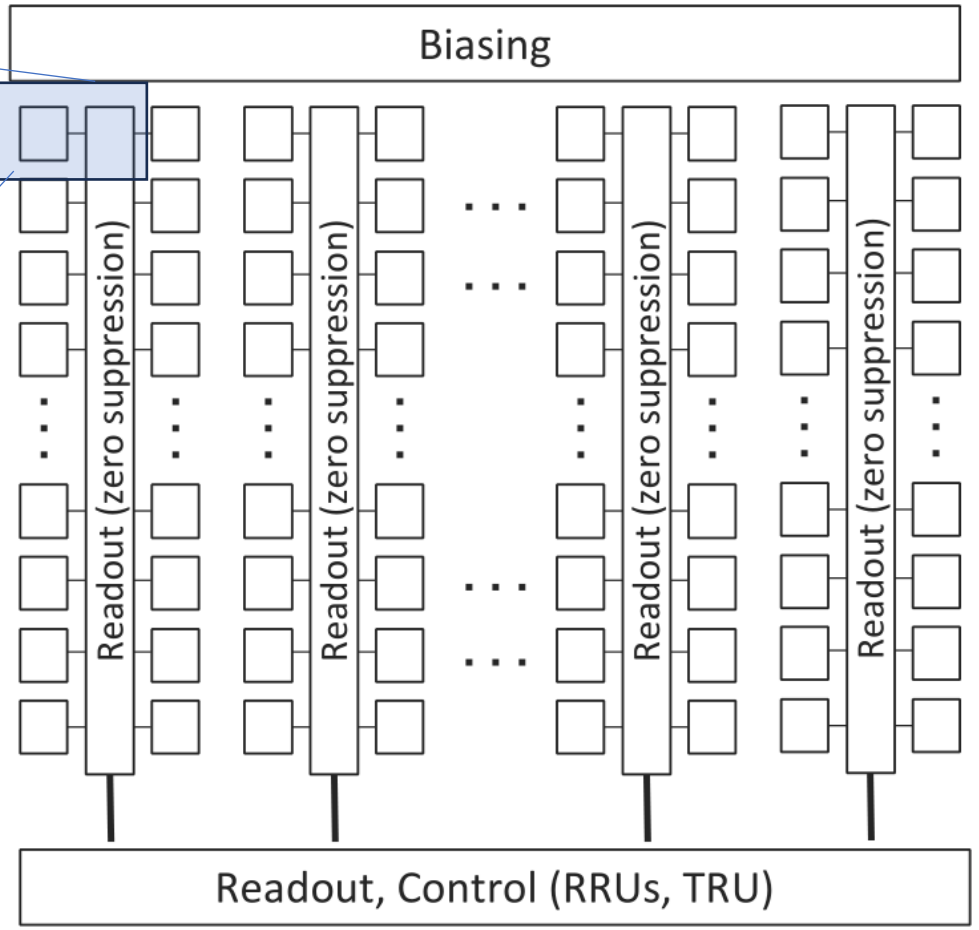


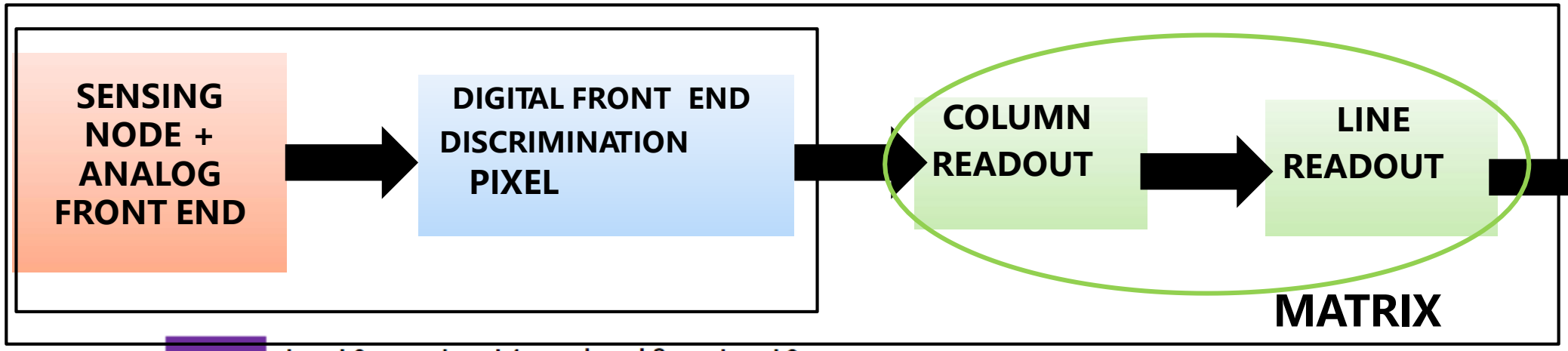
Figure 5.14: Schematic diagram of the power hopping method in MOSS.

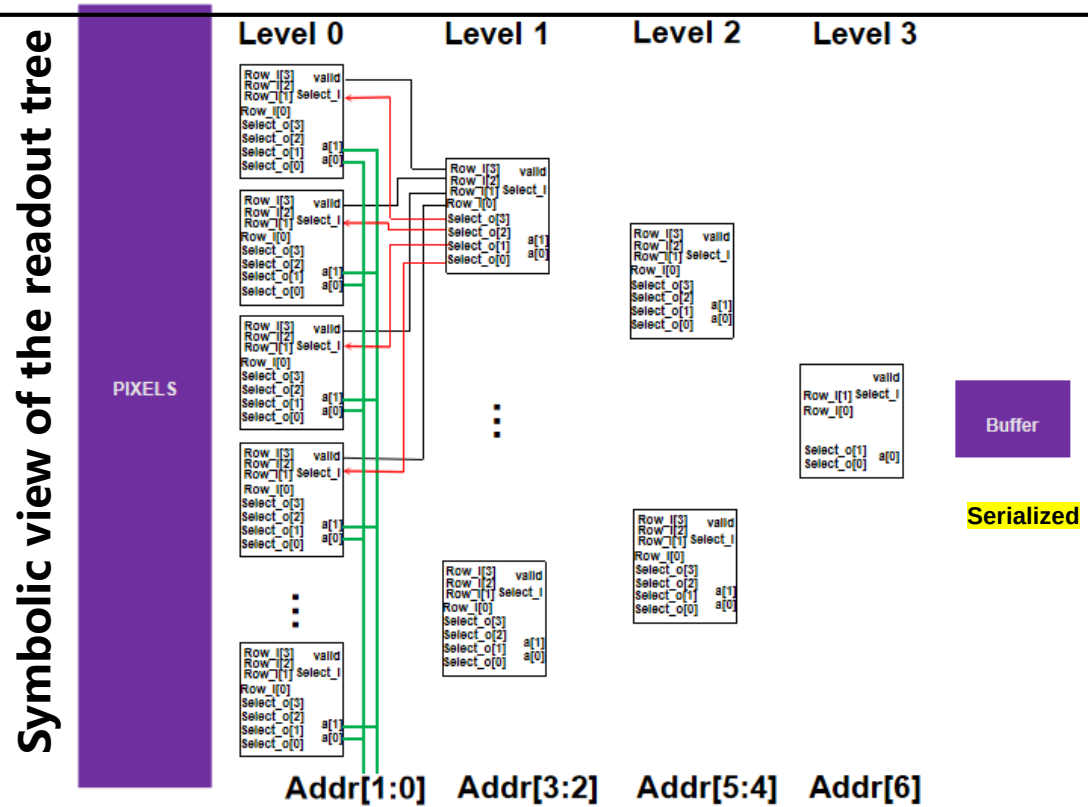
Readout Model – Matrix Readout



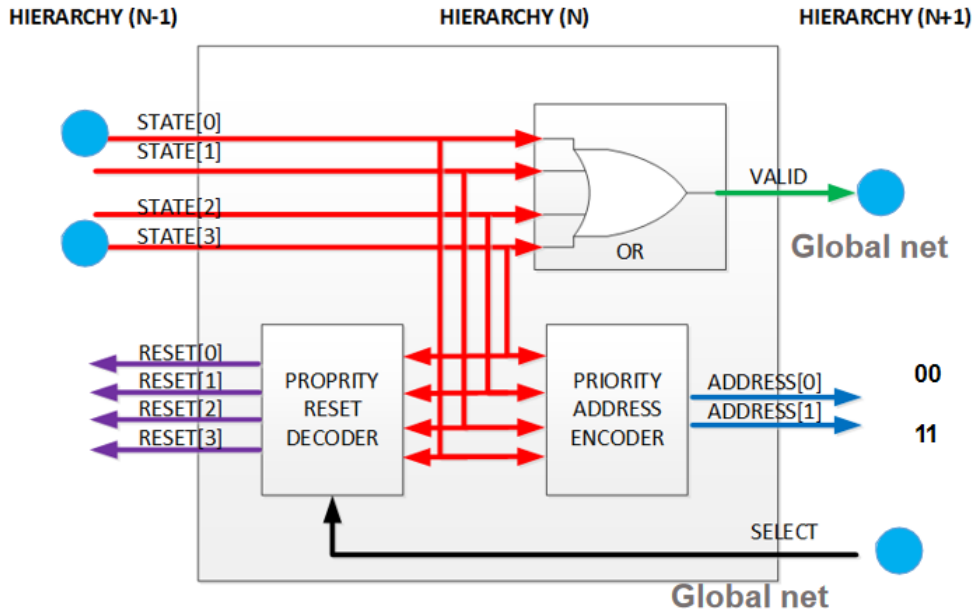


Readout- Asynchronous & priority tree

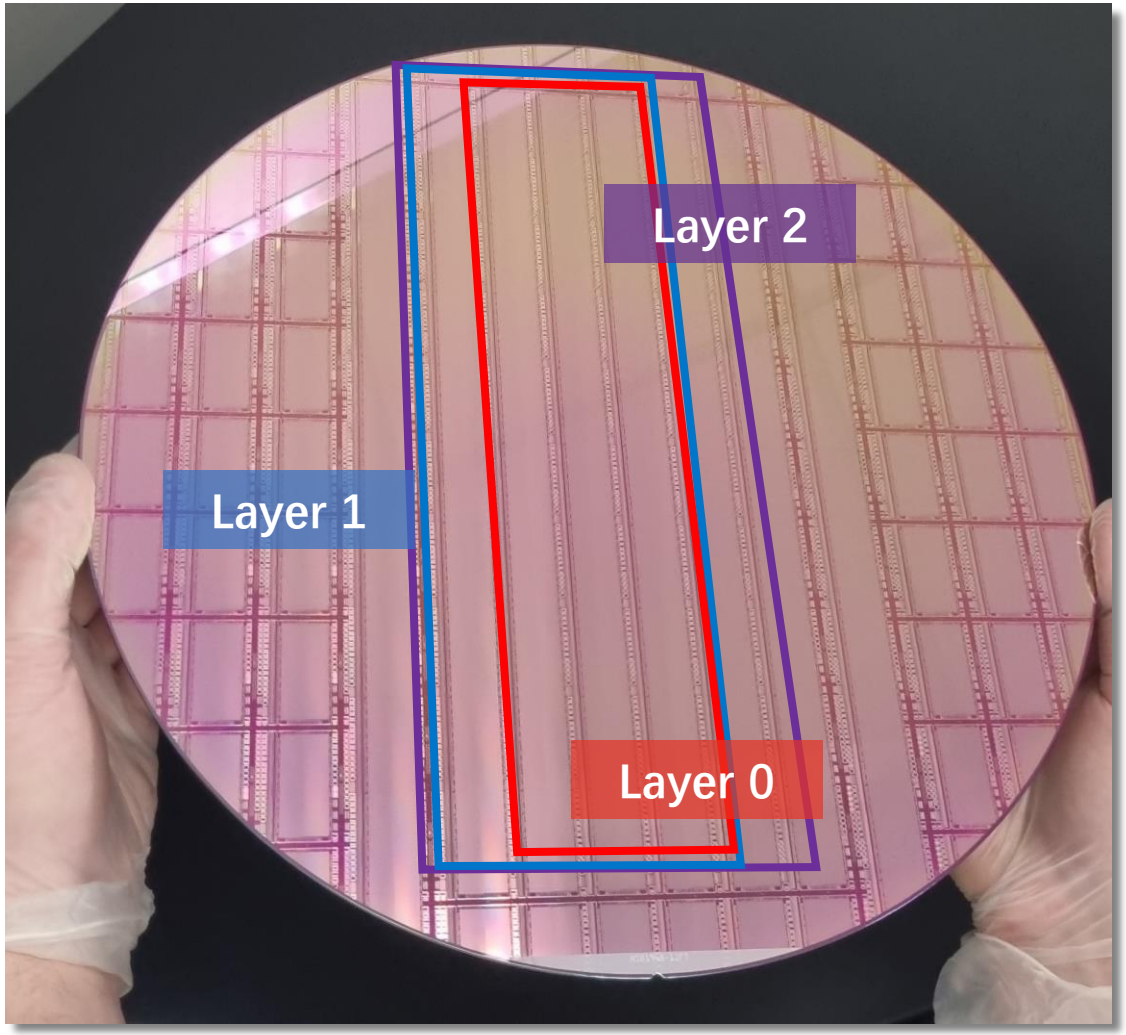


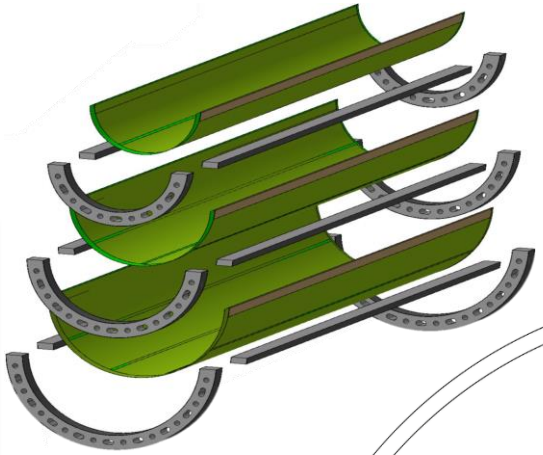


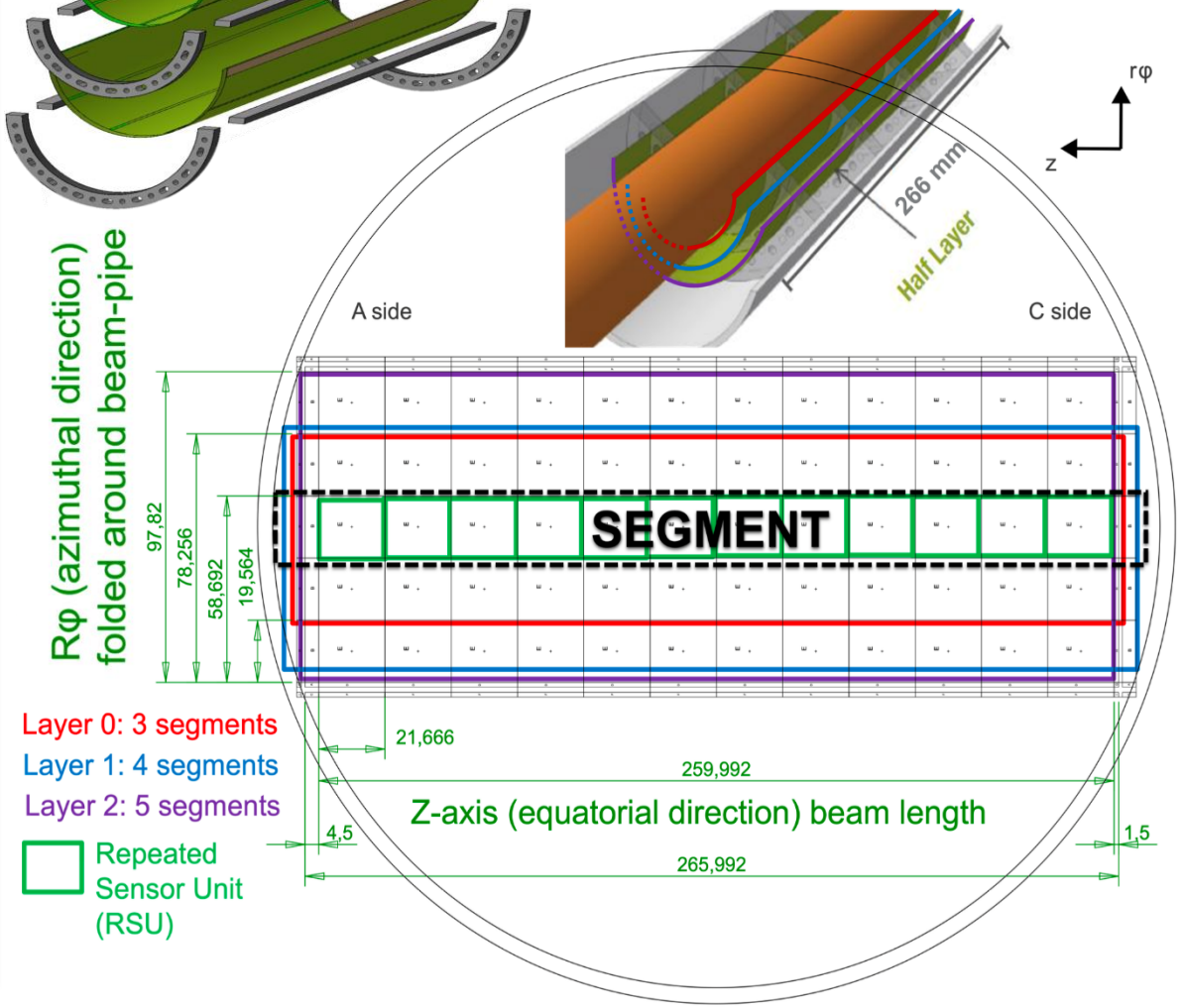
The priority encoder



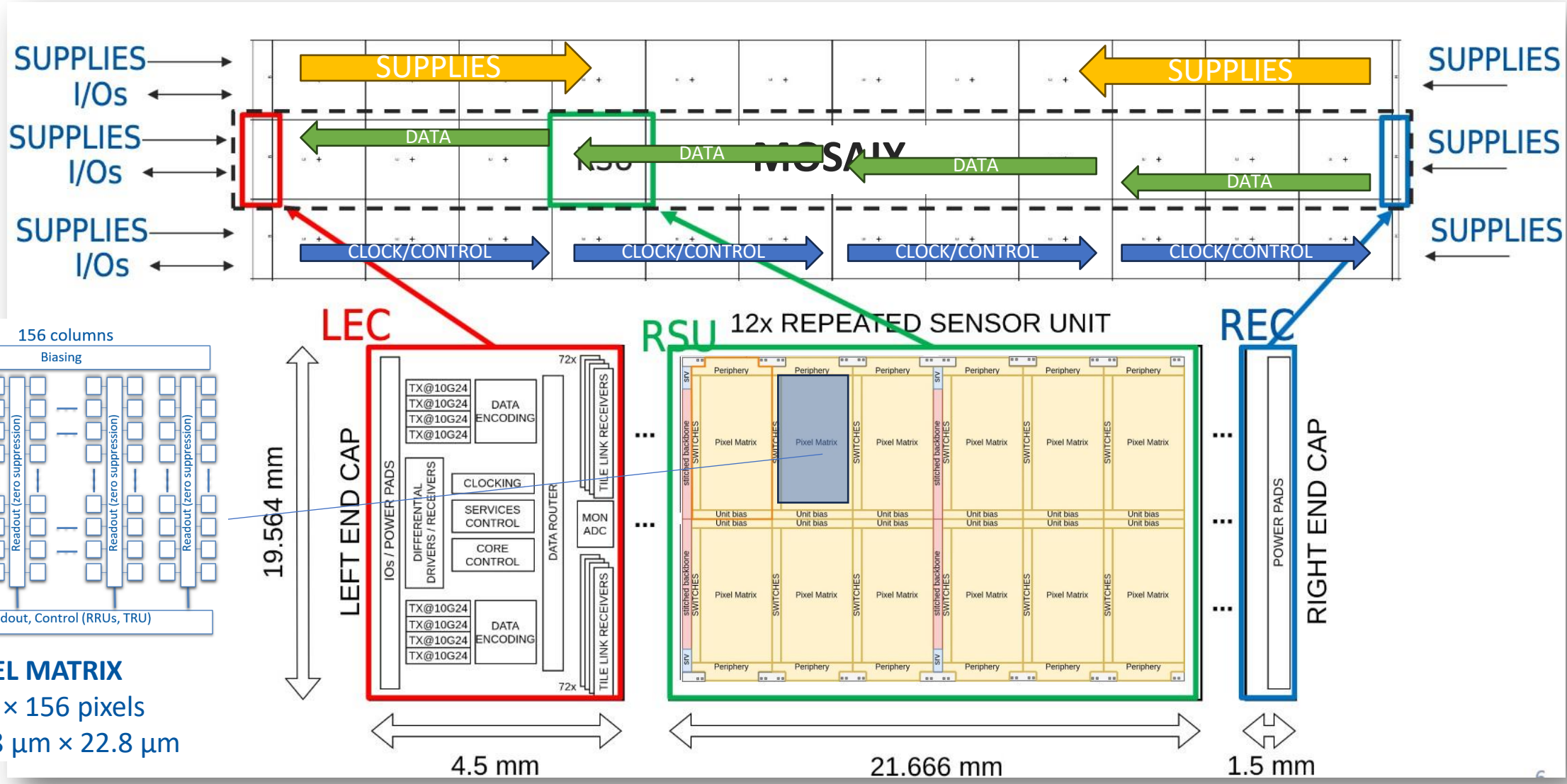
Final Sensor: MOSAIX







MOSAIX Architecture



PIXEL MATRIX

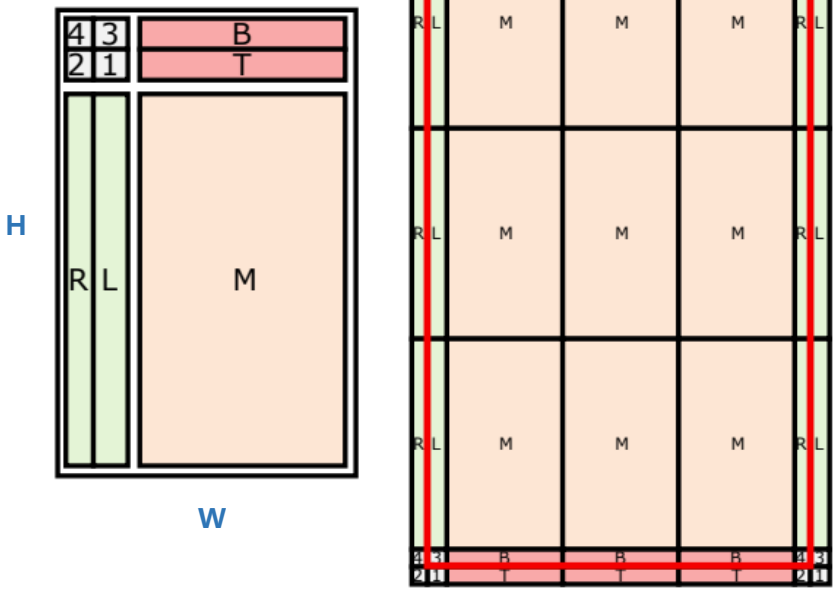
444 × 156 pixels

20.8 µm × 22.8 µm

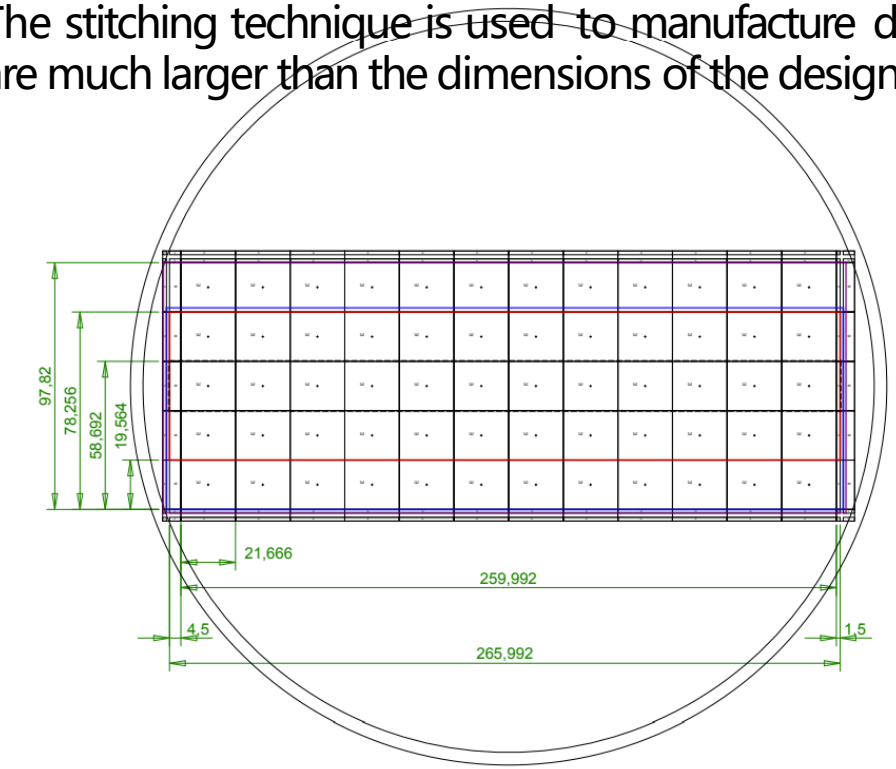
MONOLITHIC STITCHED SENSORS

Circuits on wafer

Design Reticle (typ. 2×3 cm)



The stitching technique is used to manufacture devices that are much larger than the dimensions of the design reticle



Principles of stitching.
Left: design reticle with sub-frames.

Right: resulting circuits on the wafer

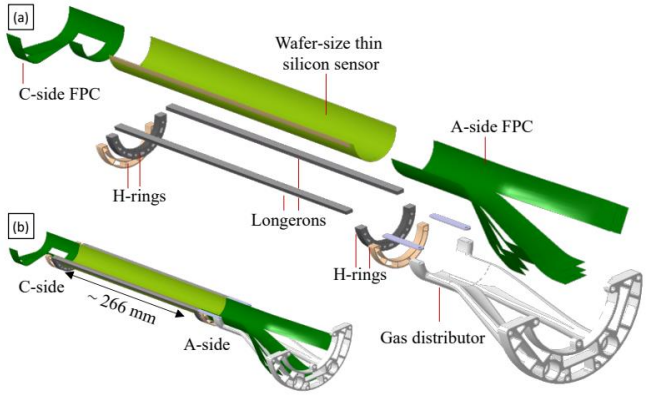
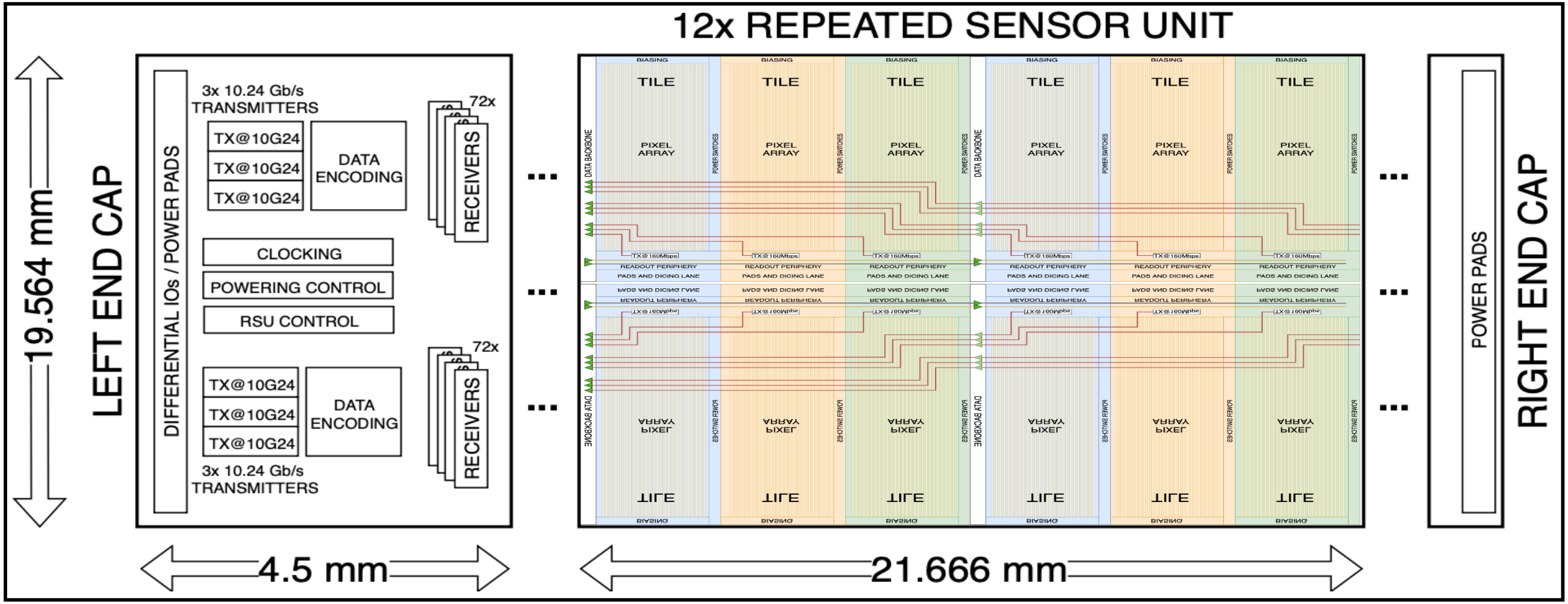


Figure 4.1: Half-layer 0. (a) Exploded view and (b) assembled view.

Metal traces cross stitching boundaries for power distribution and long range on-chip control and data transfer

MOSAIX


12x REPEATED SENSOR UNIT
19.564 mm
LEFT END CAP
DIFFERENTIAL IOs / POWER PADS
3x 10.24 Gb/s TRANSMITTERS
TX@10G24
TX@10G24
TX@10G24
DATA ENCODING
72x
RECEIVERS
CLOCKING
POWERING CONTROL
RSU CONTROL
TX@10G24
TX@10G24
TX@10G24
DATA ENCODING
72x
RECEIVERS
3x 10.24 Gb/s TRANSMITTERS
BIASING
TILE
PIXEL ARRAY
DATA BACKBONE
POWER SWITCHES
READOUT PERIPHERY
PADS AND DICING LANE
TX@160Mbps
POWER PADS
RIGHT END CAP
4.5 mm
21.666 mm

Prospects for the future

25x more pixels

	Vertex Detector	Middle Layers	Outer Tracker	ITS3
Position resolution (μm)	2.5	10		5
Pixel size (μm²)	*O*(10 x 10)	*O*(50 x 50)		*O*(20 x 20)
Time resolution (ns RMS)	100	100		100* / O(1000)
In-pixel hit rate (Hz)	94	**42 (barrel)** / 12 (foward)	1 (barrel) / **16 (forward)**	54
Fake-hit rate (/ pixel / event)	$<10^{-7}$			
Power consumption (mW / cm²)	70	20		35
Particle hit density (MHz / cm²)	94	0.6 (barrel / forward)	0.06 (barrel) **0.6 (forward**	8.5
Non-Ionising Energy Loss (1 MeV n_{eq} / cm²)*	2×10^{15}	**6×10^{13} (barrel)** 6×10^{13} (forward)	3×10^{13} (barrel) **6×10^{13} (forward)**	3×10^{12}
Total Ionising Dose (Mrad)*	11	**3 (barrel)** / 3 (forward)	0.5 (barrel) / 3 **(forward)**	0.3

20x higher radiation load

Pixel grouping

- VD: 5 x 5 pixels of 10 μm x 10 μm acting independently
- ML/OT: macro pixel combining 25 pixels of 10 μm x 10 μm