中国科学院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

Sr90 test for TaichuPix-3

Tianya Wu，Xiaomin Wei，Ziyue Yan
wuty@ihep.ac.cn
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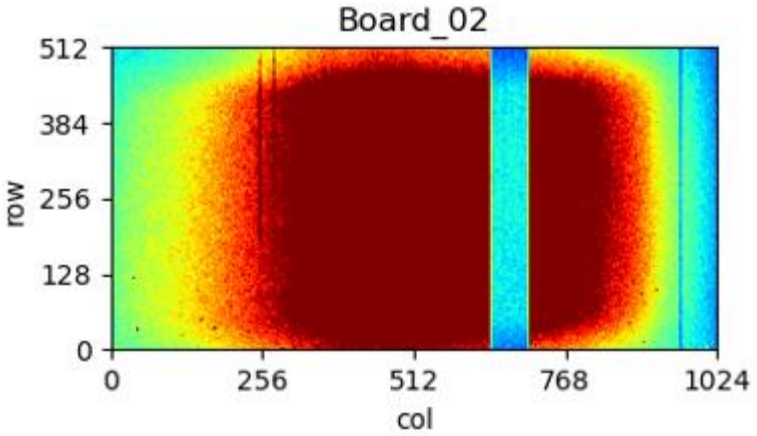
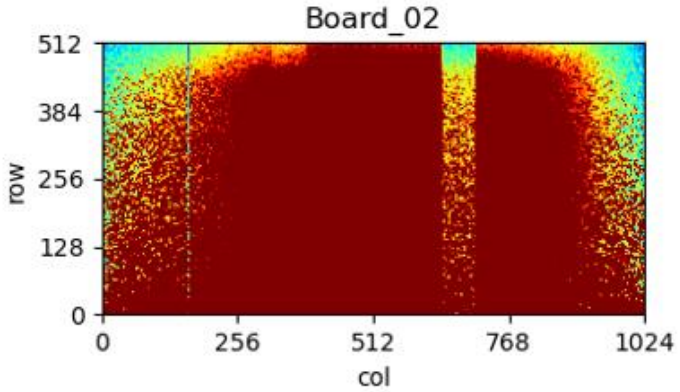
CEPC
Circular Electron Positron Collider

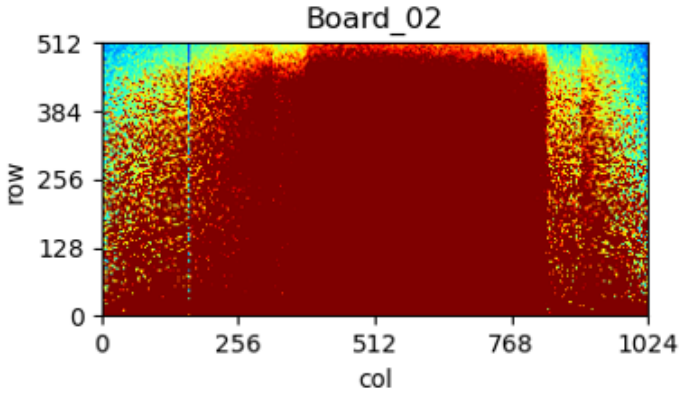
Setup

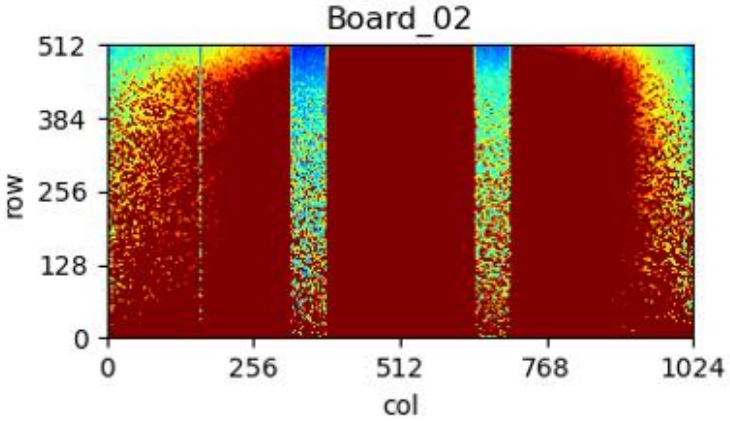
- W9R5, DUTB at DESY
- ITHR is set to 32 (218 e-)
- Sr90 is put on the backside of TaichuPix-3 with 2cm
- Power is 1.8 DVDD_0.1A/1.8 AVDD_0.06A
- Firmware: 20M array+160 M serializer
- Configuration with Python
- Taking data with MATLAB

DUTB at DESY





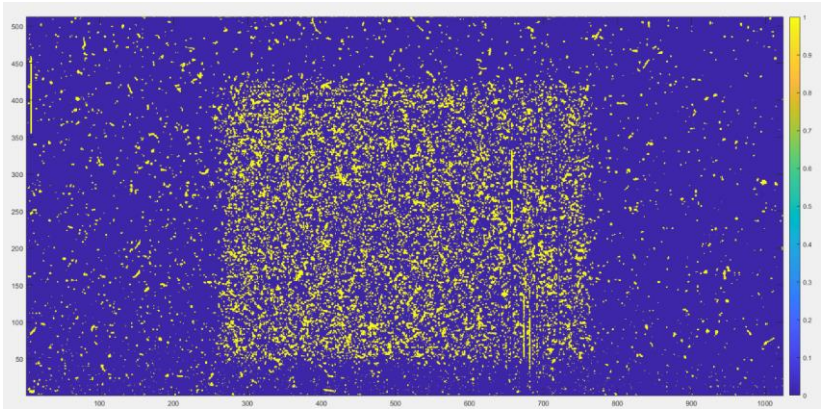




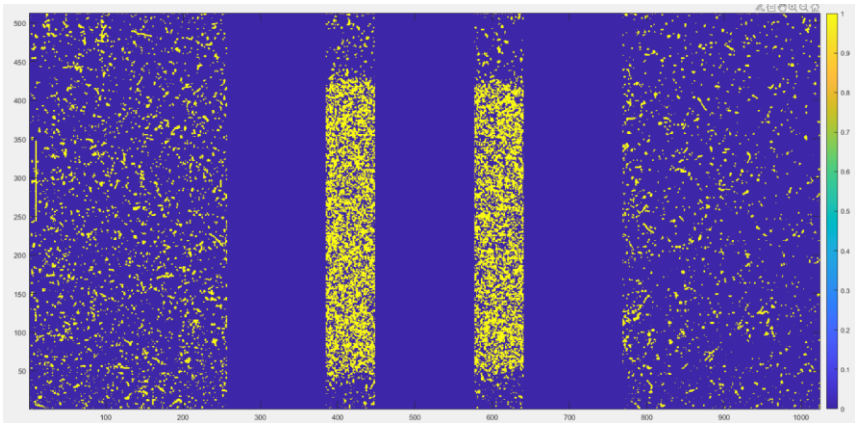
Firmware: 20 M array+80 M serializer

Sr.90 test at lab

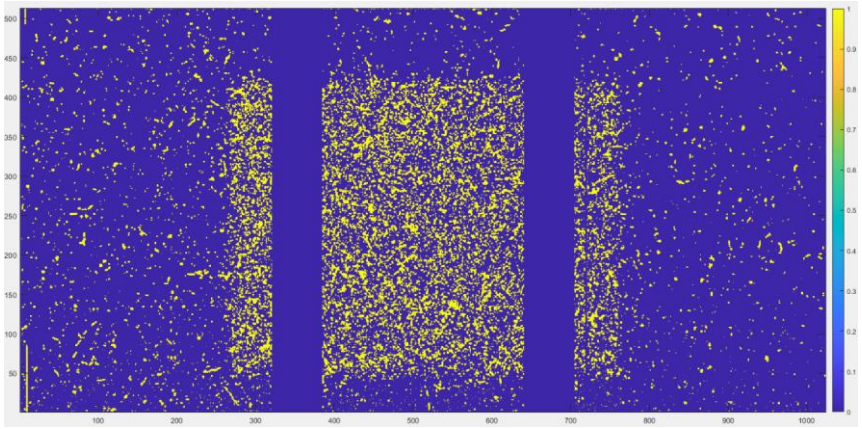
Firmware: 20 M array+80 M serializer



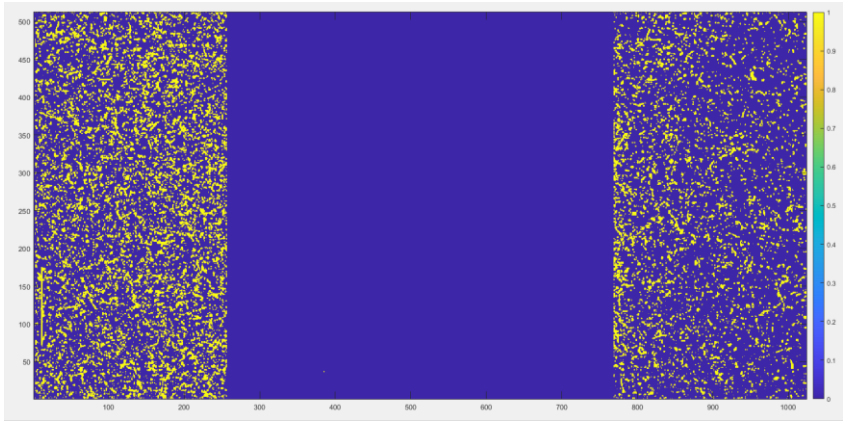
Leave for 23 minutes without beta source, then take data



Another six minutes



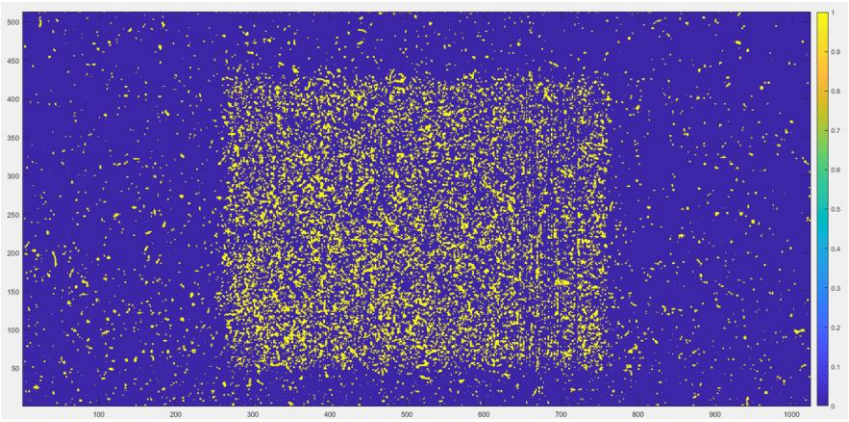
1 minutes later



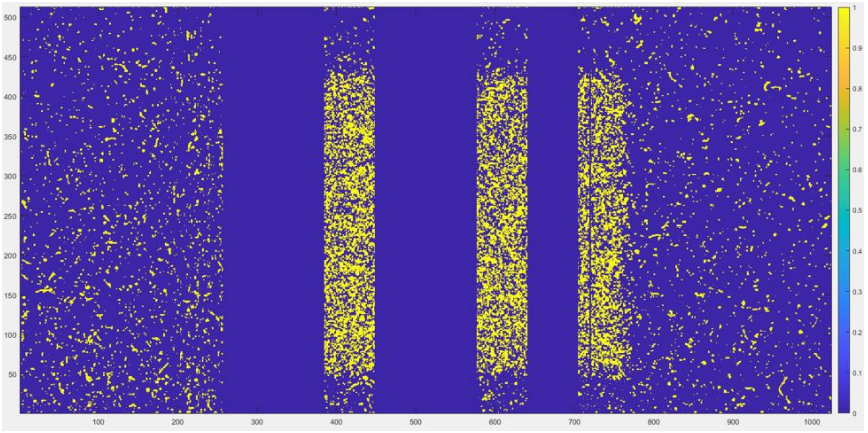
Worst case: 50 minutes after reset

Sr.90 test at lab

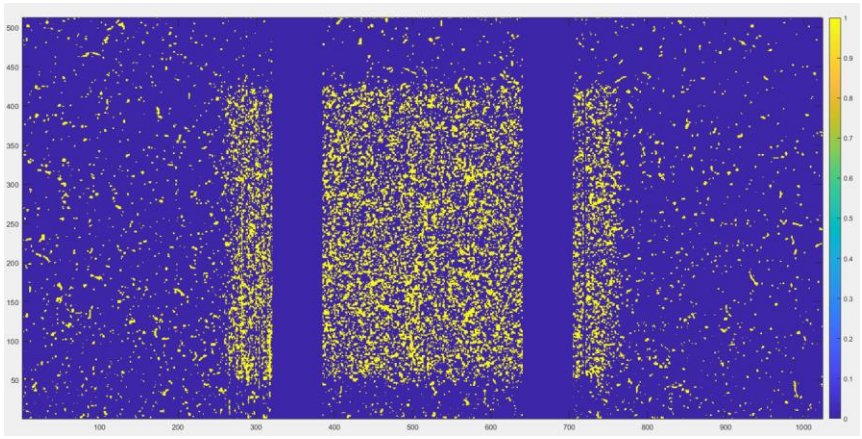
Firmware: 20 M array+160 M serializer



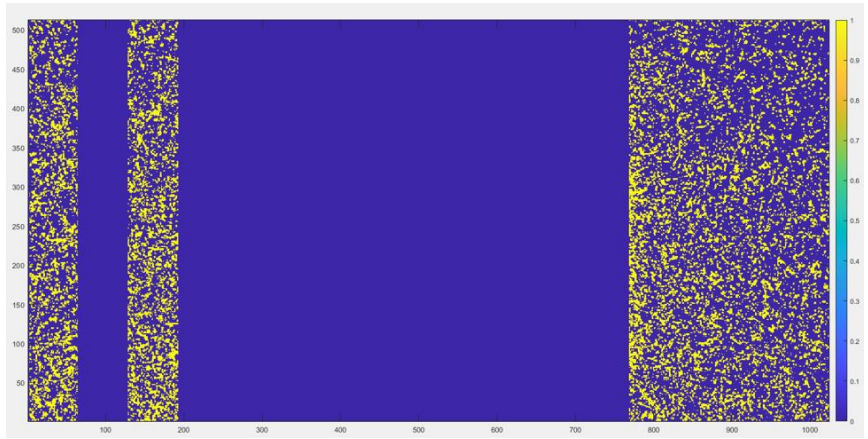
Leave for 20 minutes, then take data



Another five minutes



1 minutes later

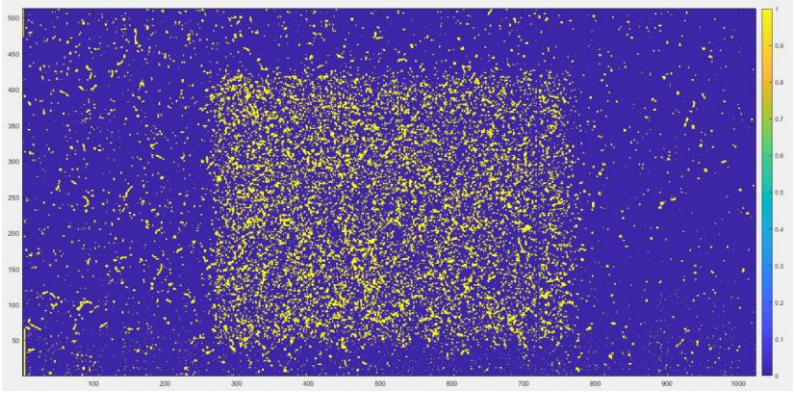


Worst case: 1 hour after reset

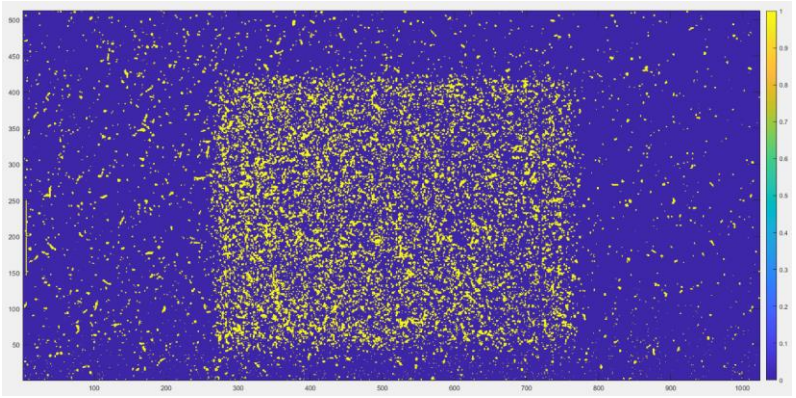
Sr.90 test at lab

Firmware: 2.5 M array+160 M serializer

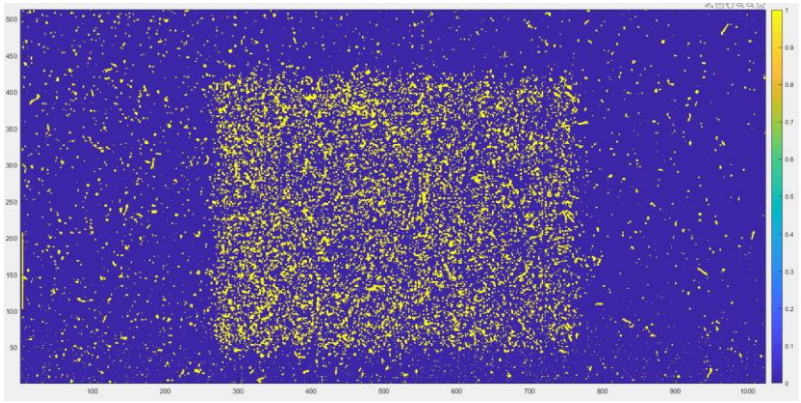
Power goes to 0.072A & 0.052A



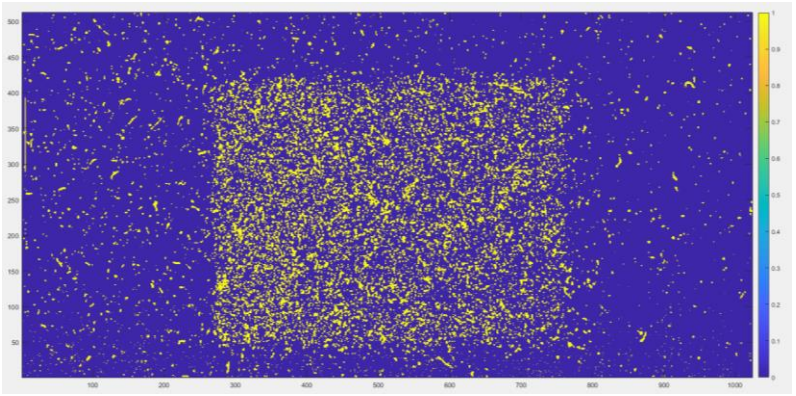
Leave for 20 minutes, then take data



Another 60 minutes



1 minutes later



5 hours after reset

Summary

- When the hit density in certain areas increases, data loss occurs due to the data readout capacity.
- The maximum clock frequency for the FPGA is 709MHz.
- The critical frequency that the PLL can lock onto is 640 MHz, PLL divider ratio is 112
- This moment we cannot increase the clock frequency directly due to the timing limitation.

Duty Cycle (%)		Drives	Use Fine PS	Max Freq. of buffer
Requested	Actual			
50.000	50.0	BUFG		709.723
50.000	50.0	BUFG		709.723
50.000	50.0	BUFG		709.723
50.000	50.0	BUFG		709.723

The phase is calculated relative to the active input clock.

Output Clock	Port Name	Output Freq (MHz)		P
		Requested	Actual	R
clk_out1	CLK_OUT	612	612.50000	0
clk_out2	CLK_OUT2	200.000	196.87500	0
clk_out3	CLK_OUT3	125.000	125.28409	0
clk_out4	CLK_OUT4	125.000	125.28409	0

Thanks for your attention!