Preliminary consideration of the Elec-TDAQ framework for the CEPC Det. Ref-TDR

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Motivation & Detector Background

System	Technologies		
Beam pipe	Φ20 mm		
LumiCal	SiTrk+Crystal		
Vertex	CMOS+Stitching	CMOS Pixel	SOI
Tracker	SPD ITrk		
	Pixelated TPC	PID Drift Chamber	
	AC-LGAD OTrk	SSD OTrk	SPD OTrk
		LGAD ToF	
ECAL	4D Crystal Bar	Stereo Crystal Bar	
	GS+SiPM	PS+SiPM+W	SiDet+W
HCAL	GS+SiPM+Fe	PS+SiPM+Fe	RPC+Fe
Magnet	LTS	HTS	
Muon	PS Bar+SiPM	RPC	
TDAQ	Conventional	Software Trigger	
BE electr.	Common	Independent	

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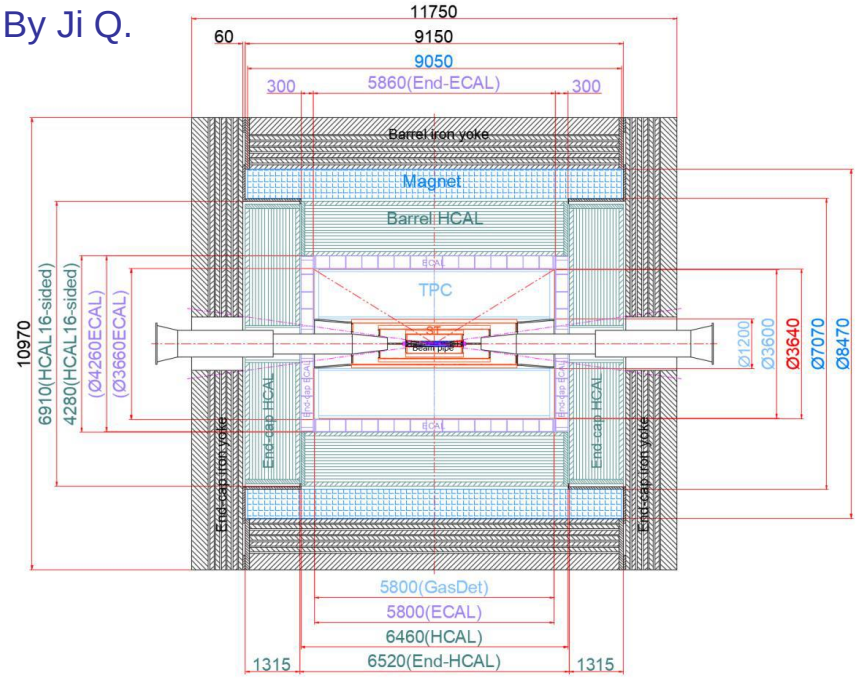
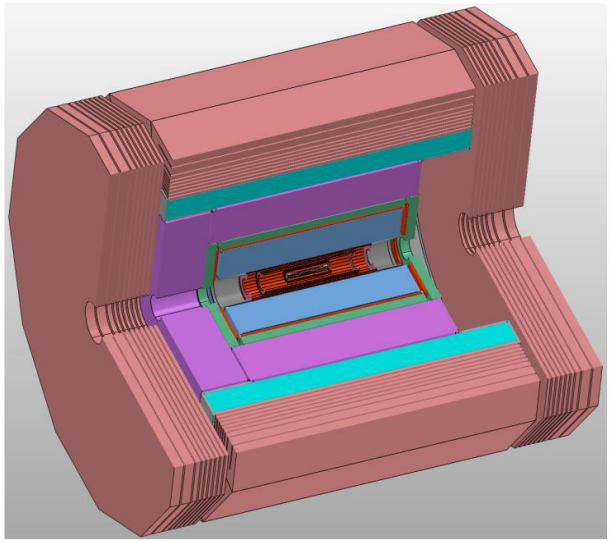
Baseline

For Comparison

By Wang JC

By Ji Q.





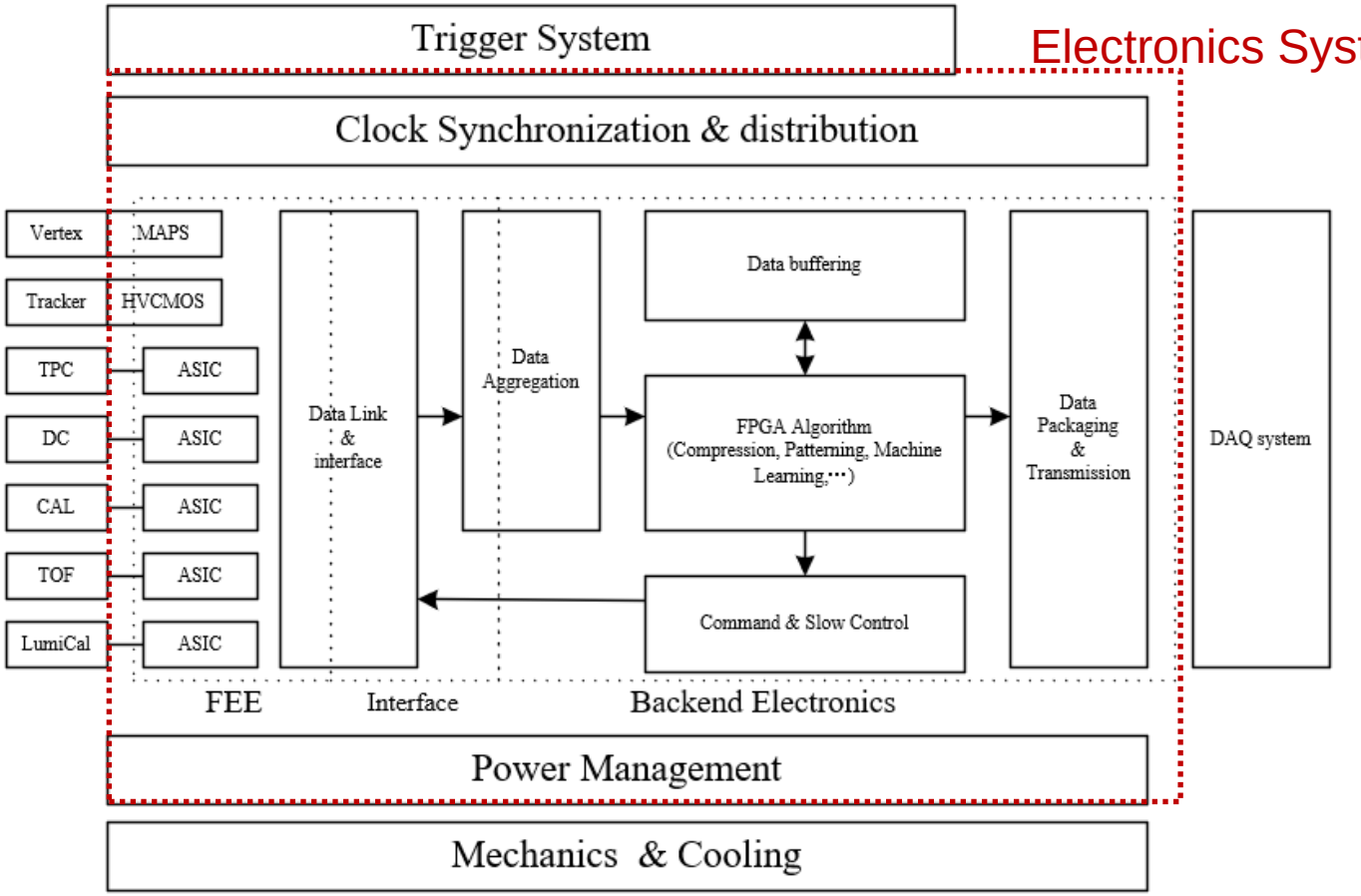
Requirements of Detector and Key Technologies

Sub-detector	Key technology	Key Specifications
Silicon vertex detector	Spatial resolution and materials	$\sigma_{r\phi} \sim 3\ \mu$m, $X/X_0 < 0.15\%$ (per layer)
Silicon tracker	Large-area silicon detector	$\sigma(\frac{1}{p_T}) \sim 2 \times 10^{-5} \oplus \frac{1\times10^{-3}}{p\times\sin^{3/2}\theta}(\mathrm{GeV}^{-1})$
TPC/Drift Chamber	Precise dE/dx (dN/dx) measurement	Relative uncertainty 2%
Time of Flight detector	Large-area silicon timing detector	$\sigma(t) \sim 30$ ps
Electromagnetic Calorimeter	High granularity	EM energy resolution $\sim 3\%/\sqrt{E(\mathrm{GeV})}$
	4D crystal calorimeter	Granularity $\sim 2 \times 2 \times 2\ \mathrm{cm}^3$
Magnet system	Ultra-thin	Magnet field $2-3$ T
	High temperature	Material budget $< 1.5X_0$
	Superconducting magnet	Thickness < 150 mm
Hadron calorimeter	Scintillating glass	Support PFA jet reconstruction
	Hadron calorimeter	Single hadron $\sigma_E^{had} \sim 40\%/\sqrt{E(\mathrm{GeV})}$
		Jet $\sigma_E^{jet} \sim 30\%/\sqrt{E(\mathrm{GeV})}$

By Wang JC

These specifications continue to be optimized

Elec-TDAQ overall framework



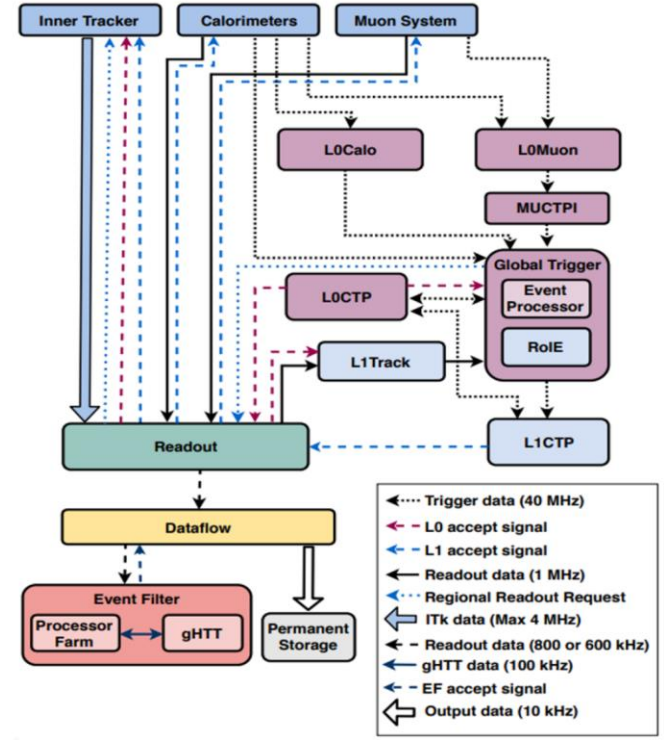
- **From the general framework towards the Ref-TDR:**

1. **To collect the detailed requirements from all sub-dets**
2. **To define the preliminary readout frame & strategy of Elec-TDAQ**

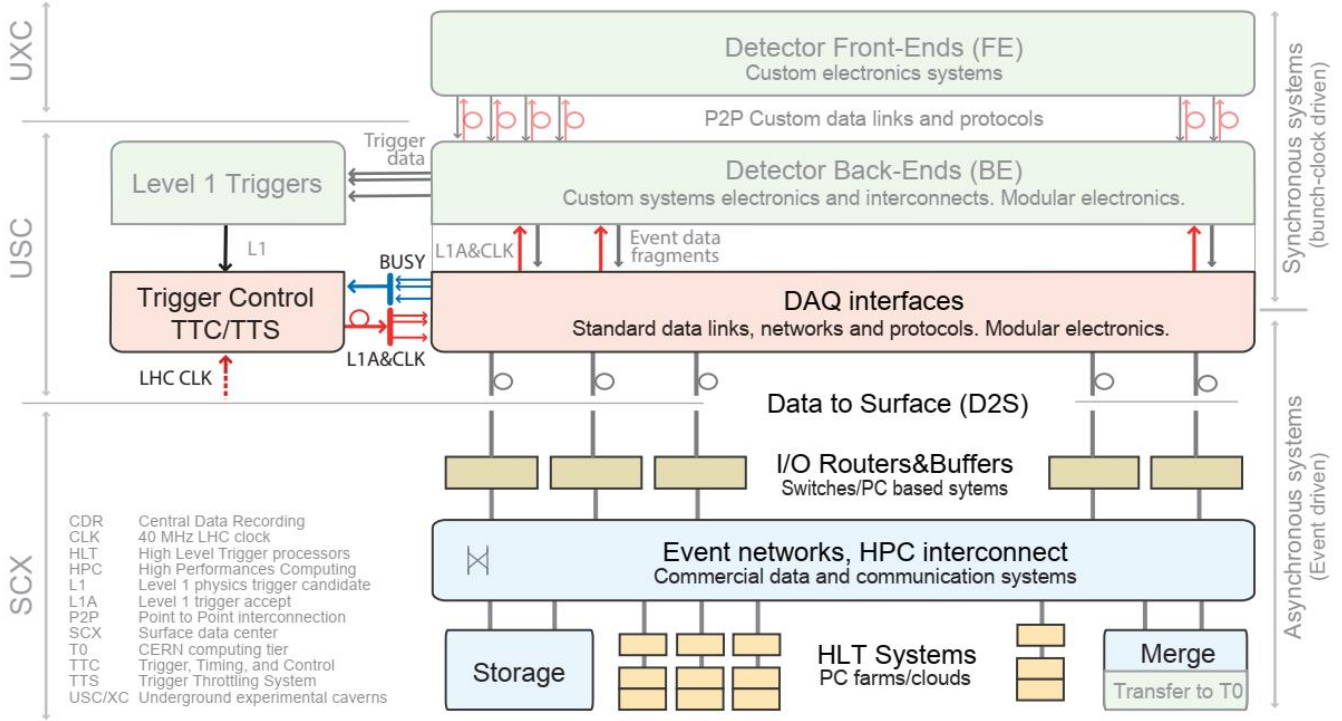
Requirement from Sub-Detector

	Vertex	Pix(ITKB)	Strip (ITKE)	TOF (OTK)	TPC	ECAL	HCAL
Channels per chip	512*1024 Pixelized	512*128 (2cm*2cm@34um*150um)	512	128	128	8~16	8~16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA	ADC + BX ID	TOT + TOA/ ADC + TDC	TOT + TOA/ ADC + TDC
Data Width /hit	32bit (10b X+ 9b Y + 8b BX + 5b chip ID)	48bit （9b X+7b Y +14b BX + 6b TOT + 5TOA + 4b chip ID）	32bit (10b chn ID + 8b BX + 6b TOT + 5b chip ID)	40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID)	48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)
Data rate / chip	1Gbps/chip@ Triggerless@ Low LumiZ Innermost	640Mbps/chip Innermost	Avg. 1.01MHz/chip Max. 100MHz/chip	Avg： 26kHz/chip @ z pole Max：210kHz/chip @z pole	~70Mbps/module Inmost	<4.8Gbps/module	<4.8Gbps/module
Data aggregation	10~20:1, @1Gbps	1. 1-2:1 @Gbps； 2. 10:1@O(10Gbps)	1. 10:1 @Gbps 2. 10:1 @O(10Gbps)	1. 10:1 @1Mbps 2. 10:1 @O(10Mbps)	1. 279:1 FEE-0 2. 4:1 Module	1. 4~5:1 side brd 2. 7*4 / 14*4 back brd @ O(10Mbps)	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)
Detector Channel/module	2218 chips @long barrel	30,856 chips 2204 modules	22720 chips 1696 modules	41580 chips 1890 modules	258 Module	1.1M chn	6.7M chn
Data Volume before trigger	2.2Tbps	2Tbps	22.4Gbps	1Gbps	18Gbps	164.8Gbps	14.4Gbps

Technology survey on global framework



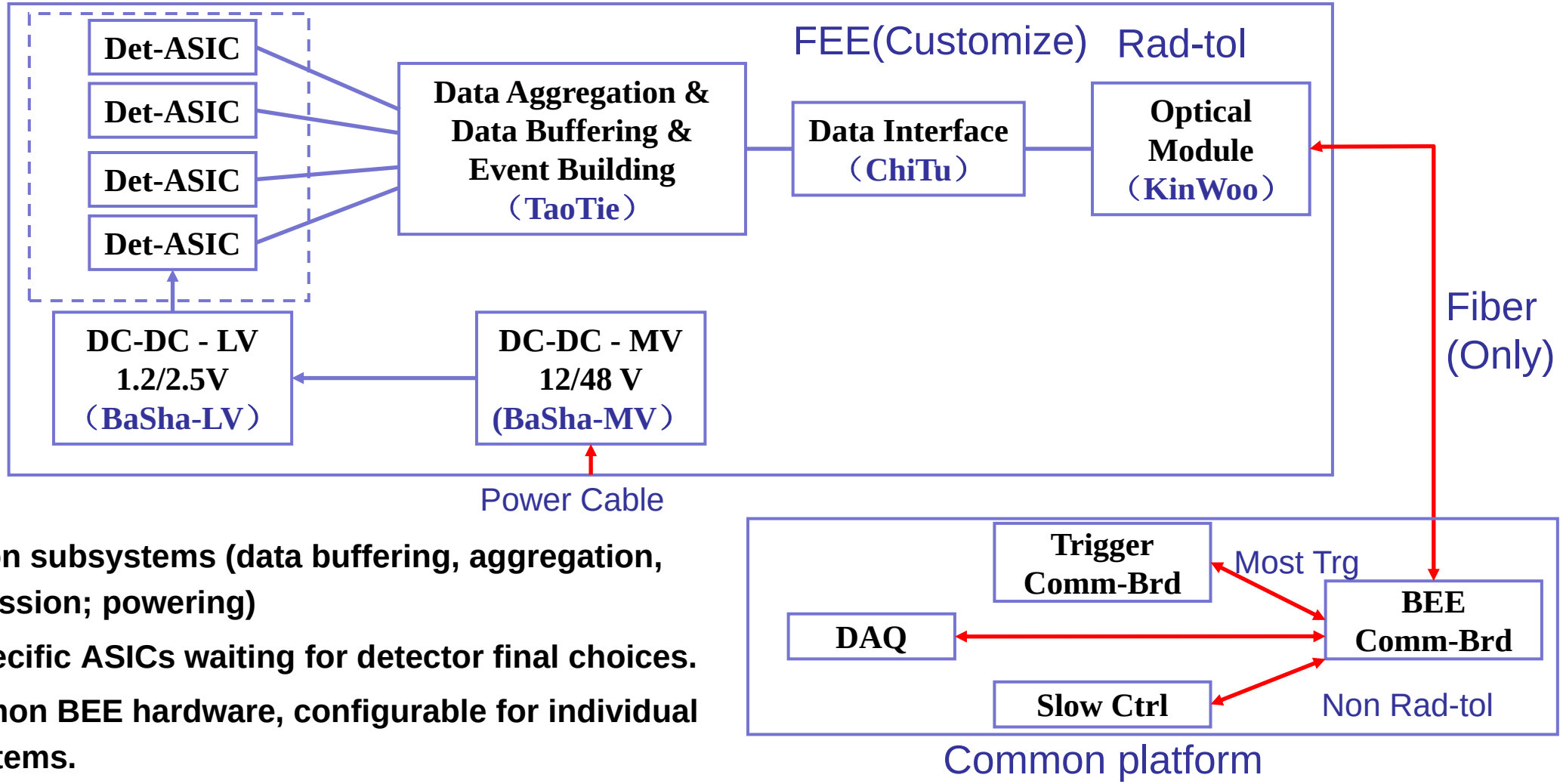
ATLAS Trigger framework



CMS Trigger framework

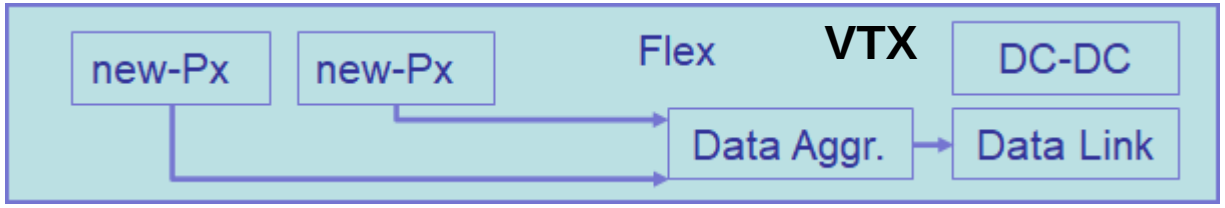
- **Two main reference frameworks of Electronics-TDAQ system are ATLAS & CMS Trigger system.**
- **While ATLAS is more like “Frontend trigger” that FEE provides the trigger information, the CMS is more like “Backend trigger” that trigger system communicates only with BEE.**
- **We choose “Backend Trigger” or “Triggerless readout” scheme as the baseline scheme.**

Global framework of the Elec system

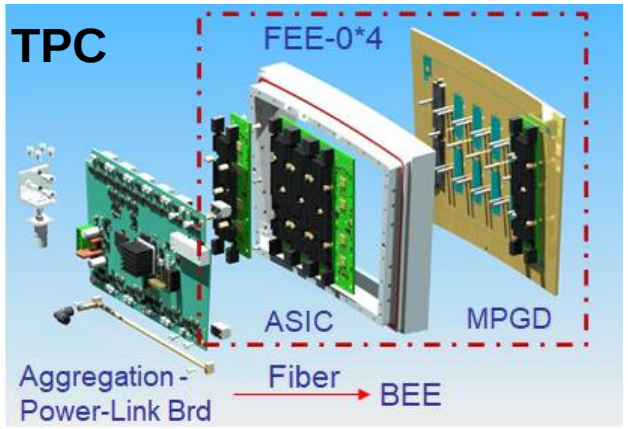


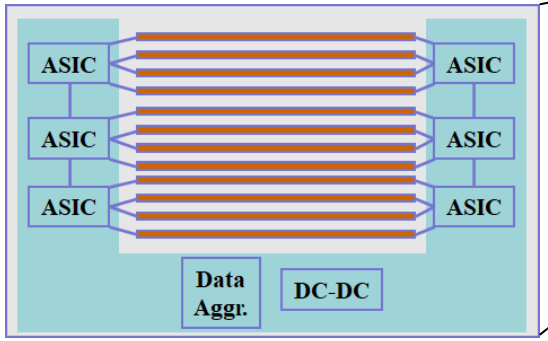
- **Common subsystems (data buffering, aggregation, transmission; powering)**
- **Det. specific ASICs waiting for detector final choices.**
- **A common BEE hardware, configurable for individual subsystems.**
- **TDAQ interface is (probably) only on BEE**

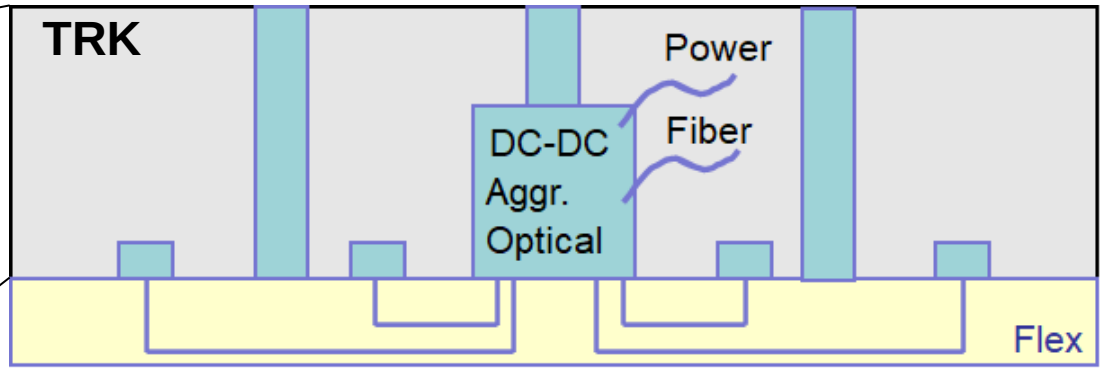
An overview of the Sub-Det readout electronics

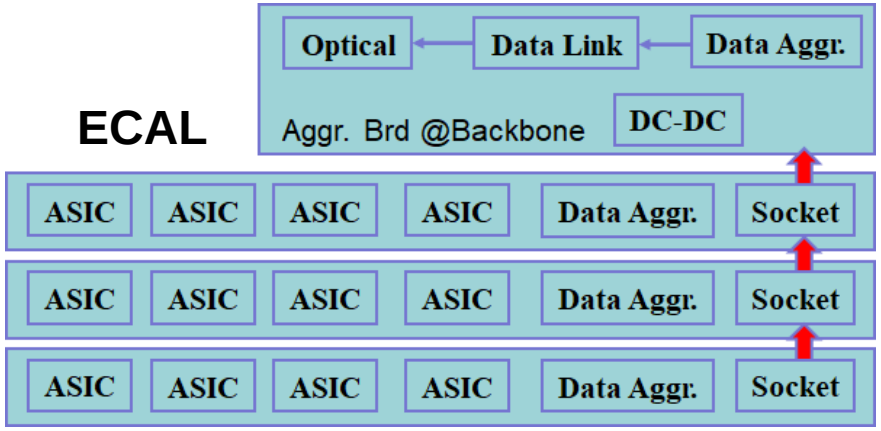


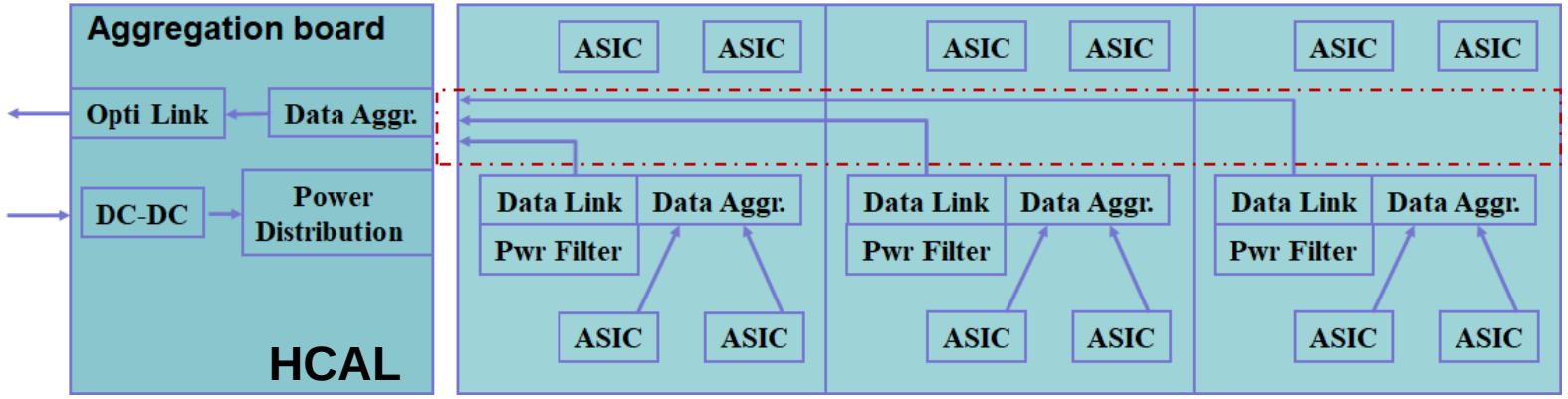
- **All sub-det readout electronics were proposed based on this unified framework, maximizing possibility of common design usage.**









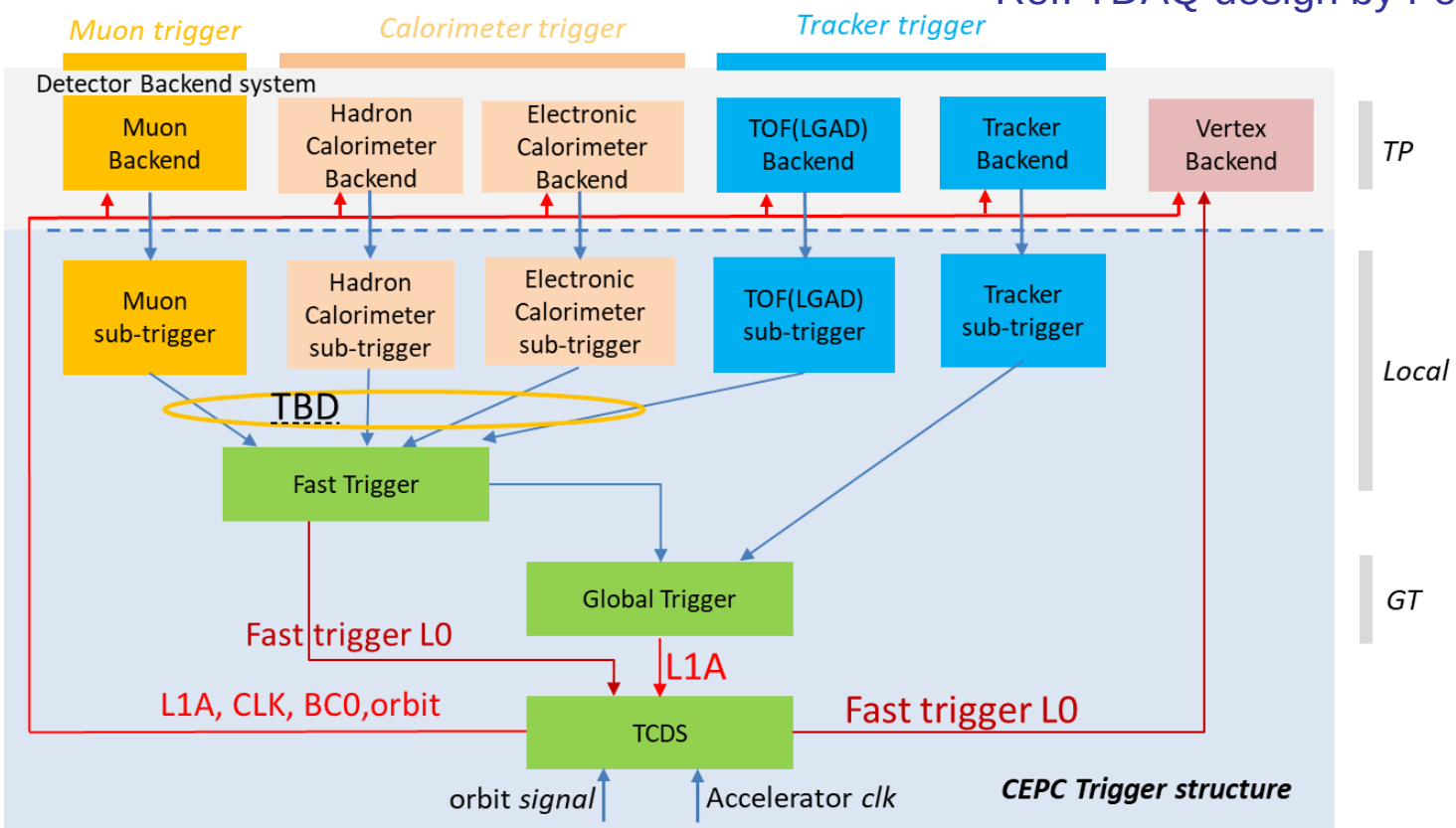


Backup scheme of the framework

- **The proposed framework was based on the estimated background rate of all sub-det.**
- **In case of under-estimation or unexpected condition:**

1. **Additional optical links can be allocated to the hottest module.**
2. **In case the background rate is too high for FEE-ASIC to process, Intelligent Data Compression algorithm can be integrated on-chip, for the initial data rate reduction.**

Ref: TDAQ design by Fei Li



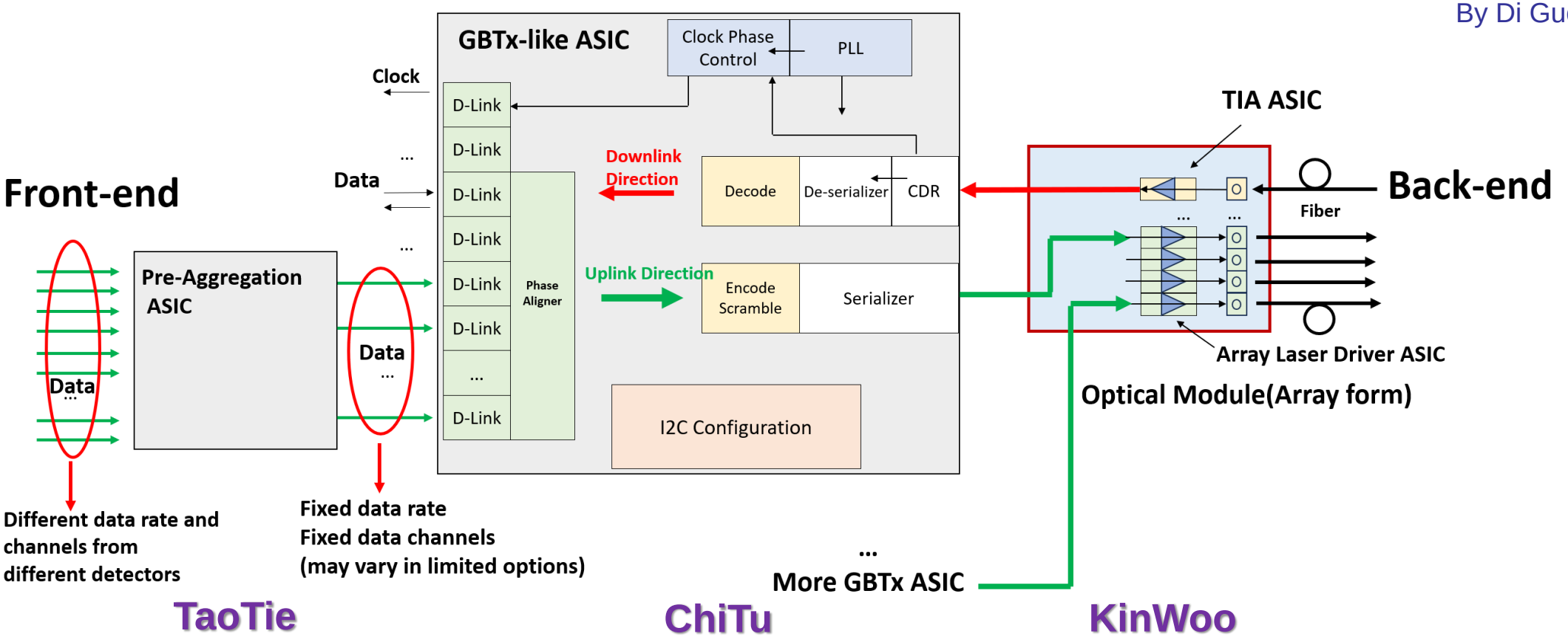
The conventional trigger scheme can always serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

Common Electronics Components

- **Common Data Link**
- **Common Powering**
- **Common Backend Electronics**
- **Backup Scheme based on Wireless Communication**

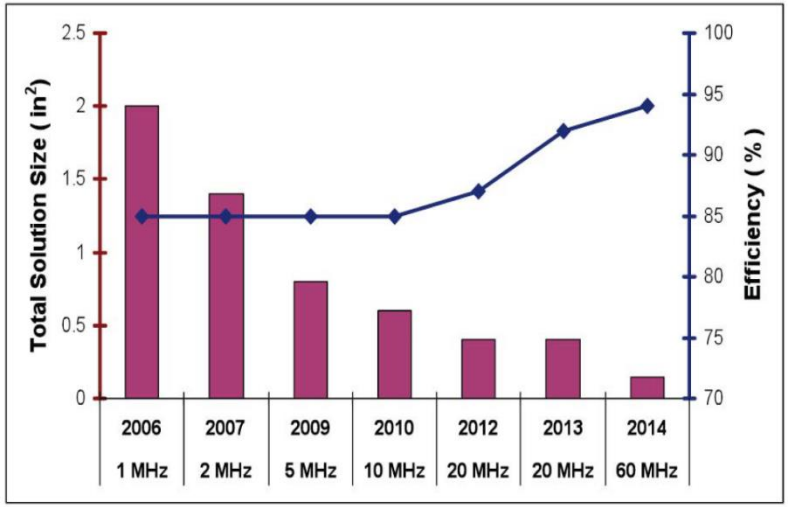
Common framework on Data Link

By Di Guo@CCNU

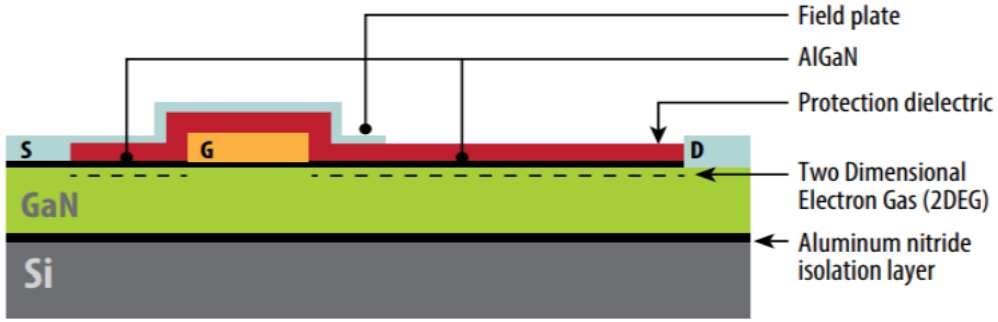


- **Pre-Aggregation ASIC (TaoTie): Intend to fit with different front-end detector (different data rates/channels)**
- **GBTx-like ASIC (ChiTu): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …**
- **Array Laser Driver ASIC + TIA ASIC + Customized Optical module (KinWoo)**

Common framework on Powering

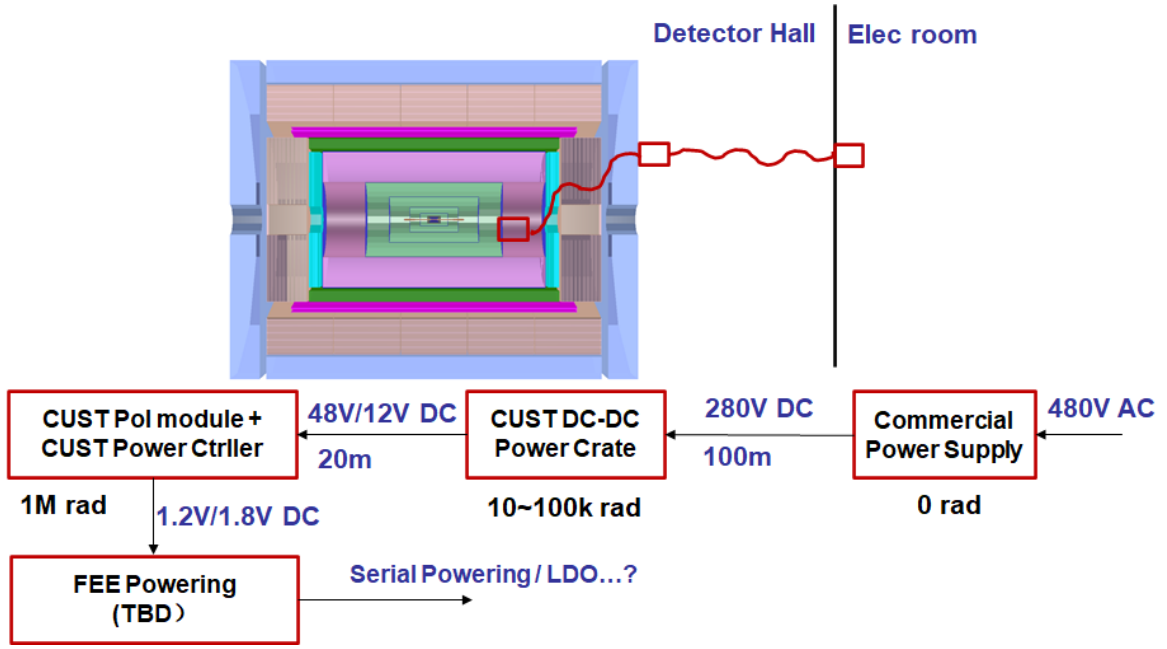


Higher switching Freq, smaller size, higher efficiency, lower on-resistance



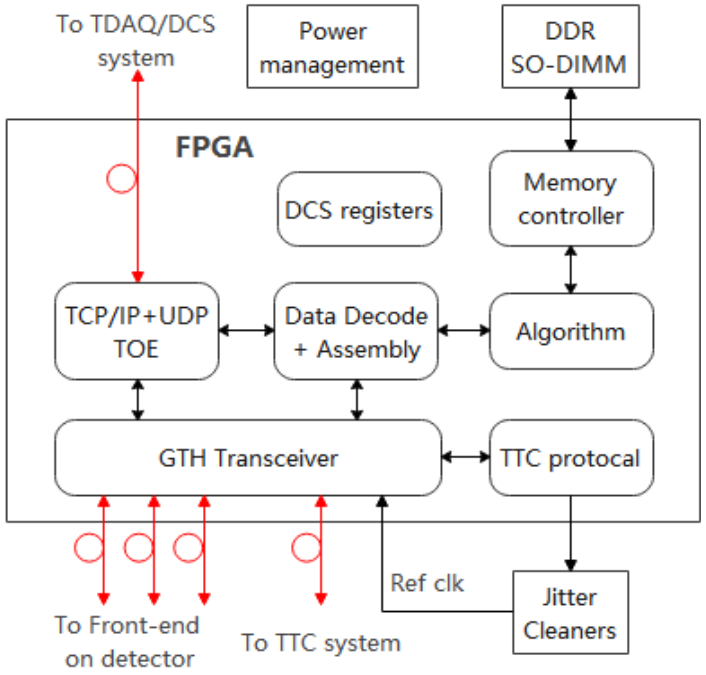
Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel)

Ref. Satish K Dhawan, 2010
Ref. S. Michelis, Prospects on the Power and readout efficiency



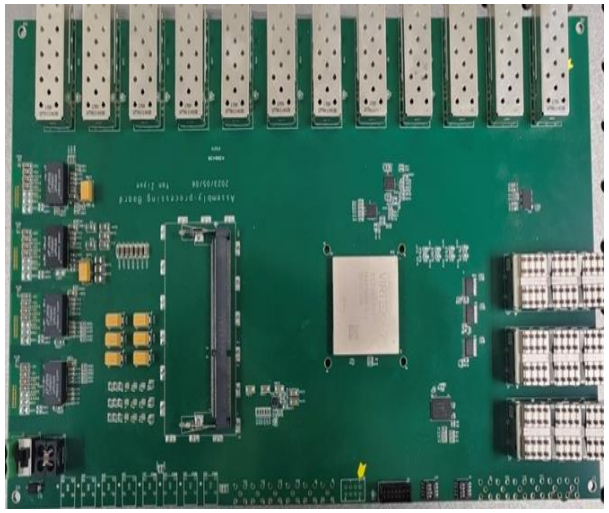
- **The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.**
- **also enables high voltage power distribution, for low cable material and low power loss**

Preliminary consideration on common BEE



The back-end Card structure

By Jun Hu@IHEP



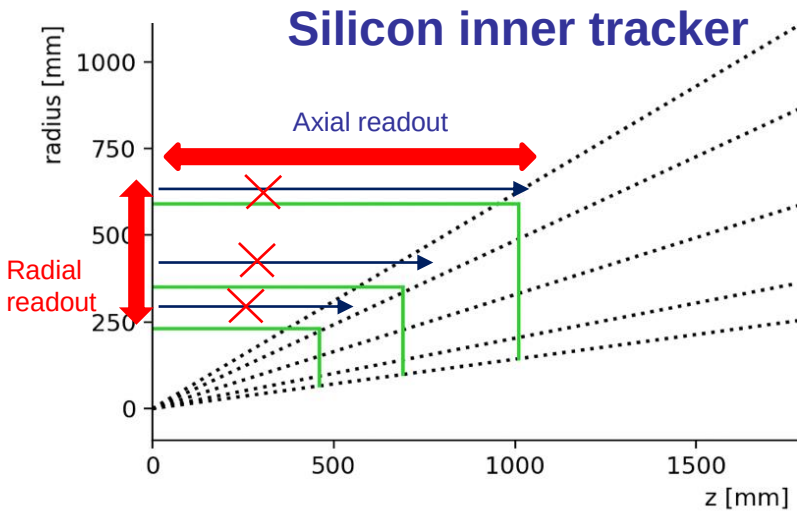
Data aggregation and processing board Prototype for Vertex detector

	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3 Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data between optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

- A cost-driven device selection: FPGA XC7VX690T
- Interface：SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

Backup scheme based on wireless communication



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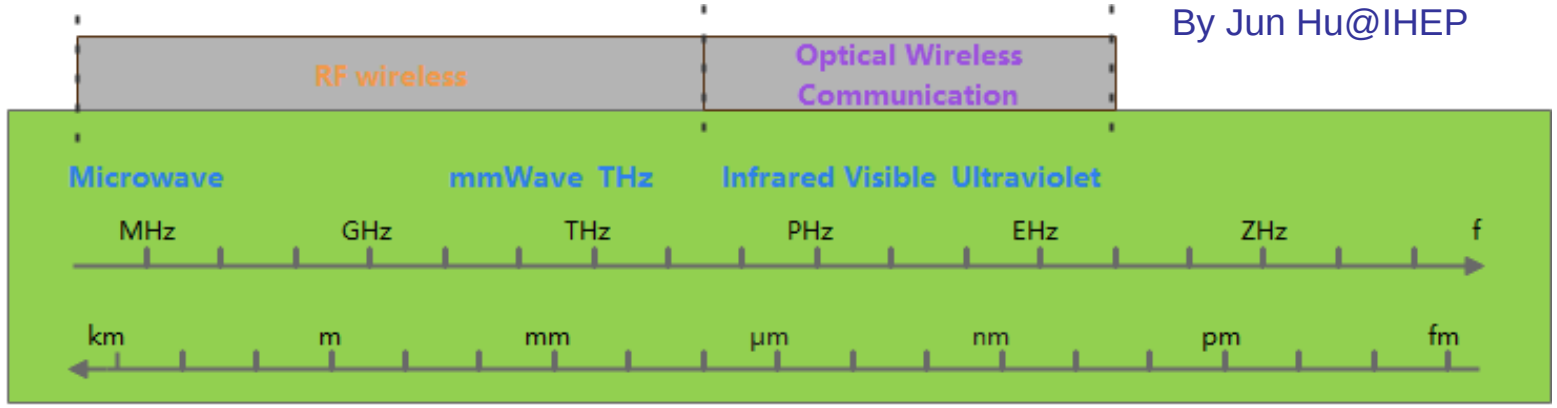


- Radial readout with mm-wave
  - 12- 24 cm transmission distance
  - Data rate : < 30Mbps
- Axial readout to endcap
  - Only at the outermost layer or dedicated aggregation layer.

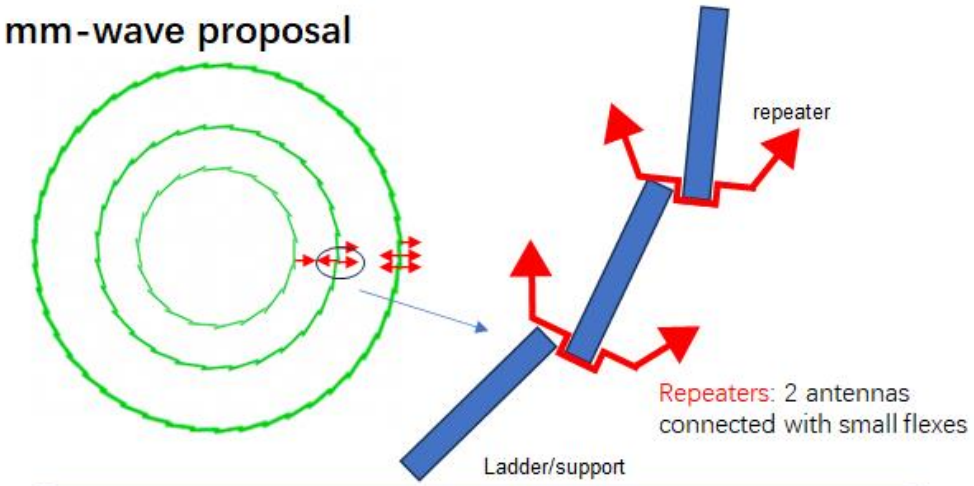
- WiFi (2.4GHz, 5GHz)
  - large antenna volume, high power consumption, narrow frequency band, and high interference
- Millimeter Wave (24GHz，45GHz，60GHz，77GHz)
- Optical wireless communication (OWC) / Free Space Optical (FSO)

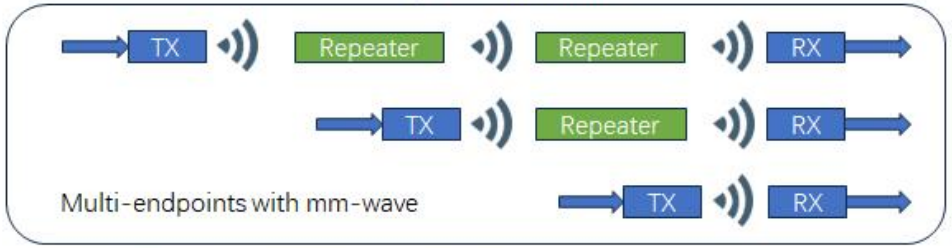
- Wireless communication based readout scheme was proposed to mitigate the cabling problem, as a backup scheme
- Three major solutions were investigated through R&D, two were selected with corresponding schemes

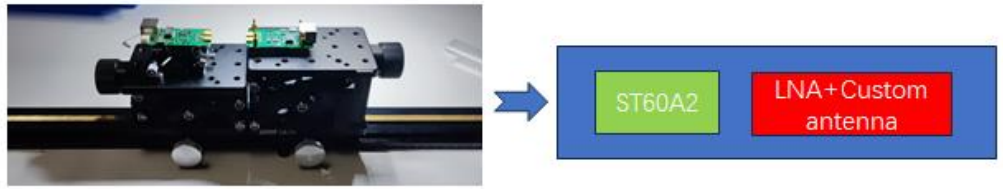
R&D efforts and results on WLess Comm

By Jun Hu@IHEP

mm-wave proposal





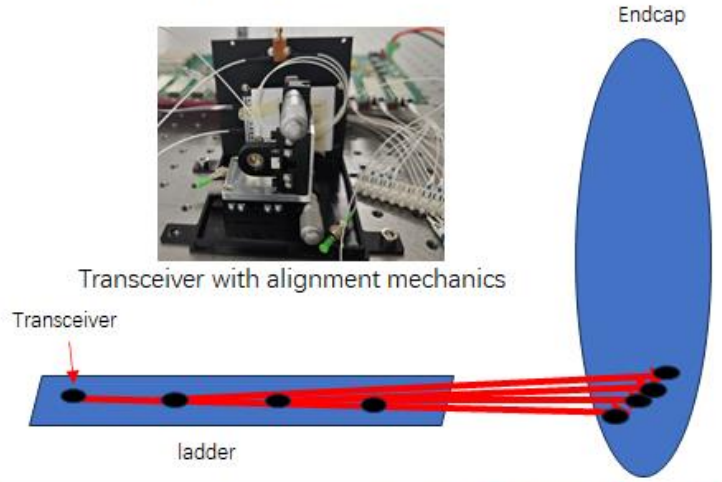


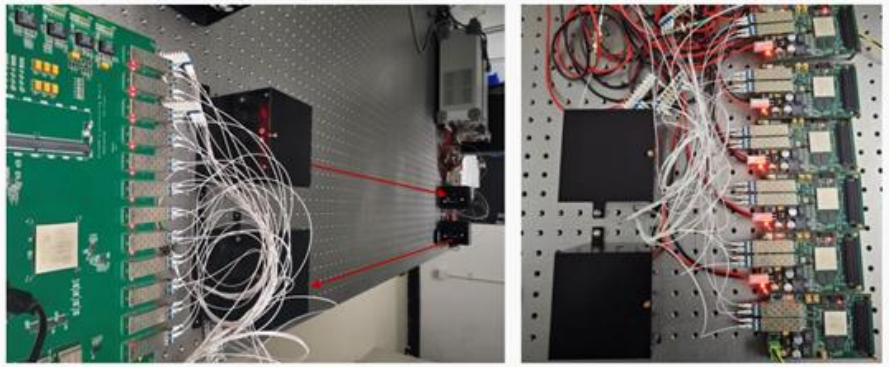
Test with evaluation boards – SK202

- Based on the commercial 60GHz RF chip ST60A2 transceiver from ST Microelectronics company.
- The transmission speed can exceed 900Mbps when the distance is less than 6 cm.

- Design a small PCB module with ST60A2. LNA and custom antenna.
- Higher bandwidth and longer distance
- Evaluate the interference with detector
- Under design, cheap and easy
- → custom transceiver + antenna +AIP

Optical wireless proposal





DWDM transceivers +AWG + lens

- Up to 6-meter free space optical transmission distance
- 10Gbps X 12 channels bandwidth
- PRBS 31bits error rate < BER-15 @ 10Gbps under 1.6m distance

Summary on current framework

- **Detectors can almost still keep with "triggerless readout" feature**
  - **All FEE raw data go to BEE losslessly**
    - **Except for the (innermost) Vertex**
  - **Trigger will almost communicate only with BEE**
    - **"Backend trigger" based**
    - **Both hardware / software trigger still possible**
- **All FEE module based on a similar framework:**
  - **ASIC – Aggr. – Data Link – Fiber + DC-DC – Pwr Cable**
  - **Minimized the module interconnection design, maximize the common platform design for BEE + Trigger**
    - **A highly compact & scalable system**
  - **Based on a successful design of GBTx-like chip & rad-hard DC-DC module**
    - **Size & height of the optical & DC-DC modules still with high challenges**
    - **Backup plan if failed: back to the cable based architecture**

Future Plan towards the Ref-TDR

- **Endcap design not ready for most sub-detectors**
- **MDI & background rate may have a big impact on the scheme**
  - **Especially for the innermost layer of endcap**
- **Some key R&Ds are urged to initiate**
  - **Rad-hard powering & link**
  - **Key ASICs which are currently absent (SiPM FEE, Strip LGAD)**
- **Additional backup and innovative schemes not included in this talk**
  - **Drift chamber as a backup scheme for the middle track to enhance dN/dx**
  - **Si Strip as a backup scheme for the outer tracker for low cost, robustness and maturity**
  - **To evaluate the possibility by using wireless communication**

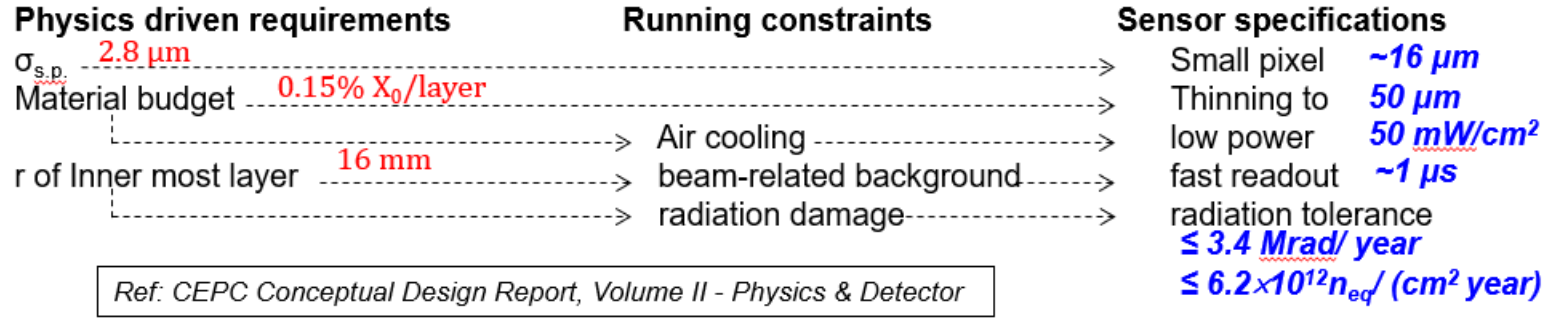
Thank you!

Backup

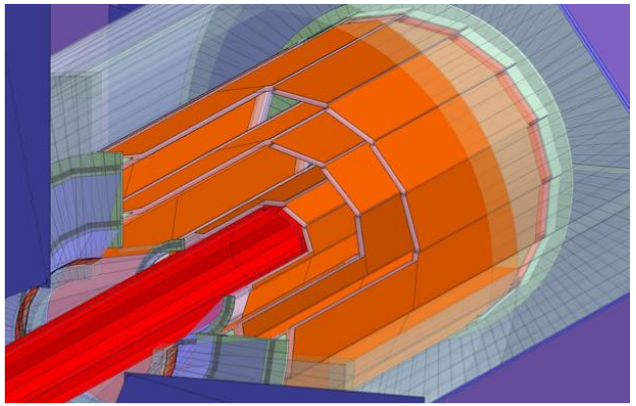
A summary of FEE power

	Vertex	Pix Tracker	TOF	Si Strip	TPC	DC	ECAL	HCAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT	E + 400psT
Channels per chip	512*1024 Pixelized	768*128 (2cm*2cm@25um*150um)	128	128	128	-	16	16
Voltage@chip	1.8V@180nm (1.2V@65nm future)	1.2V@55nm (HVCMOS Pixel)	1.2V@55nm (TDC)	1.2V@130nm (电压统一、便宜)	1.2V@65nm	±3.3V商用→1.2V@GaAs?	1.2V@55nm (TDC)	1.2V@55nm (TDC)
Power@chip	<200mW/cm2 <0.8W/chip	<200mW/cm2 <0.8W/chip 尚无设计	<40mW/ch <5W/chip	5mW/ch 640mW/chip	35mW/chip	?	20mW/chn 160~320mW/chip	20mW/chn 160~320mW/chip
chips@module	10~20:1	<10:1 尚无设计	10:1	10:1	279:4:1	需FPGA、ADC供电，可统一1.2V?	112~280:1 侧板无DCDC 仅电容	~10:1
Power@module	8~16W @1.8V 4.4~8.9A	8~16W @1.8V 4.4~8.9A	50W (???) @1.2V 41.7A	6.4W @1.2V 0.53A	40W @1.2V 33.3A		44.8W @1.2V 37.3A	3.2W @1.2V 2.6A
Other	辐照TID 7.3Mrad/y @ HLumi Z		需进一步优化			On FPGA	可能SiPM可共用60V中压电源	可能SiPM可共用60V中压电源

Vertex Detector



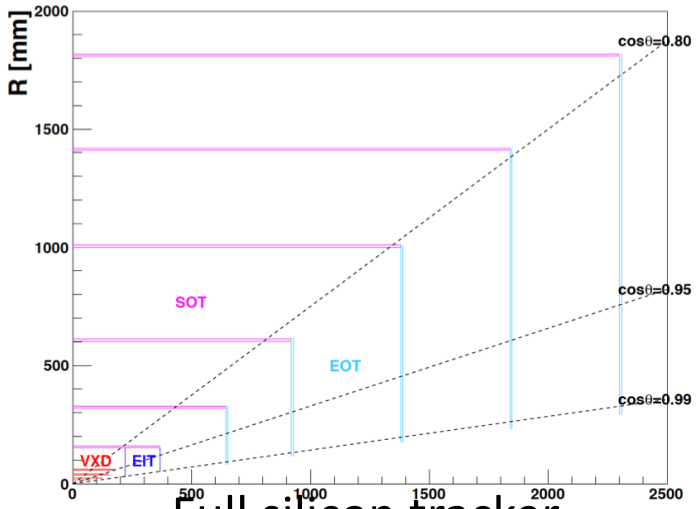
Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector



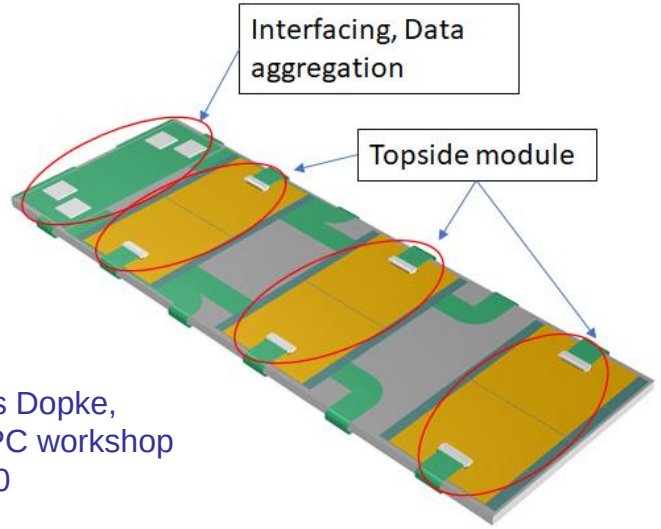
	R (mm)	|z| (mm)	Number of ladders	Number of chips
Layer 1	16	125.0	10	200
Layer 2	18	125.0		
Layer 3	37	125.0	22	440
Layer 4	39	125.0		
Layer 5	58	125.0	32	640
Layer 6	60	125.0		

- **A thin pixel detector with a small pixel size**
  - Small electrode MAPS
- **Detector channels**
  - 64 double-sided ladders, ~1280 chips
  - ~ 0.5~1M pixels/chip
- **2D resolution ~3μm, with fast readout capability**
  - Hit rate ~40MHz/cm^2 @ W, ~32bit/hit
  - Timestamp with 25ns resolution for Z pole
  - Data rate
    - 205Gbps@Trigger；5.12Tbps@Triggerless
- **Overall system**
  - Lower material budget
    - Low power & air cooling & lower material mechanics
  - Radiation tolerance

Inner Tracker – Si Pixel



Full silicon tracker



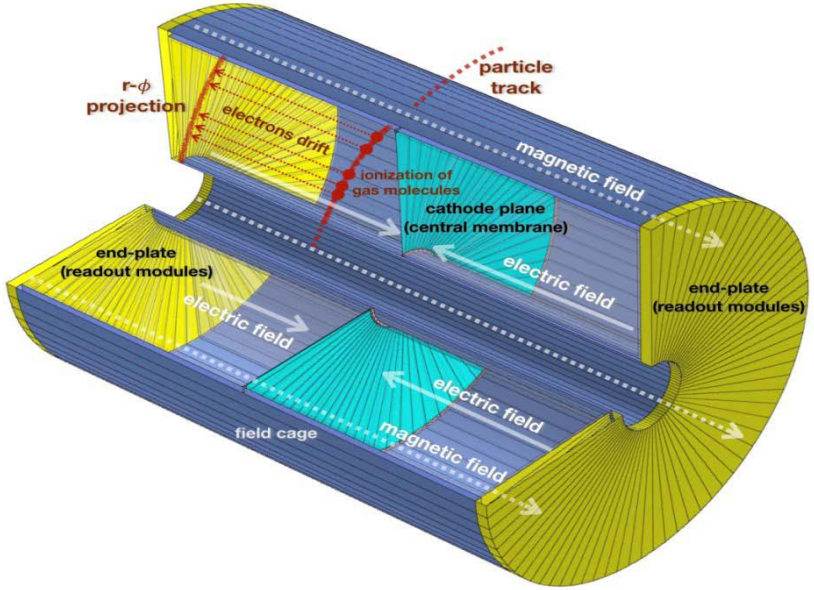
Jens Dopke, CEPC workshop 2020

silicon tracker module

- **A large area silicon tracker with ~10μm spatial resolution @ r-φ** Yiming Li
  - ~70-140m^2 with ~50μm pixel pitch
  - Should be cost effective (HVCMOS is proposed to be used)
- **Hit rate and signal measurement**
  - 10^{-4} hit/cm^2/event @ Z, ~10bits per hit, ~10ns time resolution
    - 10b time stamp + 7b TOT
- **Detector channels**
  - ~60k modules (each with 4 chips)
  - 1Gbps data link per module and 10+ Gbps high speed link per structure
- **Overall system**
  - 160mW/cm^2 => 2.6W/module (O(100kW) for all)
  - Liquid cooling expected @-20 ℃

ATLASPix3 features
- TSI 180nm HV process on 200 Ωcm substrate
- Pixel size 50 × 150 μm^2
- 132 columns × 372 rows (20.2 × 21 mm^2 chip)
- Each pixel has 7-bit TOT + 10-bit timestamp
- Continuous / triggered readout with 8b10b / 64b66b coding
- Power consumption ~160 mW/cm^2.

Middle Tracker – Pixel TPC

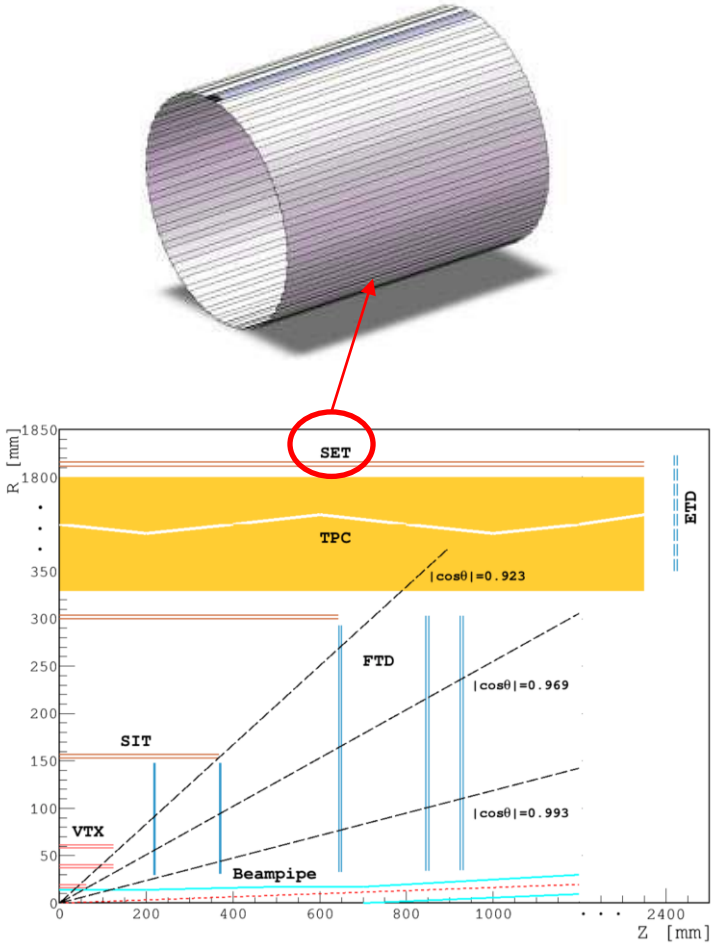


Parameter	Specification
Noise	<200e
Conversion gain	>15mV/fC
Peaking time (defaul)	100ns
Non lineartity	<1%
Cross talk	<0.3%
Dynamic range	>2000
Power consumption	<5mW/ch

- **~100μm spatial resolution @ r-φ** Huirong Qi
  - Material budget: <1%X0 including outer field cage
  - GEM+μMEGAS / Pixel TPC
- **Hit rate and signal measurement**
  - Momentum resolution: ~10^{-4}/GeV/c
  - dE/dx resolution: <5%
  - Time resolution : ~100ns
- **Detector channels**
  - 5k chn/module; 84 module/endplate; 2 endplate => 840K channels => should be really low power
  - 6.5K ASIC chip if 128chn/chip
- **Data rate**
  - 48K chn/hit @10^{-4}/ BX / channel
  - 7b chn ID + 9b ADC per hit + 2B per ASIC = 22KB / BX = 110Gbps for the overall detector
- **Overall system**
  - CO_2 cooling
  - Trigger or triggerless

Outer Tracker – AC-LGAD TOF

Zhijun Liang



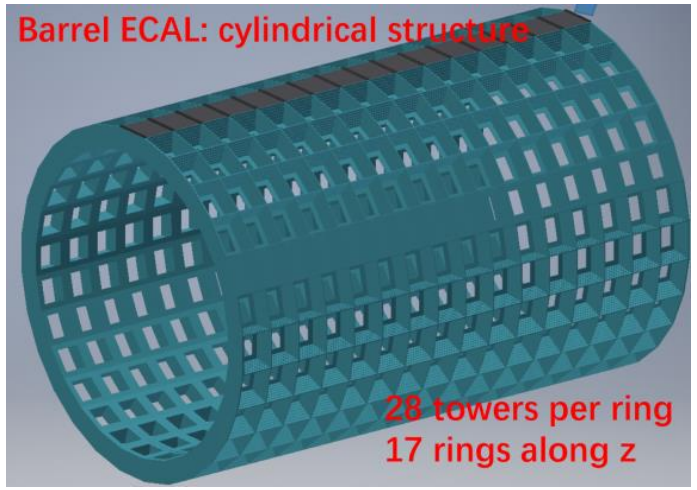
Baseline detector concept in CDR

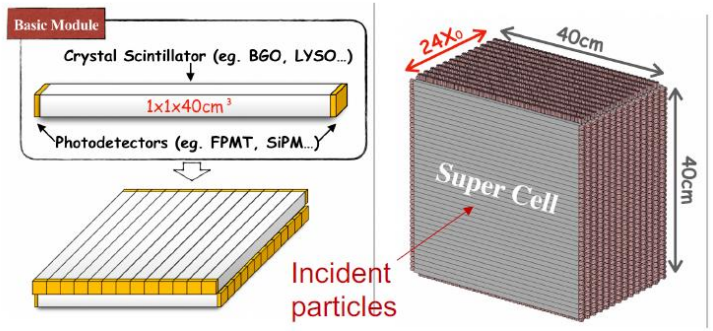
- **Recommended by the Int. Advisory Committee**
- **Detector concept**
  - Area of detector (Barrel : 50 m^2 , Endcap 20 m^2)
  - Strip-like sensor (4cm × 0.1 cm)
- A Timing detector and part of the tracker (SET)
  - Timing resolution: 30-50 ps
  - Spatial resolution: ~ 10 μm
- **Signal measurement**
  -

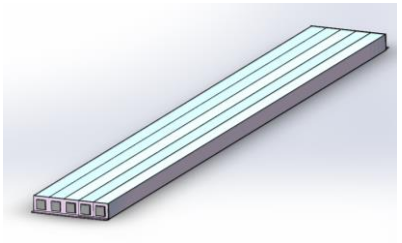
	ATLAS HGTD	CEPC TOF
Area (m^2)	6.4	~ 70
Granularity	mm^2 (1.3 mm ×1.3mm)	~ cm^2 (40m × 0.2mm)
Channel number	**~ 3.6 × 10^6**	**~ 7×10^6**
Module assembly	Bump bonding	Wire bonding at strip
MIP Time resolution	30-50 ps	30-50 ps
Spatial resolution	~ 300 μm	~ 10 μm
探测器信号幅度	2fC- 20fC	2fC- 20fC

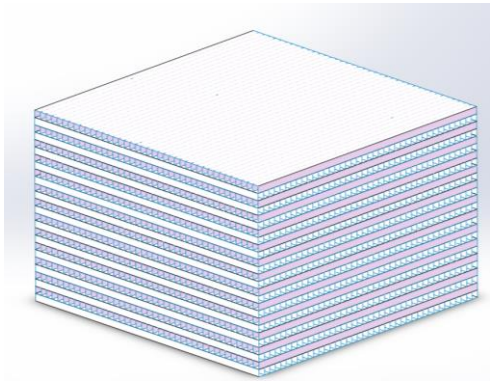
- **Data rate**
  - 200kHz event @ 16bit/event (9bTOT + 7bTOA)
  - 100k chips for 70m^2
- **Power: <** 2W per chip

ECAL concept – crystal bar







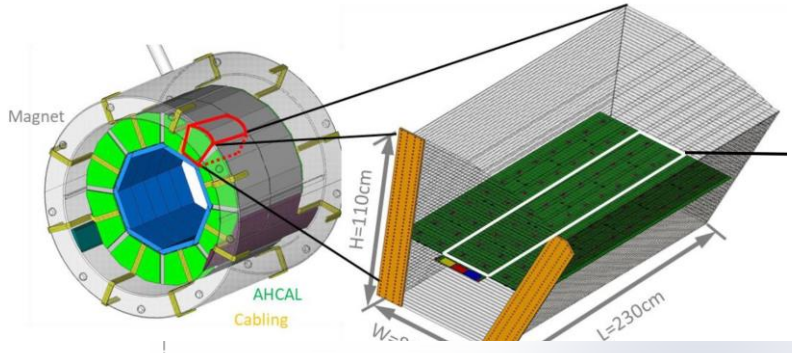


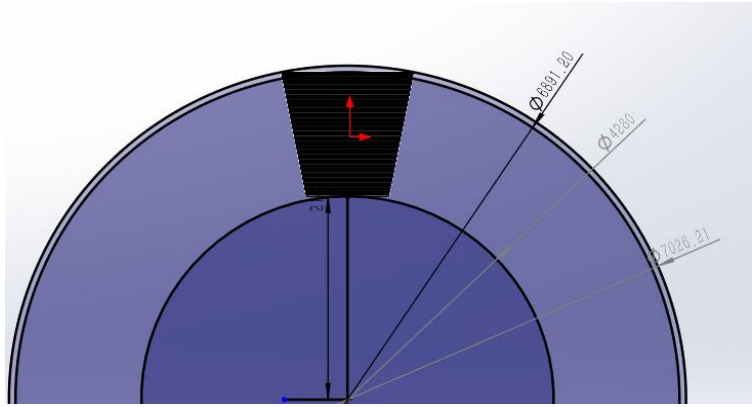
Yong Liu, Shaojing Hou

40bars*26layer=1 unit

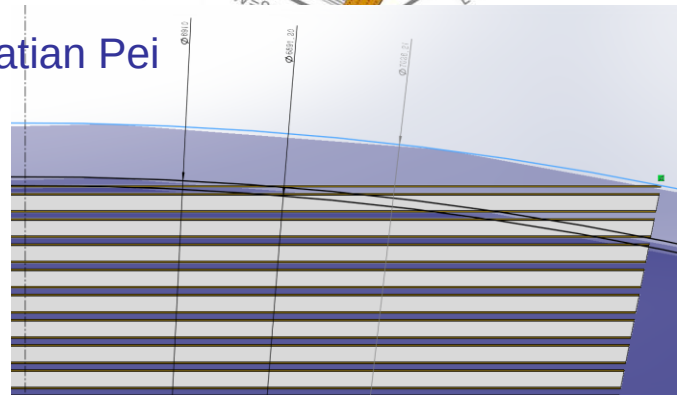
Key Parameters	Value/Range	Remarks
MIP light yield	~200 p.e./MIP	~8.9 MeV/MIP in 1 cm BGO
Dynamic range	0.1~10^3 MIPs	Energy range from ~1 MeV to ~10 GeV
Energy threshold	0.1 MIP	Equivalent to ~1 MeV energy deposition
Timing resolution	~400 ps	Limits from G4 simulation (validation needed)
Crystal non-uniformity	< 1%	After calibration
Temperature stability	Stable at ~0.05 Celsius	Reference of CMS ECAL
Gap tolerance	~100 μm	TBD via module development

HCAL concept – glass scintillator

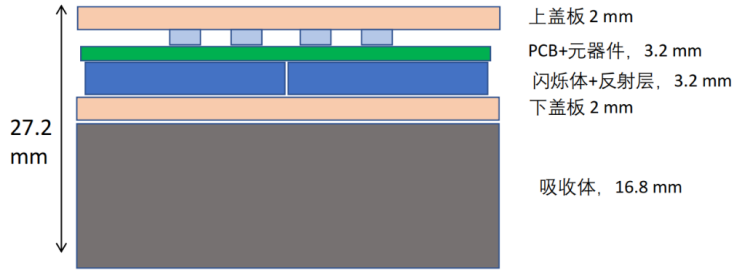




Yong Liu, Yatian Pei

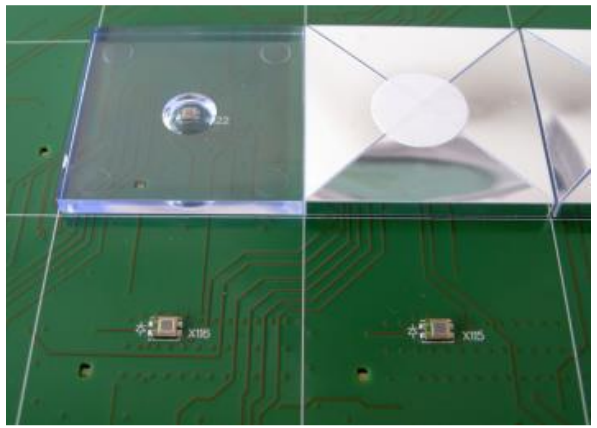


CEPC PS-AHCAL

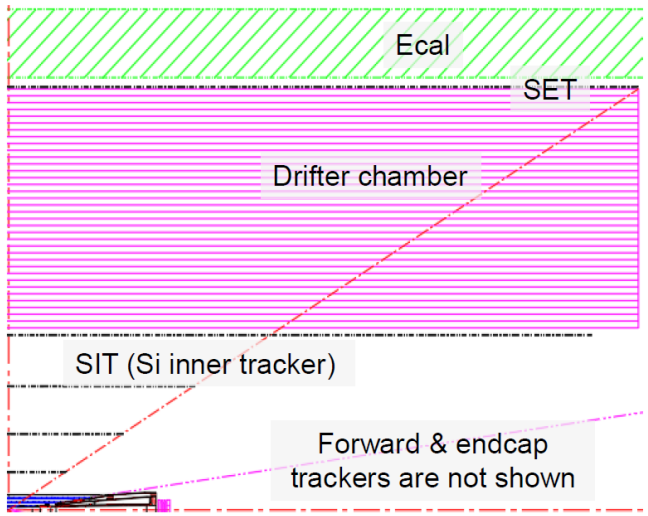


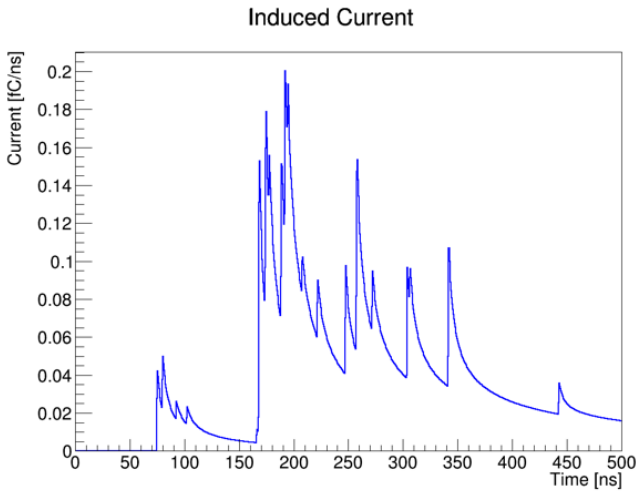
Specifications for front-end electronics

Parameters	Requirement	Remarks
SiPM readout	Single photon calibration	Inputs to SiPM monitoring and saturation corrections at large signals
Dynamic range	1 – 10,000 p.e.	Energy deposition up to 100 MIPs
Integration	125 ns* ($\rightarrow \sim 1\mu s$)	Can/should be optimised: balance of energy resolution and SiPM noise
Timing resolution	1ns* ($\rightarrow \sim 100ps$)	Can/should be optimised: fast timing would help better PFA performance and better energy resolution



Middle tracker backup scheme - Drift Chamber





Mingyi Dong

- **A Drift Chamber optimized for PID**
  - better than 2σ K/π separation for P < 20GeV/c
- **Signal measurement**
  - dN/dx for cluster counting method
- **Signal characteristics**

Parameters	Value	Parameters	Value
Rising	0.5~1ns	Falling	~tens ns
Pulse width	Hundreds ns	Pulse spacing (overlapping)	few~dozen ns
Amplitude	Dozen~hundred nA	Pulse charge	Ten~dozen fC

- **Detector channels and data rate**

		Higgs	Z
Trigger-less		256 Gbps	6.4 Tbps
Trigger	Trigger rate	1 kHz	100 kHz
	Max #wires/event	25k	10k
	bandwidth	20 Gbps	800 Gbps

50 peaks/wire*, 16bit/peak from F.Grancagnolo

FY Guo, CEPC workshop 2021

On LumiCal

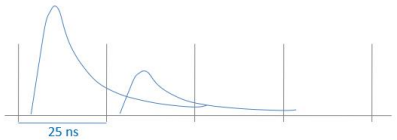
- **Schemes for the Elec readout**
  - Si detector: to re-use a strip detector readout, either AC-LGAD or Si Strip
  - LYSO: to re-use SiPM readout in ECAL, but has to consider the issue of pile-up
    - Waveform sampling may generate too many data(and power), try to think about a better solution
- **Trigger**
  - Requires a dedicated trigger design for Bhabha event

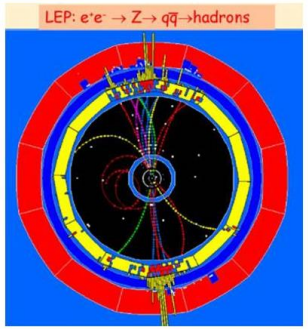
$Z \rightarrow q\bar{q}$ pile-up rate @High-Lumi Z

1. High-Lumi Z (2021 design) L_{max}/IP = **115 x 10^{34}/cm^{2}s**
2. **$Z \rightarrow q\bar{q}$**, X-sec = **41 nb**
   Event rate = (41x10^{-33}) x (115 x 10^{34}) /sec = ***47 kHz***
   bunch cross = 40 MHz
3. Event rate / 25 ns bunch crossing = **0.001 events /b.c.**
4. **next b.c. having a $Z \rightarrow q\bar{q}$**

Pile-up rate 4π coverage ~ 1x 10^{-3}

if BCID not identified
- **pileup of two 2-jets ➔ 4-jet**
- **rare decay precision ~1x 10^{-3}**





6

Specification calculation- from hit density

		Hit density (Hits/cm^2/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm^2)	Hit Pix rate (M Px/cm^2)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	0.017
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	3.6
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

- TDR raw hit density: Higgs 0.54，Z 0.3；Safety factor: TDR 1.5, CDR 10;
- Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)
- Area: 1.28cm*2.56cm=3.27cm^2 (@pixel size 25um*25um)
- Word length: 32bit/event (@Taichu's scale, 512*1024 array)
- Trigger rate：20kHz@CDR，120kHz@Z, 10Hz@Higgs, 2kHz@W TDR
  - Trigger latency: 3us(very likely not enough), Error window: 7 bins
  - FIFO depth: @3us * hit rate/chip
  - Data rate=pixel/bunch*trigger rate*32bit*error window