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Sr90 test for TaichuPix-3

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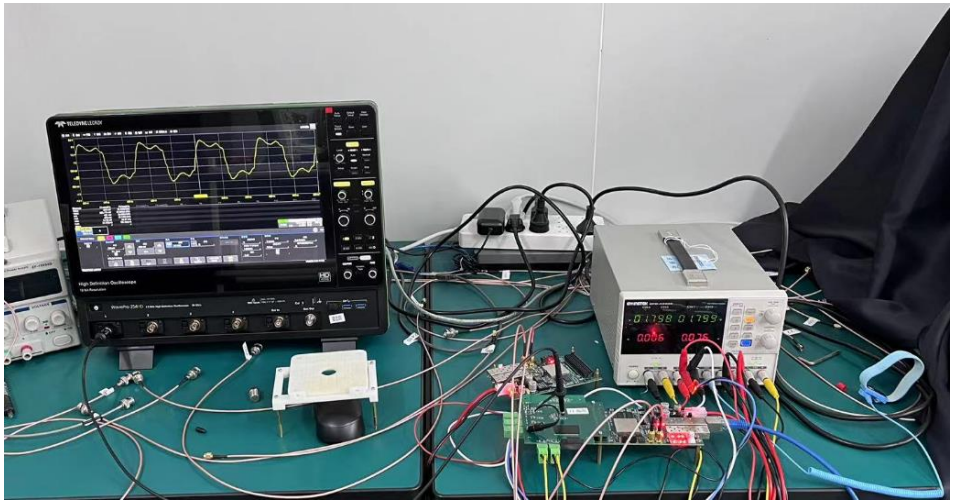
CEPC
Circular Electron Positron Collider

Setup

- W9R5, DUTB at DESY
- ITHR is set to 32 (218 e-)
- Sr90 is put on the backside of TaichuPix-3 with 2cm
- Configuration with Python
- Taking data with MATLAB



Set 640Mbps

W/R	1	00001	TRIGN (default:0)	CPRN (default:0)	DOFREQ[1:0] (default:01)	SMOD (default:0)	CTM (default: 0)	SPI_D (defau lt:0)	TMOD (default:0)	
W/R	21	10101	Resrved8 [15:8] >>>>>>DAC_REG [111:104] Default: 0000 0111							
W/R	22	10110	BSEL (default:0)	ISEL1 (default: 0)	ISEL0 (default: 0)	EXCKS (default: 0)	DSEL (default:0)	CKESEL (default:0)	RCKI (default:0)	RCKO default:0)

Register 10110: PLL&Ser setting, Refer the presentation of Xiaoting Li.

BSEL: Loop bandwidth configuration

ISEL1, ISEL0: charging current configuration

(TMOD : It should be setting in Register 00001)

DSEL: Input data selection. DSEL=0 for pixel array data; DSEL=1 for PRBS data.

CKESEL: Clock-sampling edge set bit of the MUX first stage.

RCKI: Reference clock source set bit, 0: clock from chip bus, 1: clock from PCB bus.

RCKO: Output clock set bit, 0: clock from chip bus, 1:clock from PLL.

EXCKS: 0 :PLL clock; 1 ： external clock (EXCK)

More control bits for PLL&Ser are defined in Register 11110.

1: Assert a start pulse.

DOFREQ[1:0] :Set the data output (DOUT[31:0]) frequency in trigger mode.

00: 2MHz

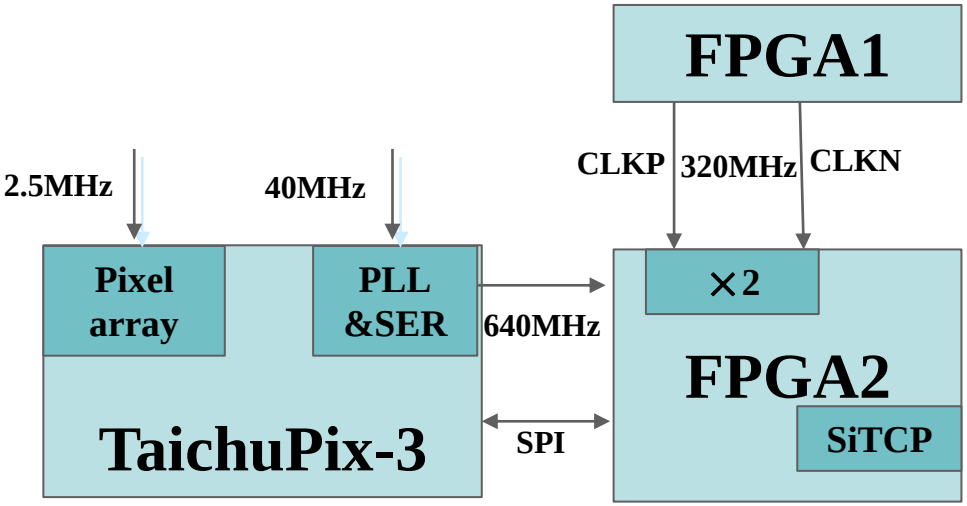
01: 5MHz (default),

10: 10MHz,

11: 20MHz

DOFREQ=’11’
TMOD=‘0’
RCKI=‘1’

Firmware setup



chipID	Ts	Ts_FPGA	col	row	ptn	valid
13	97	464493	0	323	0	1
13	97	464493	128	323	0	1
13	97	464493	128	323	0	1
13	118	464493	128	323	0	1
13	118	464493	511	323	0	1
13	118	464493	0	323	0	1
13	118	464493	0	323	0	1
11	186	167773184	192	72	0	0
10	171	185204736	0	0	2	1
13	139	464493	0	323	0	1
13	139	464493	128	323	0	1
13	139	464493	256	323	0	1
13	139	464493	511	323	0	1
13	160	464493	0	323	0	1
13	160	464493	128	323	0	1
13	160	464493	256	323	0	1
13	160	464493	256	323	0	1
13	181	464493	511	323	0	1
13	181	464493	0	323	0	1
11	186	167773184	192	72	0	0
10	171	185204736	0	0	3	0
13	181	464493	128	323	0	1
13	181	464493	128	323	0	1
13	202	464493	128	323	0	1
13	202	464493	511	323	0	1
13	202	464493	0	323	0	1

- One FPGA cannot fully satisfy all the clock domain requirement.
- DELAY: write.reg(UDP_BASE_ADDR, 0x14, '03')

- The same timestamp will poll four pixel addresses.
- There will be repeated reads or data loss.

Lower down speed

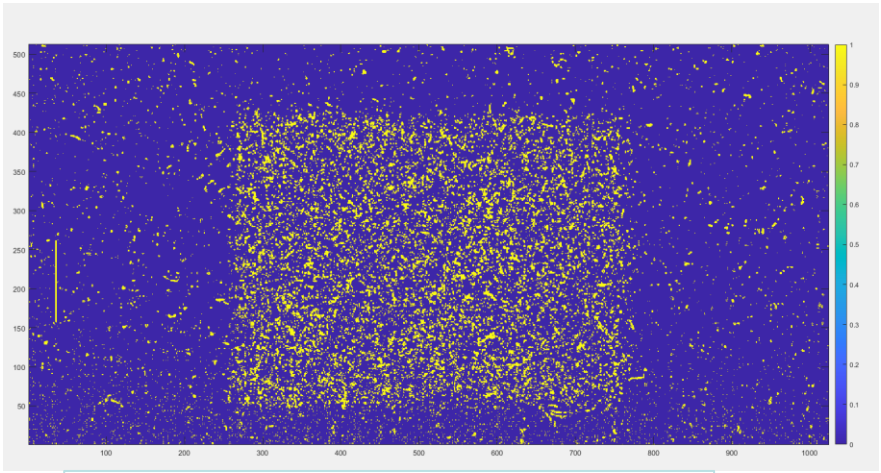
13	85	332991	256	323	0	1
13	85	332991	511	323	0	1
13	85	332991	0	323	0	1
13	85	332991	128	323	0	1
13	106	332991	128	323	0	1
13	106	332991	256	323	0	1
13	106	332991	511	323	0	1
13	106	332991	0	323	0	1
13	127	332991	0	323	0	1
13	127	332991	128	323	0	1
11	186	167773184	192	72	0	0
10	171	185204736	0	0	1	0
13	127	332991	256	323	0	1
13	127	332991	511	323	0	1
13	148	332991	511	323	0	1
13	148	332991	0	323	0	1
13	148	332991	128	323	0	1
13	148	332991	256	323	0	1
13	169	332991	256	323	0	1
13	169	332991	511	323	0	1
13	169	332991	0	323	0	1
13	169	332991	128	323	0	1
11	186	167773184	192	72	0	0
10	171	185204736	0	0	1	1
13	190	332991	128	323	0	1
13	190	332991	256	323	0	1
13	190	332991	511	323	0	1
13	190	332991	0	323	0	1
13	211	332991	0	323	0	1
13	211	332991	128	323	0	1
13	211	332991	256	323	0	1
13	211	332991	511	323	0	1
13	232	332991	511	323	0	1

- 160Mbps decoder +2.5M array

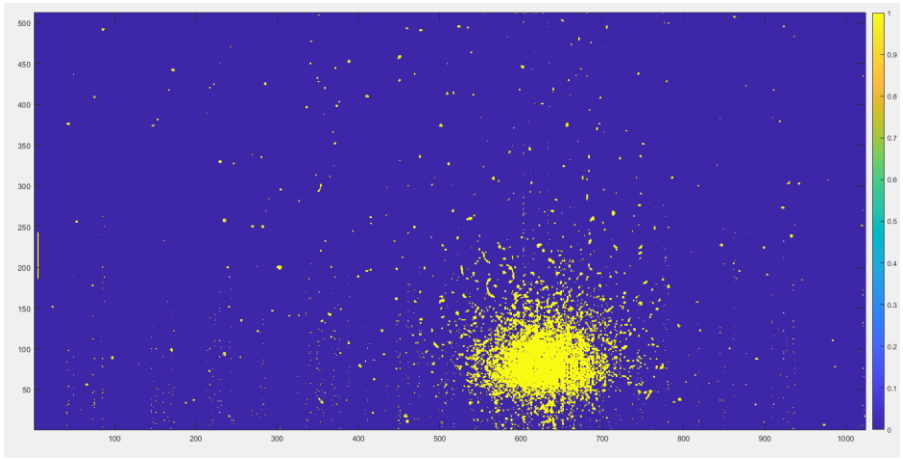
A	B	C	D	E	F	G	H
13	42	1009177	511	323	0	1	
13	42	1009177	0	323	0	1	
13	42	1009177	128	323	0	1	
13	42	1009177	256	323	0	1	
13	63	1009177	256	323	0	1	
11	186	1.68E+08	192	72	1	0	
10	171	1.85E+08	0	944	1	0	
13	63	1009177	511	323	0	1	
13	63	1009177	0	323	0	1	
13	63	1009177	128	323	0	1	
13	84	1009177	128	323	0	1	
13	84	1009177	256	323	0	1	
13	84	1009177	511	323	0	1	
13	84	1009177	0	323	0	1	
13	105	1009177	0	323	0	1	
13	105	1009177	128	323	0	1	
13	105	1009177	256	323	0	1	
11	186	1.68E+08	192	72	1	0	
10	171	1.85E+08	0	944	1	1	
13	105	1009177	511	323	0	1	
13	126	1009177	511	323	0	1	
13	126	1009177	0	323	0	1	
13	126	1009177	128	323	0	1	
13	126	1009177	256	323	0	1	
13	147	1009177	256	323	0	1	
13	147	1009177	511	323	0	1	
13	147	1009177	0	323	0	1	
13	147	1009177	128	323	0	1	
13	168	1009177	128	323	0	1	
11	186	1.68E+08	192	72	1	0	
10	171	1.85E+08	0	944	2	0	
13	168	1009177	256	323	0	1	

- 320Mbps decoder +2.5M array

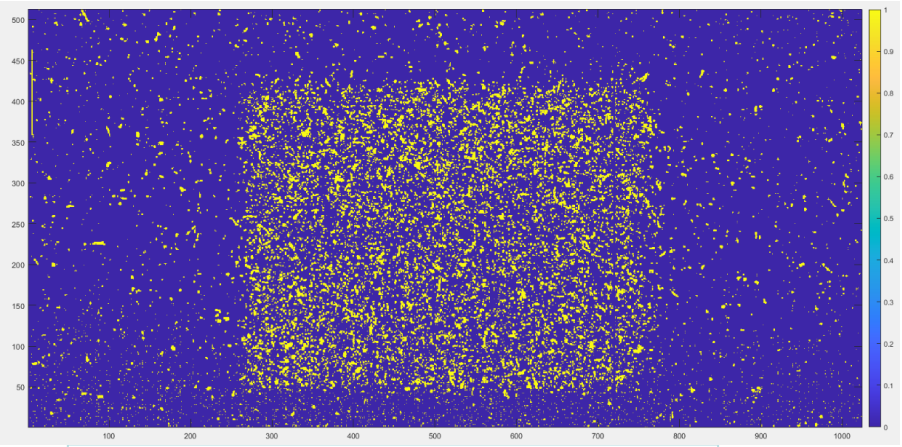
Hitmap



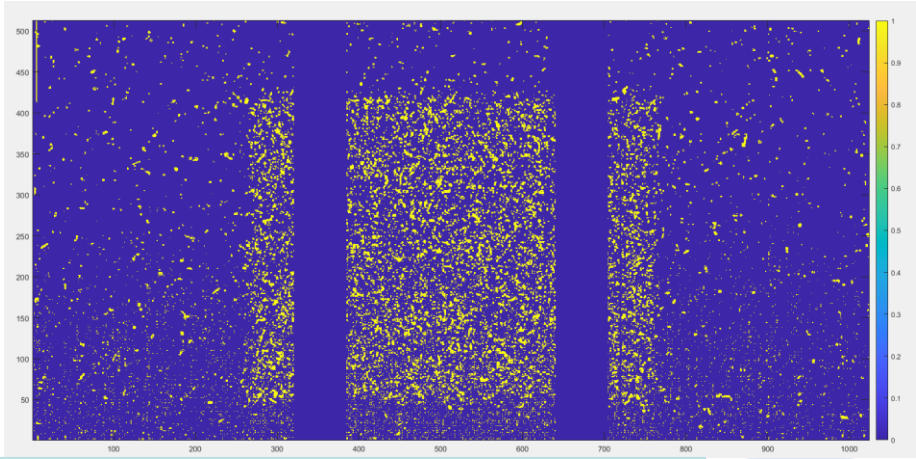
- 640Mbps decoder +2.5M array, no obvious data loss for 1 hours



- 640Mbps decoder +5M array, no obvious data loss for 3 hours with small beta source



- 320Mbps decoder +2.5M array, no obvious data loss for 5 hours



- 640Mbps decoder +5M array, obvious data loss when replace to big beta source.

Data rate calculation

Ser_OUT	Array	Ts_FPGA	Hits	Period	time	Average
160	2.5	21	1955	400ns*21*64=537.6us	537.6	3.636532738
160	20	1646	1232	50ns*64*1646=5267.2us	5267.2	0.233900365
80	20	280	383	50ns*64*280=896us	896	0.427455357
320	2.5	16	1882	400ns*64*16=409.6us	409.6	4.594726563
640	5	37	1755	200ns*64*37=473.6us	473.6	3.705658784

Thanks for your attention!