Progress of Silicon Pixel Detector

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CEPC detector reference TDR tracker meeting 2 Feb 2024

Introduction

- CEPC requires a high-resolution and low-material tracking system
- Large area of silicon!
 - > 70 m² for baseline design: Silicon + TPC
 - ~ 140 m² for Full Silicon Tracker
- CMOS is the promising technology for cost effectiveness and performance





CMOS Tracker Collaborators

Australia

• University of Adelaide

China

- Harbin Institute of Technology
- Hunan University
- Institute of High Energy Physics, CAS
- Northwestern Polytechnical University
- Shandong University
- T. D. Lee Institute Shanghai Jiao Tong University
- University of Science and Technology of China
- University of South China
- Zhejiang University

Germany

• Karlsruhe Institute für Technologie

Italy

- INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
- INFN Sezione die Pisa e Università di Pisa
- INFN Sezione di Torino e Università degli Studi di Torino
- UK UK
 - Lancaster University
 - Queen Mary University of London
 - STFC Daresbury Laboratory
 - STFC Rutherford Appleton Laboratory
 - University of Bristol
 - University of Edinburg
 - University of Liverpool
 - University of Oxford
 - University of Sheffield
 - University of Warwick

HVCMOS sensors

- HVCMOS sensors features large charge collection electrode encapsulating pixel electronics
- Achieving HV bias (> 50 V) without process modification
 => Cost-effective solution for large area detectors
- Intrinsic radiation hardness
 - Verified by radiation tests up to $10^{15} n_{eq}/cm^2$
- Large capacitance due to the large electrode
 - Causing increased noise and power consumption



A sensor candidate: ATLASPix3

- ATLASPix3 features
 - TSI 180nm HV process on 200 Ωcm substrate
 - Pixel size $50 \times 150 \ \mu m^2$
 - 132 columns \times 372 rows (20.2 \times 21 mm² chip)
 - Each pixel has 7-bit TOT + 10-bit timestamp
 - Continuous / triggered readout with 8b10b / 64b66b coding
 - Power consumption ~160 mW/cm².
- NB: TSI stops service for HEP recently, so impossible to use the same technology for production





Time-Over-Threshold: proxy of signal amplitude



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Readout system

- GEneric Configuration and COntrol System
 - Versatile system for different applications designed at KIT
 - LFP-FMC connection to Nexys FPGA, PCIe x16 to DUT, allows extensive tests
 - Configurations: Single-board; Telescope; Quad



ATLASPix3 tests

- IV scan confirms sensor electrical characteristics: breakdown up to 60V
- The 3-bit TDAC in pixel allows tuning threshold for each pixel to gain homogenous response across sensor array (Trimming)
- ToT: a measure of deposited energy; calibration needed due to non-linearity





Sigma: 66.31 mV -> 12.17 mV

Noise ~60 e-For threshold ~1700 e-



Quad module

- Readout unit based on 4 ATLASPix3 chips with common power and data readout
- Flex designed, assembled and tested by INFN Milan
 - Shared service by common power connections and configuration lines
- Readout using GECCO system with dedicated adapter card and data flex









Test setup with GECCO

Beam test

- Testbeam at DESY in April 2022 using electron beam up to 6 GeV
 - Two standalone telescope systems in interleaved configuration
 - Each equipped with 4 chips
 - Quad module located downstream

L.Meng @ VERTEX2022 R. Zanzottera, E. Hutchinson @Pixel2022



From quad to stave demonstrator

- A stavelet demonstrator with 12 quad modules under development
 - Aggregation of data + optical conversion at end-of-stave; serial powering
 - Foreseen to be populated with ATLASPIX3



Mechanical design



Development in small feature size HVCMOS

- HLMC 55nm HVCMOS process
 - Cancelled MPW plan in 2022
- SMIC 55nm Low-Leakage process
 - Not HV, yet with a similar deep n-well structure
 - MPW submitted in Oct 2022 in normal wafer
 - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
 - HVCMOS process, with $1k\Omega \cdot cm$ wafer
 - MPW submitted in Aug 2023
 - COFFEE2 received in Dec 2023



COFFEE1 laser test

- Ten pixel diode connected and a common output is read by an external ASIC (IDE1140)
- Red laser with beam spot ~0.5mm shines on top through opening above the sensor diodes
- Small yet clear signal response to laser







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COFFEE2: MPW in HVCMOS process

MPW with SMIC HV 55nm

- High-res wafer of 1k or 2k Ω cm available
- Real validation of the sensor!
- 4mm * 3mm in area
- Passive arrays similar as COFFEE1
- Two pixel arrays with in-pixel amplifier and more digital design
- Submitted in Aug 2023
- Received in Dec 2024
- Test started

Cross-section of pixel strucure



COFFEE2 floorplan

COFFEE2 photo





First test results

- Breakdown voltage up to 70V
- Capacitance (with offset subtracted) scales with sensor area

CV 1I, feq:

10kHz

100kHz

IMHz

50

60

70

- More tests to come
- Further development on this process will be planned
 - Funding of 2 potential MPW secured

Capacitance [fF] CV_10, feq: 340 10kHz 320 F 100kHz 300 IMHz 800 E 280 700 E 260 F 600 E 240 500 E 30 40 0 10 20 0 20 30 40 50 60 70 10 Reverse Voltage [V] Reverse Voltage [V] CV of 8-pixel connected CV of a single pixel C(8) = 8*C0 + offset?C(1) = 1 C + offset?

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dC(8)/dV = 8* dC(1)/dV !

Summary

- R&D carried out with ATLASPix3, sensor chip in TSI 180nm process
 - Chip tested extensively
 - Module design and prototype exists
 - Mechanical design started
- Sensor R&D on advanced 55nm process is promising
 - Initial MPW proved it feasible to serve as sensor
 - More development needed in the next ~3 years towards a full-functioning chip