Status of PID software

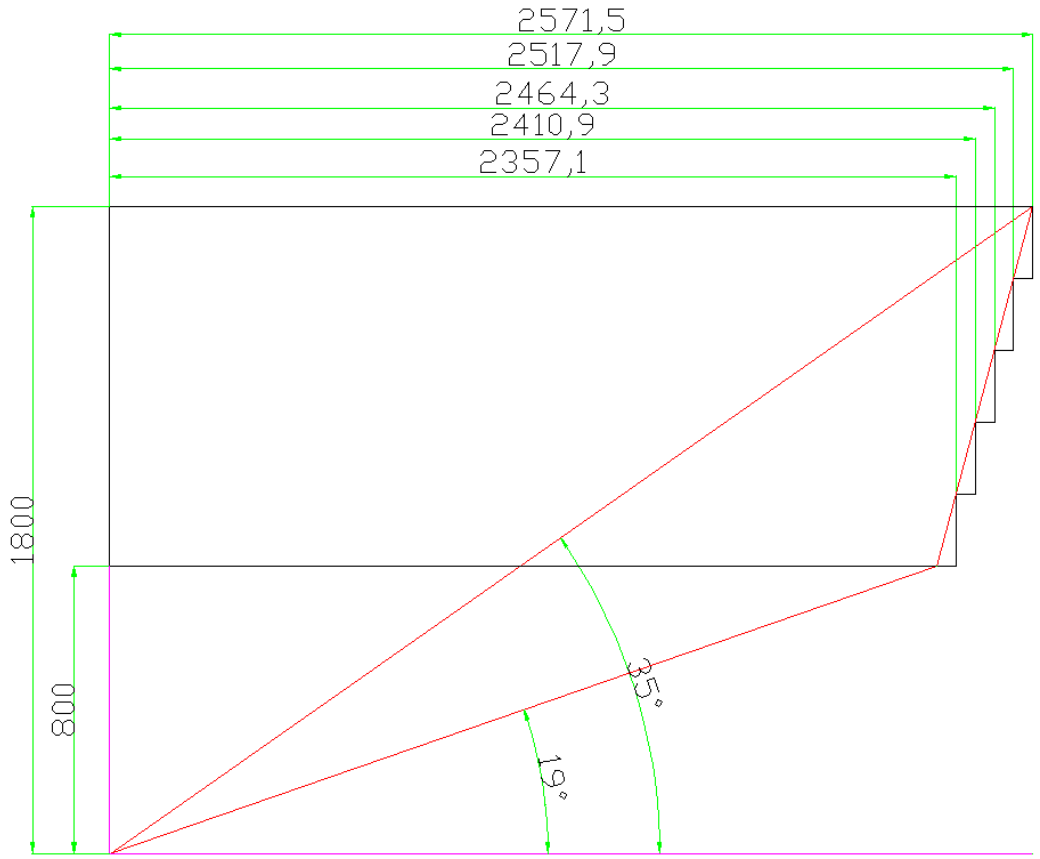
Guang Zhao

zhaog@ihep.ac.cn

Preliminary DC design

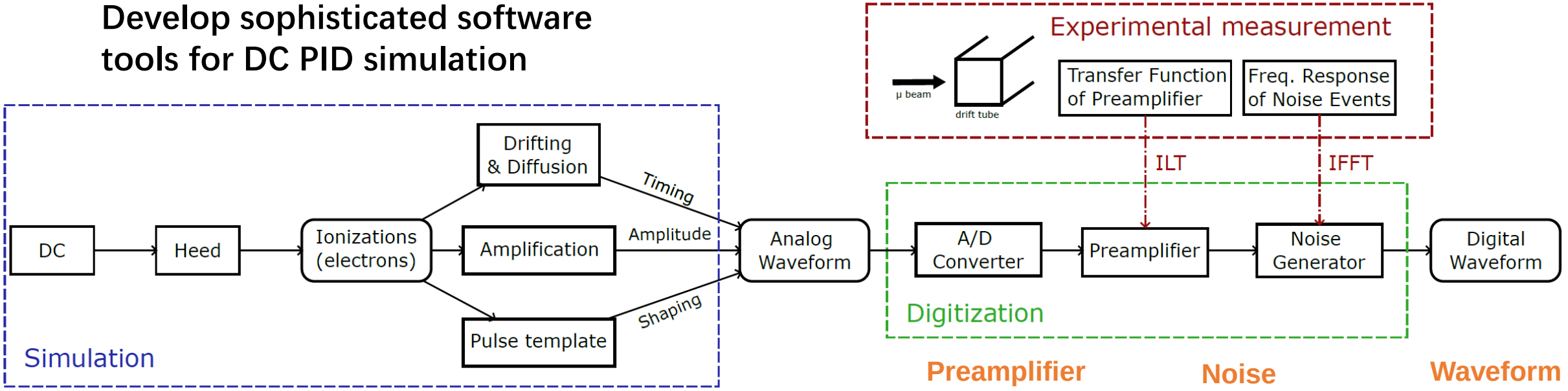
Optimized DC Parameters

DC Parameters	
Radius extension	800-1800 mm
Length of outermost wires （cosθ=0.82）	5143 mm
Thickness of inner CF cylinder	200 μm
Outer CF frame structure	Equivalent CF thickness: 1.63 mm
Thickness of end Al plate	35 mm
Cell size	18 mm × 18 mm
# of cells	24766
Ratio of field wires to sense wires	3:1
Gas mixture	He/iC_4H_{10}=90:10

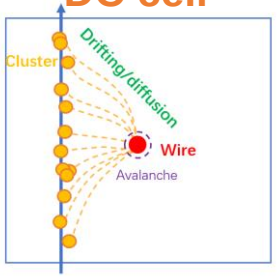


Waveform-based simulation

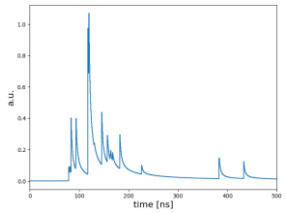
Develop sophisticated software tools for DC PID simulation



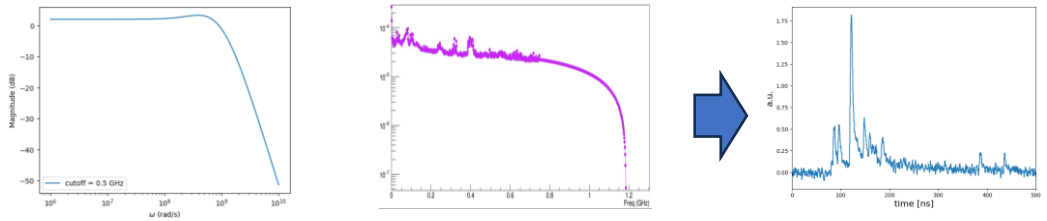
DC cell



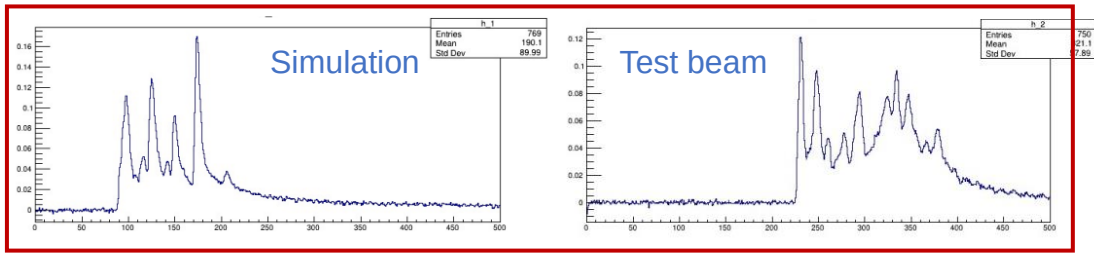
Induced signal



Preamplifier **Noise** **Waveform**

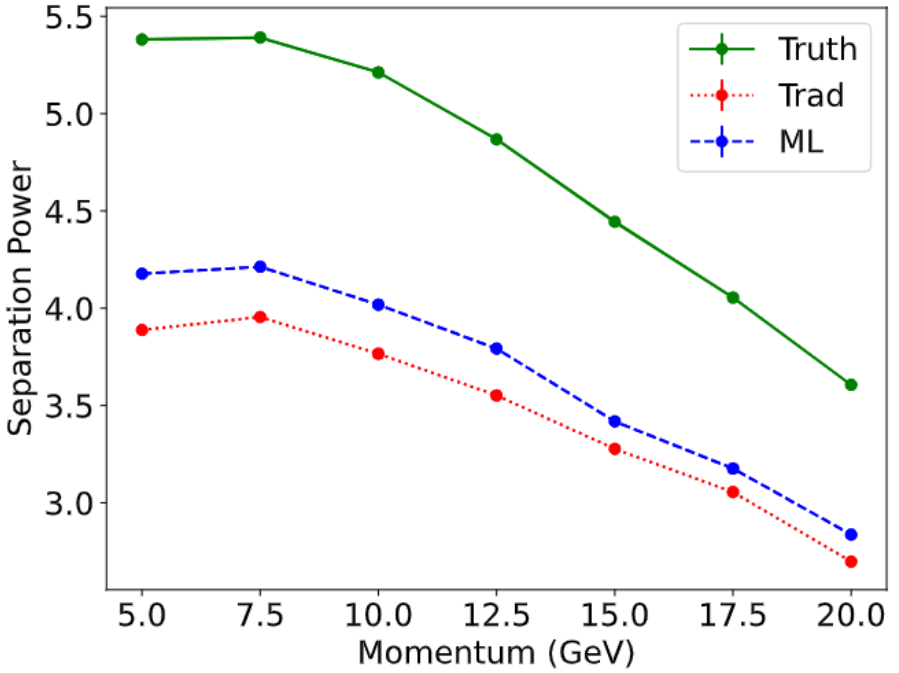


Tuned MC is comparable to data



Reconstruction and PID performance

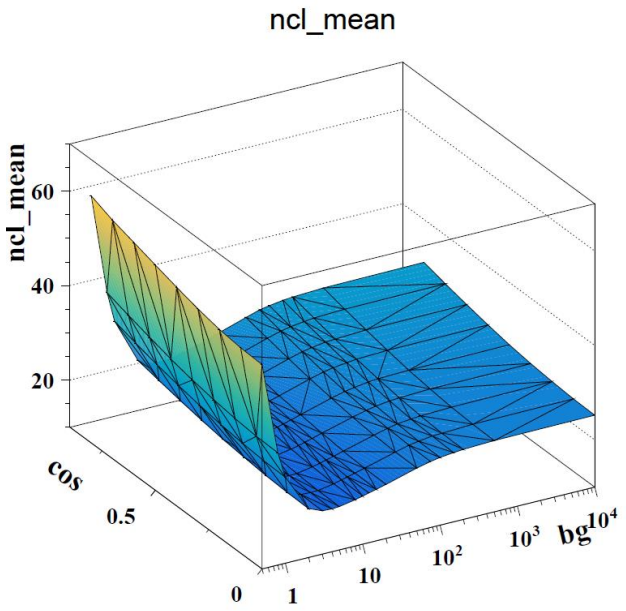
- **Traditional algorithm**
  - Derivative-based peak finding
  - Peak merging clusterization
- **ML algorithm (supervised, MC)**
  - LSTM-based peak finding
  - DGCNN-based clusterization
- **ML algorithm (semi-supervised, data)**
  - Domain adaptation

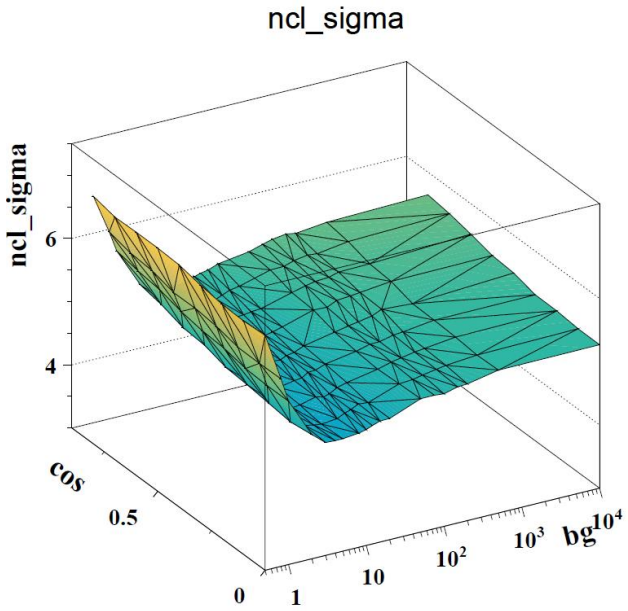


- **For 1m track, close to 3σ K/π separation @ 20 GeV/c**
- **~10% improvement with ML (equivalent to a detector with 20% larger radius)**

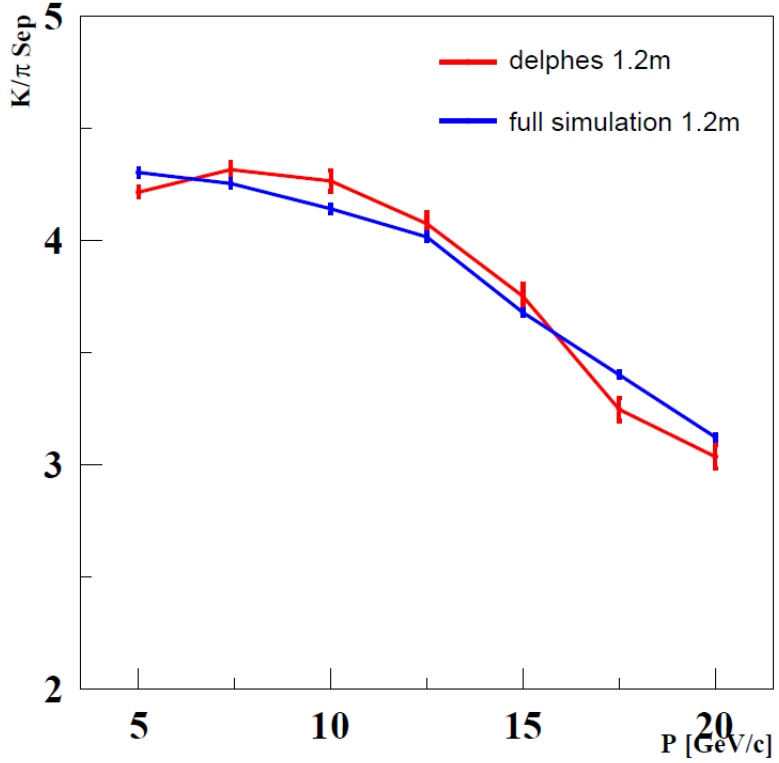
Track-level parameterization interface

- Input: βγ and cosθ
- Output: Track-level dN/dx and ToF



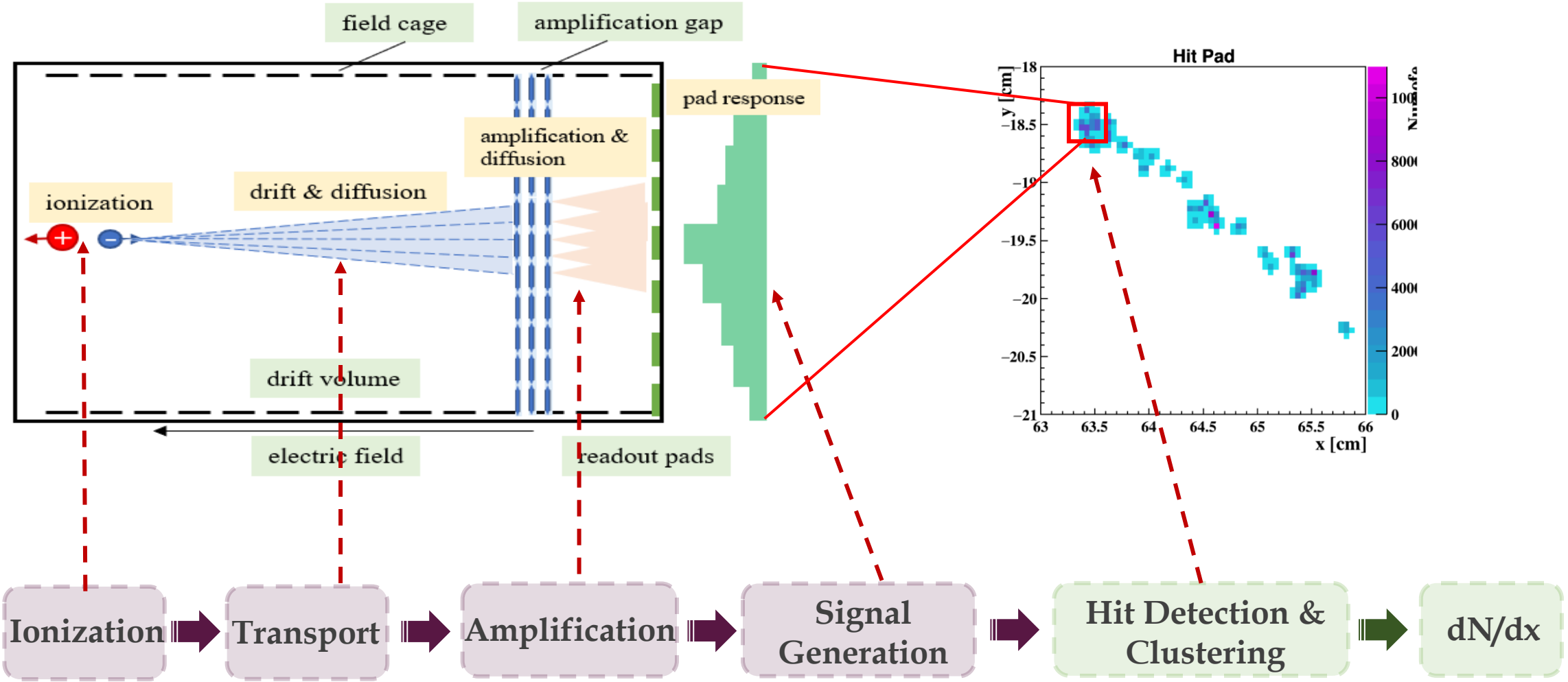


K/π separation power

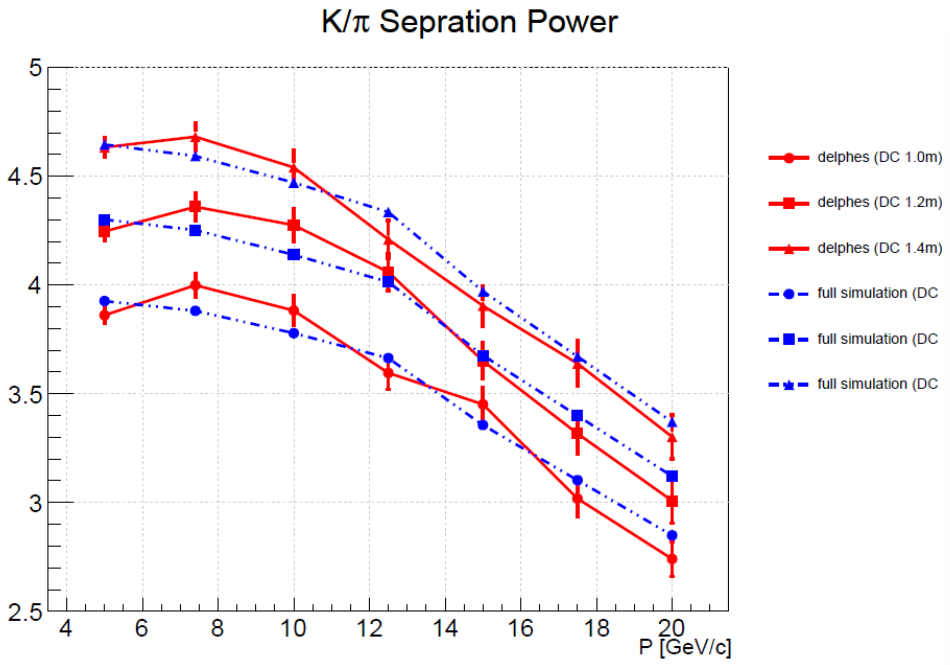


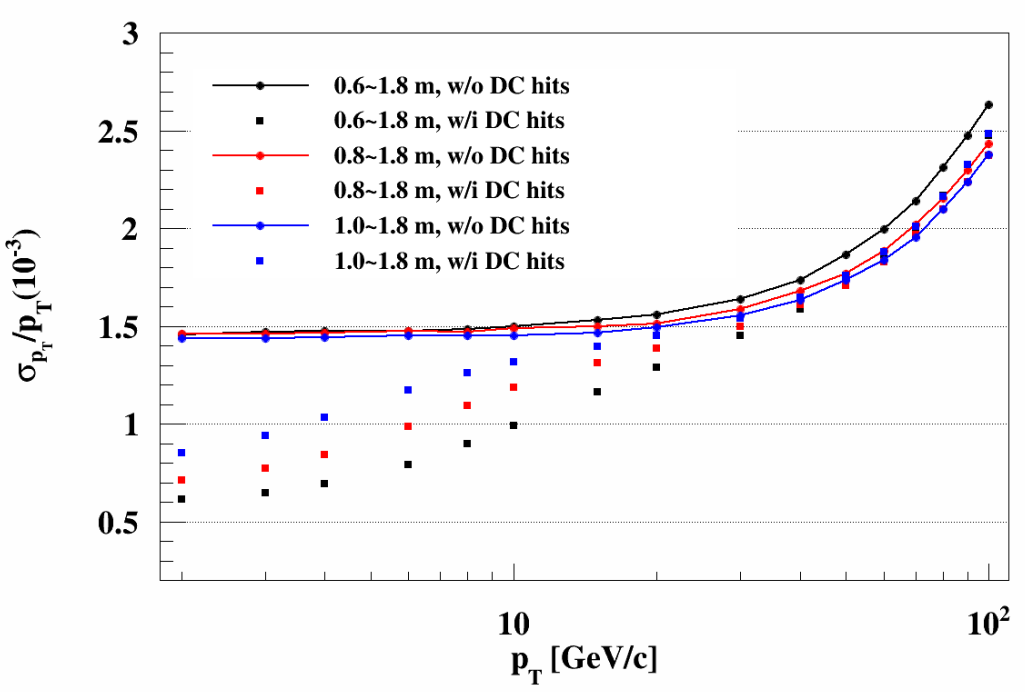
Good consistent to full simulation

TPC software



Towards TDR





PID software is ready for layout optimization

Smaller inner radius is

- better for PID ➔ From 2.8σ to 3.1σ even 3.3σ @ 20 GeV/c
- better for tracking resolution
- more engineering challenges and more beam backgrounds

Towards TDR

- **Drift chamber:**
  - Fast simulation of dN/dx + ToF (1~2 month)
    - End-cap model implementation
  - Full simulation of dN/dx in CEPCSW
    - Track-level parameterization method (fast sim. model, 1 month)
    - Hit-level waveform-based method: digitization, reconstruction (optional, ~3 months)
- **Time projection chamber:**
  - Fast simulation of dN/dx and its implementation in CEPCSW (~3 months)
    - Digitization and reconstruction
    - Track-level parameterization