

Update on the CMOS tracker

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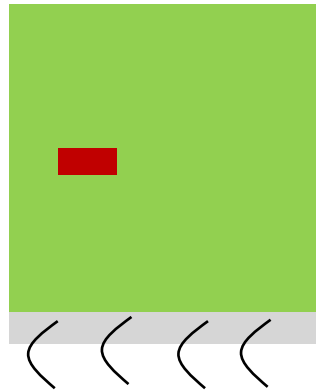
On behalf of CMOS tracker group

CEPC detector reference TDR tracker meeting

8 Mar 2024

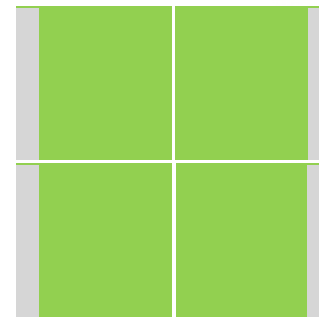
Module concept for ATLASPix3

- Quad module to form stave
 - Note: 2mm gap between 2 neighbouring modules

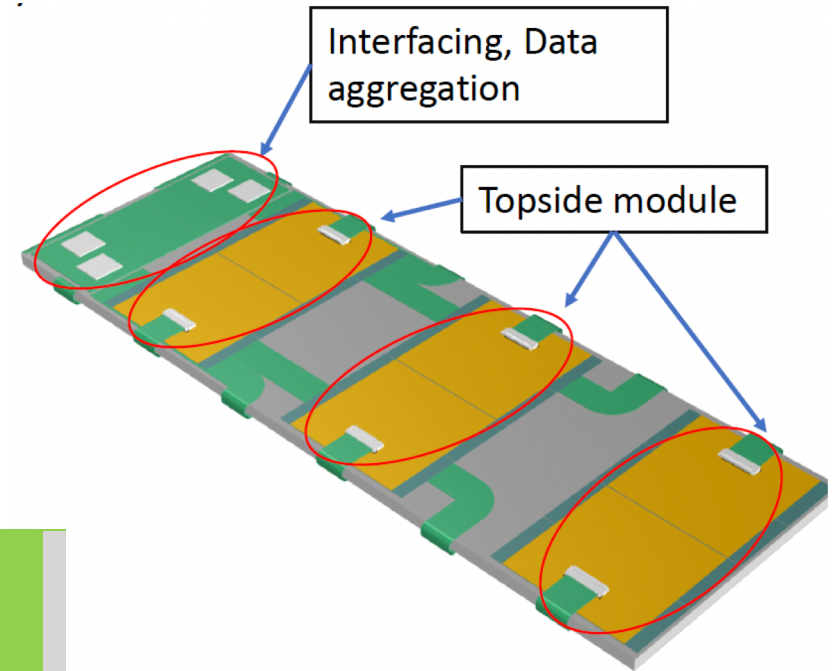


ATLASPix3

- Chip size: 20mm * 21mm
- Sensitive area: 20mm * 19mm
- Pixel size: 50 um * 150 um



Quad



Stave

Towards COFFEE in 55nm process

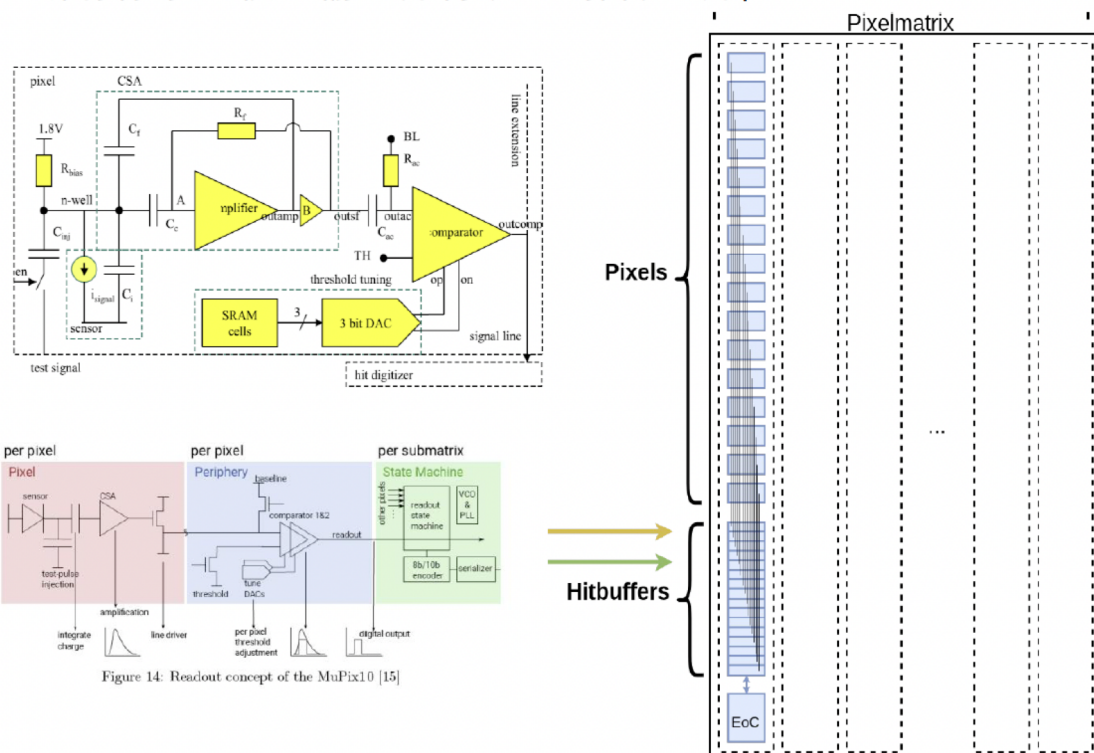
Driving R&D goal: 5-10 ns timing resolution

性能需求	CEPC径迹探测器	LHCb UT升级
像素大小	10 um 以内空间分辨率 => 25 um × 150 um	< ~50 um × 150 um
时间分辨率	< ~10 ns @ Z pole	25ns bunch tagging => < ~ 5 ns
功耗	可使用液冷, 但越低越好 => < ~ 150 mW/cm ²	可使用液冷, 但越低越好 => < ~ 150 mW/cm ²
抗辐照性能	Tbd	3×10^{15} n _{eq} /cm ² , 240 MRad TID
读出速度	Tbd	9 Gb/s, 与 IpGBT 等 common electronics兼容

Discussion on readout scheme



所有像素比较器输出并行读出到阵列底部



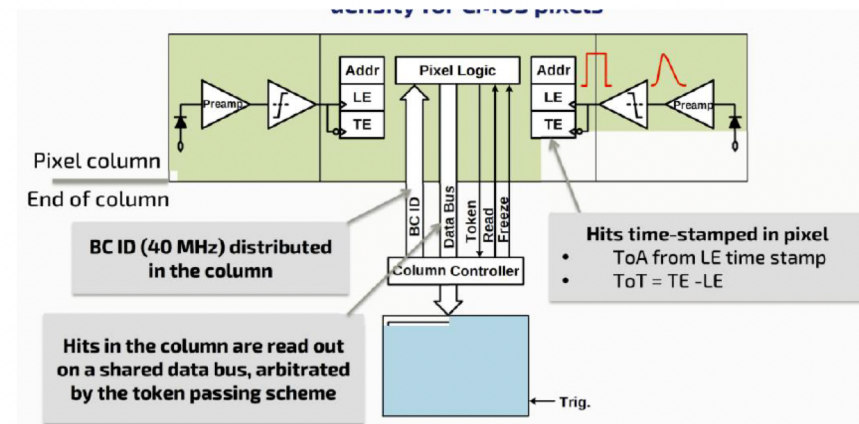
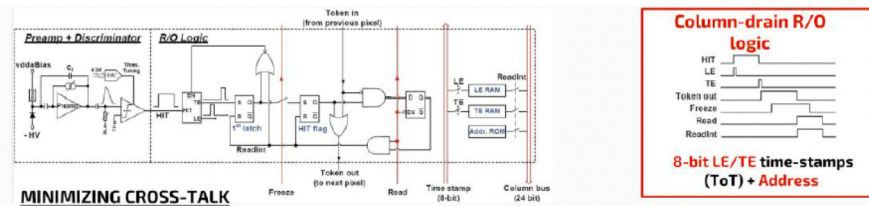
ATLASPIX3, MightyPix, MuPix

减小了数字模块对sensor的串扰，需要优化布线以减小长数据总线之间的cross-talk，需要大量的布线资源，ATLASPIX3有近5万条1.8cm的纵向数据线



Yang Zhou

列总线优先级读出：Column-drain readout



RD50-MPW3, Monopix-LF、TimePix, FE-I3

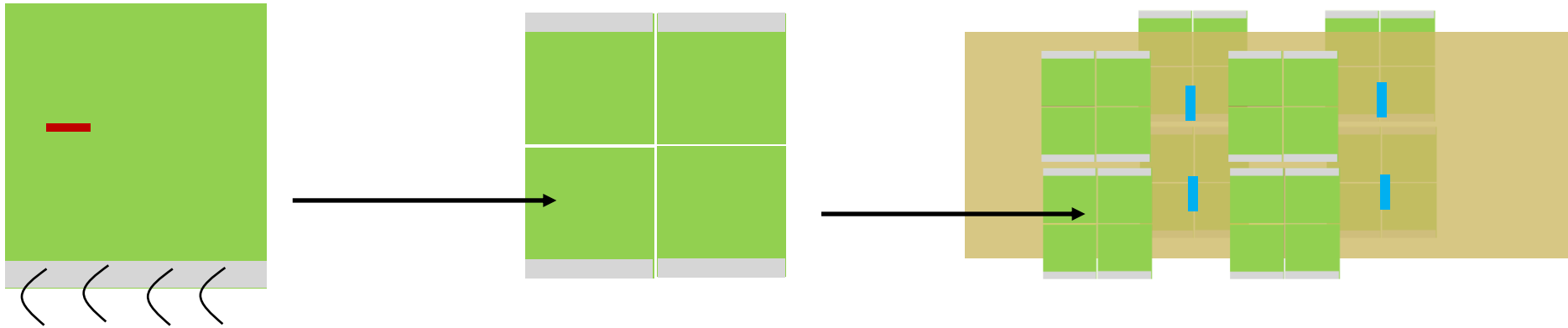
LF工艺（有deep Pwell），谨慎的版图设计以应对数字模块对sensor的串扰；

TimePix和FE-I3非单片型芯片，不存在以上问题

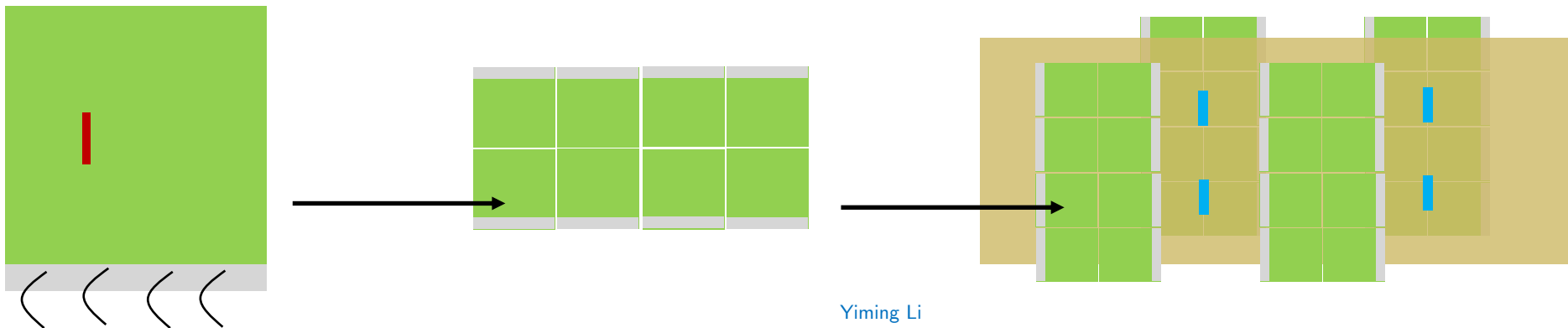
Module concept based on future COFFEE?

Key geometrical size:

- Chip size: 20mm * 21mm (similar as APX)
- Pixel size: 25 um * 150 um (point resolution in one direction at least <10um)
- Insensitive area: <~ 20mm * 2mm



2*quad
A la ATLASPix
- NB: gaps!

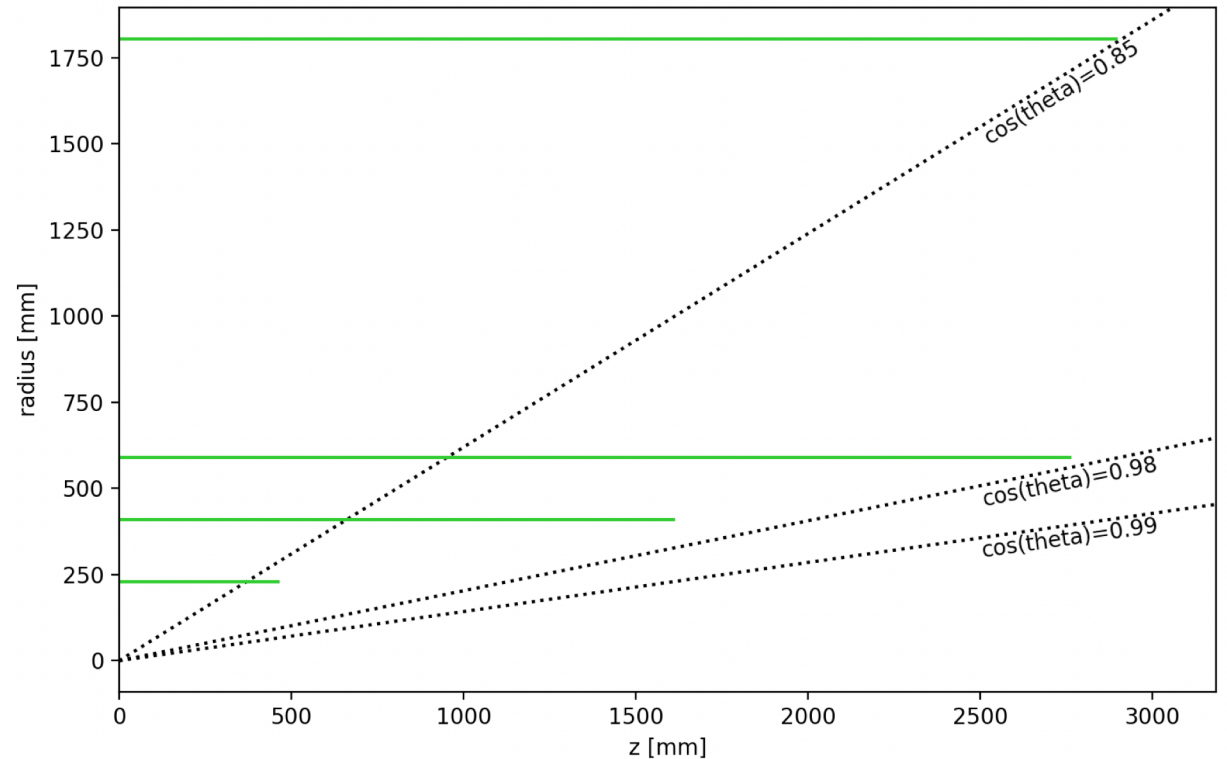


8 chip module
w/o gap, with
flexibility
- But hard for
chip design

An initial layout for CMOS-based barrel

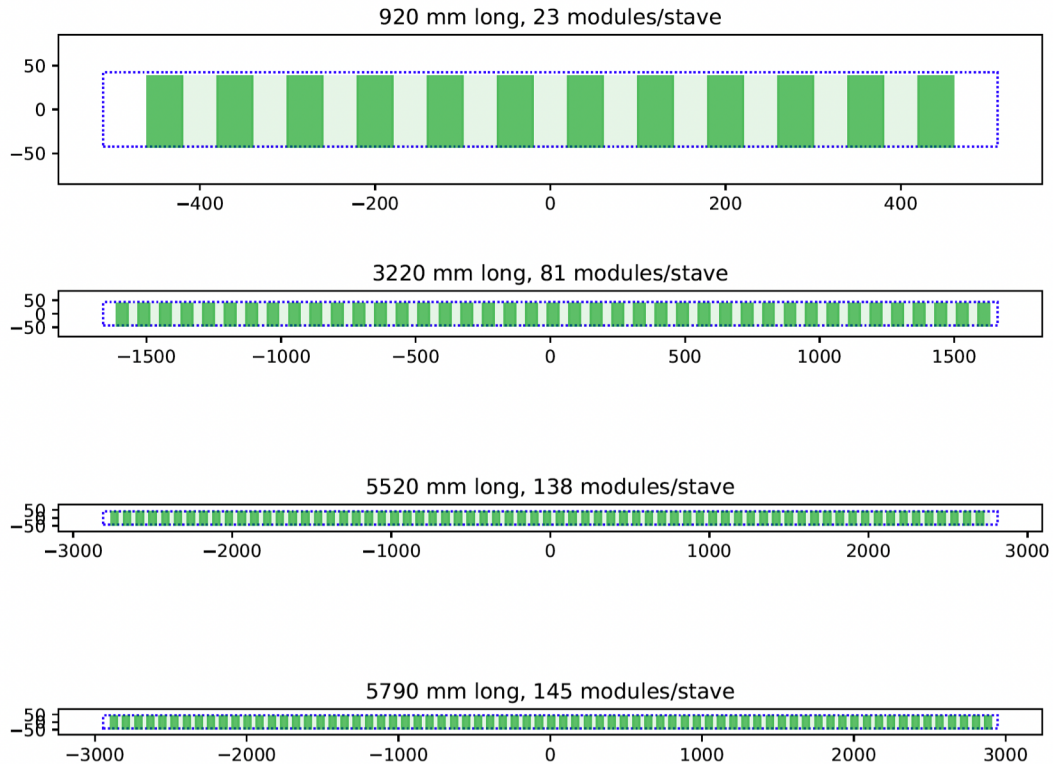
- Parameters from Quan's mechanical plot v0
- Many thanks for discussion with Chengdong, Jinyu, Gang ...
- Serves as a starting point for optimization
- No estimation of readout yet (hit density info to come)

Input parameters



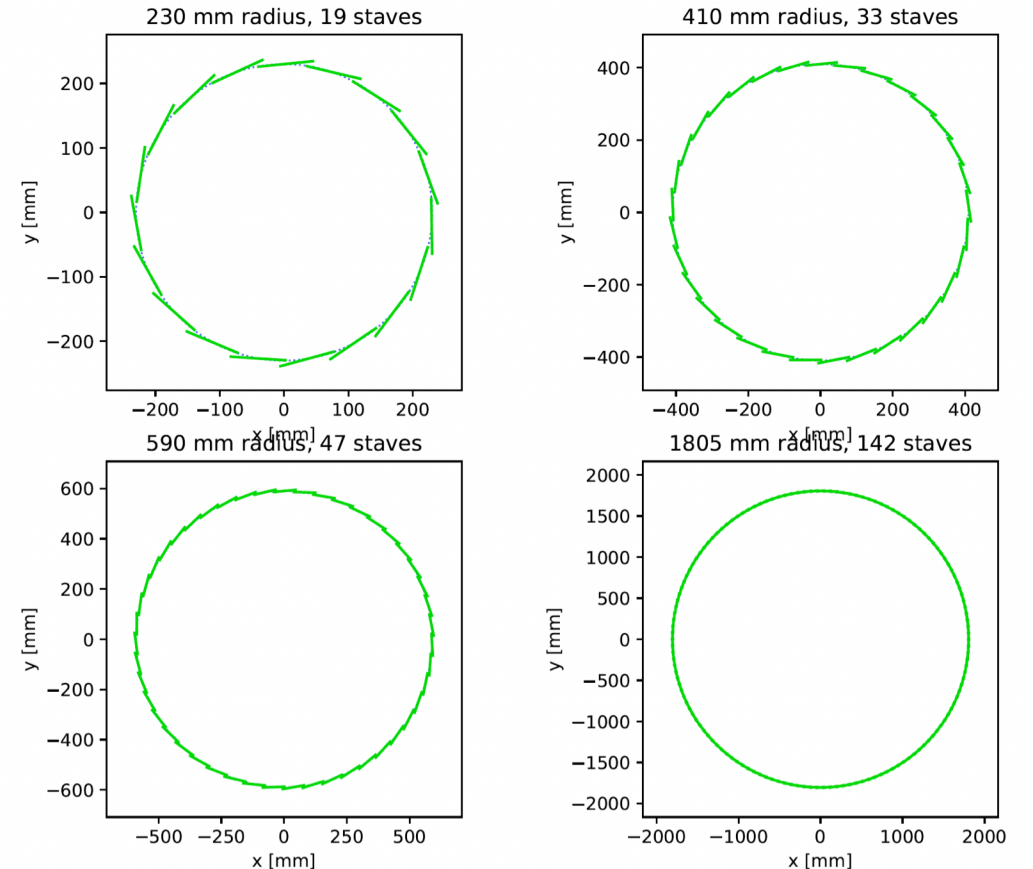
An initial layout for CMOS-based barrel

99 staves, 9596 modules for 3 inner layers



Each box is a 2*4-chip module

241 staves, 30186 modules for all 4 layers



- Staves tilted by an angle to ensure charge sharing of incident track
 - 5.7deg assuming 25um pitch on 250um thick substrate

Plan and ongoing work

- ▣ Prepare sample for a quick estimation of hit density/ occupancy
- ▣ => data rate estimation (NB: inner and outer layers can differ largely)
- ▣ Supporting structure & cooling? => material budget
- ▣ And endcap!