

CEPC Silicon Strip Outer Tracker

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On behalf of the SDD Tracker Team

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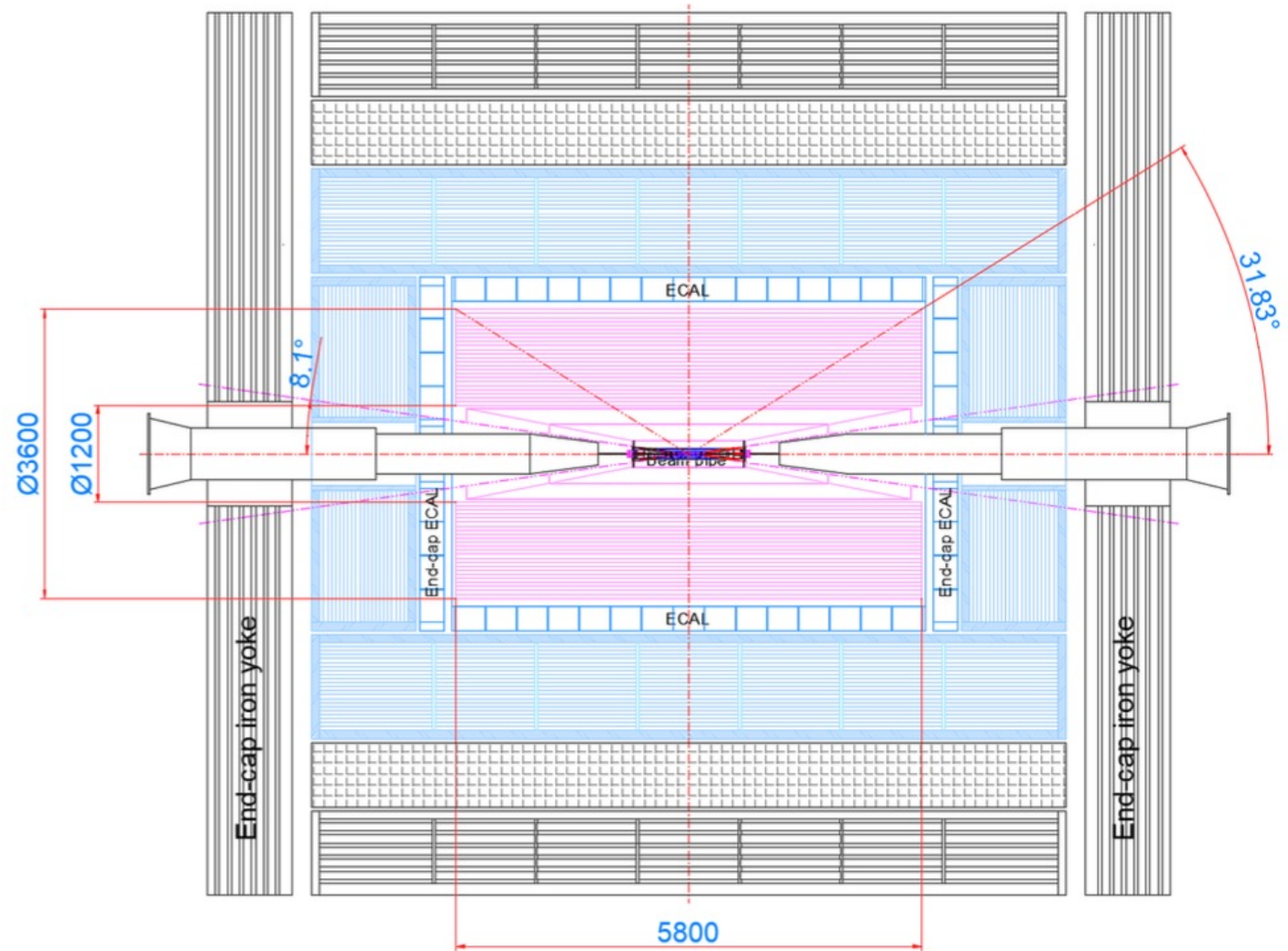
Tracker Design V0

$\text{Ø}1200 \text{ mm} = r 0.6 \text{ m}$

$\text{Ø}3600 \text{ mm} = r 1.8 \text{ m}$

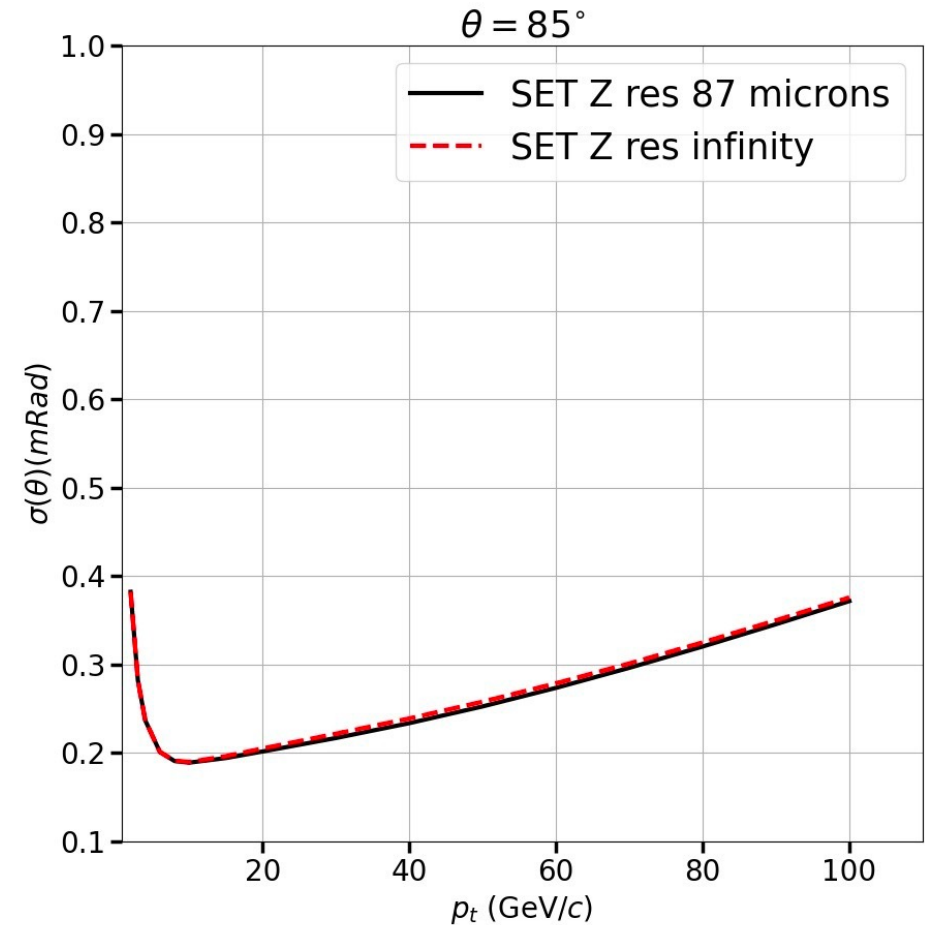
长度: 5800 mm (arccos0.85)

Silicon Tracker : 三层



Layer: Single or Double?

- Single or double layer influence the Z resolution, which may influence physics performance
- Shown that Z res concerns little about theta res and pz res
- When theta = 85 degree, it shows no difference in theta res though Z res changes.
- **Single layer is acceptable**

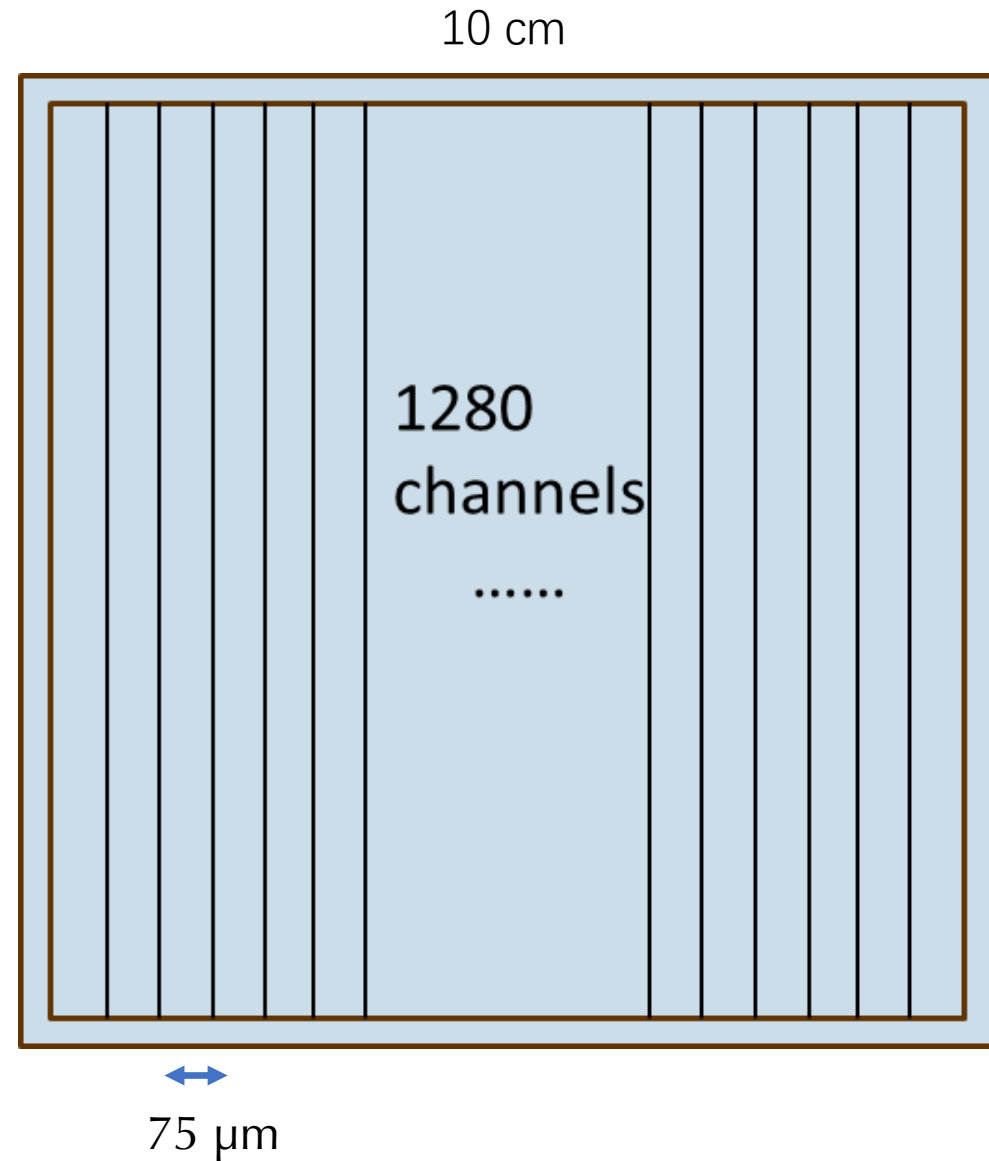


Gang Li

SET Module

- Strip length 10cm
- Strip pitch 75 μ m
 - hard to wire-bonding with 50 μ m
- 1280 channels per module
 - Compatible with ASIC design

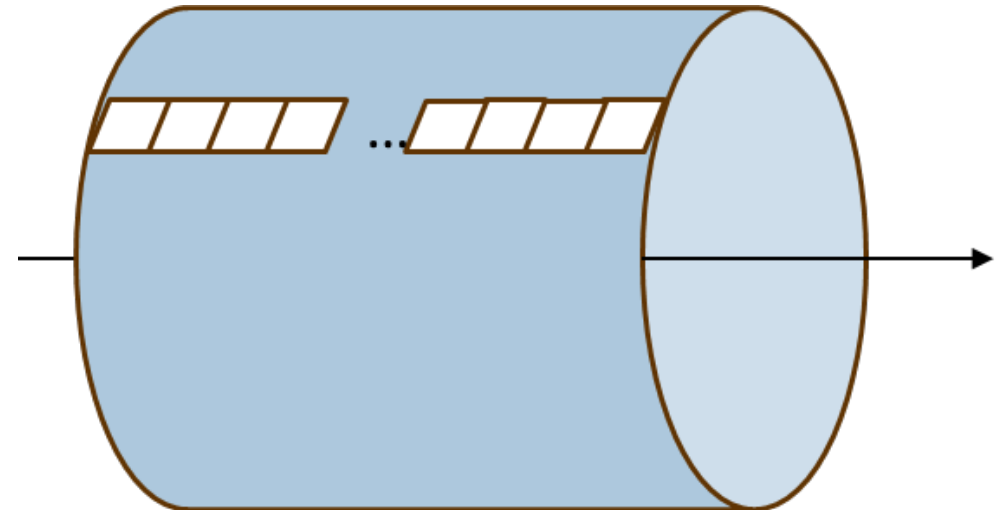
Single Module	
Area	10cm*10cm
Strip pitch	75 μ m
# channels	1280



Number of Modules

- Total length in z direction: 5.8 m
- Surface area: $\sim 66 \text{ m}^2$
- Number of modules: ~ 6610
- Number of channels:
 - $6610 \times 1280 = 8.4 \text{ M}$ channels

SET	
Radius	1811mm
+/- z	2904mm
Strip Length	$\sim 10\text{cm}$
Strip Pitch	75 μm



Next Steps

- Converge on the Front-end electronics design (Xiongbo)
- Simulation of HitMap with CEPCSW (Zhan)
- Mechanical design of stave structure (Jinyu)
- End-Cap ...