Data rate estimation for CMOS tracker

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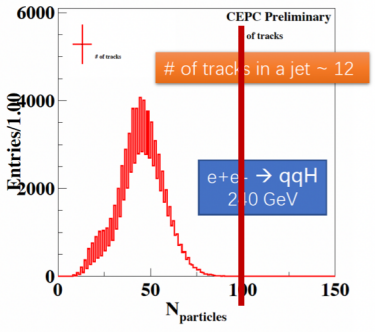
CEPC reference TDR tracker meeting
15 Mar 2024

Assumptions

- Event rate ?
- Geometric layout ?
- FE design ?

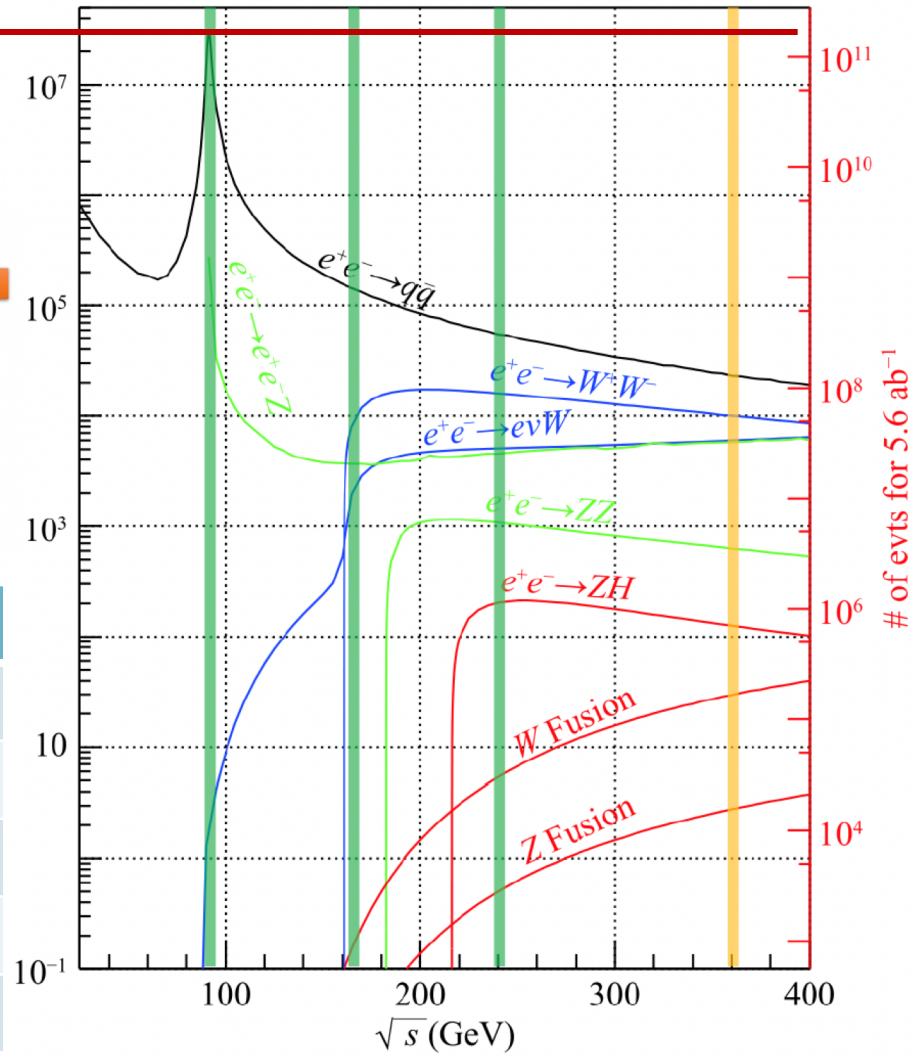
Assumption: Event rate

- Z pole: ee -> qqbar dominating.
  - $\sigma \sim 3\times10^7$ fb
  - ×2 to account for other physics + background
  - $f = \sigma \cdot \mathcal{L} =$ 115 kHz
  - Note: Beam bkg can be significant!
  - Will update when MDI input available
- Track multiplicity: 100 (conservative)
- Cluster size: 3



L[e34cm-2s-1]	H	Z	W	Ttbar
Sqrt(s)[GeV]	240	91	160	360
L@30MW	5	115	16	0.6
L@50MW	8.3	192	26.7	0.8
years	10	2	1	5
#bunches	268	11934	1297	

CEPC Acc. TDR



Gang LI

Geometrical layout

- Layout to be optimized!
- A starting point to give an idea
- Different from Mar 8 Tracker meeting:
  - Stave length shrunken
- Already we have hit rate density

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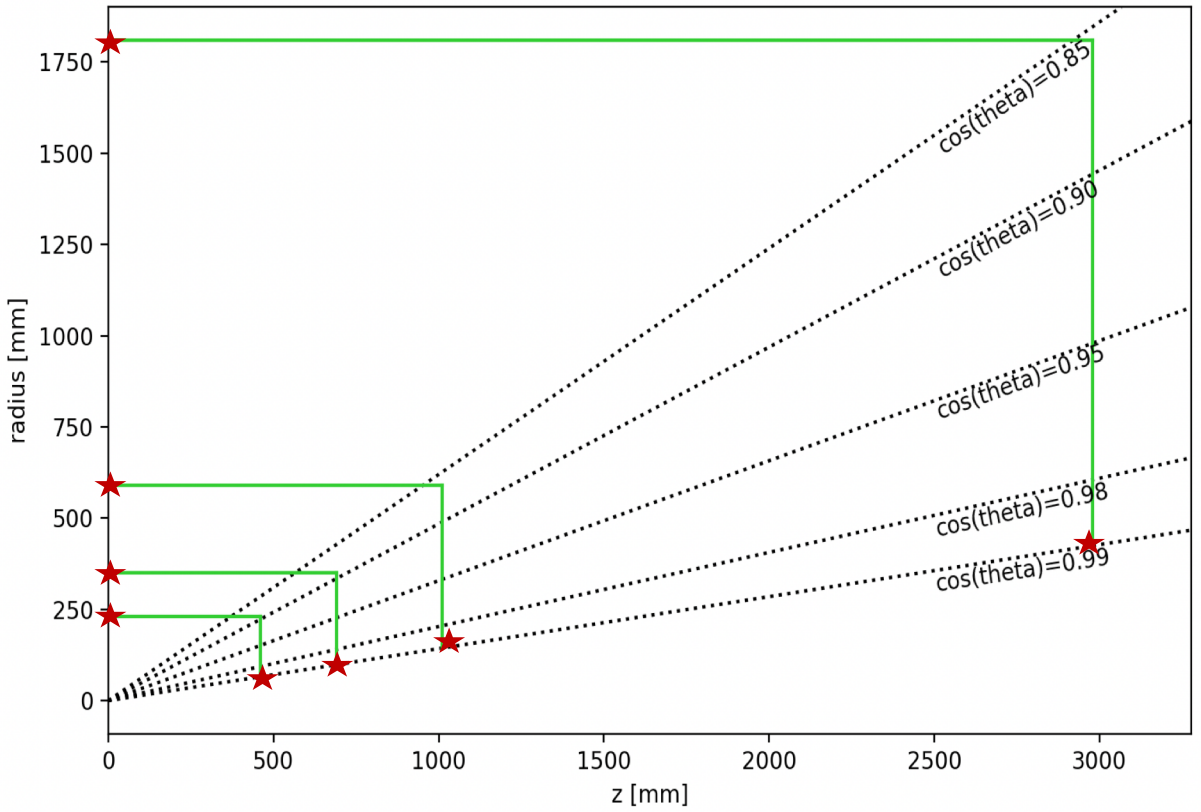
Assuming track multiplicity 100, cluster size 3.0
event rate: 115 kHz, total hits rate: 34.6 MHz
Assuming readout interval (RO) 10 us
Assuming 48 bits/hit
                                          |       Hits/cm2/s
  layer     |    r [cm]    |   Z/2 [cm]   |    barrel    |    endcap
    0       |      23      |      46      |   5.2e+03    |   1.3e+03
    1       |      35      |      69      |   2.2e+03    |   5.7e+02
    2       |      59      |     101      |   7.9e+02    |   2.6e+02
    3       |     181      |     298      |   8.4e+01    |   3.0e+01
```

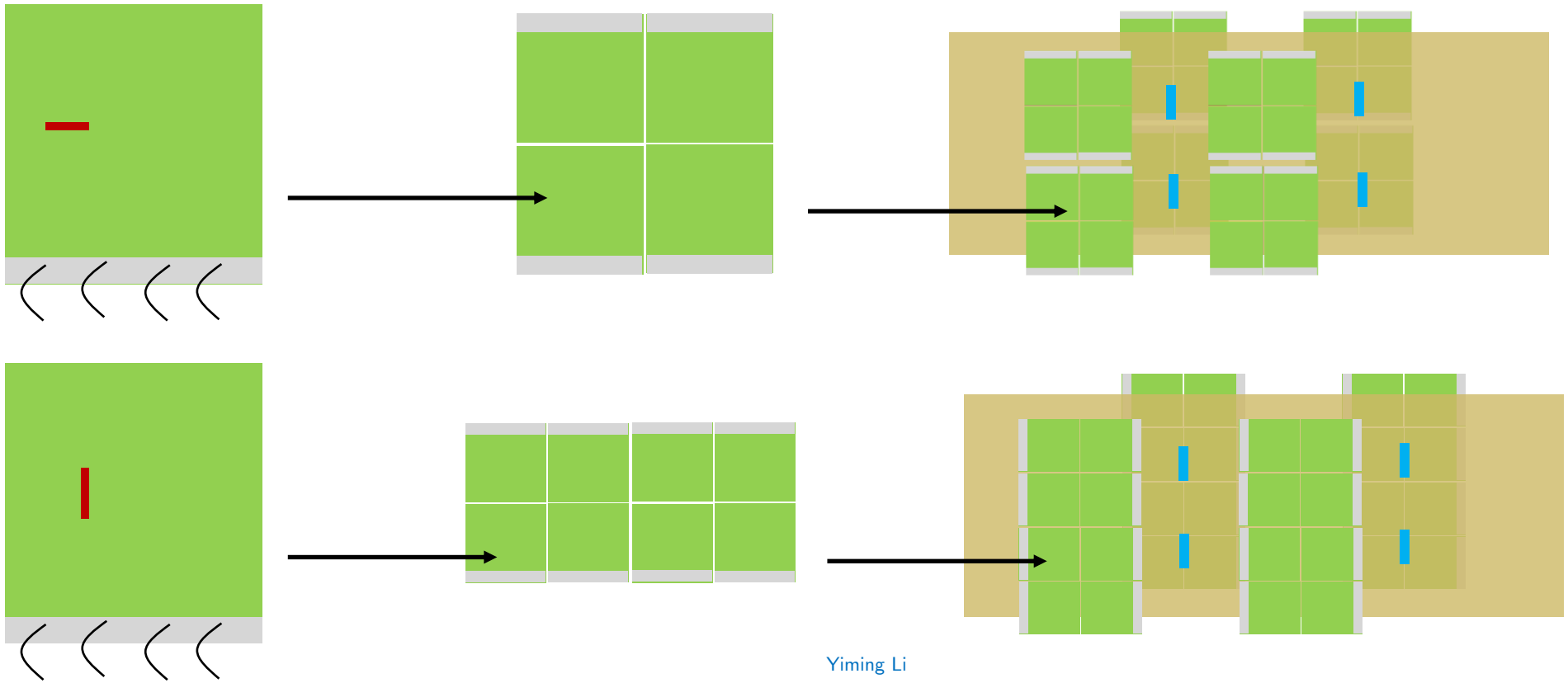


FE design

- Bits per hit?
- ATLASPix3 as reference
  - Hit-driven mode (triggerless): 8/10b encoding, up to 96 bit/hit, target link speed 1.6 Gbps
  - Triggered mode: 64/66b encoding, up to 128 bit/hit, target link speed 1.28 Gbps
- CEPC HVCMOS hit size?
  - 14b timestamp (may be reduced)
  - 10b + 8b address (25um * 150 um => 800 col * 134 row)
  - 1b parity
  - 10b TOT (may be reduced)
  - 48 bit/hit should be enough
- Readout scheme?

Module concept based on future COFFEE?

- Key geometrical size:
  - Chip size: 20mm * 21mm
  - Pixel size: 25 um * 150 um (point resolution in one direction at least <10um)
  - Insensitive area: <~ 20mm * 2mm
- Module consists of 8 chips



2*quad
A la ATLASPix
- NB: gaps!

8 chip module
w/o gap, with
flexibility
- But hard for
chip design

Data rate estimation

Key assumptions: Event rate 112kHz, track multiplicity 100, cluster size 3, bits per hit 48; Beam bkg to be added

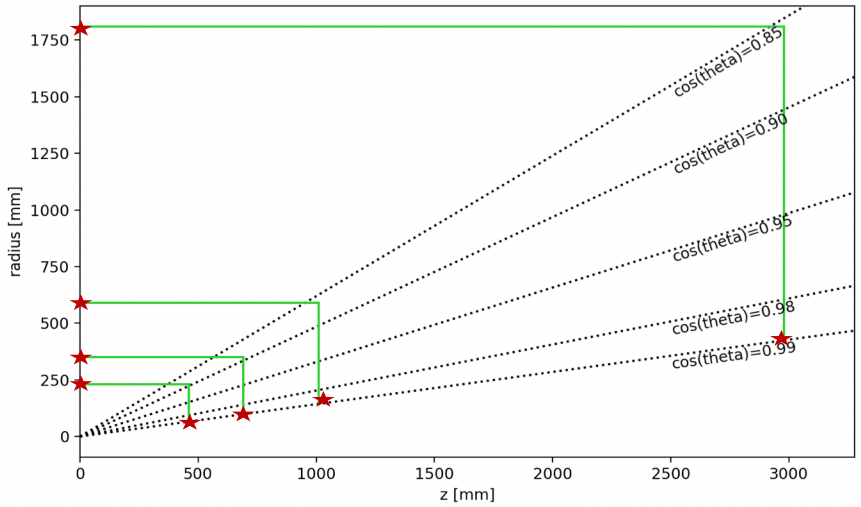
Layer	Hit density [kHz/cm^2]	Data rate /chip [Mbps]	Data rate / module [Mbps]	Data rate / layer [Gbps]
Barrel SIT 1	5.2	1.0	8.0	1.5
SIT 2	2.2	0.43	3.5	1.5
SIT 3	0.79	0.15	1.2	1.4
SET	0.08	0.02	0.13	1.4
Endcap SIT 1	1.3	0.24	2.0	0.17
SIT 2	0.57	0.11	0.87	0.17
SIT 3	0.26	0.05	0.41	0.22
SET	0.03	0.006	0.05	0.24

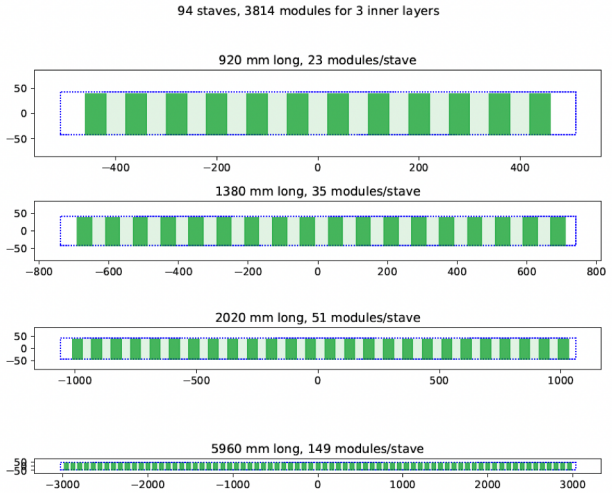
Total data rate: 6.6 Gbps for SIT+SET, or 5.0 Gbps for SIT only

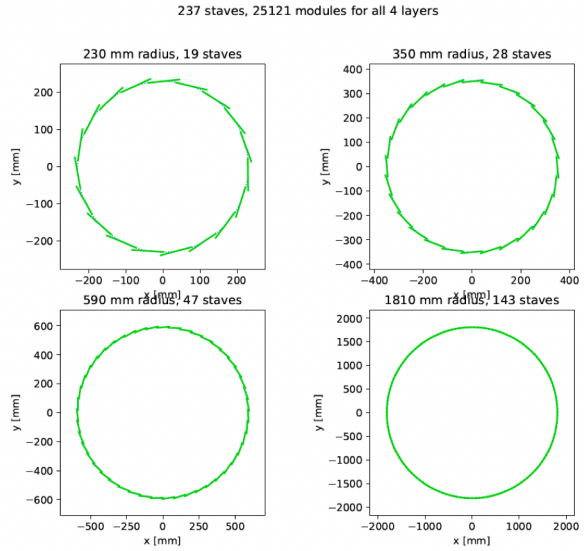
A possible layout and counts of modules - barrel

- Layout is being optimized, subject to change! Just to give a feeling of order of magnitude
  - 94 staves, 3814 modules for 3 inner layers; 237 staves, 25121 modules for all 4 layers

Layer	r [mm]	Z/2 [mm]	# staves	# modules
SIT 1	230	460	19	437
SIT 2	350	690	28	980
SIT 3	590	1010	47	2397
SET	1810	2980	143	21307





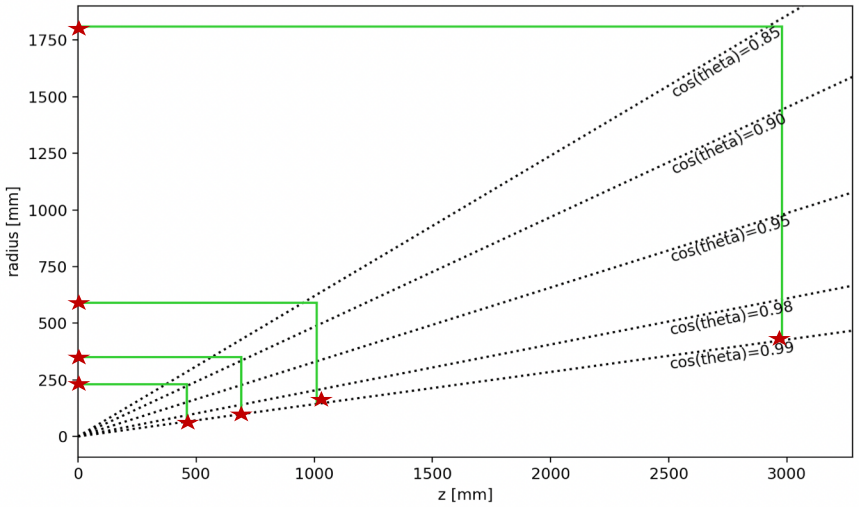


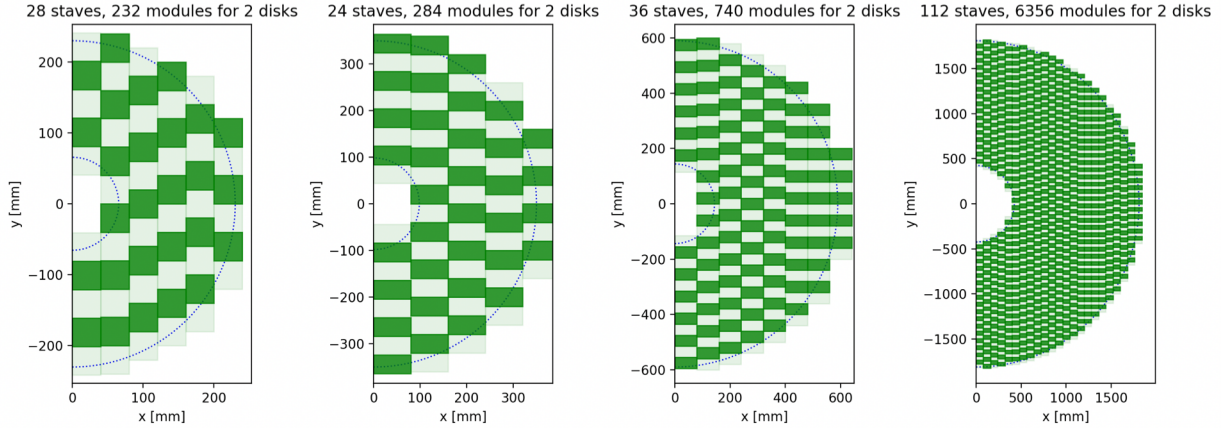
A possible layout and counts of modules - endcap

- Not the actual configuration but just to estimate a count for modules!
  - 88 staves, 1256 modules for 3 inner layers; 200 staves, 7612 modules for all 4 layers

Layer	r [mm]	Z/2 [mm]	# staves	# modules
SIT 1	230	460	28*	232*
SIT 2	350	690	24	284
SIT 3	590	1010	36	740
SET	1810	2980	112	6356

*4-chip modules

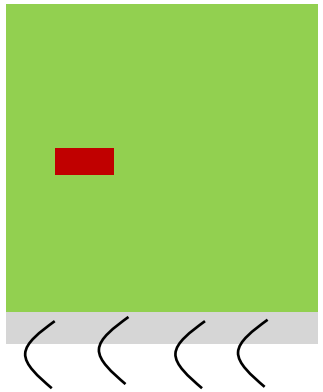




BACKUP

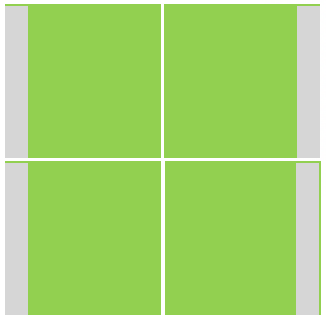
Module concept for ATLASPix3

- Quad module to form stave
  - Note: 2mm gap between 2 neighbouring modules

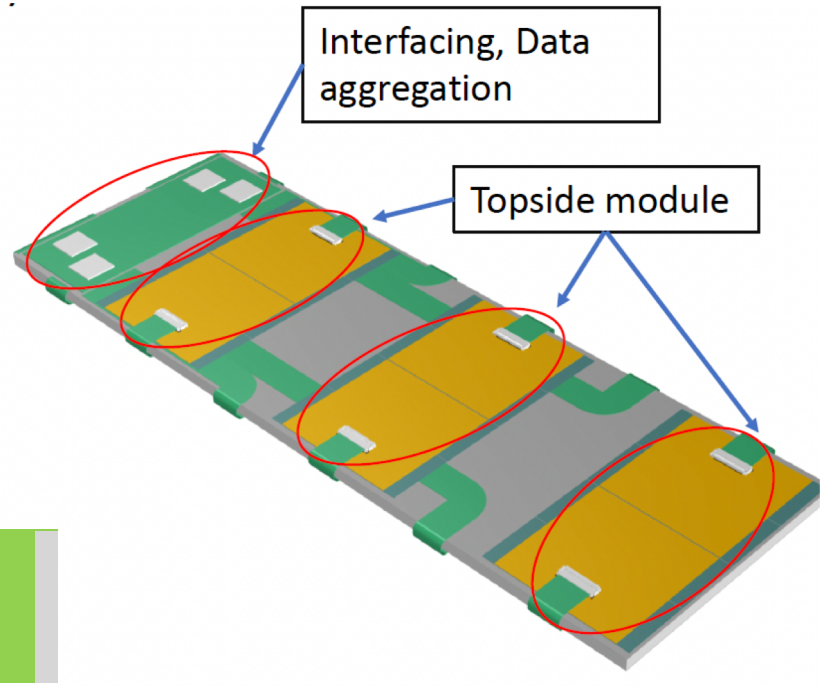


ATLASPix3

- Chip size: 20mm * 21mm
- Sensitive area: 20mm * 19 mm
- Pixel size: 50 um * 150 um



Quad



Stave

Towards COFFEE in 55nm process

Driving R&D goal: 5-10 ns timing resolution

性能需求	CEPC径迹探测器	LHCb UT升级
像素大小	10 um 以内空间分辨率 => 25 um × 150 um	<~50 um × 150 um
时间分辨率	<~10 ns @ Z pole	25ns bunch tagging => <~ 5 ns
功耗	可使用液冷，但越低越好=> <~ 150 mW/cm^2	可使用液冷，但越低越好=> <~ 150 mW/cm^2
抗辐照性能	Tbd	3 × 10^{15} n_{eq}/cm^2, 240 MRad TID
读出速度	Tbd	9 Gb/s, 与 lpGBT 等 common electronics兼容

Discussion on readout scheme

Yang Zhou

☹

所有像素比较器输出并行读出到阵列底部

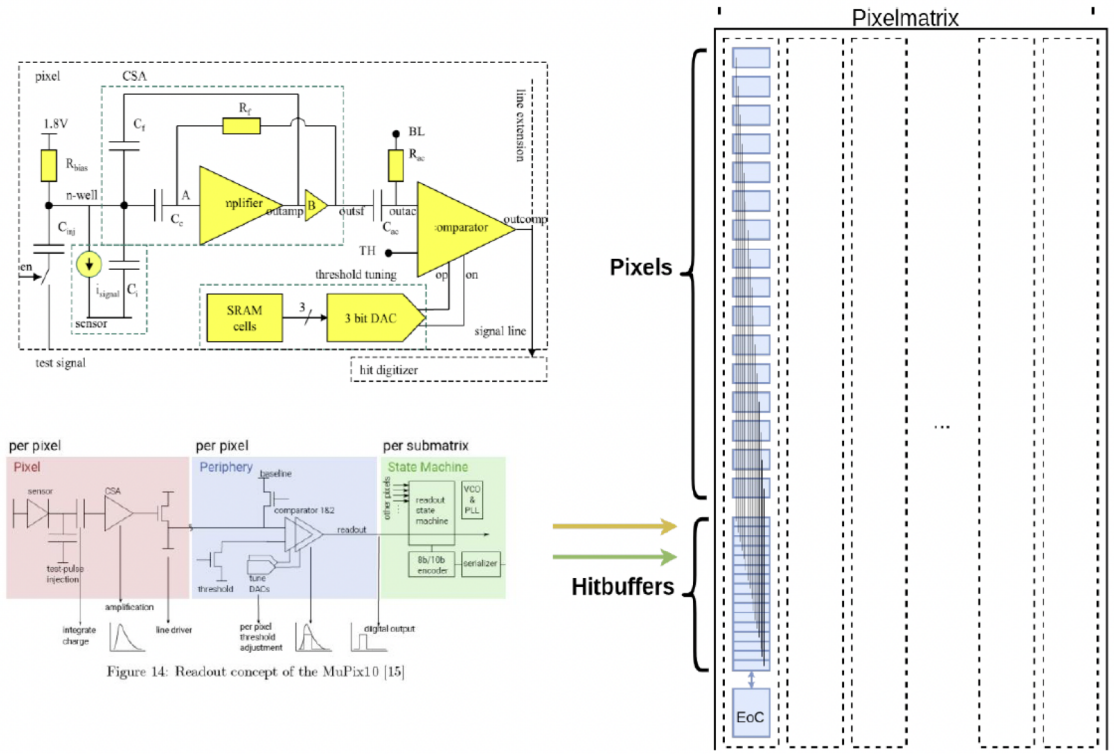


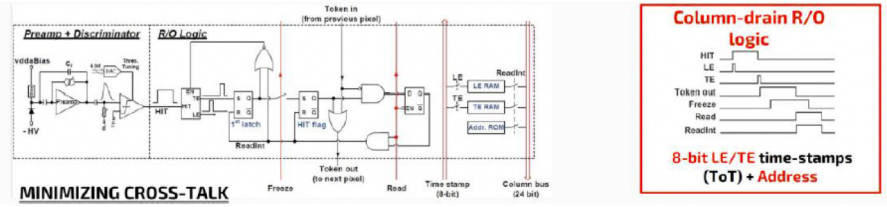
Figure 14: Readout concept of the MuPix10 [15]

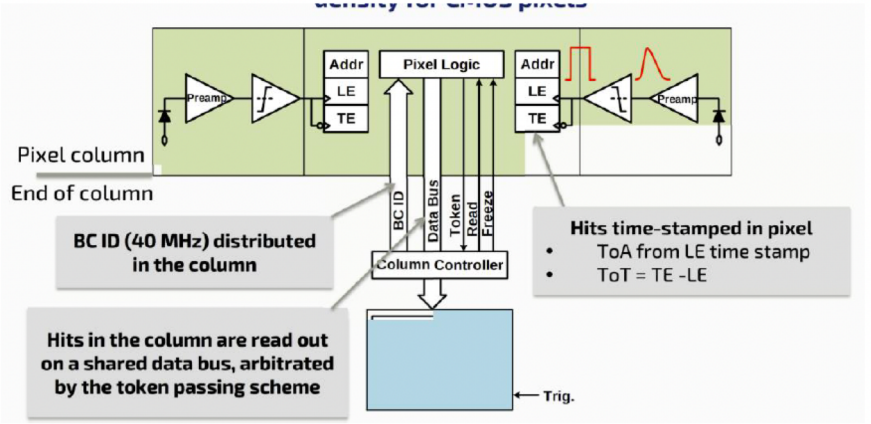
ATLASPIX3, MightyPix, MuPix

减小了数字模块对sensor的串扰，需要优化布线以减小长数据总线之间的cross-talk，需要大量的布线资源，ATLASPIX3有近5万条1.8cm的纵向数据线

☺

列总线优先级读出：Column-drain readout





RD50-MPW3，Monopix-LF、TimePix，FE-I3

LF工艺（有deep Pwell），谨慎的版图设计以应对数字模块对sensor的串扰；
TimePix和FE-I3非单片型芯片，不存在以上问题