Progress of High granularity readout TPC for CEPC TDR

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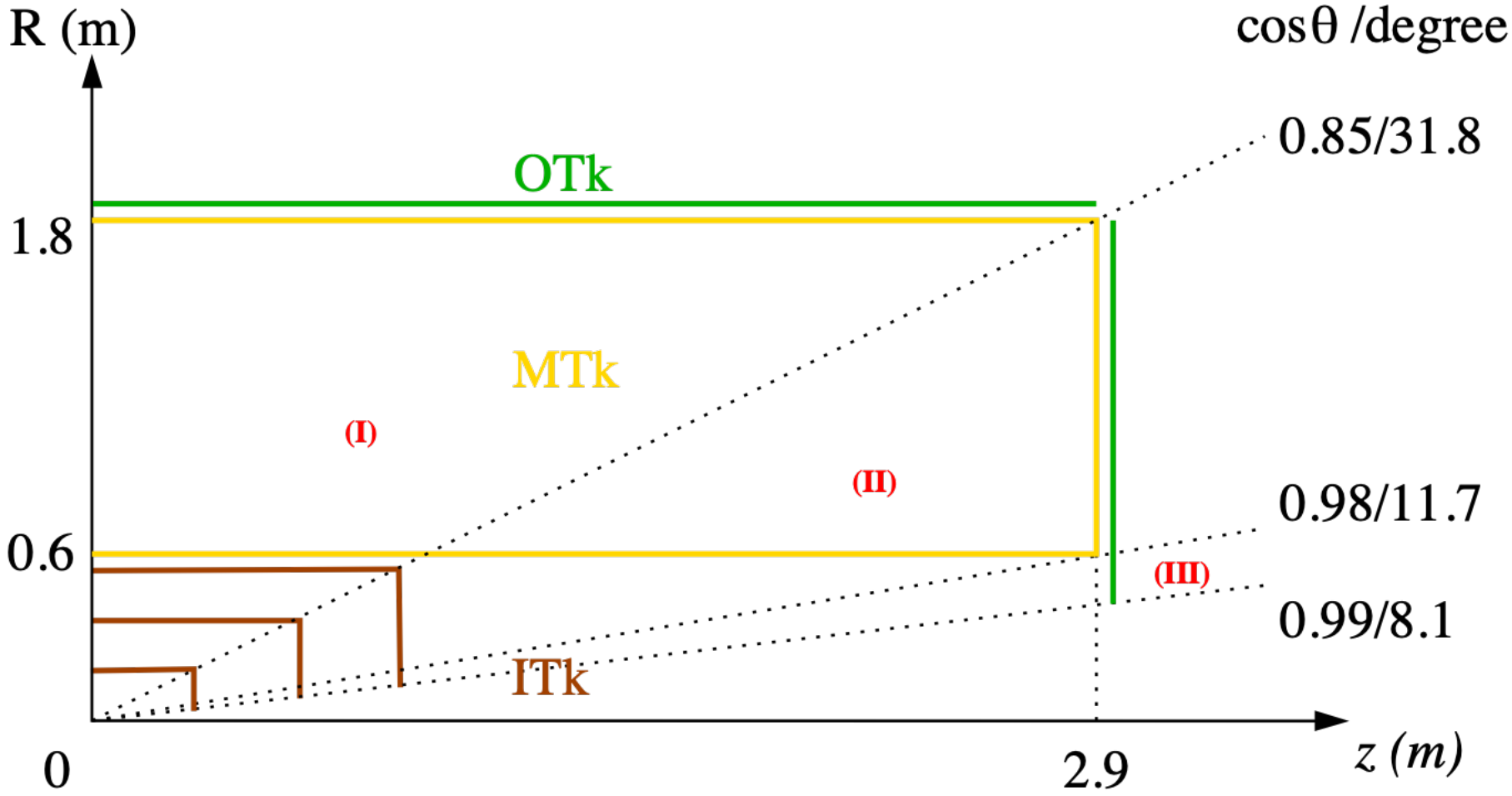
- **High granularity readout TPC as the main track**

Track detector system in CEPC Phy.&Det. TDR

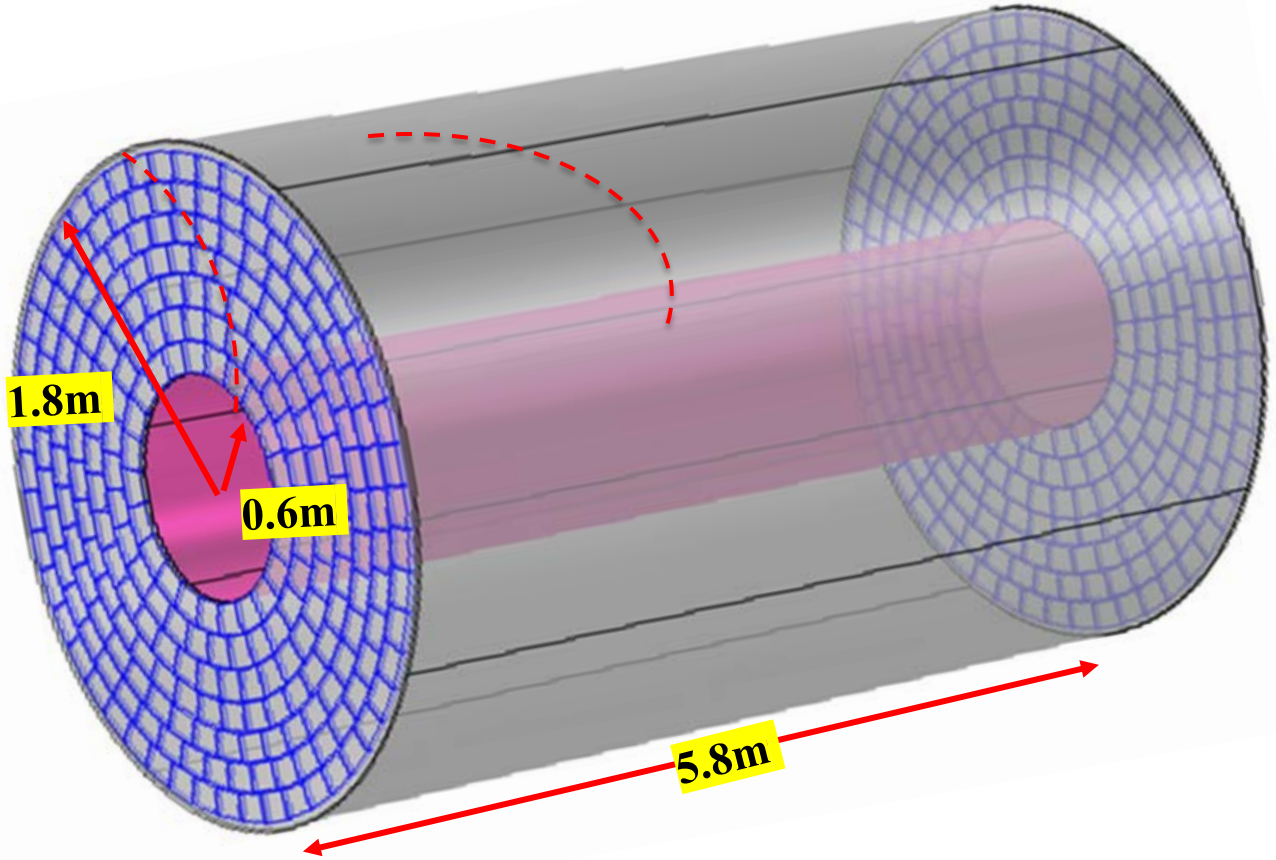
- The track detector system's geometry was finalized.
  - Converging geometries as quickly as possible in preparation for physics simulation
  - Geometry diagram almost finalized

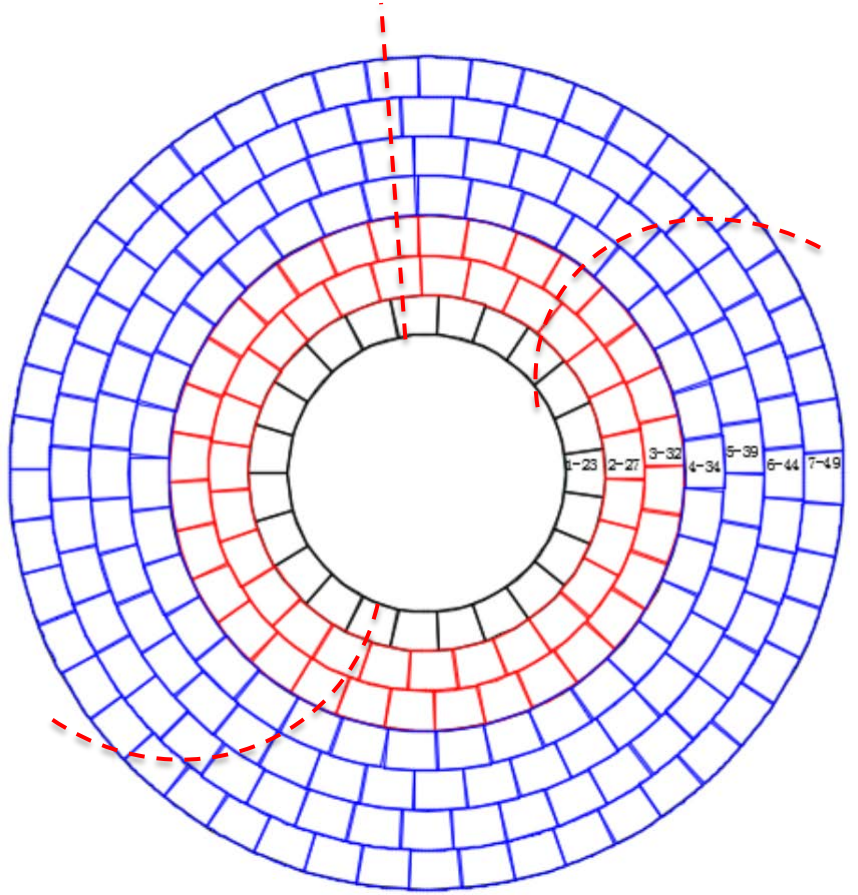


Almost finalized Geometry of the track detector system

Optimization the endcap of TPC

- Optimization modules in the endcap
  - ILD TPC: Coverage of the sensitivity readout area **~89%**
  - Coverage of the sensitivity readout area increased from **92% to 96%**





Optimization of Geometry of TPC detector and the Endplate

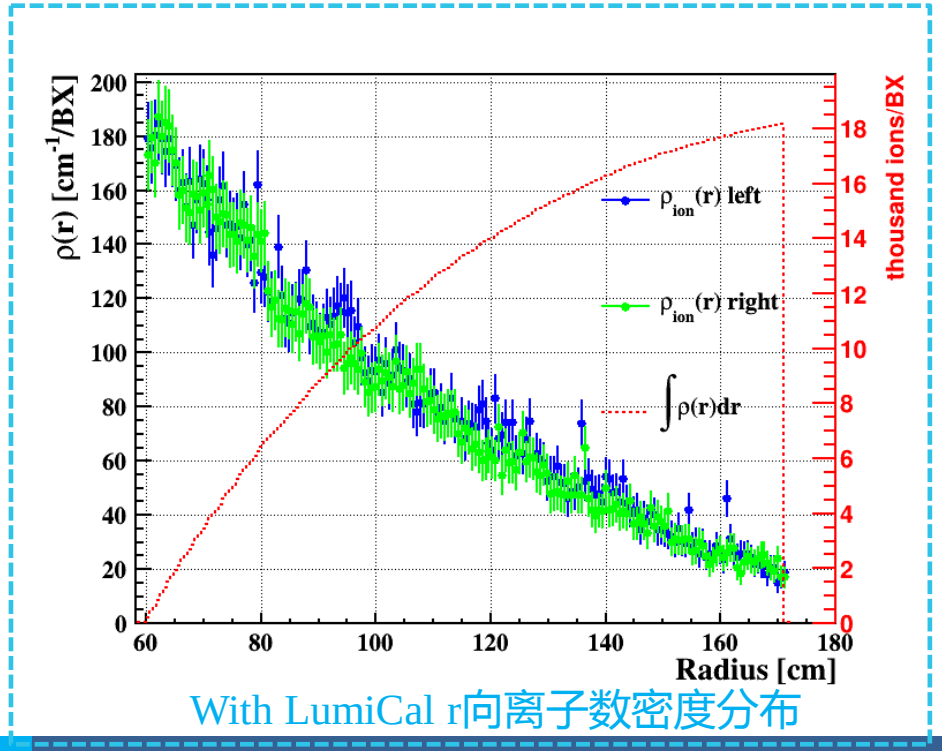
High granularity readout TPC @cosθ≃0.98

Parameters	Higgs run	Z pole run
B-field	3.0T	2.0T
Pad size (mm)/All channels	0.5mm×0.5mm /2×3×10^7	0.5mm×0.5mm /2×3×10^7
Material budget barrel	0.012 X_0	0.012 X_0
Material budget endcap	0.17 X_0	0.17 X_0
Points per track in rφ	2300	2300
σ_{point} in rφ	120μm (full drift)	400μm (full drift)
σ_{point} in rz	≃ 0.1 – 0.4 mm (for zero – full drift)	≃ 0.2 – 0.8 mm (for zero – full drift)
2-hit separation in rφ	0.5mm	0.5mm
K/π separation power @20GeV	3 σ	3 σ
dE/dx	3.2%	3.2%
Momentum resolution normalised: $\sigma_{1/pT} = \sqrt{a^2 + (b/pT)^2}$	a = 1.210 e -5	a = 2.69 e -5
	b = 0.589 e -3	b = 0.90 e -3

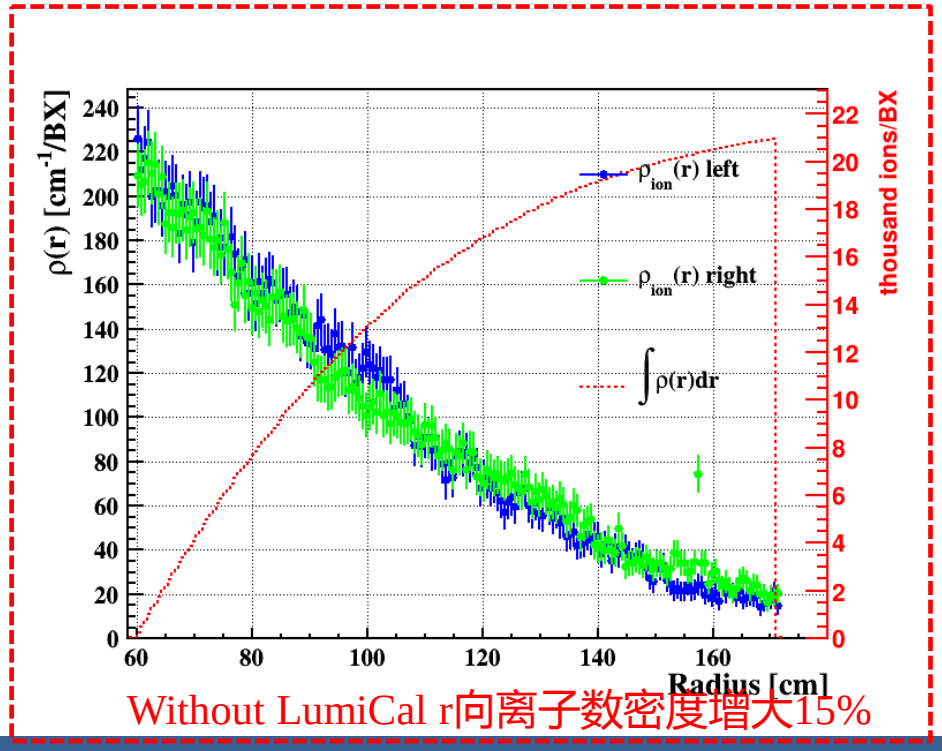
Estimation of the LumiCal at the inner of TPC

- With and without the LumiCal in the MDI region
- Optimization of the LumiCal position

With LumiCal	Without LumiCal
Edep~4.73GeV (10000BX)	Edep~5.45GeV (10000BX)
18.20k ions/BX	20.97k ions/BX
Max. $\rho_{sc} = 5.46\, nC/m^3$	Max. $\rho_{sc} = 6.18 nC/m^3$



With LumiCal r向离子数密度分布



Without LumiCal r向离子数密度增大15%

Power Consumption – TPC - Validation

- High granularity readout TPC： 3×10^7
- Total power: <10 kW to need the power consumption **<100mW/cm^2**

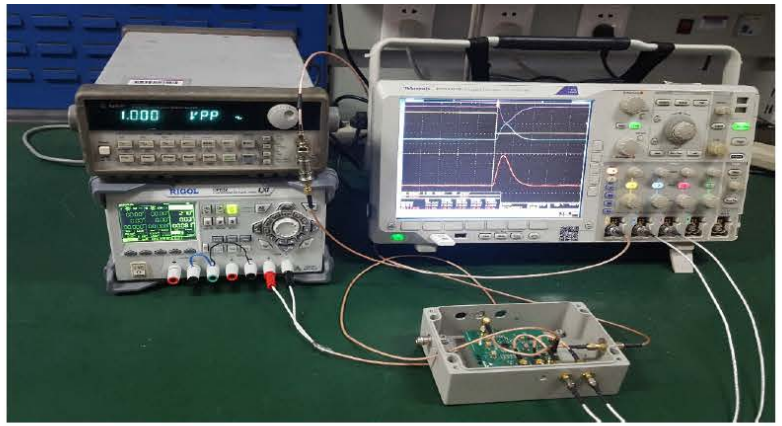
■ R&D on pixel TPC readout for CEPC

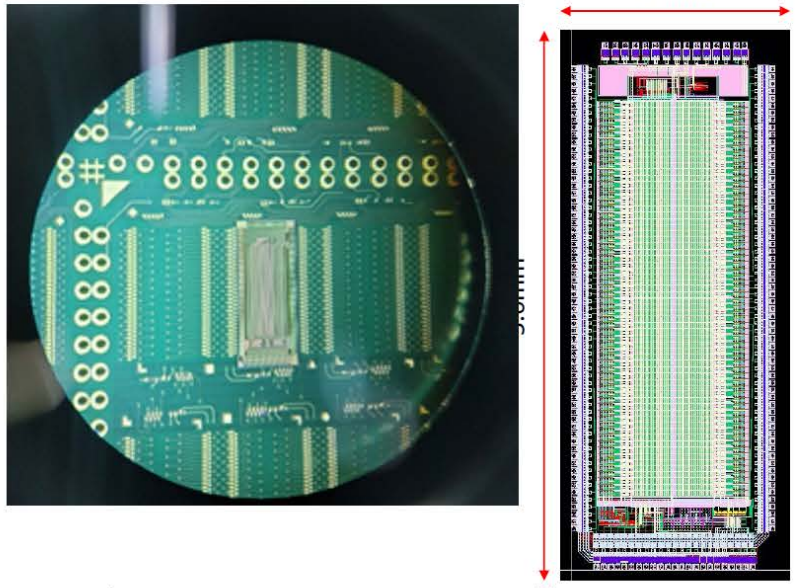
Pixel TPC ASIC chip was started to develop in 2023 and 1st prototype wafer standalone tested in May.

- ✓ Power consumption: <1.1mW/ch (1st prototype)
- ✓ <400mW/cm^2 (Test)

- 2nd prototype wafer design done
  - ✓ < 100mW/cm^2 (Goal and final design)

■ The TOA and TOT can be selected as the initiation function in the ASIC chip.





1st readout PCB board and the ASIC layout

Pad size optimization

- Pad size optimization ongoing.
  - Optimized the pad size to validate the PID performance

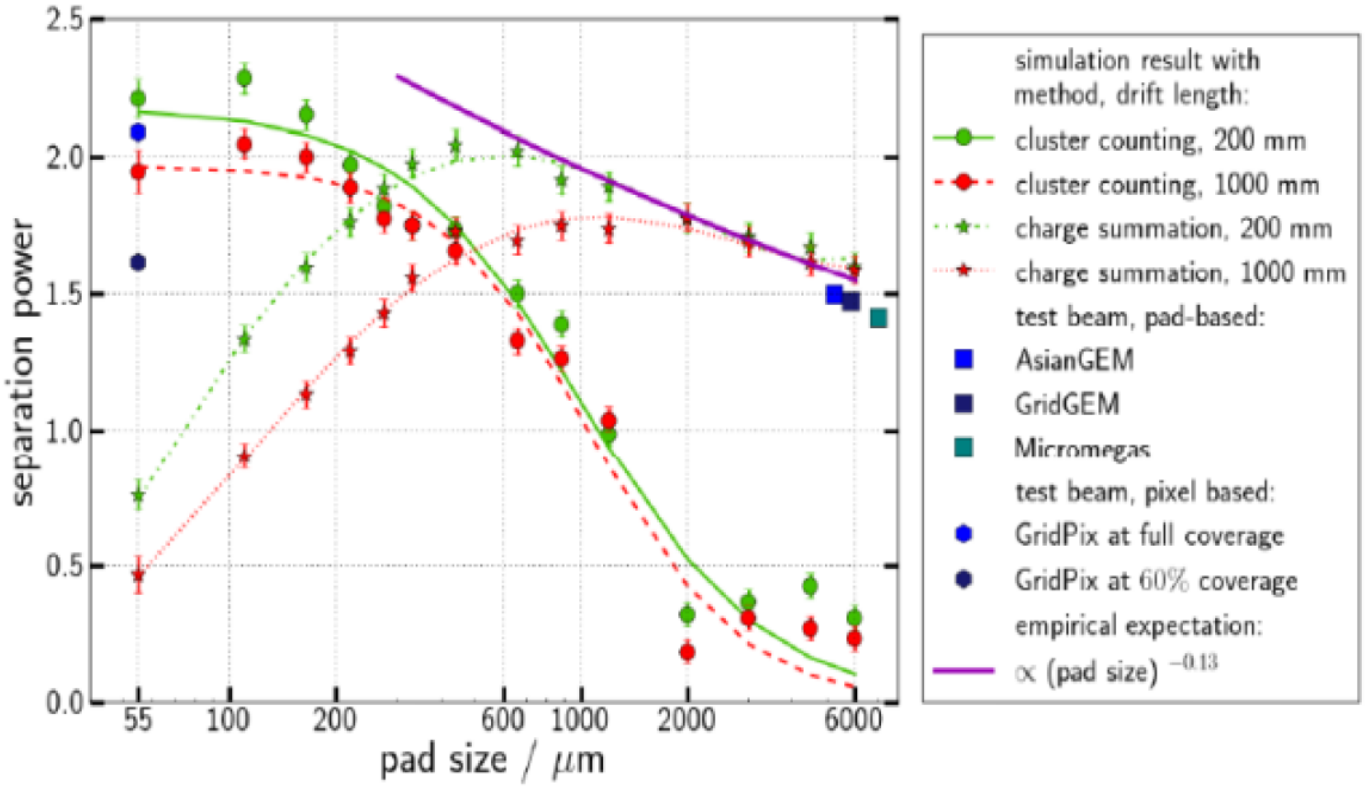
- **dN/dx (and tracking) can be beneficial from smaller pad size**

$$\rho_{cl} \approx 30cm^{-1} \Rightarrow Pad\ size \approx 300\mu m$$

(To detect single e⁻)

- **Need to find out the optimal pad size considering cost/power consumption**

Simulation with 30 cm track length



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Many thanks!