

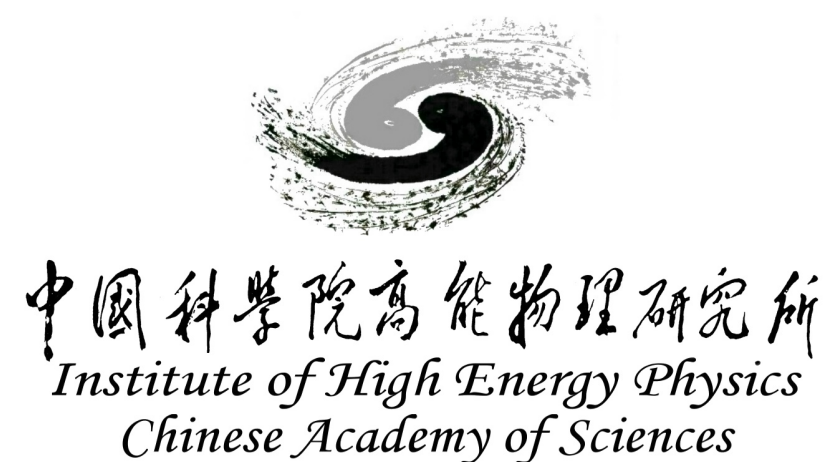
用于CEPC顶点探测器的单片式 像素探测器原型样机的研制

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For the CEPC vertex detector group

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CEPC 简介

→ 环形正负电子对撞机 (Circular Electron Positron Collider)

- 2012年希格斯粒子发现后, 由中国粒子物理学家提出
- 100 km 周长的双环正负电子对撞机

→ 多个物理项目

- 在 240 GeV: 希格斯工厂 (4×10^6 个)
- 在 90 GeV: Z 玻色子 ($> 4 \times 10^{12}$ 个)
- 在 160 GeV: W^+W^- ($> 10^8$ 个)

CEPC Operation mode		ZH	Z	W^+W^-	$t\bar{t}$
\sqrt{s} [GeV]		~ 240	~ 91.2	~ 160	~ 360
Run time [years]		7	2	1	-
CDR (30MW)	L / IP [$\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$]	3	32	10	-
	$\int L dt$ [ab^{-1} , 2 IPs]	5.6	16	2.6	-
	Event yields [2 IPs]	1×10^6	7×10^{11}	2×10^7	-
Run time [years]		10	2	1	5
Latest TDR (50MW)	L / IP [$\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$]	8.3	191.7	26.6	0.8
	$\int L dt$ [ab^{-1} , 2 IPs]	20	96	7	1
	Event yields [2 IPs]	4×10^6	4×10^{12}	5×10^7	5×10^5

CEPC 顶点探测器

- 高精度的顶点探测器对CEPC物理目标的实现至关重要

味物理 (大量的b/c夸克喷注, τ 轻子)

希格斯物理 ($H \rightarrow bb/cc/gg$ 和 $H \rightarrow \tau\tau$)

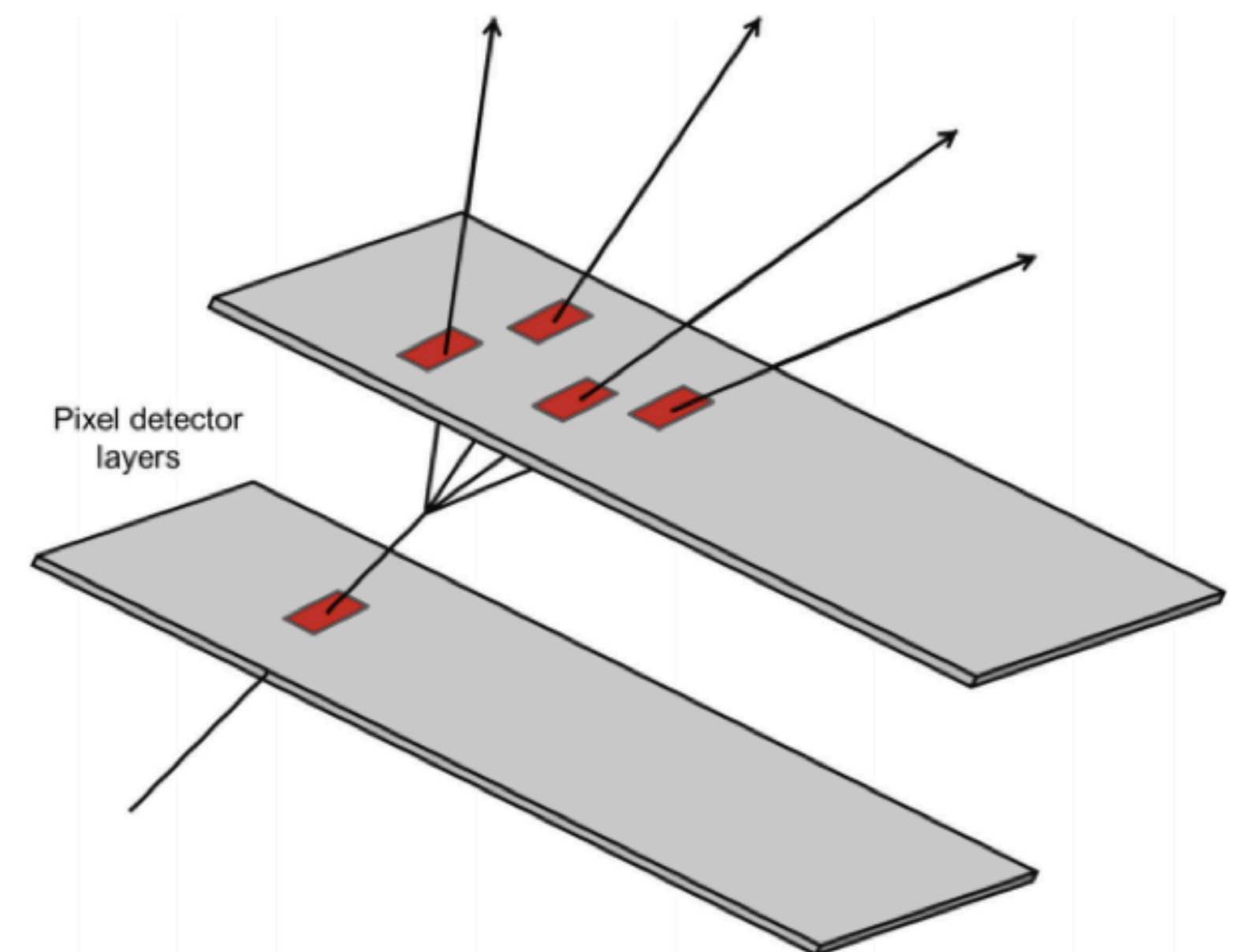
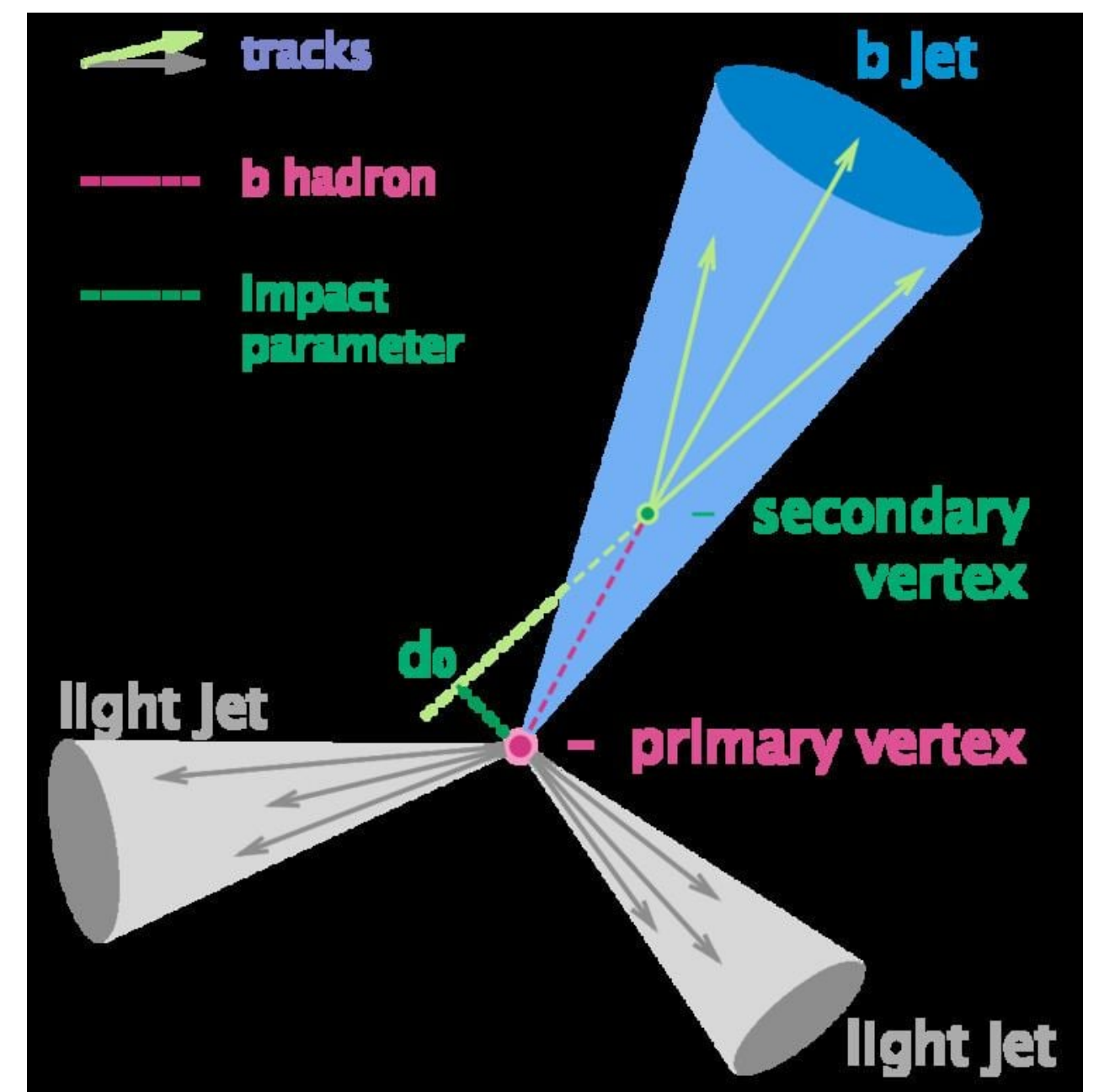
-> flavor tagging

- CDR的需求

单点分辨率: $< 3 \mu\text{m}$ ($\sim 16 \mu\text{m}$ pixel pitch)

物质的量: $< 0.15 \% X_0/\text{layer}$

功耗: $< 50 \text{ mW}/\text{cm}^2$, if air cooling used



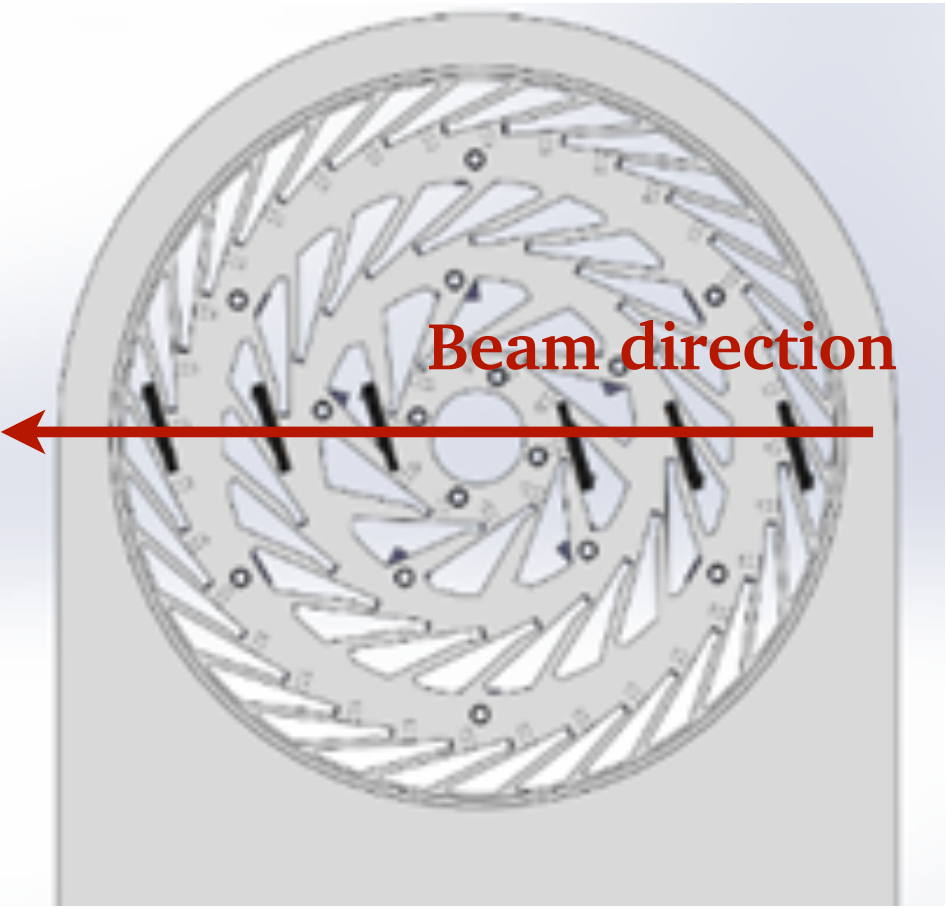
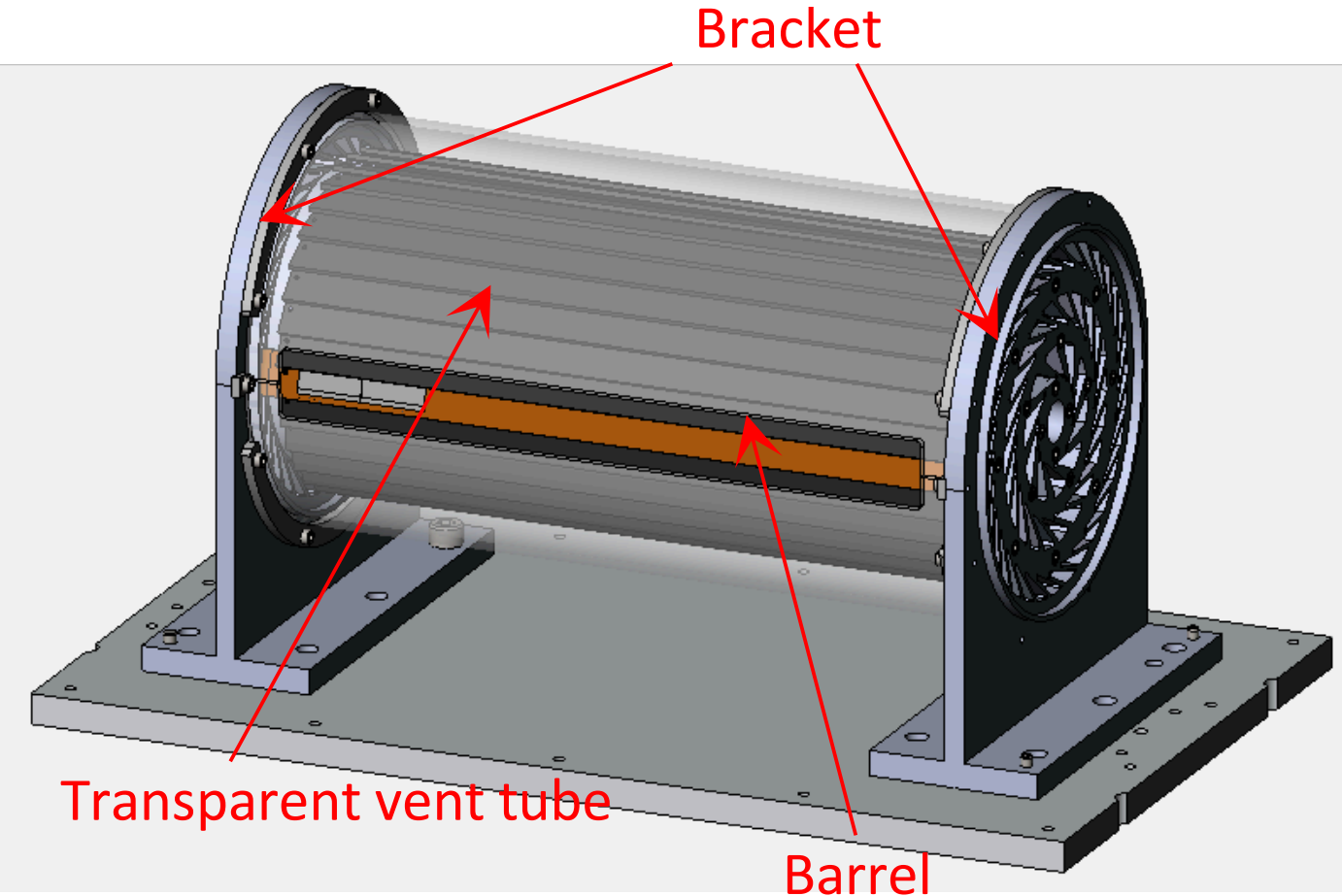
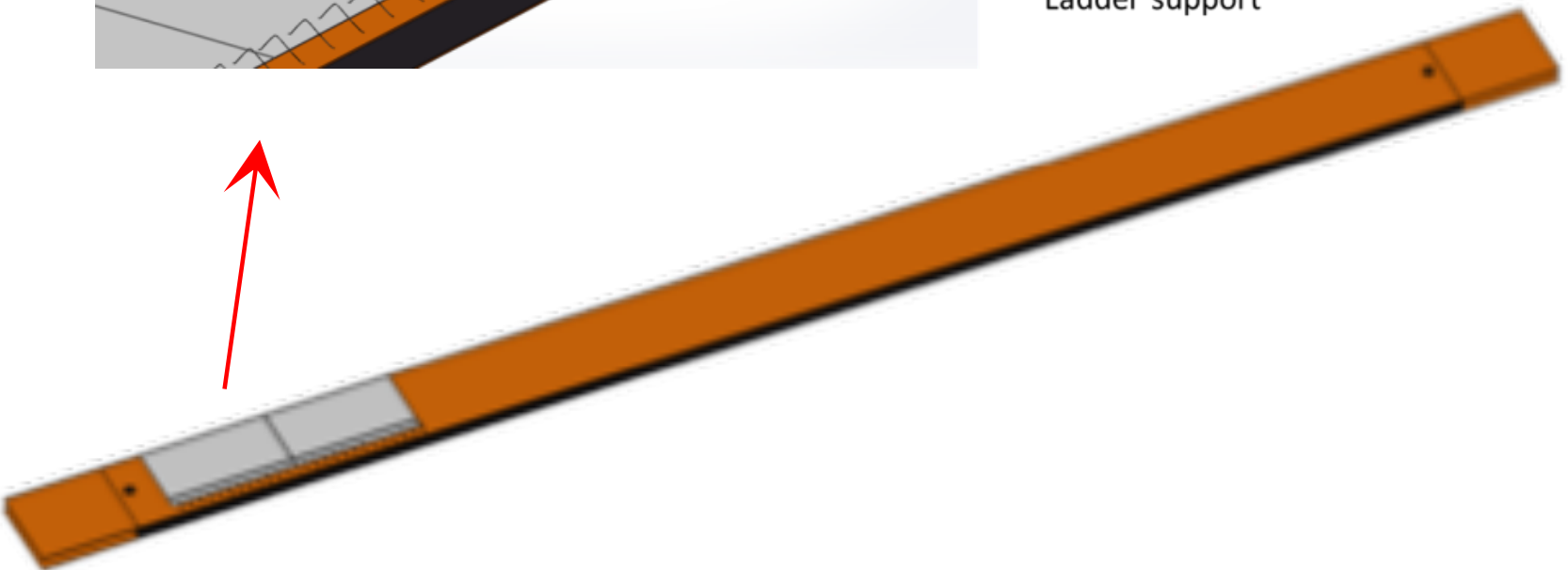
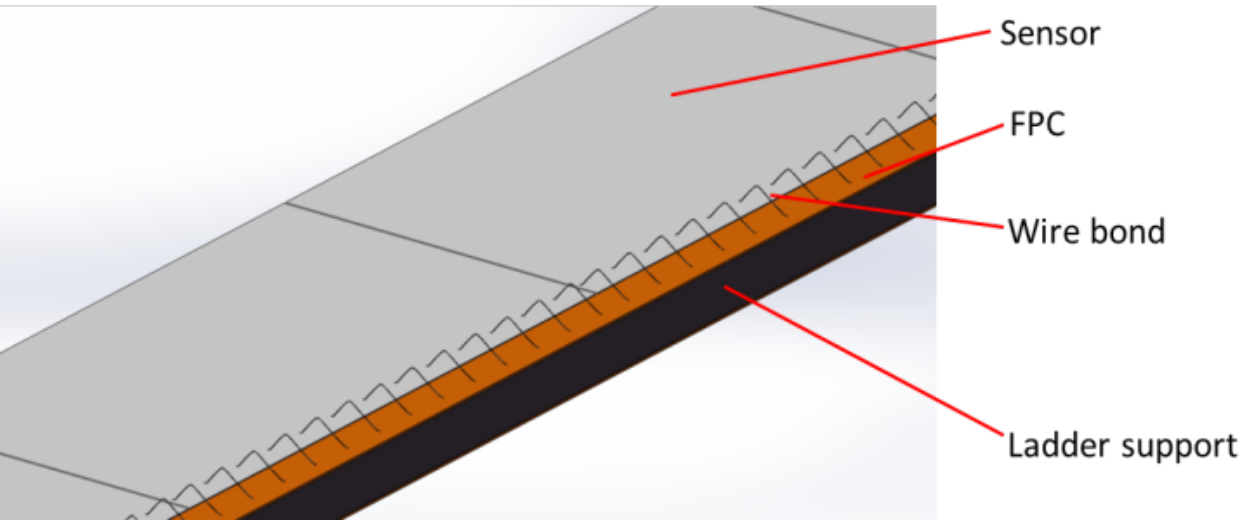
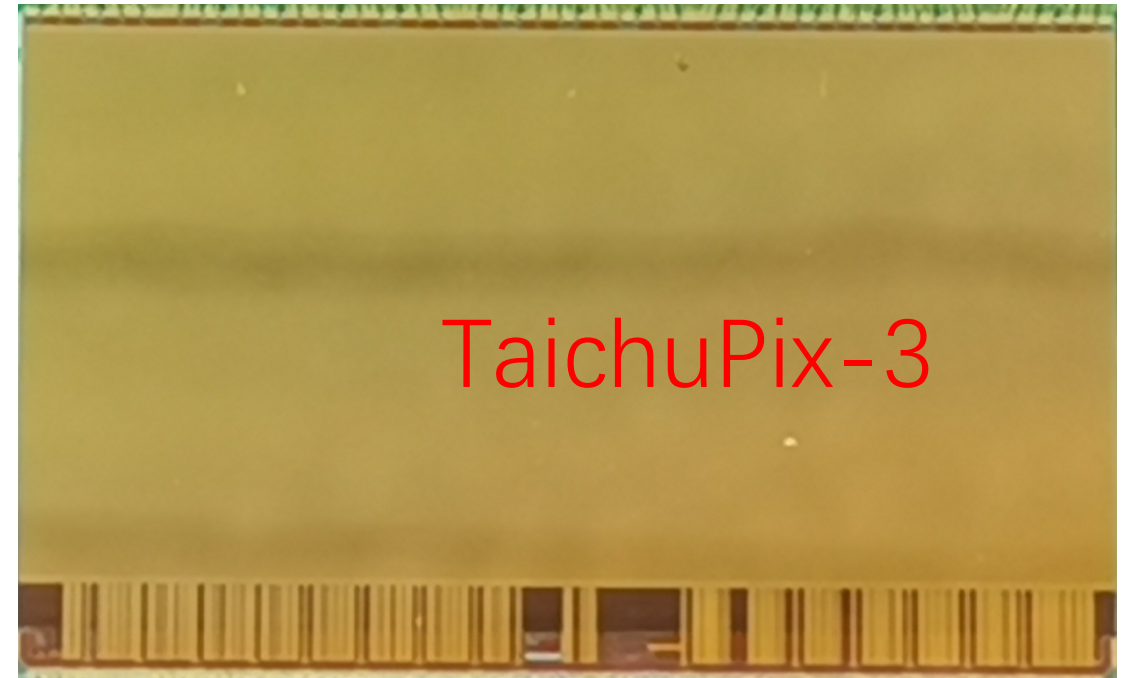
CEPC 顶点探测器原型机的研发

原型机组装与束流测试

CMOS 图像传感器芯片设计

模块组装

CMOS pixel sensor prototyping



CMOS 图像传感器芯片 —— TaichuPix

➔ 现有的单片集成型CMOS传感器不能满足CEPC的要求

- 像素尺寸小 -> 高分辨率 ($< 3 \mu\text{m}$)
- 抗辐照能力: $> 1\text{Mrad/year}$
- 高计数率 -> CEPC Z pole 高亮度运行 (40MHz的对撞速率)

➔ 单片集成型传感器(MAPS): TaichuPix (180 nm CMOS 工艺)

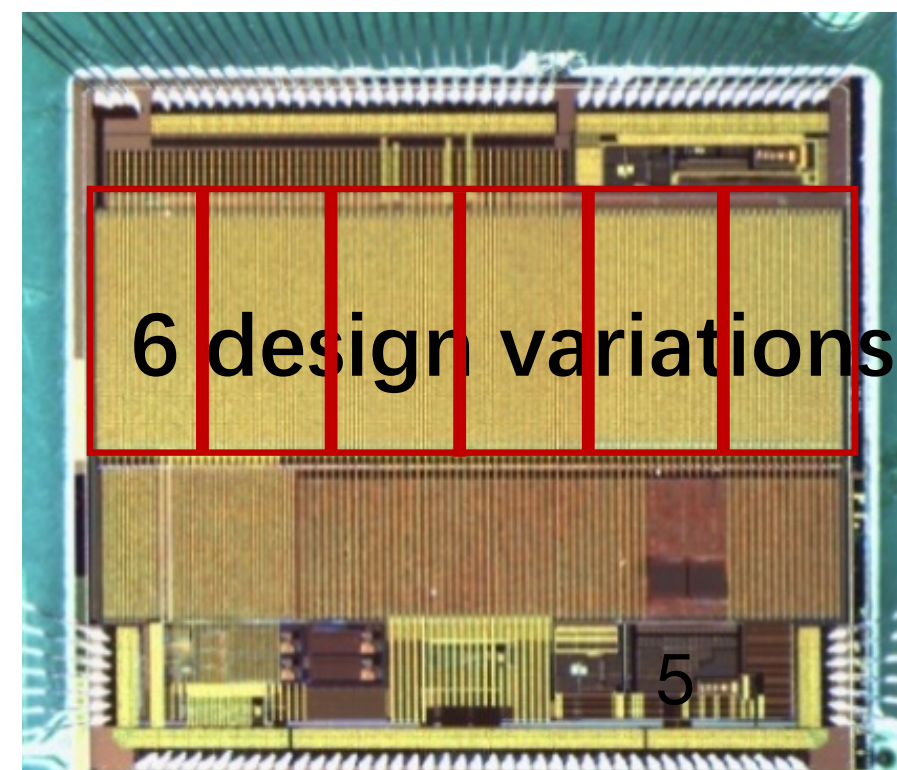
TaichuPix-1 和 TaichuPix -2 小尺寸芯片，用于验证功能和优化设计

TaichuPix-3 全尺寸、全功能的芯片，并应用到CEPC顶点探测器原型机上

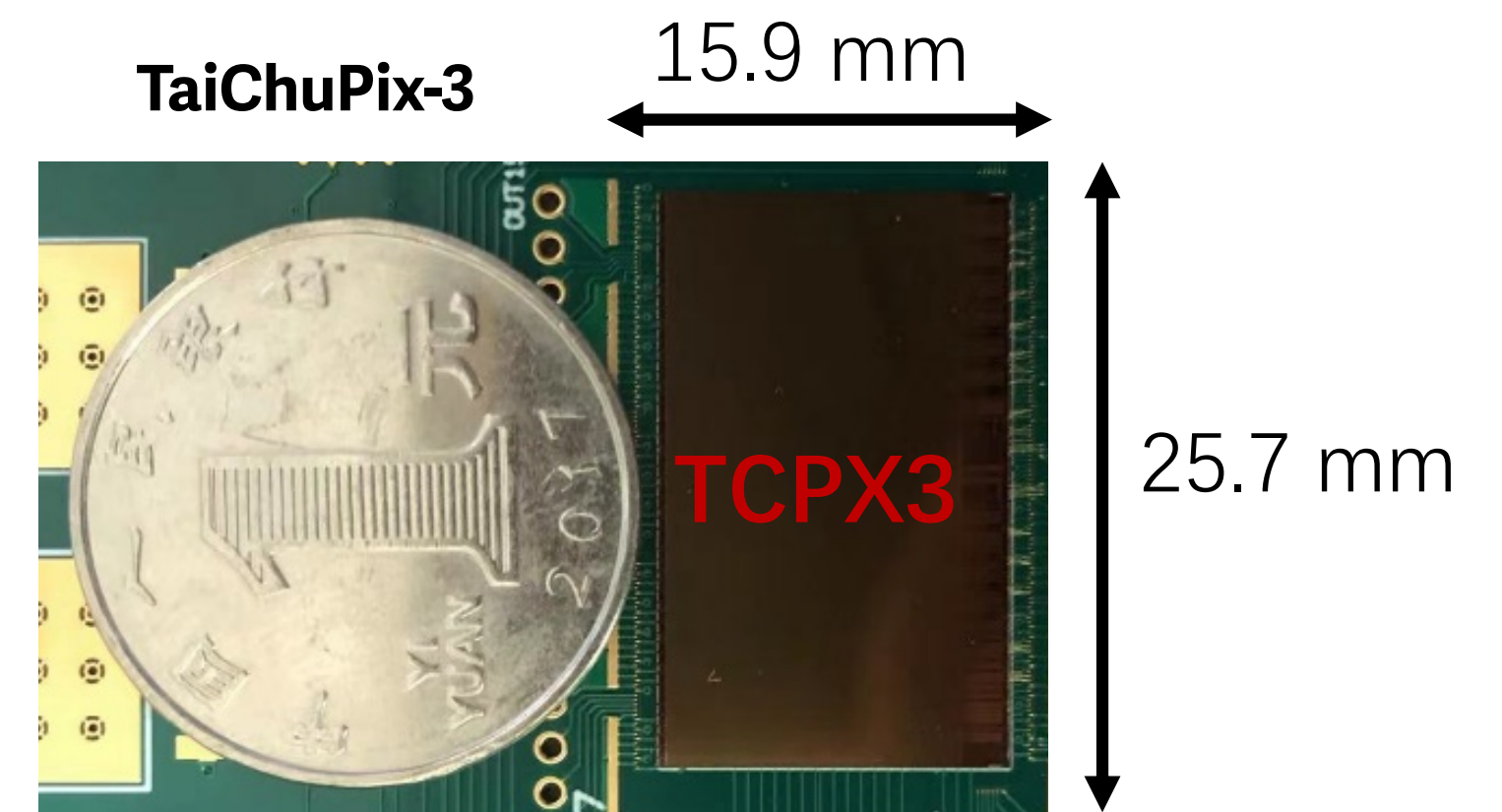
TaiChuPix-1



TaiChuPix-2



TaiChuPix-3



→ TaichuPix-3 (太初-3)

- 读出架构

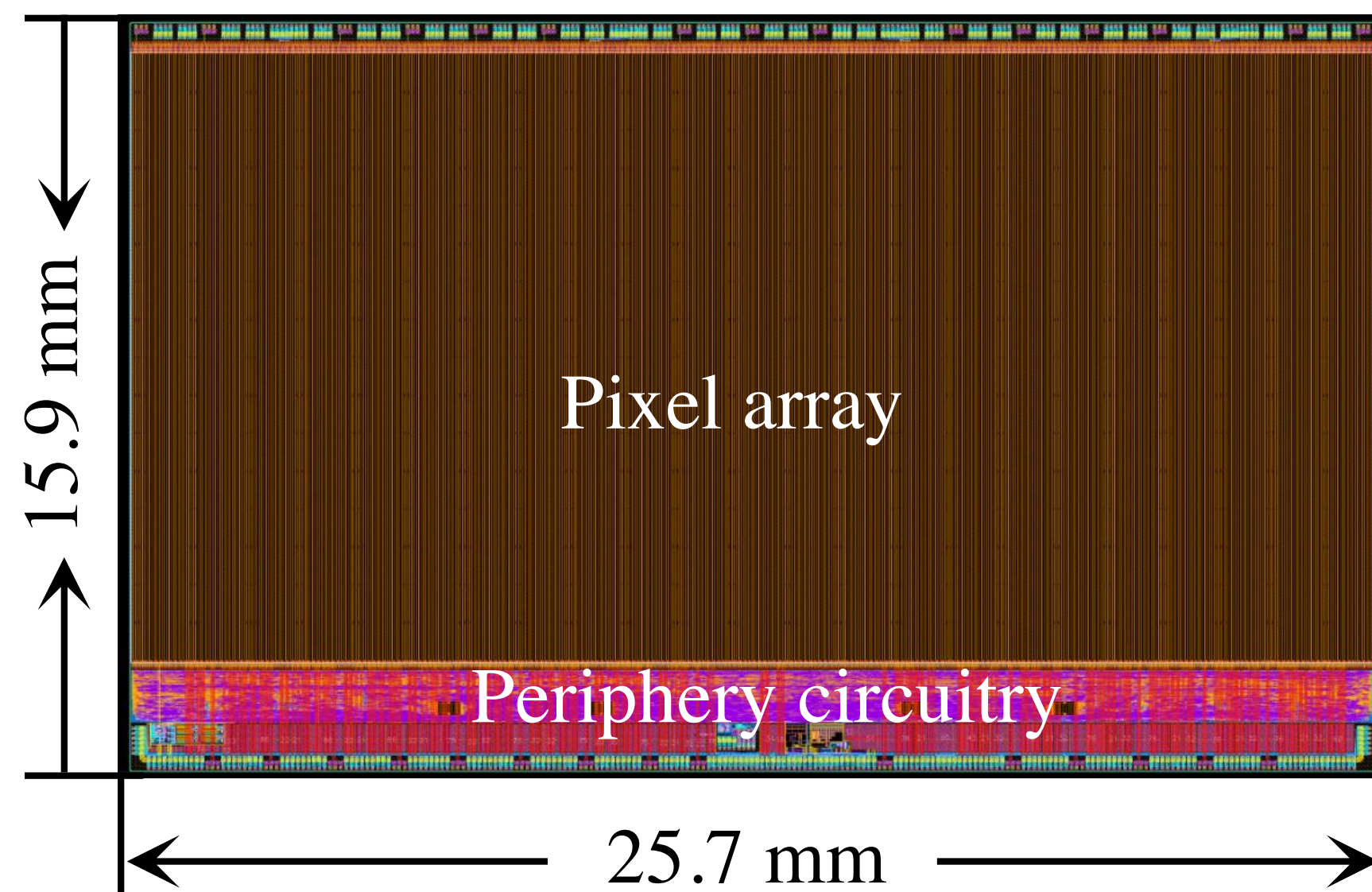
Double Column-drain 读出以适应CEPC的高击中率

- 数据驱动读出
- 像素读出时间 50 ns

触发和非触发模式兼容 → 无触发模式下所有的击中数据都会被读出

二进制读出 → 每个像素只能给出是否有击中的信息，无法给出电荷信息

TaichuPix-3芯片只有一个共用的DAC用来设置像素阈值 → 不同像素间的阈值差异



芯片尺寸: 1024 列 × 512 行

像素单元尺寸: 25 μm × 25 μm

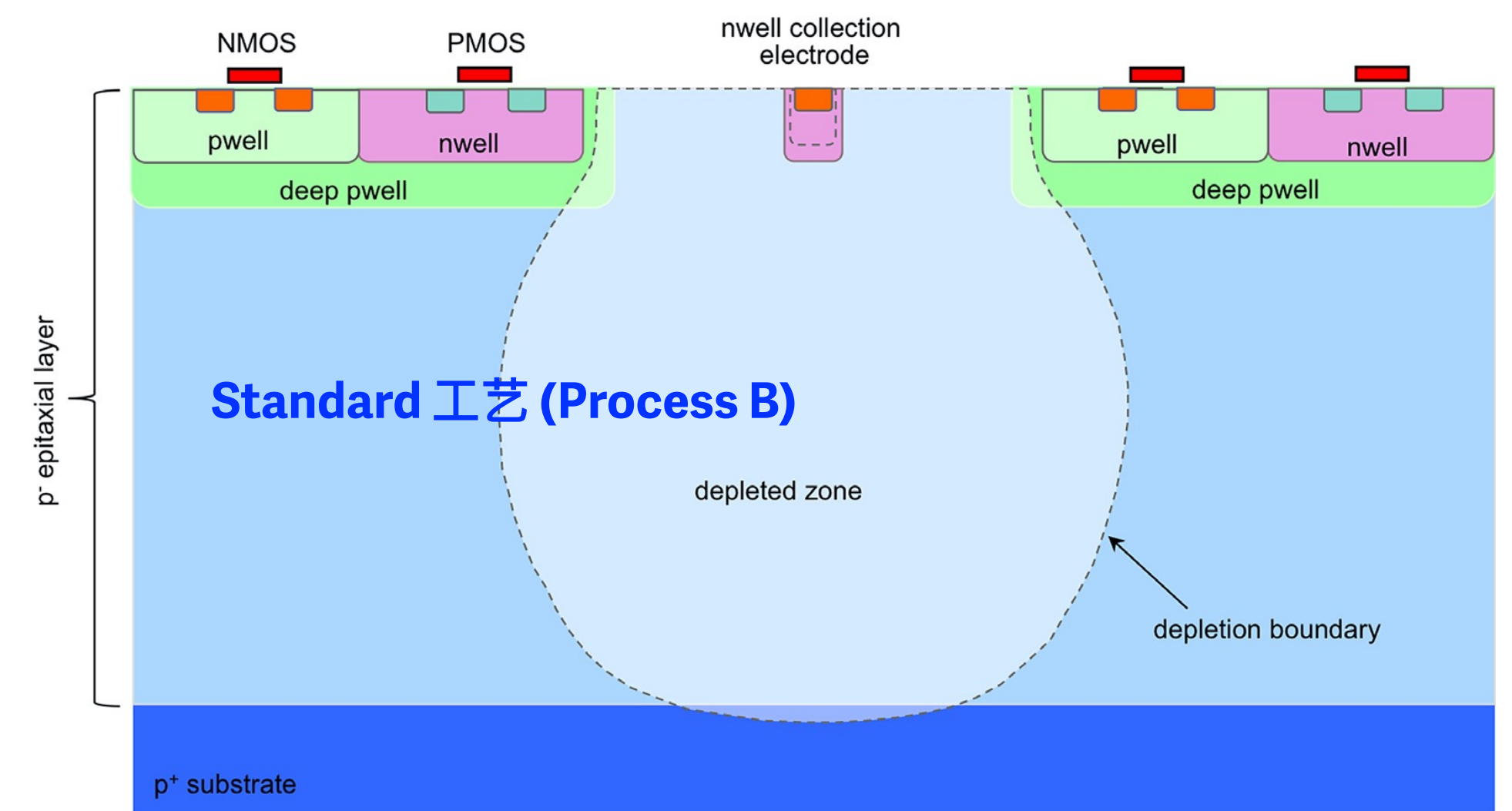
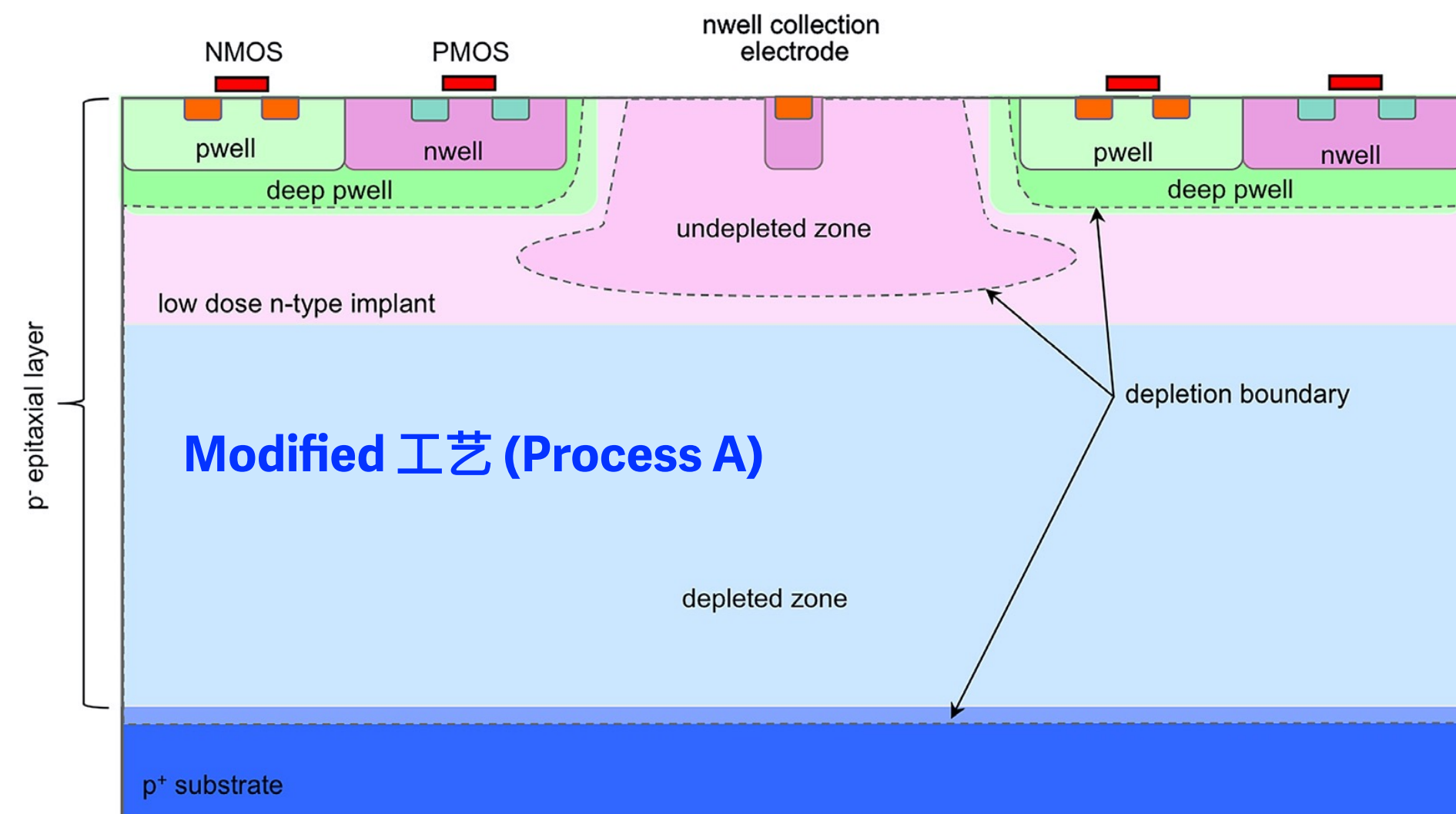
芯片厚度: 150 μm

- 工艺

传感器和读出电路集成在同一片硅衬底上 → 低物质的量，低像素电容，易组装

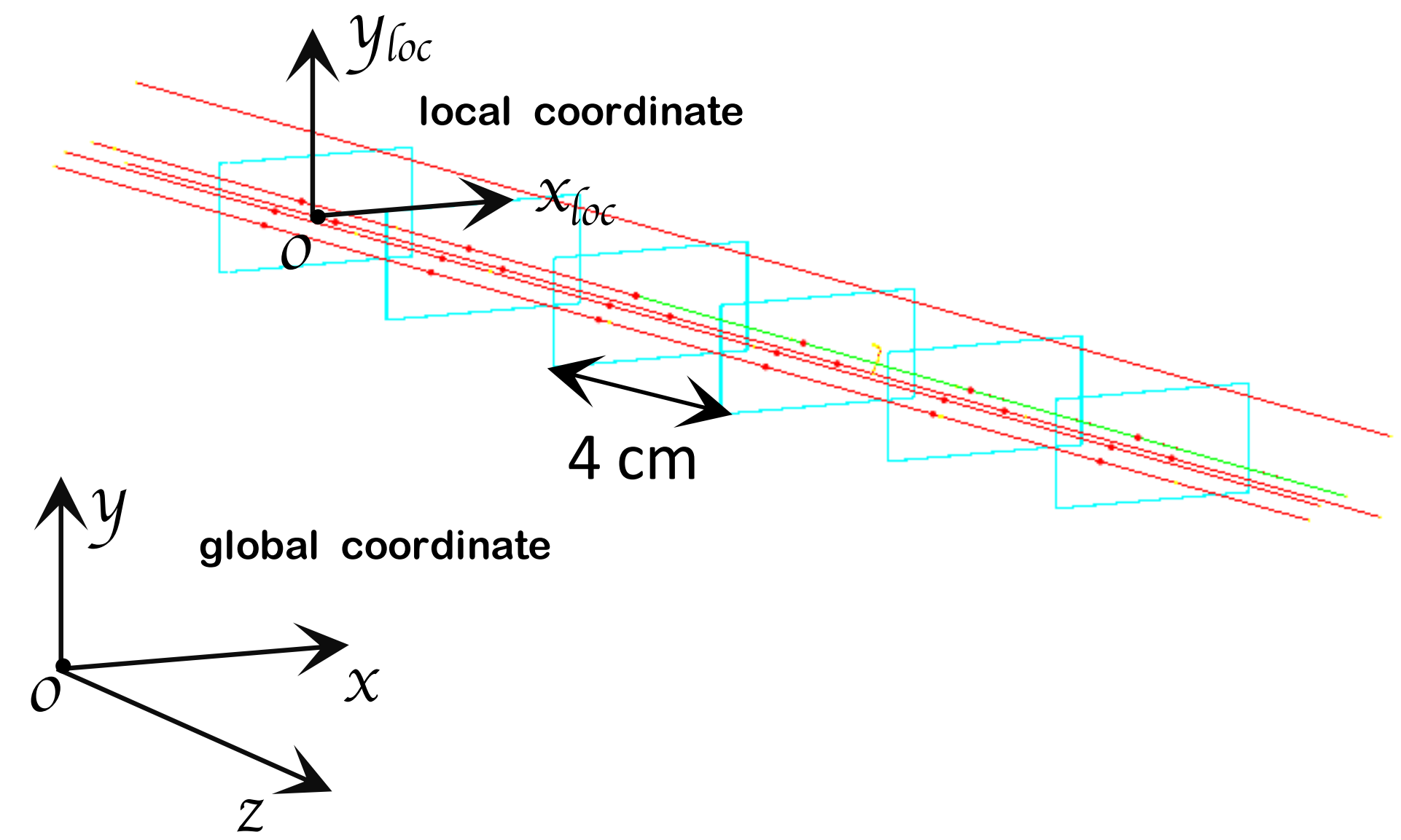
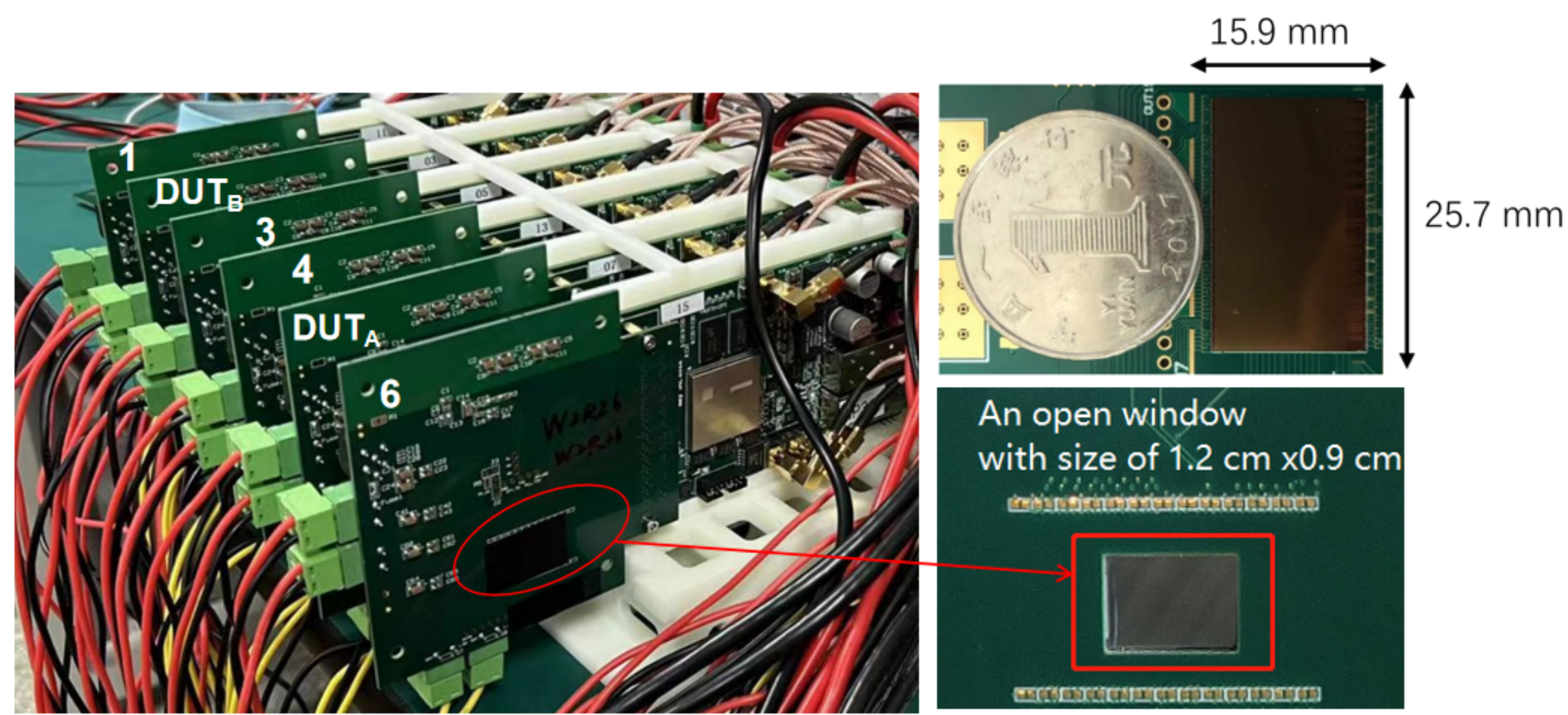
两种工艺的TaichuPix-3

- 标准 (Standard) 工艺
- 修正 (Modified) 工艺
 - ➔ 添加了一个额外的低剂量的 n - type 层
 - ➔ 可实现全耗尽，实现更快的电荷收集，提高抗辐照能力
 - ➔ 减小了电荷扩散的概率，电荷共享效应会变弱

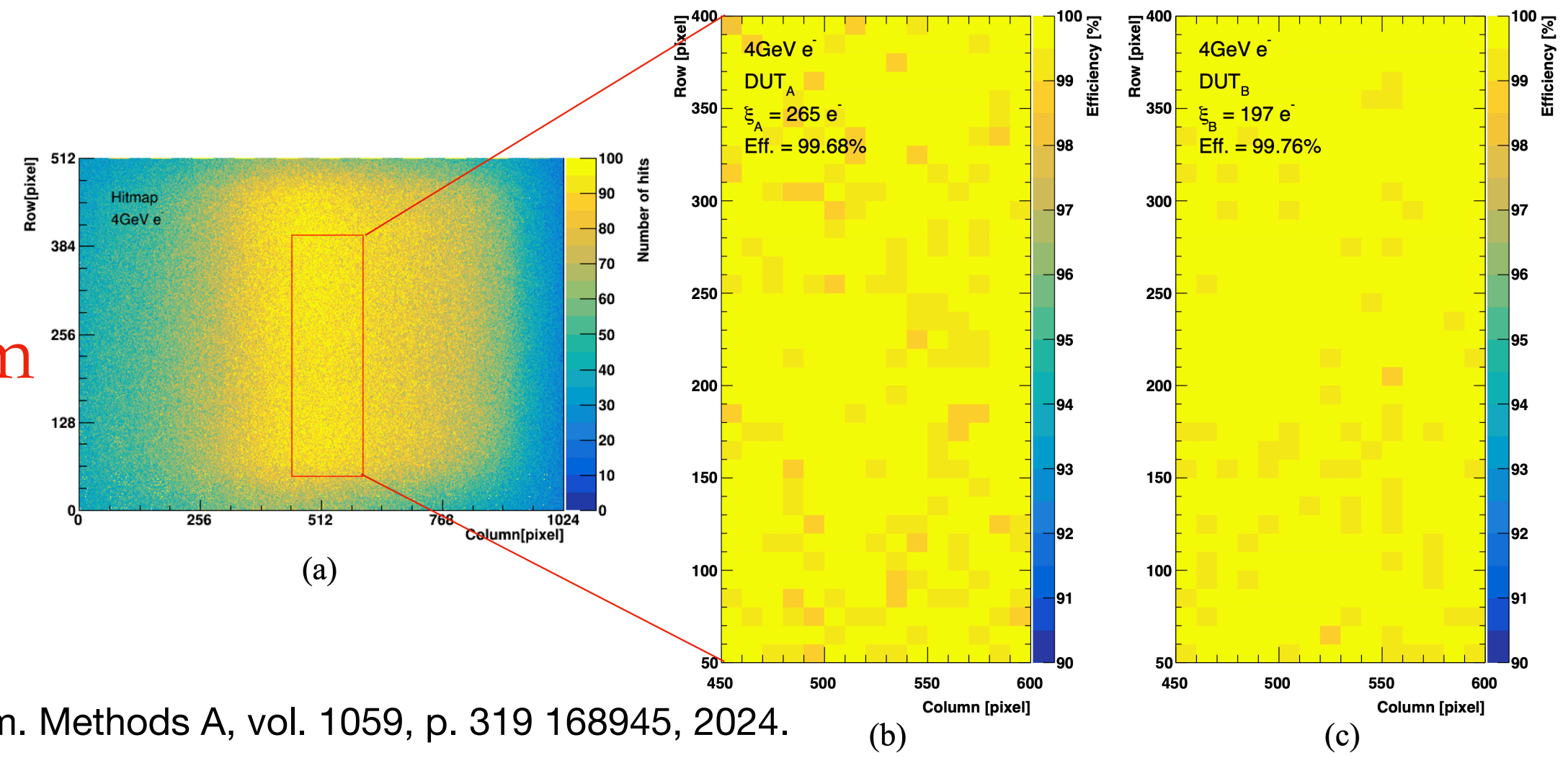


- TaichuPix-3 束流望远镜测试

由6个TaichuPix-3芯片组成的望远镜系统在DESY II 4 GeV 电子束流下进行了测试 (2022. 12)



- 标准工艺 —— DUT_B
- 修正工艺 —— DUT_A
- 分析束流数据后得到^[2]:
 - 空间分辨率标准工艺 4.5 μm , 修正工艺 4.8 μm
 - 探测效率: > 99%



[2] T. Wu, S. Li, W. Wang et al., "Beam test of a 180 nm cmos pixel sensor for the CEPC vertex detector," Nucl. Instrum. Methods A, vol. 1059, p. 319 168945, 2024.

顶点探测器原型机的探测模块与机械结构

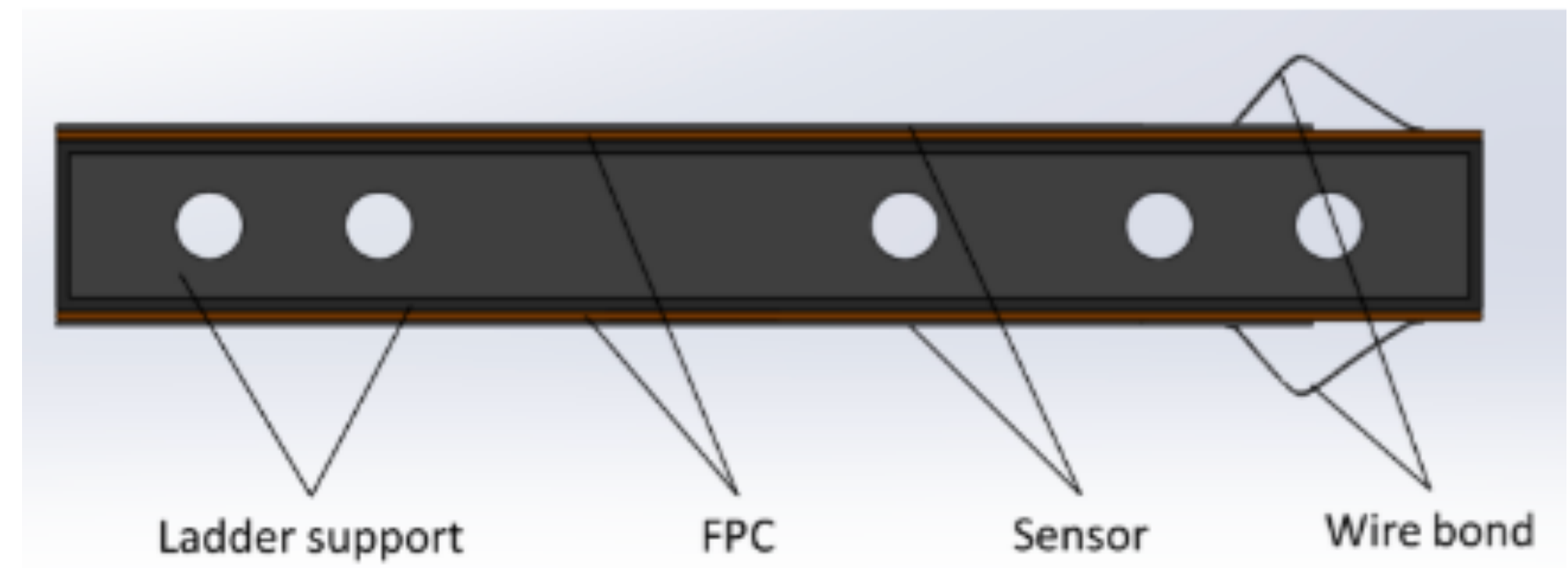
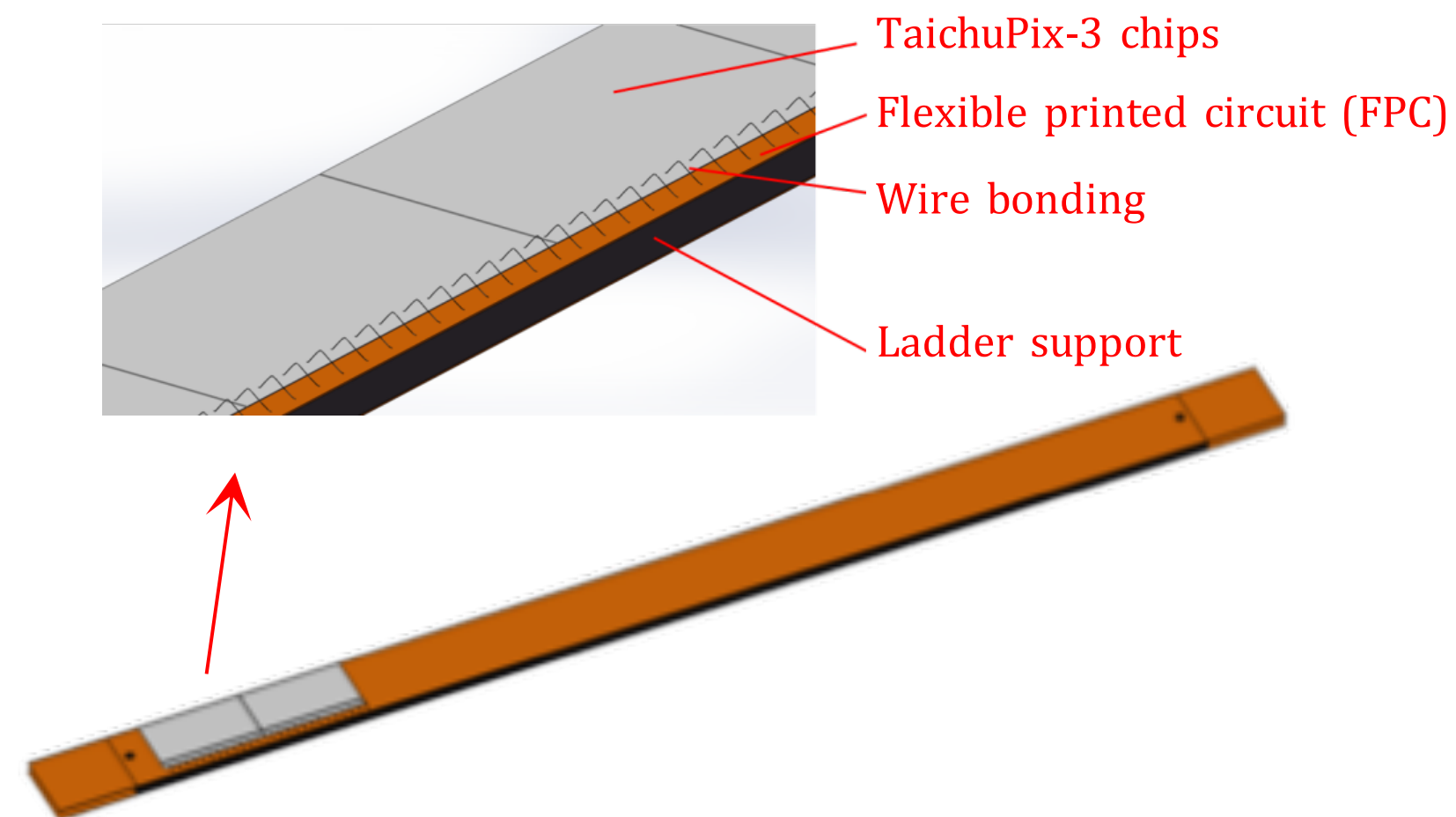
- 探测模块 (Ladder) 的组成

TaichuPix-3 芯片 - 柔性电路板 (FPC) - 碳纤维支撑结构 - FPC - TaichuPix-3 芯片

- 双面探测
- TaichuPix-3 芯片先粘贴到FPC上再打线
- FPC和支撑结构之间通过胶水粘贴在一起
- FPC的长度大约是 553 mm, 最多可以放置10个TaichuPix-3芯片

挑战

- 柔性电路板太长，在电源与CEPC需要的高速信号传输方面有挑战
- 物质质量要低，柔性金属层少，有屏蔽等问题

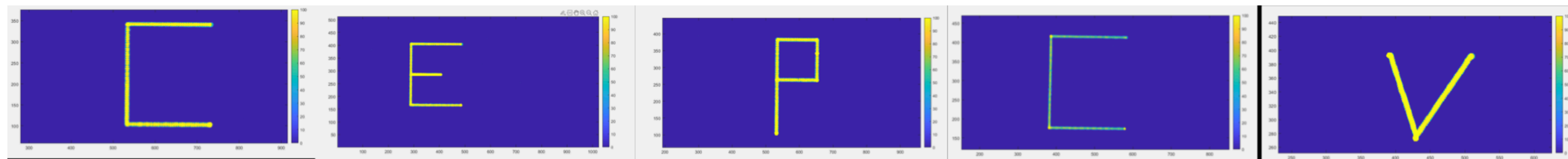
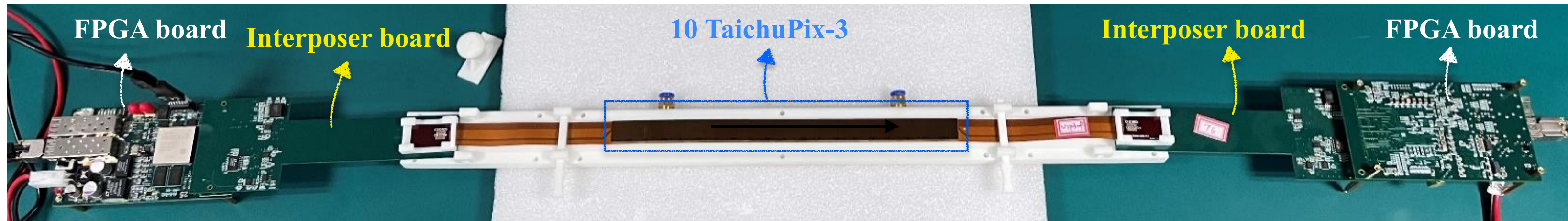
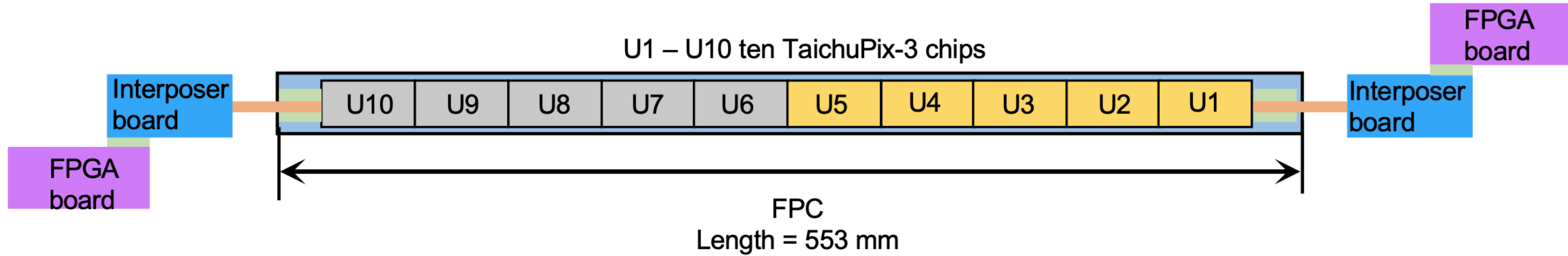


- 探测模块的读出

每5个芯片为一组，从两端分别读出

- FPC: 电源和地控制总线，接收数据和时钟
- Interposer board: 线性稳压器，DAC，数据连接传输
- FPGA board: 芯片控制、数据打包、FIFO

装有10个TaichuPix-3芯片的ladder的基本功能在实验室下得到了验证



- 原型机的机械结构

全尺寸的机械结构

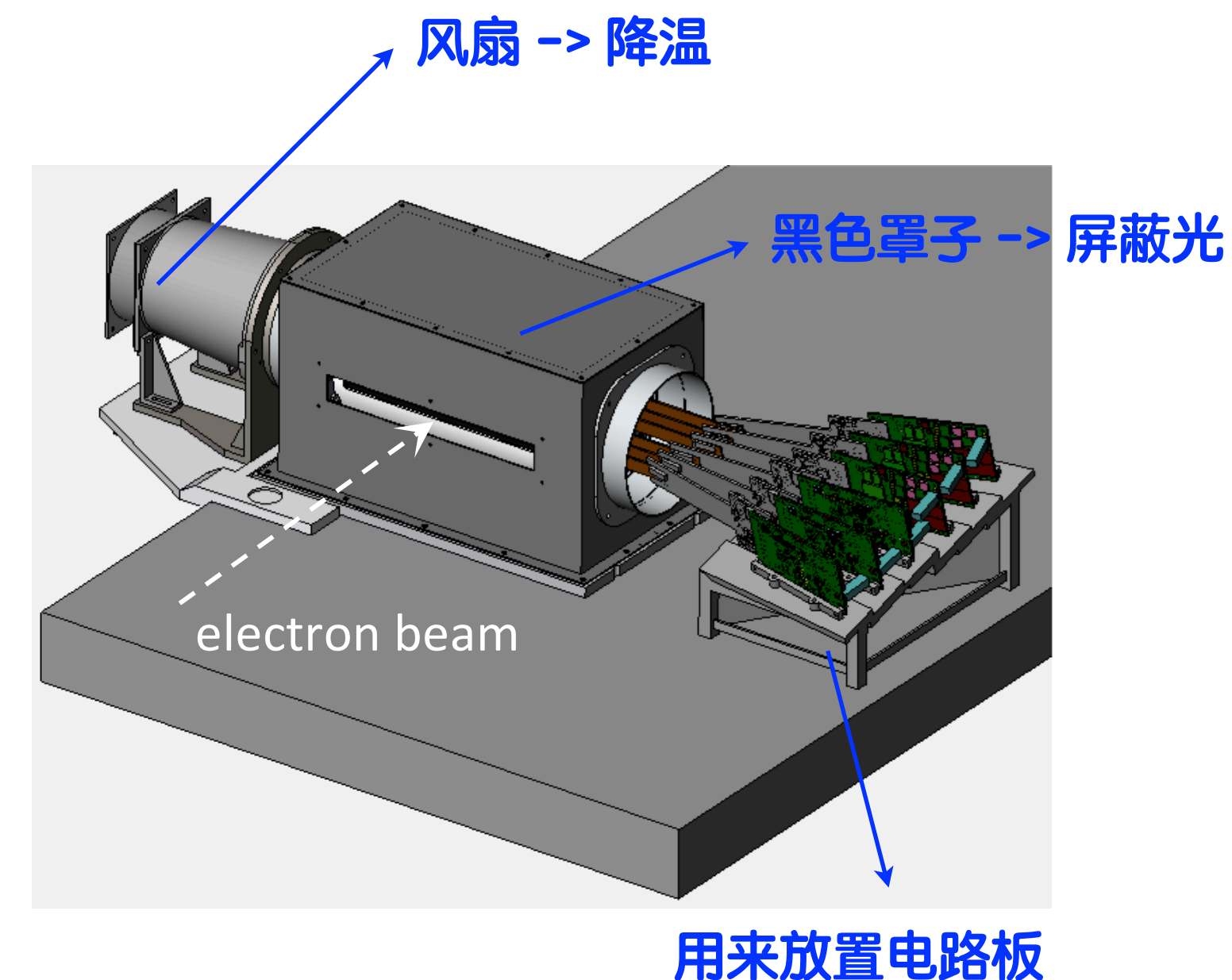
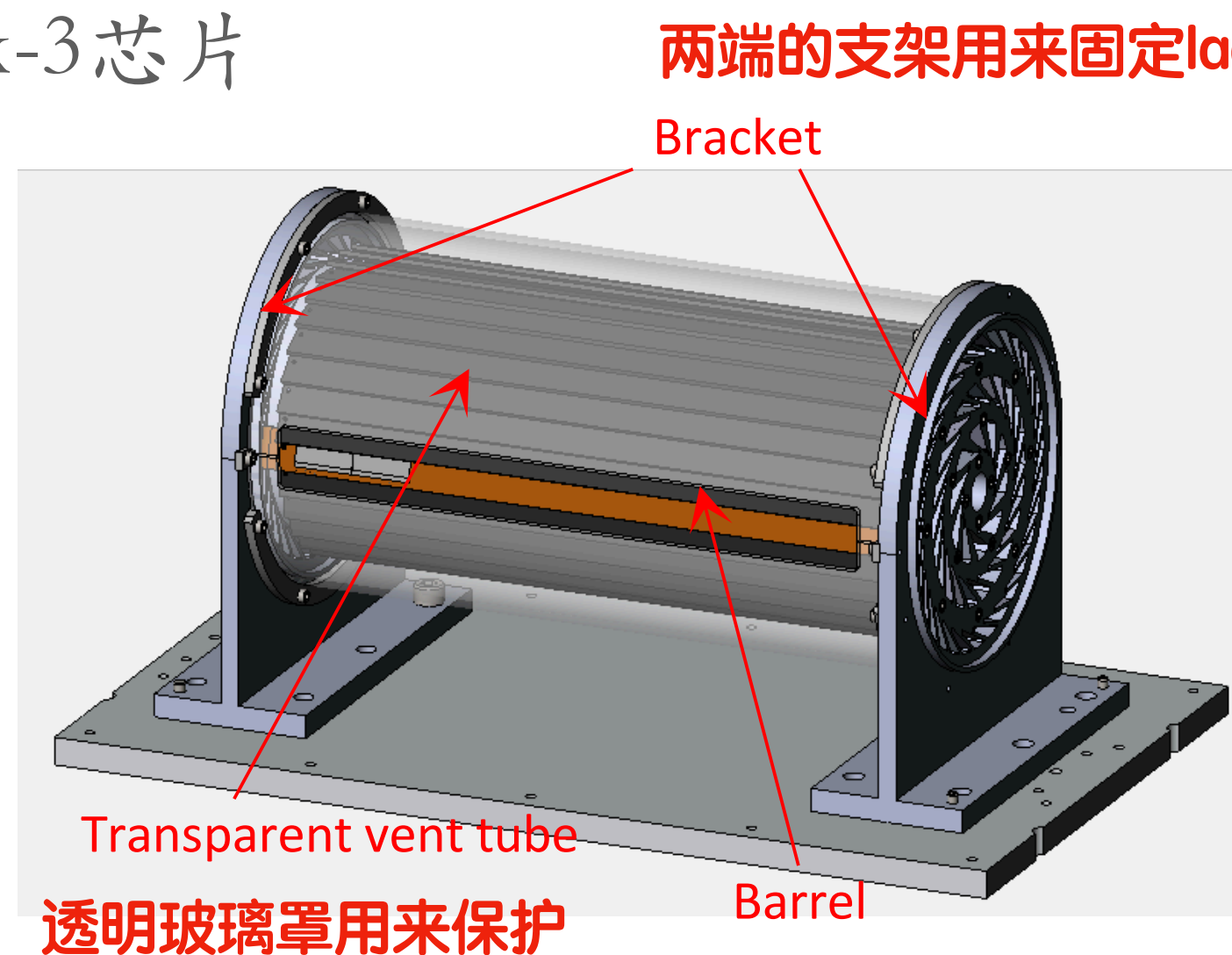
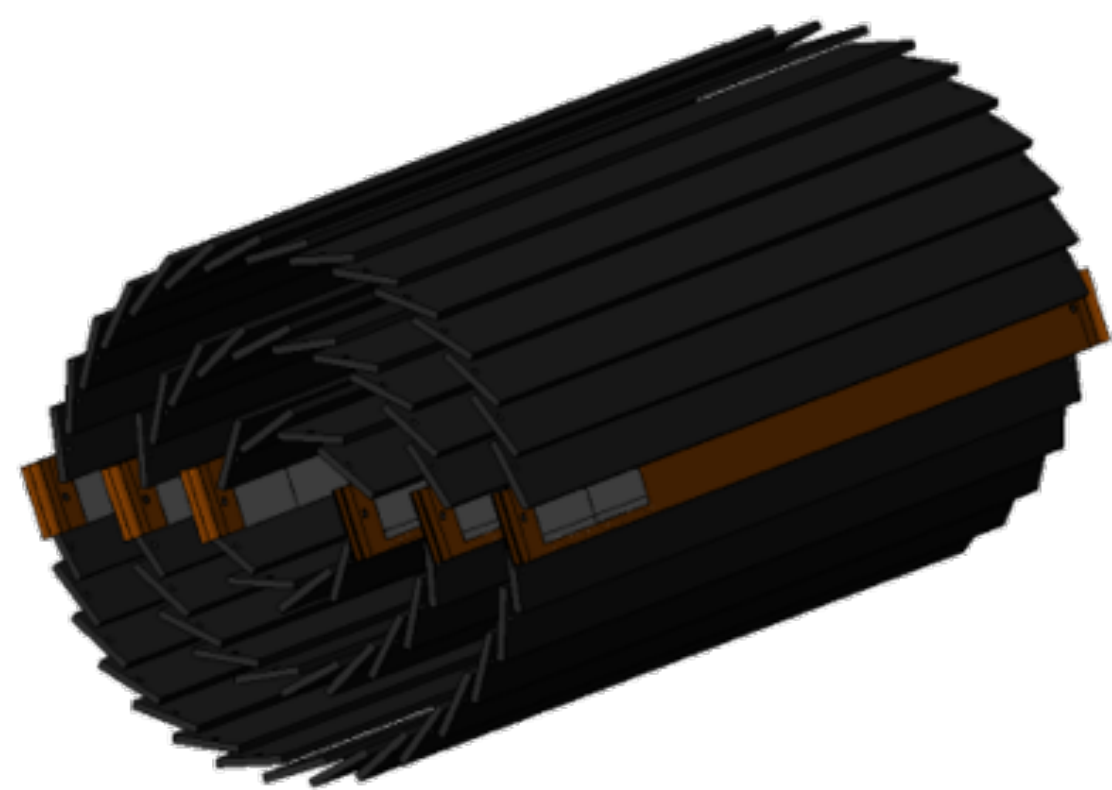
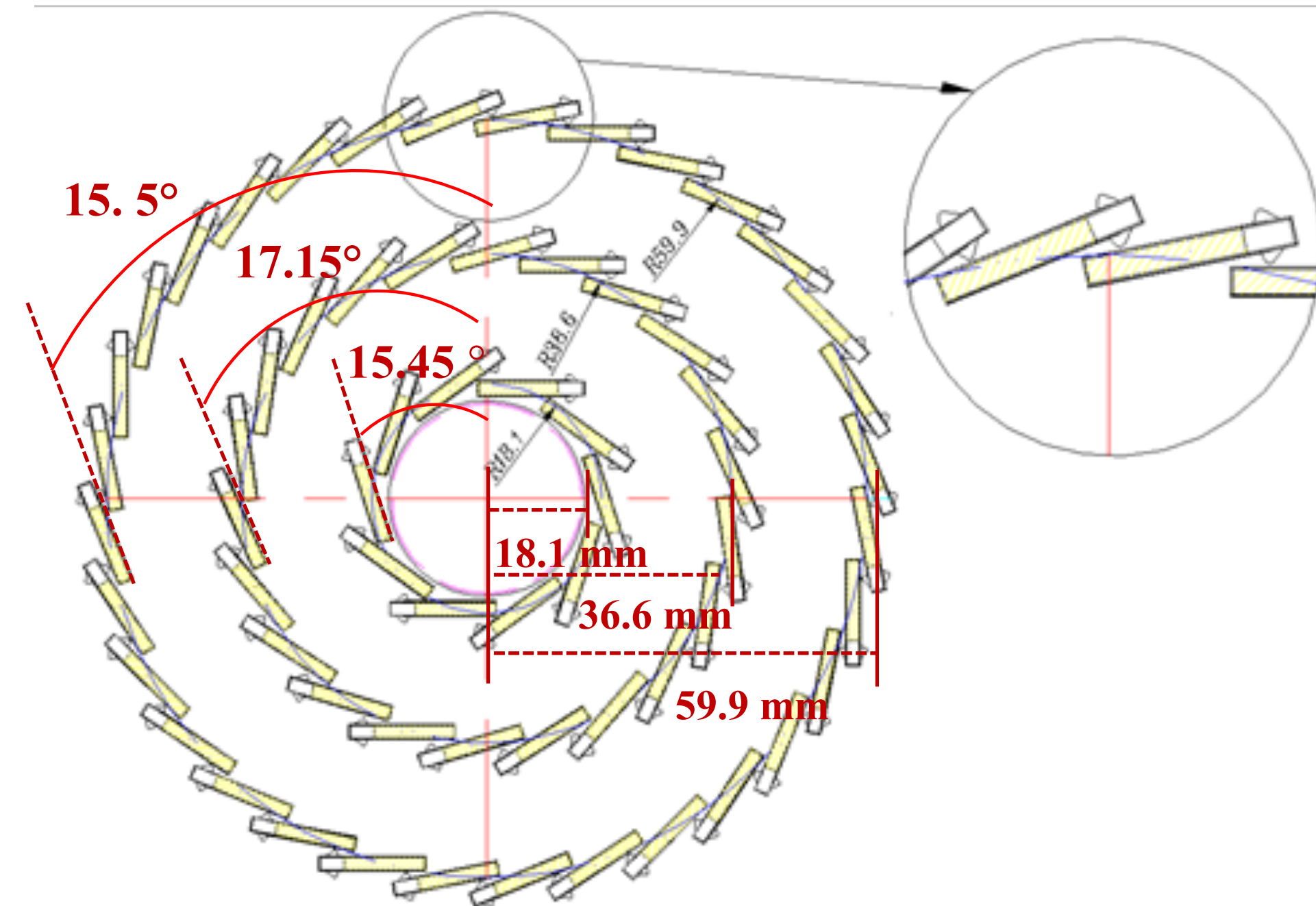
三层圆筒，每层圆筒最多可以放置 32, 22, 10 个ladders

在束流测试时，沿桶的径向安装了6个ladders

- 束流依次穿过 6 个 ladders
- 每个ladder与竖直方向存在一定夹角， 15.5° , 17.15° , 15.45°
- 桶的半径, $\sim 18.1\text{ mm}$, 36.6 mm , 59.9 mm

DESY 可提供的最大束斑面积是 $2.5\text{ cm} \times 2.5\text{ cm}$

- 每个Ladder的每侧安装了两个TaichuPix芯片
- 总共安装了24个TaichuPix-3芯片



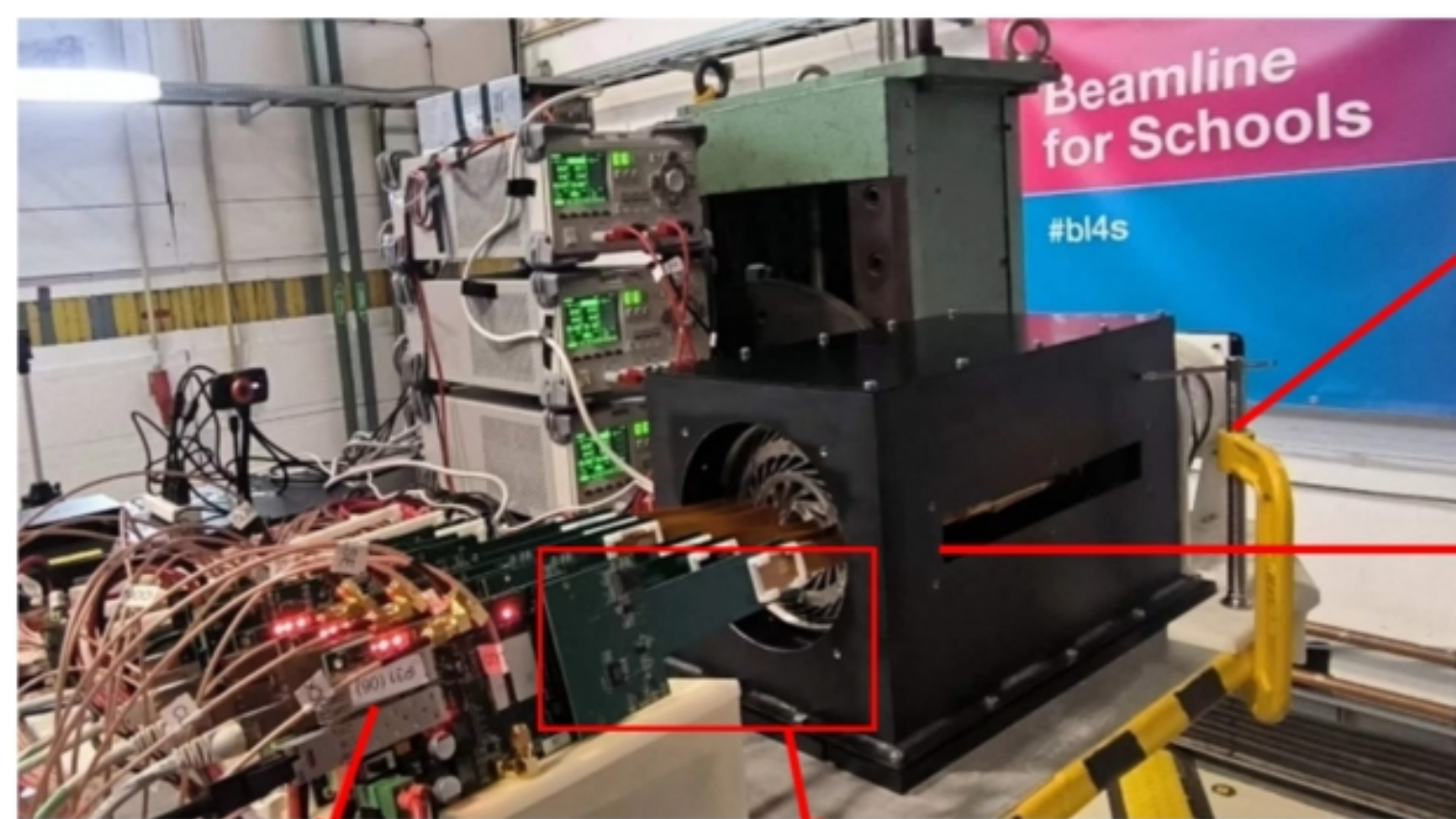
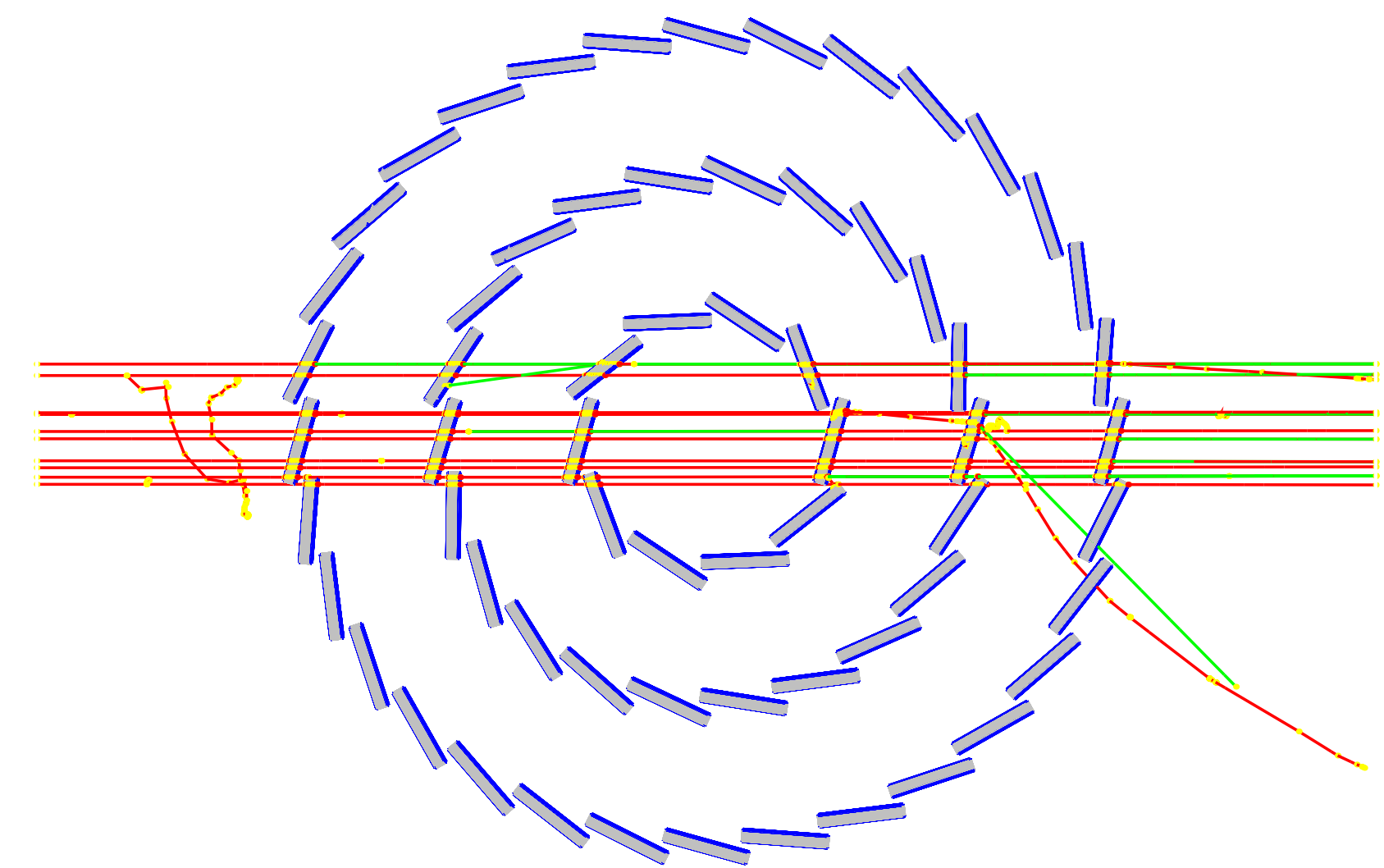
顶点探测器原型机的束流测试及性能分析

- 2023年4月对顶点探测器原型机在束流下进行了测试

DESY II 提供的 4 - 6 GeV 电子束流

风扇冷却装置使原型机的温度从 40°C \rightarrow 28°C ，保证了原型机良好的性能表现

- 取数期间电子学读出系统、数据获取系统稳定运行
- 最大数据率 $18 \text{ Mb} \cdot \text{s}^{-1}$
- 同样对两种工艺的TaichuPix-3芯片进行了研究

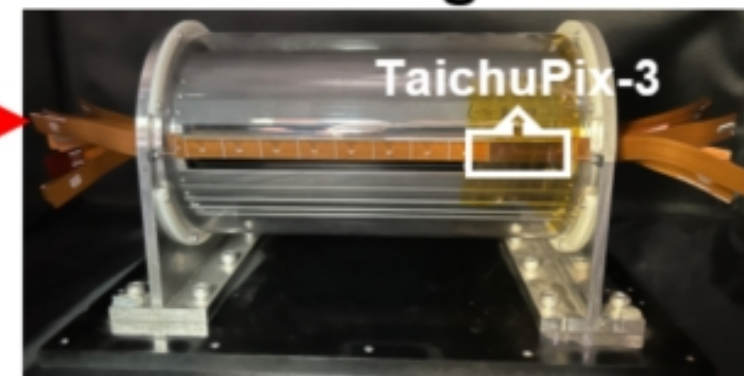


FPGA board

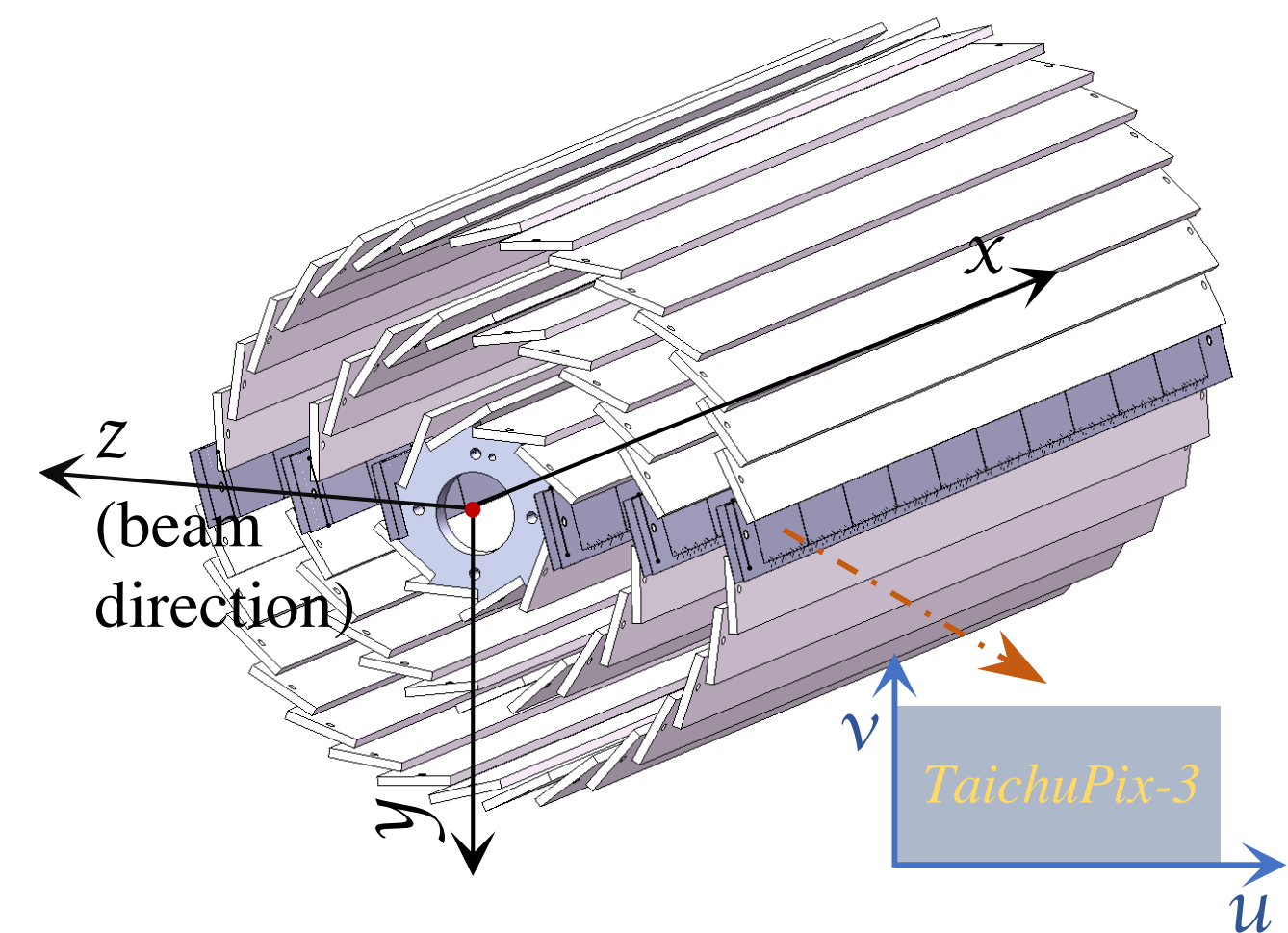
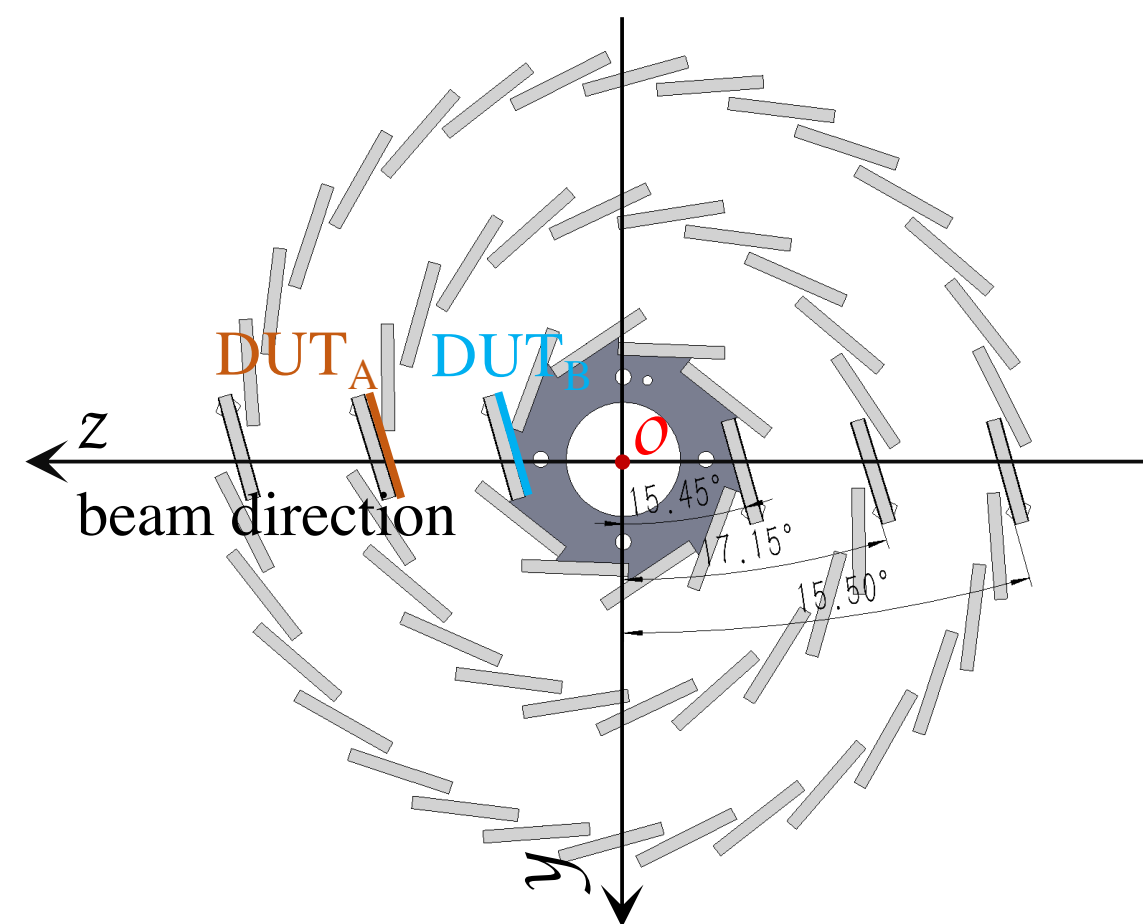
Interposer board



Air cooling fan



Baseline vertex detector prototype



- 6个ladders, 共24个芯片的击中图

- 缺失的芯片的击中信息不影响离线数据的分析

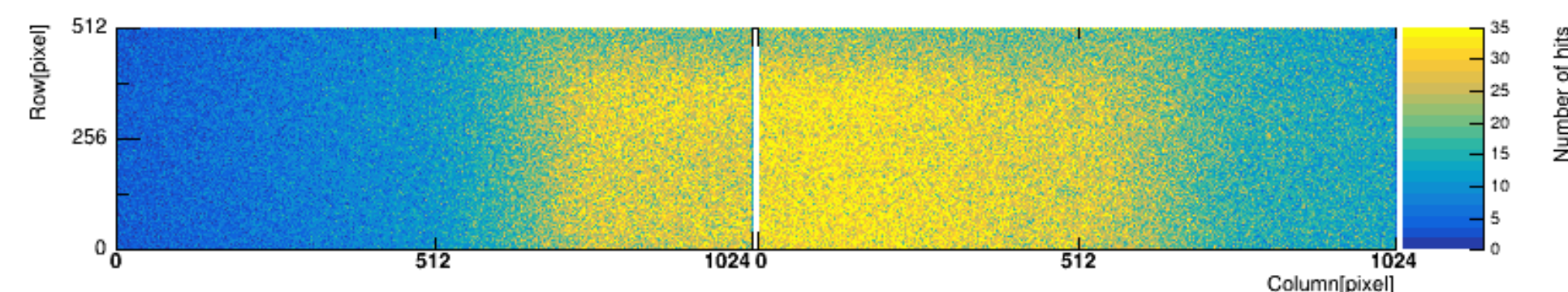
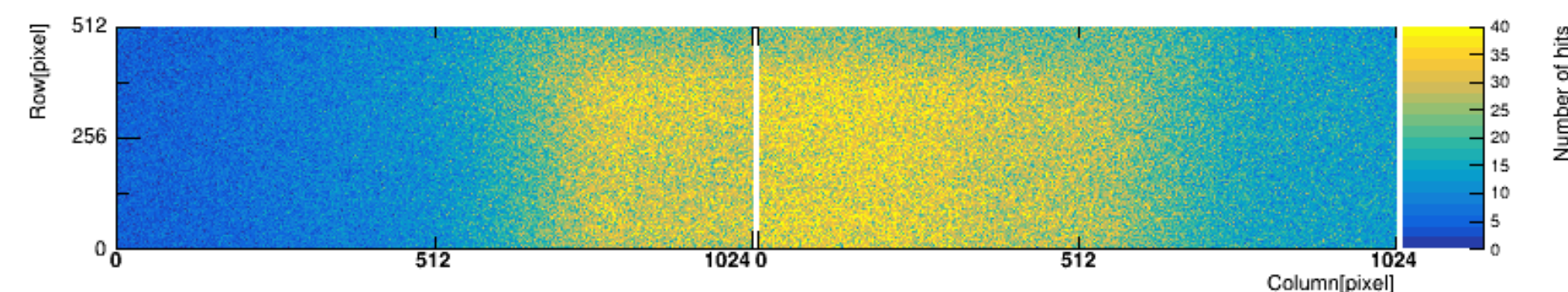
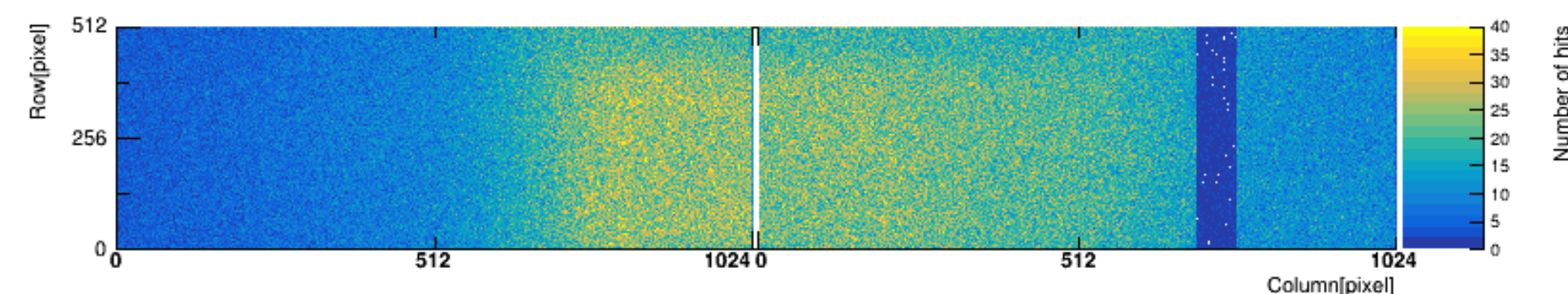
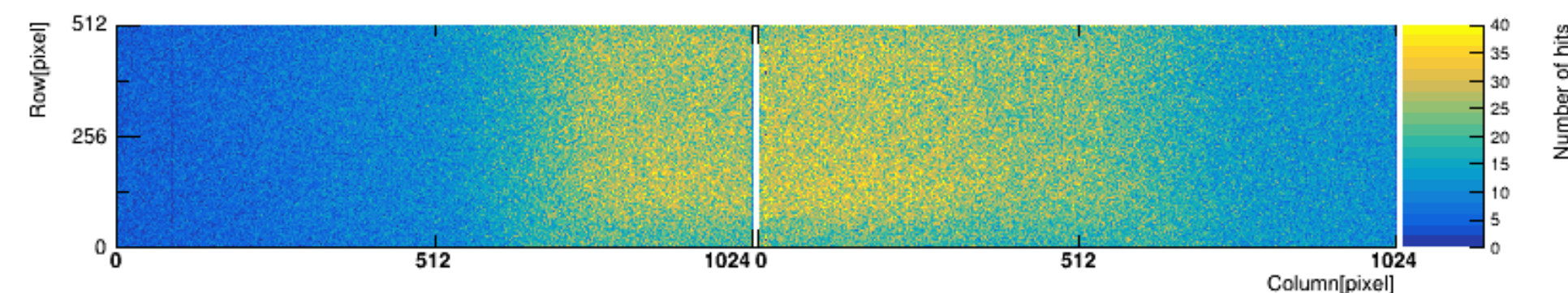
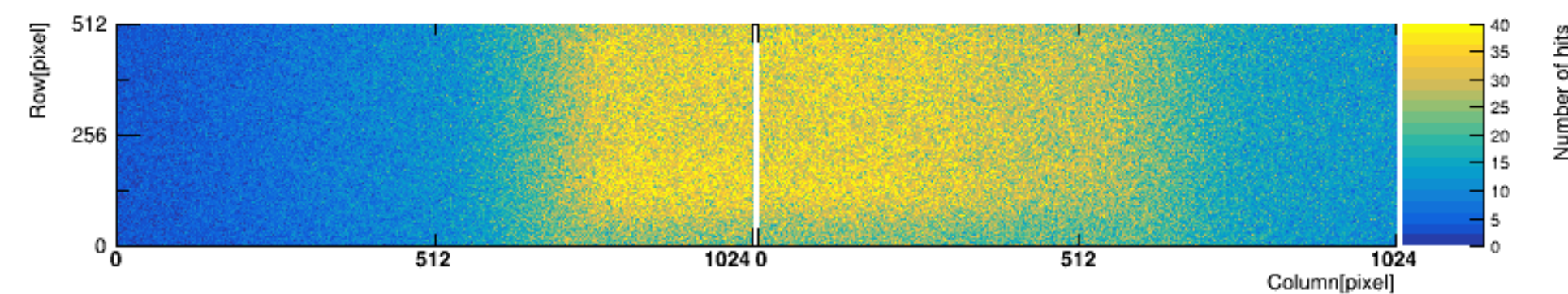
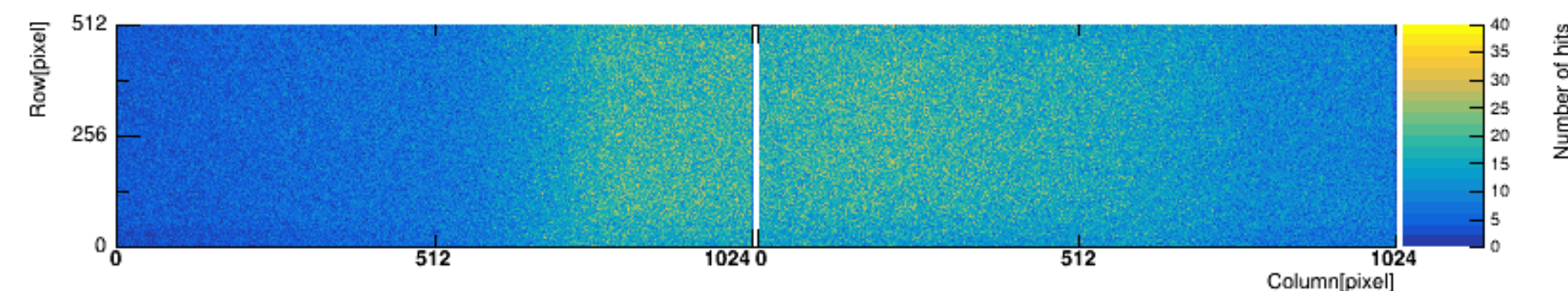
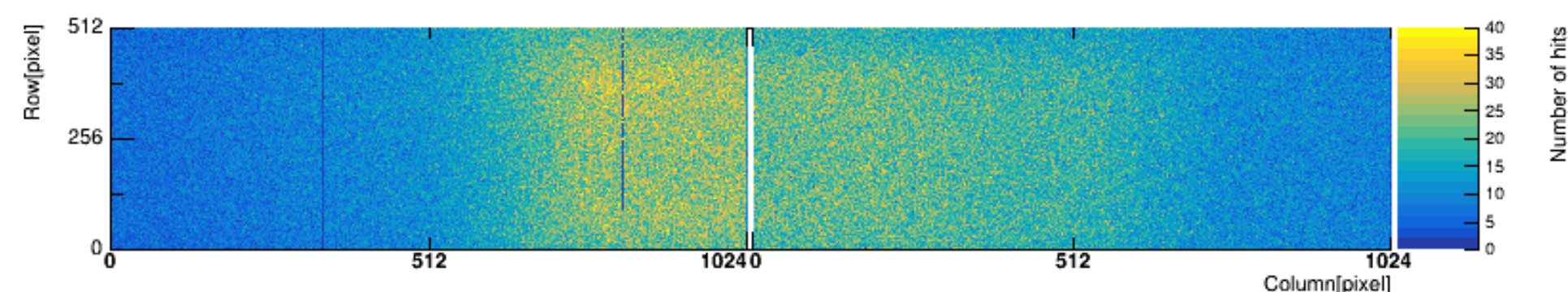
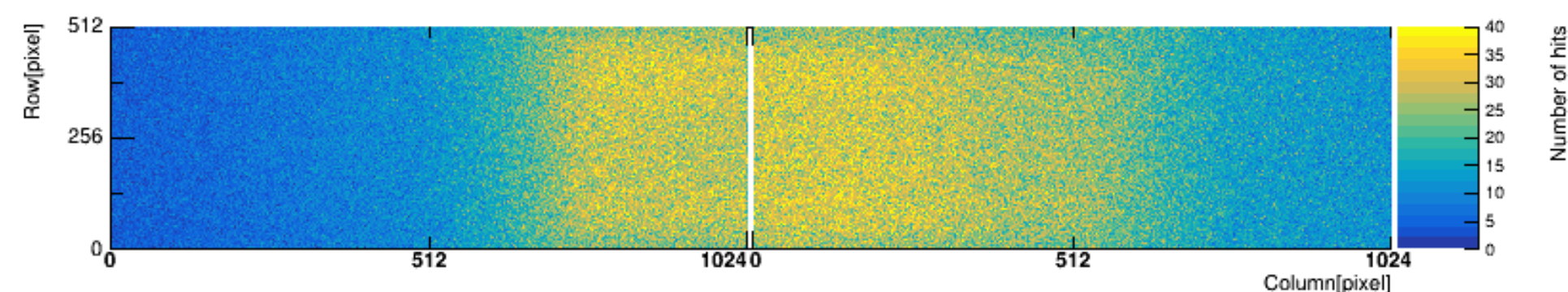
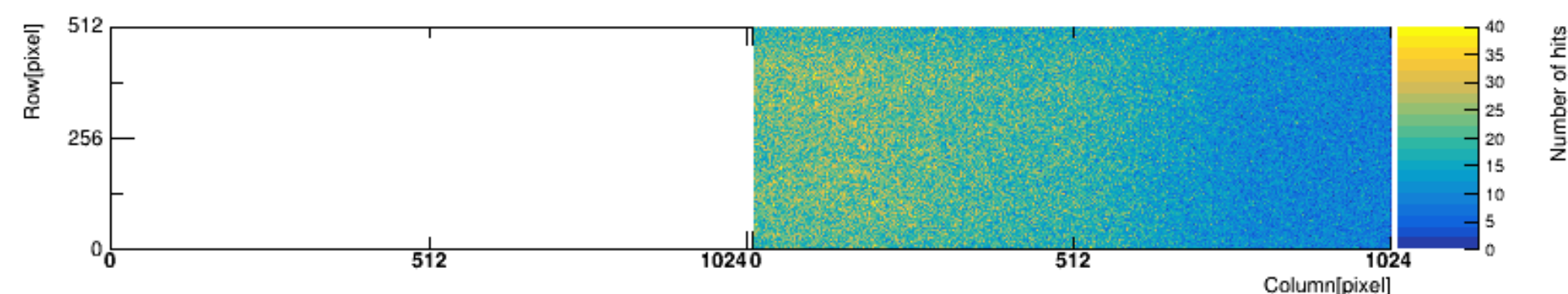
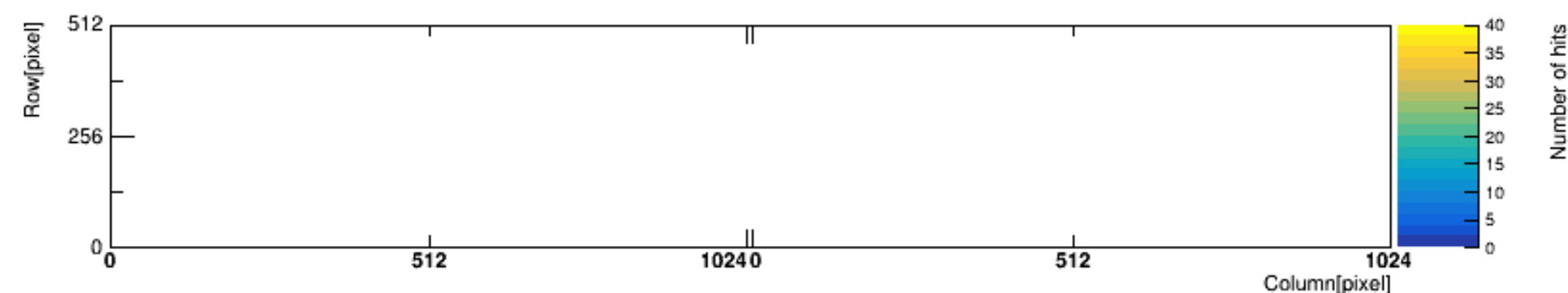
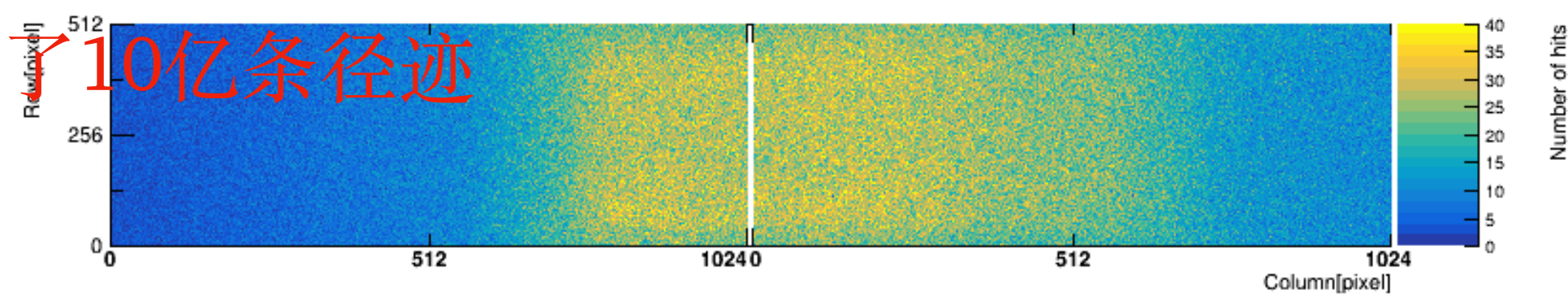
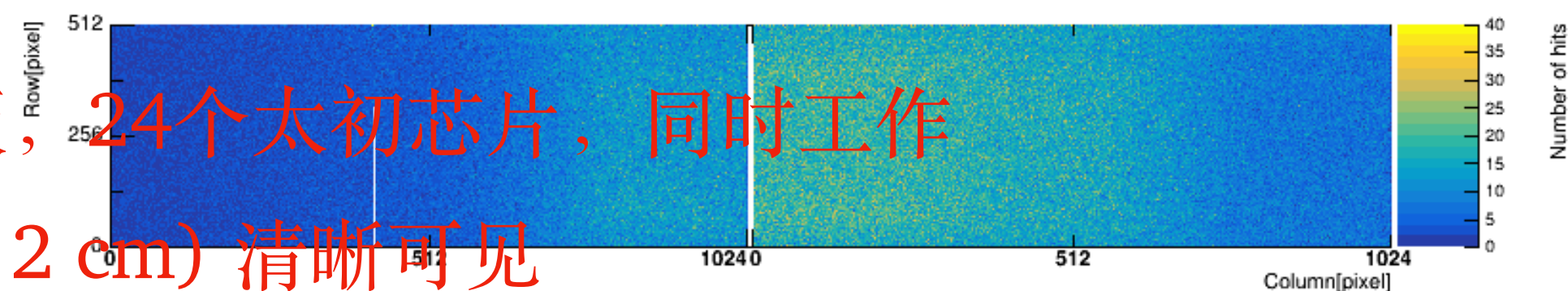
12个柔性电路板, 24个太初芯片, 同时工作

电子束斑 (~2 x 2 cm) 清晰可见

两周取数, 记录了10亿条径迹

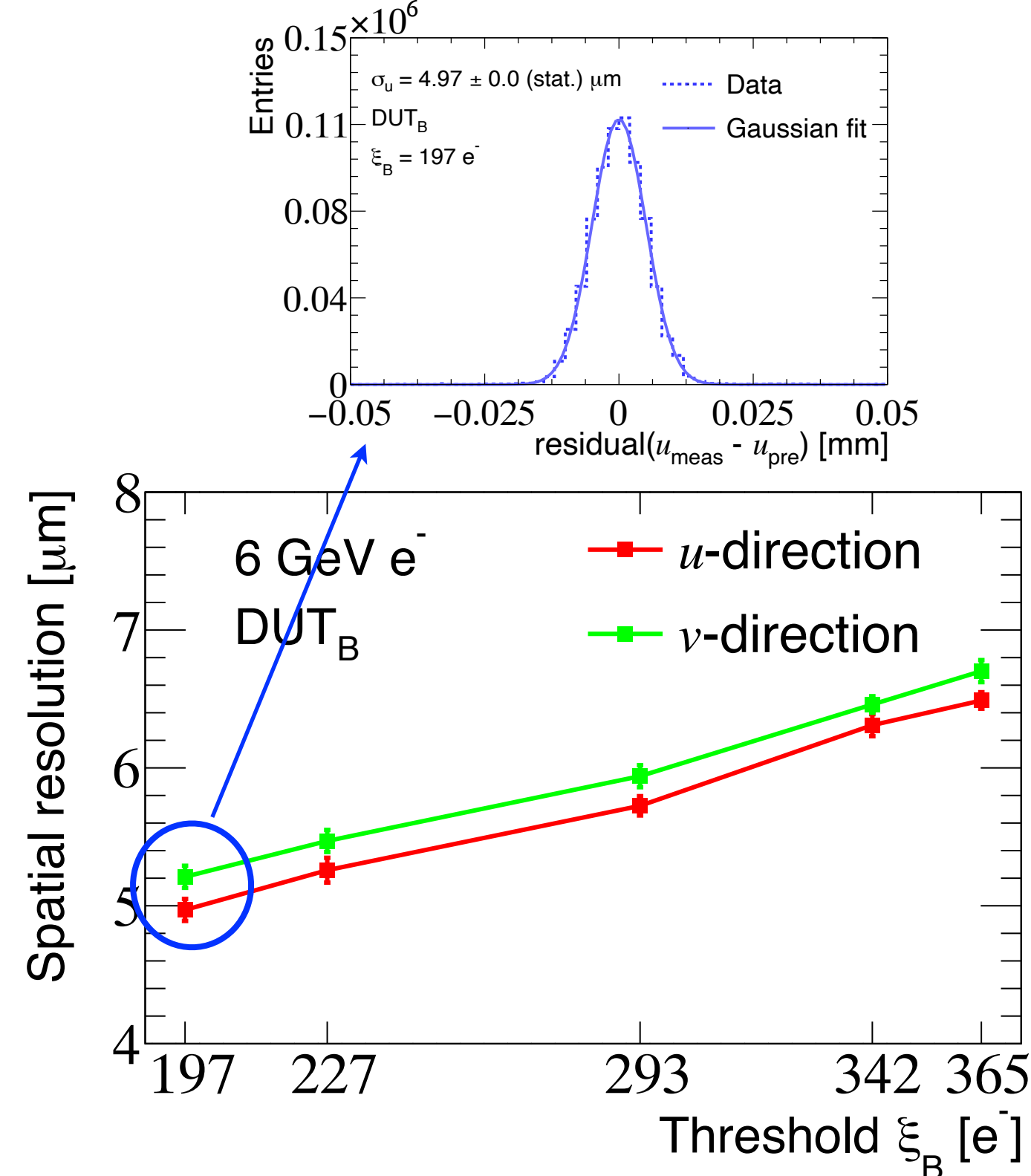
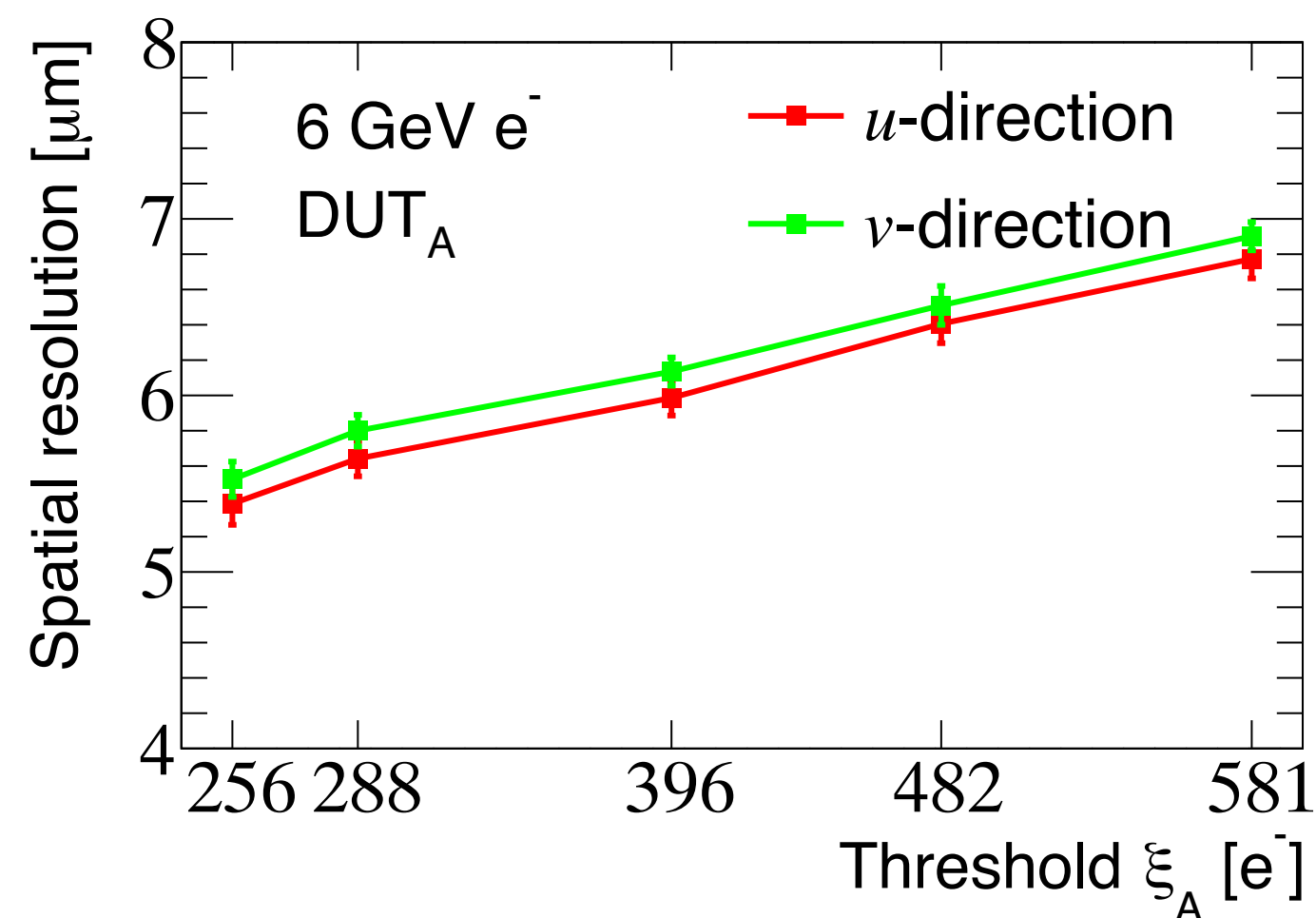
FPC 无法工作 <-

芯片无法正常取数 <-



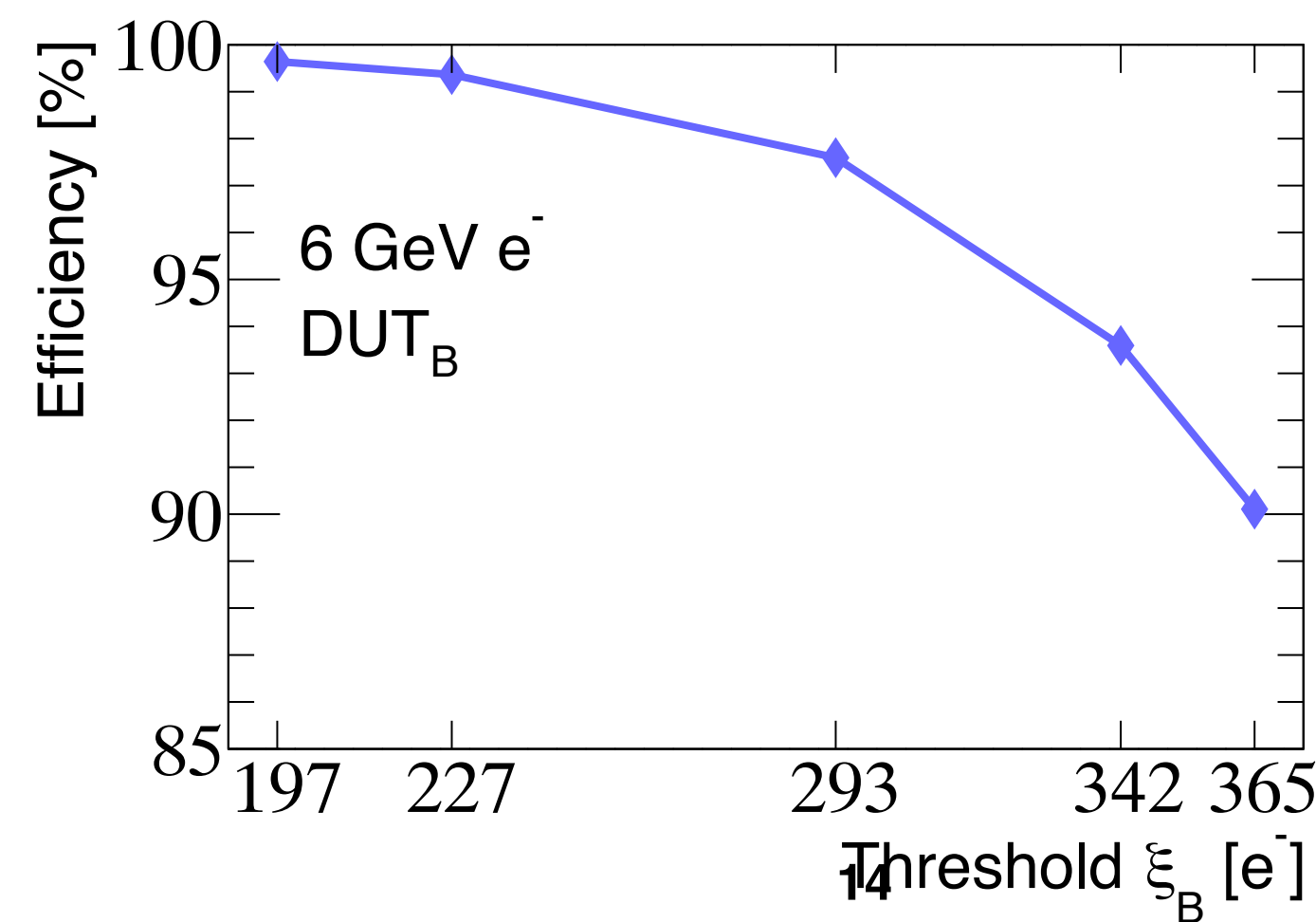
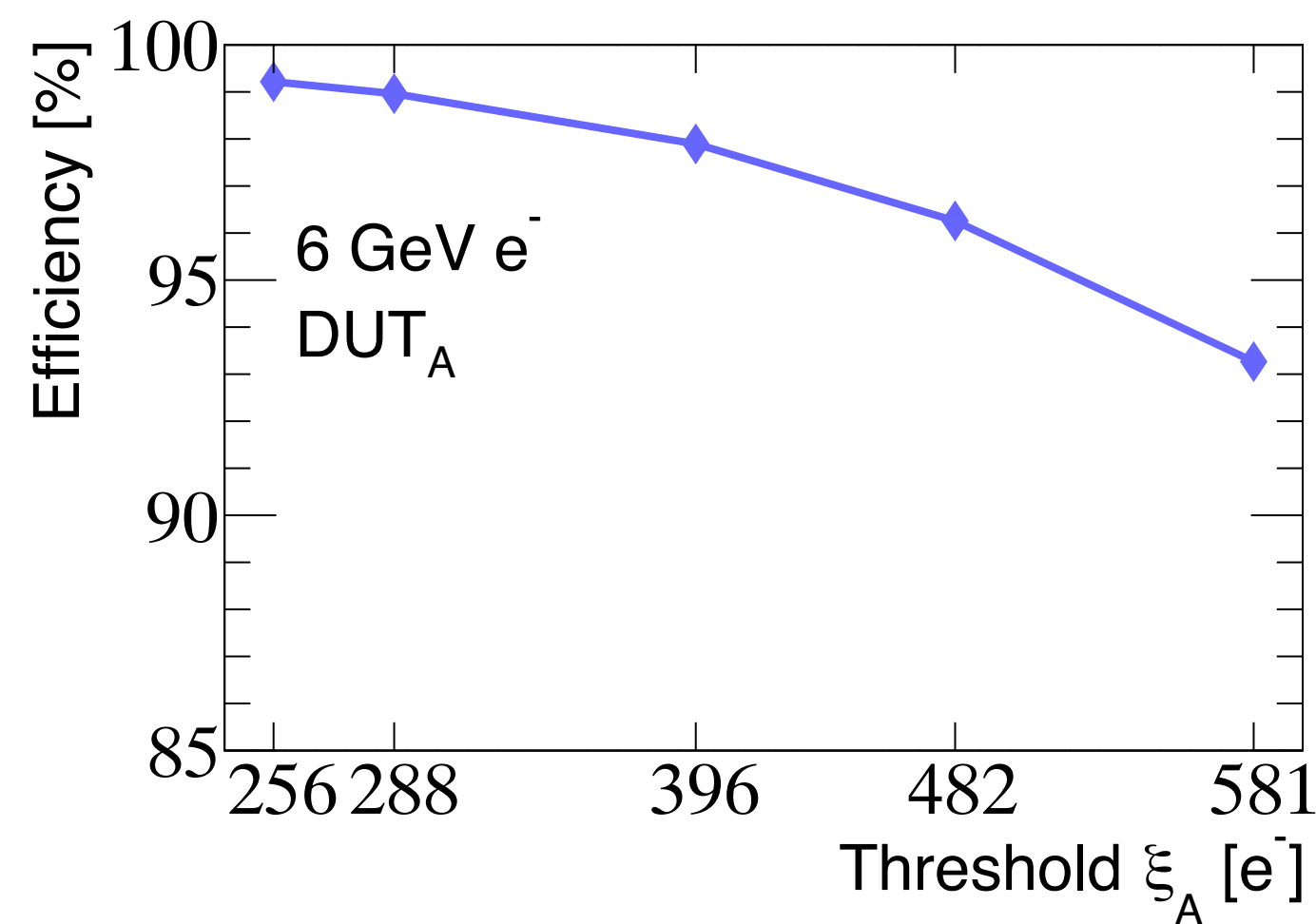
离线数据的分析结果

1. 空间分辨率



- 此处的空间分辨率是无偏残差的宽度
- 为了展示原型机的整体性能，没有减去参考径迹的不确定度
- 空间分辨率随阈值的增加而变差
 - > DUT_A: 5.4 μm
 - > DUT_B: 5 μm
- 系统误差来源
 - > : 11% 的散射角理论预测精度
 - > 5% 的束流能散

2. 探测效率



- 两种工艺的探测效率都可以达到 99 %

总结与展望

- 面向CEPC顶点探测器需求，开展TaichuPix芯片的研发
 - 经过三次流片实现了全尺寸全功能
 - 空间分辨率可达4.5 um, 探测效率 > 99 %
- 基于全尺寸太初芯片研制了国内第一个顶点探测器原型机
 - 空间分辨率达到 5 um, 探测效率 > 99 %

- 正在准备 CEPC 顶点探测器部分的Ref-TDR

• 从CDR到TDR的主要改变

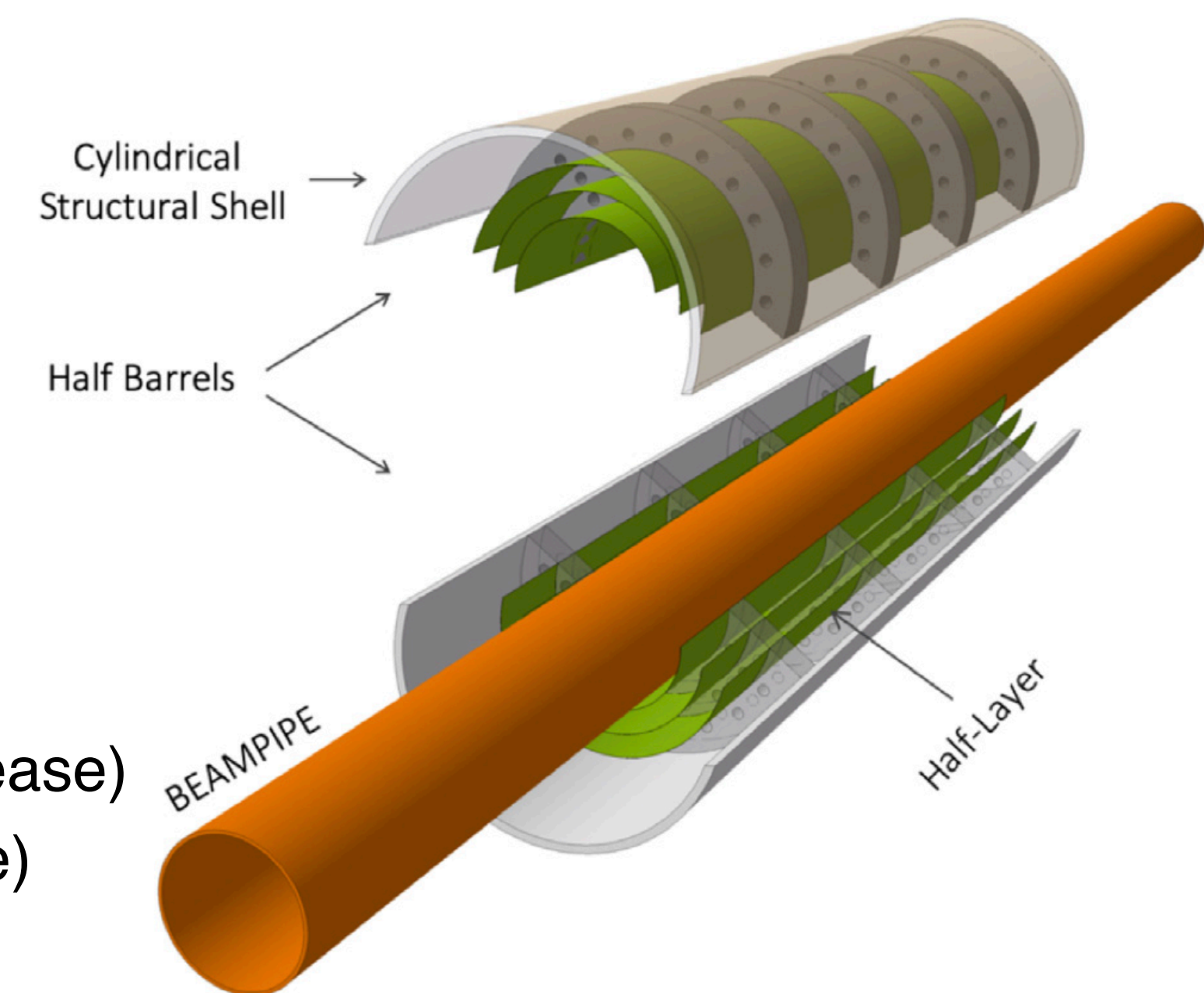
- 束流管直径: 28 mm (CDR) \rightarrow 20 mm (TDR)
- 瞬时亮度/IP:
 - Z pole: $32 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (CDR) \rightarrow $192 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (TDR, 50MW) (6 times increase)
 - ZH: $5.6 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (CDR) \rightarrow $8.3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (TDR) (\sim 1.5 times increase)

• Baseline option for silicon pixel chip moved to **CMOS stitching technology**

• CMOS ladder as back-up

• CEPC vertex 团队正在模拟和设计基于65nm工艺的太初芯片

• Stitching technology相应的几何和重建软件等也在为TDR准备中



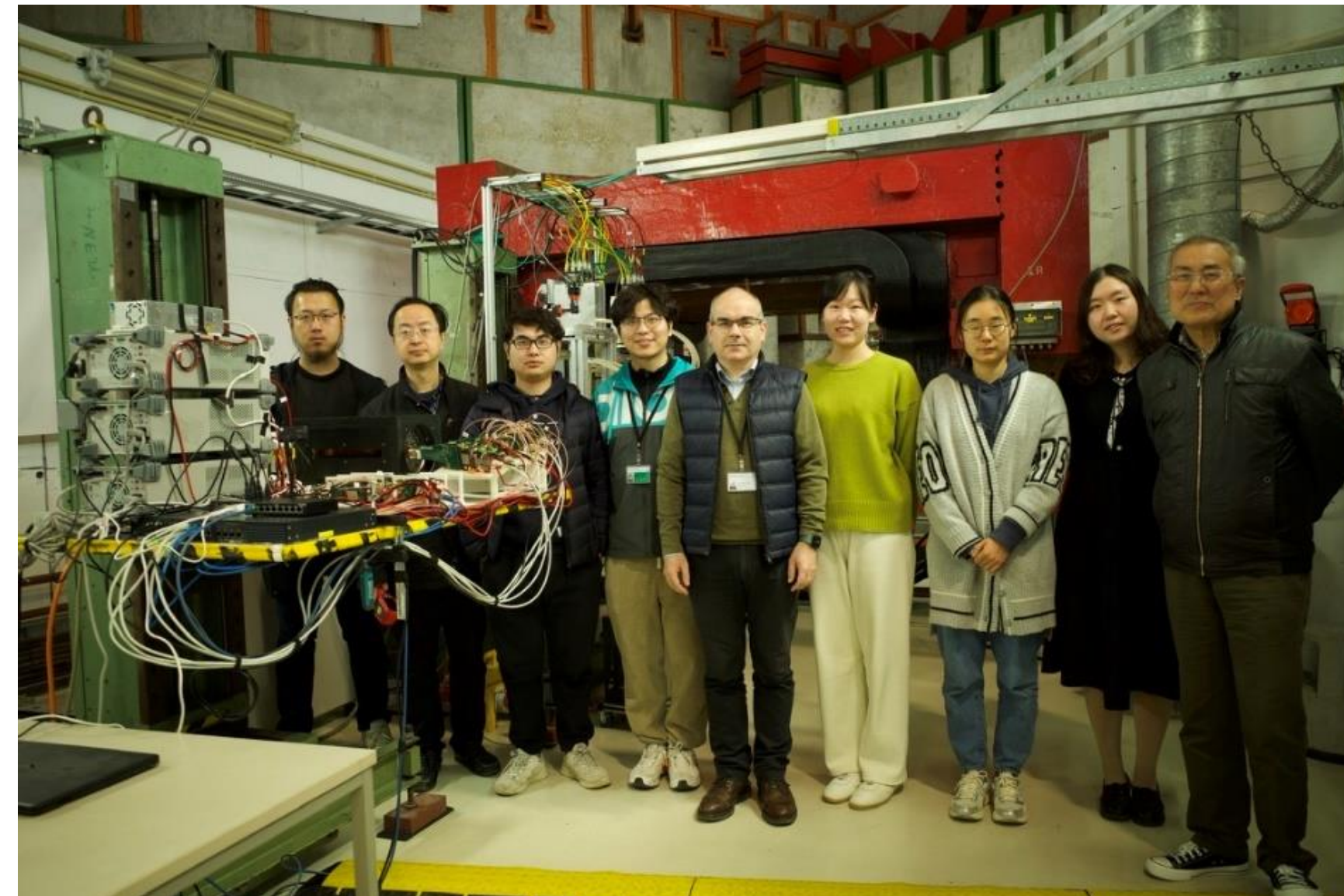
CEPC Vertex detector team

- IHEP, CAS, China: João Guimarães da Costa, Wei Wei, Zhijun Liang, Ying Zhang, Tianya Wu, Shuqi Li, Wei Wang, Jia Zhou, Ziyue Yan, Xinhui Huang, Hao Zeng, Xuwei Jia, Jun Hu, Jinyu Fu, Hongyu Zhang, Gang Li, Linghui Wu, Mingyi Dong, Xiaoting Li, Weiguo Lu, etc.
- Nanjing University: Ming Qi, Lei Zhang, Xiaoxu Zhang, Yiming Hu, etc.
- Northwestern Polytechnical University: Xiaomin Wei, Jia Wang, Ran Zheng, etc.
- Shandong University: Liang Zhang, Jianing Dong, etc.
- IFAE, Barcelona, Spain: Sebastian Grinstein, Raimon Casanova, etc.

2022.12 @ DESY II TB21 for TaichuPix-3 telescope level tests



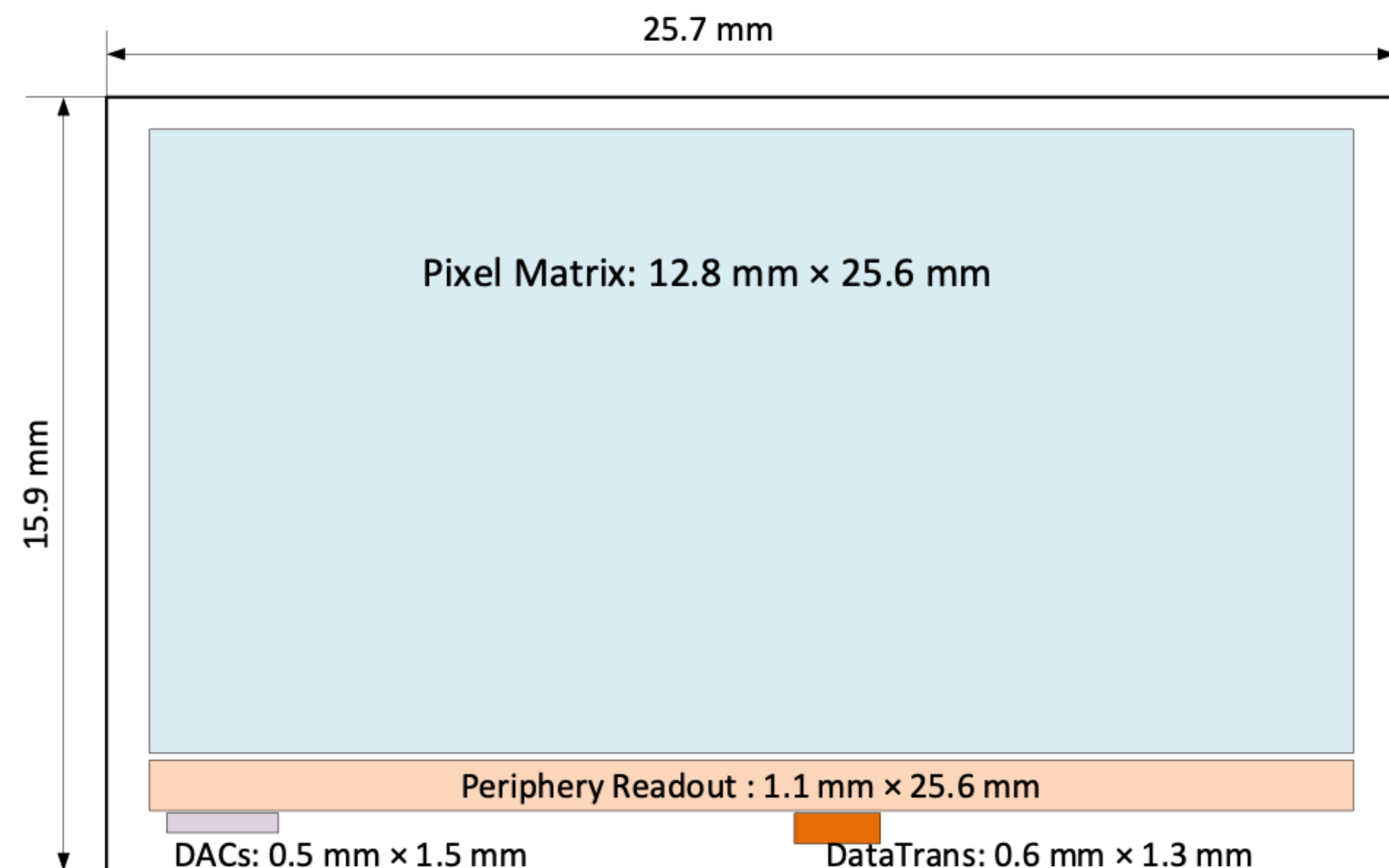
2023.04 @ DESY II TB21 for prototype level tests



VTX像素芯片功耗分布估算

(from [Weiwi.Ying](#))

➤ Power consumption estimation is based on 25*25um pixel size

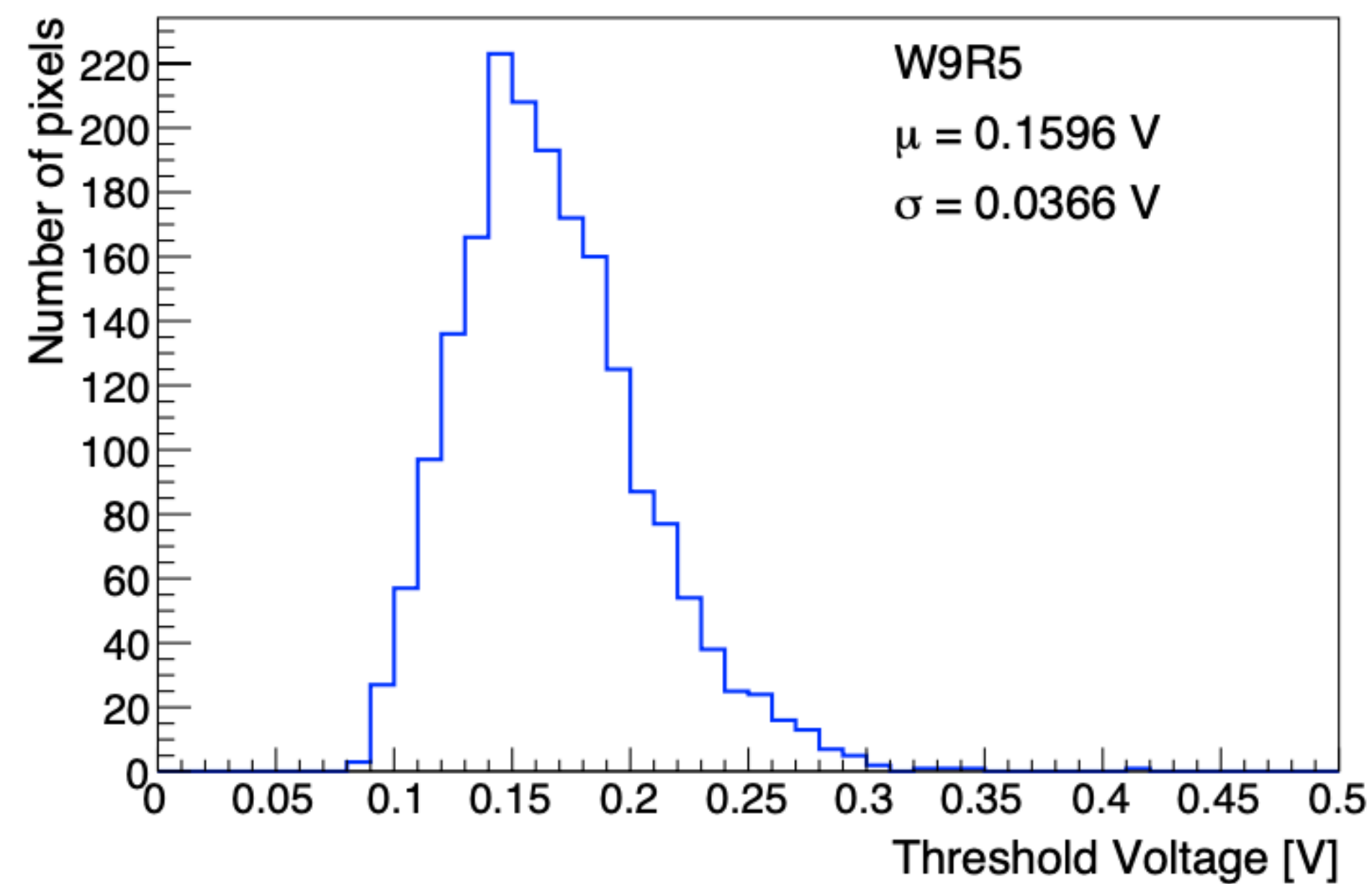
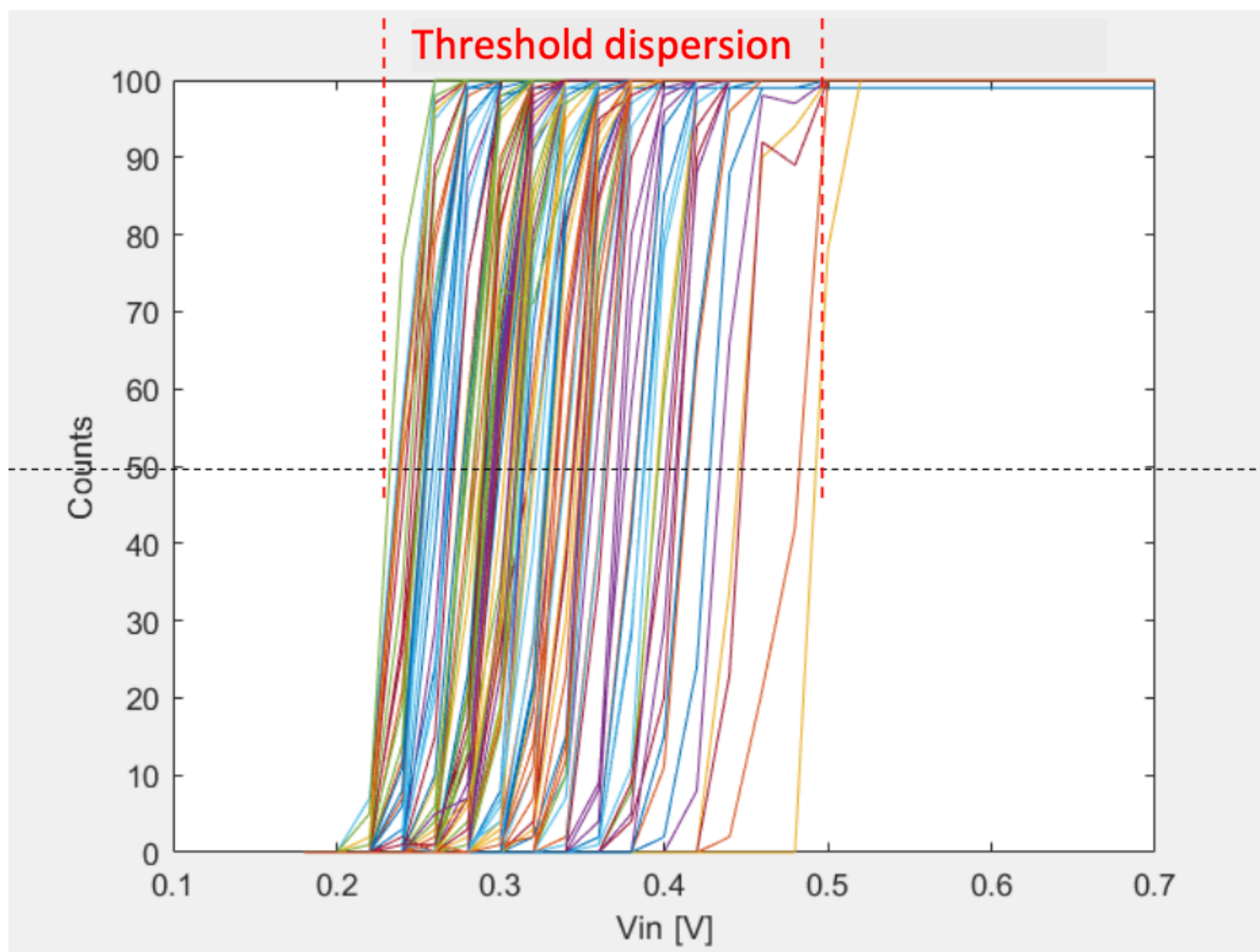
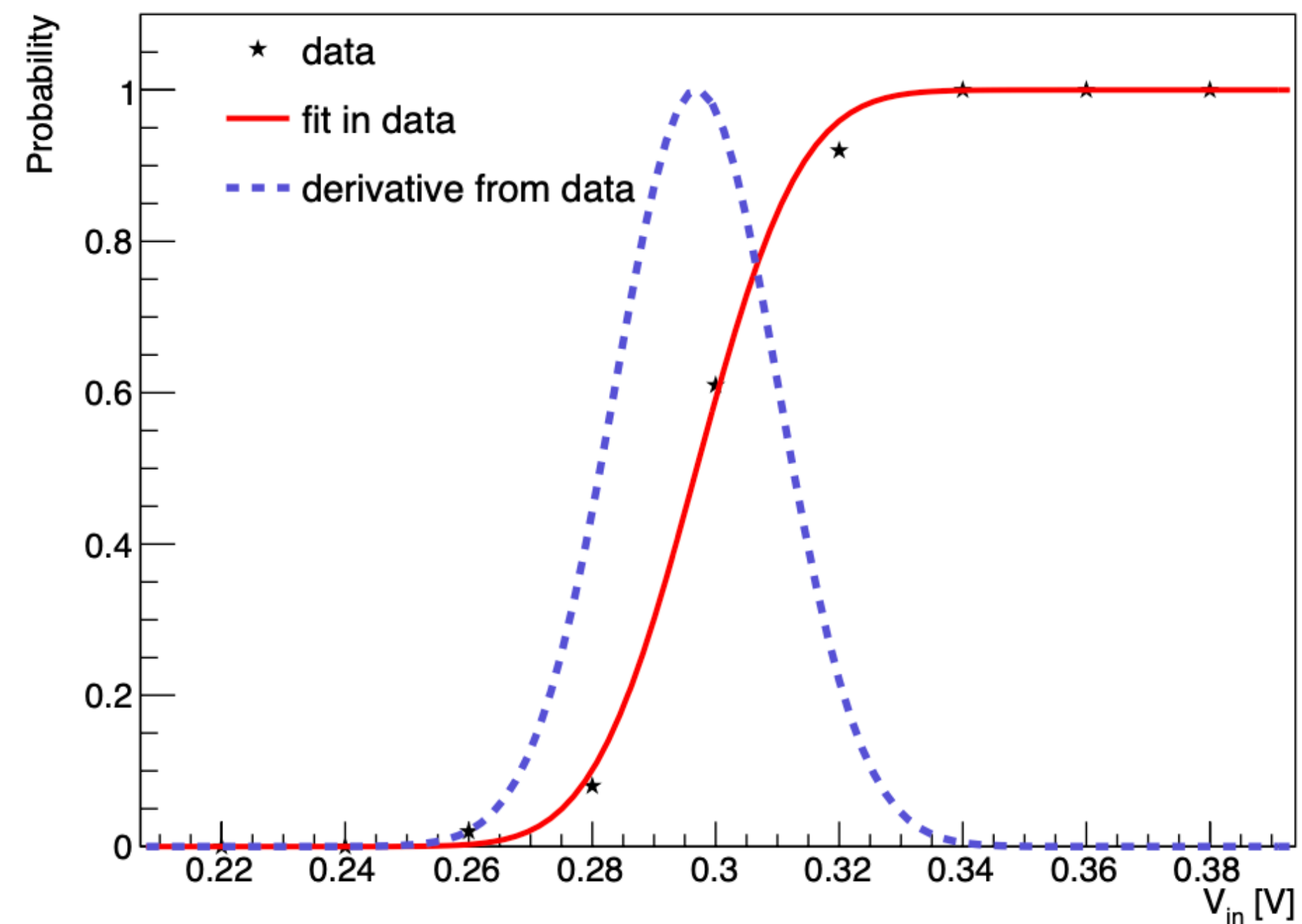


估算说明:

- 太初3芯片: 180 nm工艺, 电源1.8 V;
- 65 nm芯片: 电源1.2 V;
- Data rate@Triggless-CDR: 4.48 Gbps /chip
bunch spacing (min.): 25 ns需要快前沿前端
- Data rate@Triggless-TDR (Low Lumi):
1 Gbps/chip
- Low Lumi@TDR: bunch spacing ~几百ns, 像素前端不需要快前沿, Matrix功耗可降低到60 mW

	Matrix	Periphery	DataTrans.	DACs	Total Power
太初3芯片 @ triggerless (CDR)	304 mW	135 mW	206 mW	10 mW	655 mW
65nm 芯片 @ 1 Gbps/chip (TDR LowLumi)	60 mW	80 mW	36 mW	10 mW	186 mW

片内像素间阈值的不均匀性。TaichuPix-3 芯片 W9R5 的芯片像素在 ITHR DAC code = 16 时的阈值以及瞬态噪声分布如图 6-12 所示，根据公式 (6-1)，平均阈值大约为 $175 e^-$ ，固定模式噪声为 $\sim 40 e^-$ ，瞬态噪声为 $\sim 11 e^-$ 。



3. 对撞参数 (Impact parameter) 分辨率

- 对撞参数的定义
 - > 径迹与初级顶点的垂直距离
- 初级顶点
 - > 穿过 6 个 ladders 的径迹被分成上游径迹和下游径迹
 - > 上游径迹和下游径迹与 $z = 0$ 平面交点的中心
- IP 的分辨率
 - > 径迹与PV的垂直距离的分布的宽度
 - > 分辨率大约是 $5.1 \mu\text{m}$

