LHCb 探测器升级
中国团队的贡献

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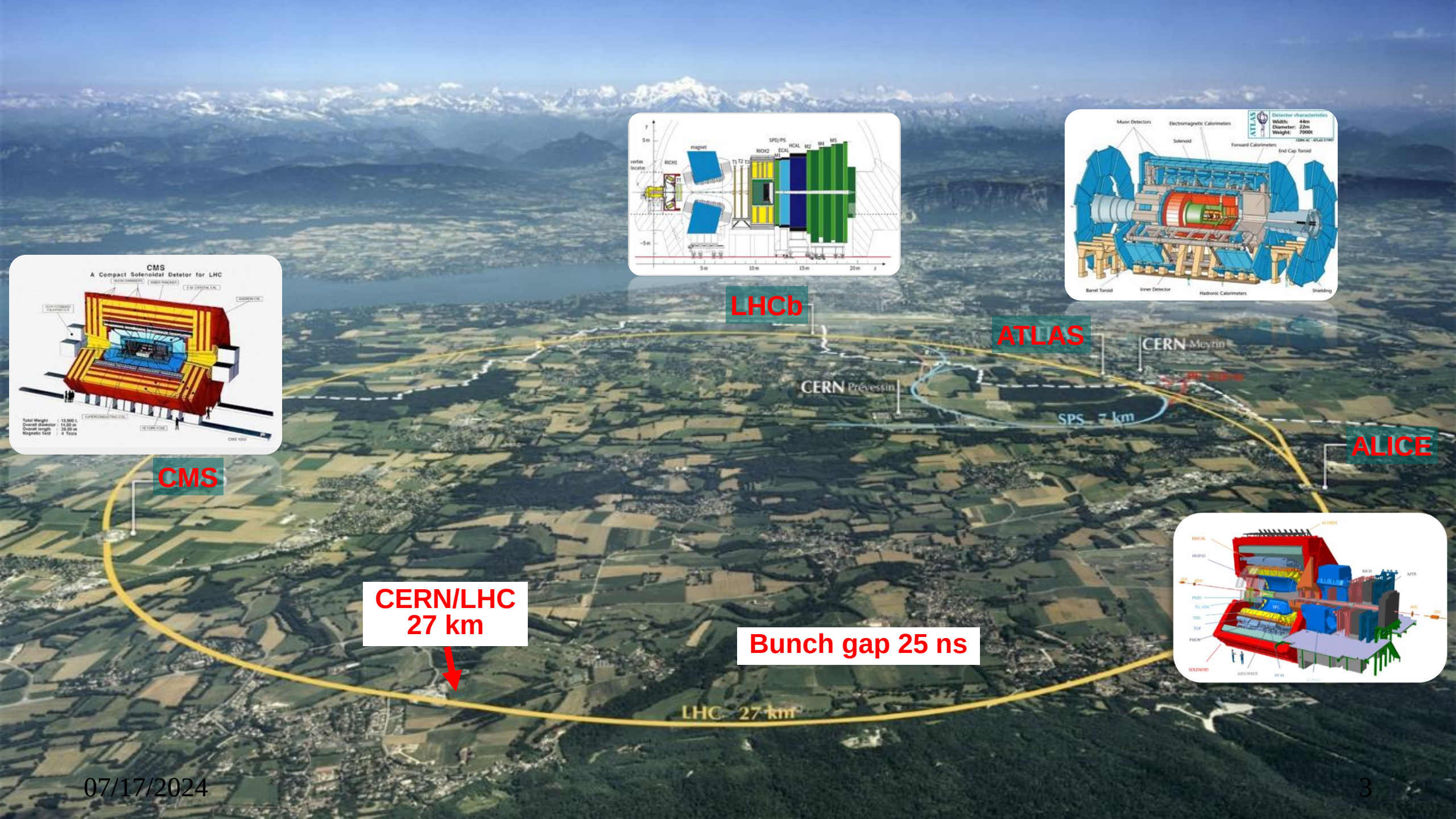
For the LHCb Chinese Team

NED & CAGD2024, July 15-17, 2024, Qingdao

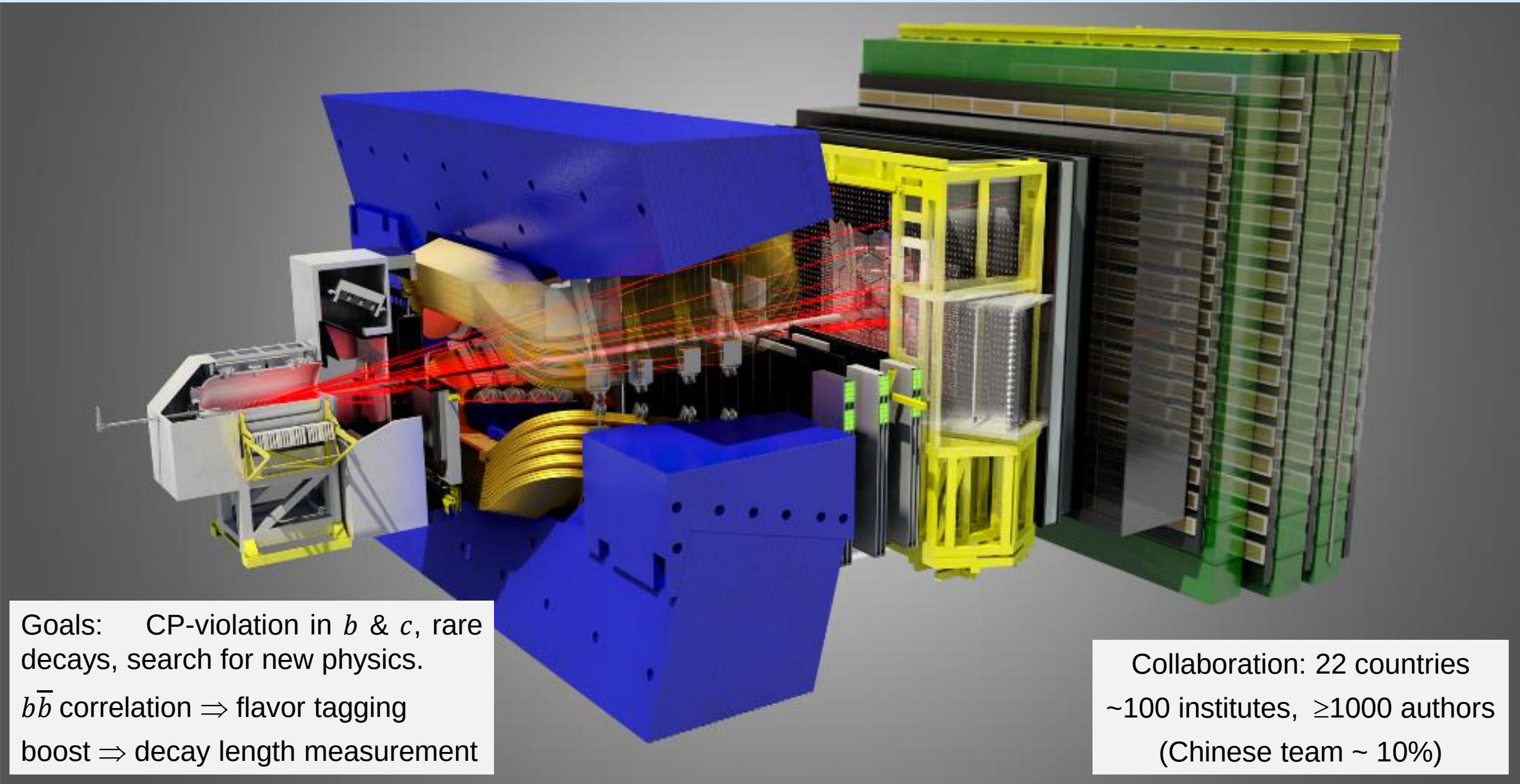
报告提纲

- LHCb 探测器和升级简介
- 中国团队在LHCb升级中
  - 一期升级：闪烁光纤径迹探测器 SciFi
  - 一期升级：上游径迹硅微条探测器 UT
  - 二期升级：上游径迹硅像素探测器 UP
  - 二期升级：电磁量能器 PicoCal / SPACAL
- 小结

中国团队在物理分析、模拟、实时分析等方面做出很多显著成绩，本报告只聚焦硬件方向的贡献


CMS
A Compact Solenoidal Detetor for LHC
LHCb
ATLAS
CERN Meyrin
CERN Prévessin
SPS 7 km
ALICE
CMS
CERN/LHC
27 km
Bunch gap 25 ns
LHC 27 km

LHCb – A Forward Spectrometer @ LHC



Goals: CP-violation in b & c, rare decays, search for new physics.

$b\bar{b}$ correlation $\Rightarrow$ flavor tagging

boost $\Rightarrow$ decay length measurement

Collaboration: 22 countries

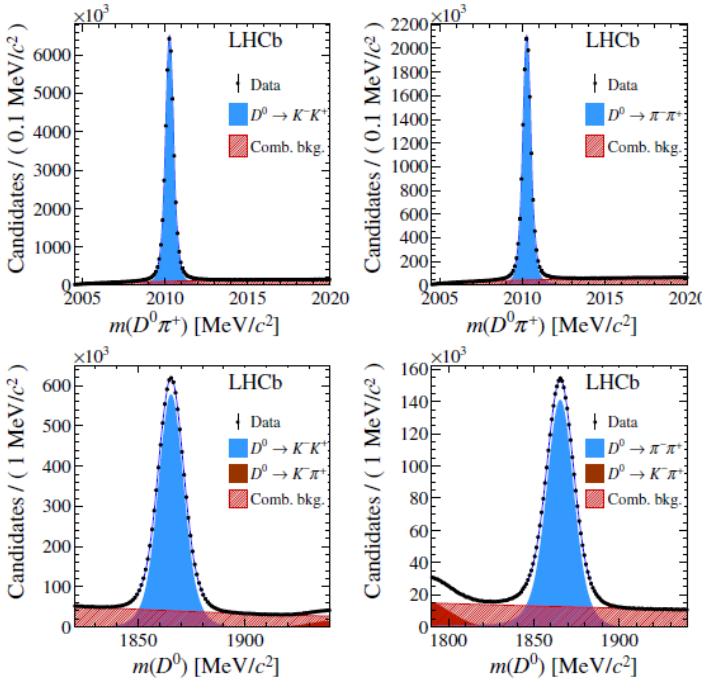
~100 institutes, ≥1000 authors

(Chinese team ~ 10%)

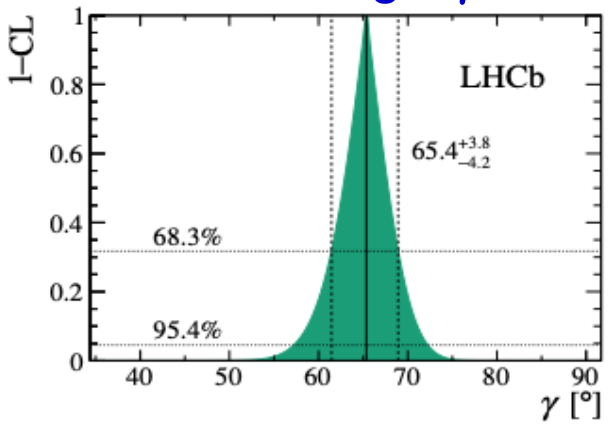
LHCb Physics Performance

Selected precision measurements

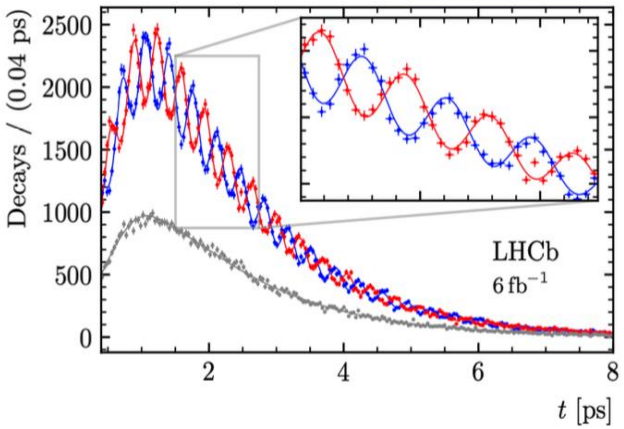
CPV in Charm decays



CKM angle γ

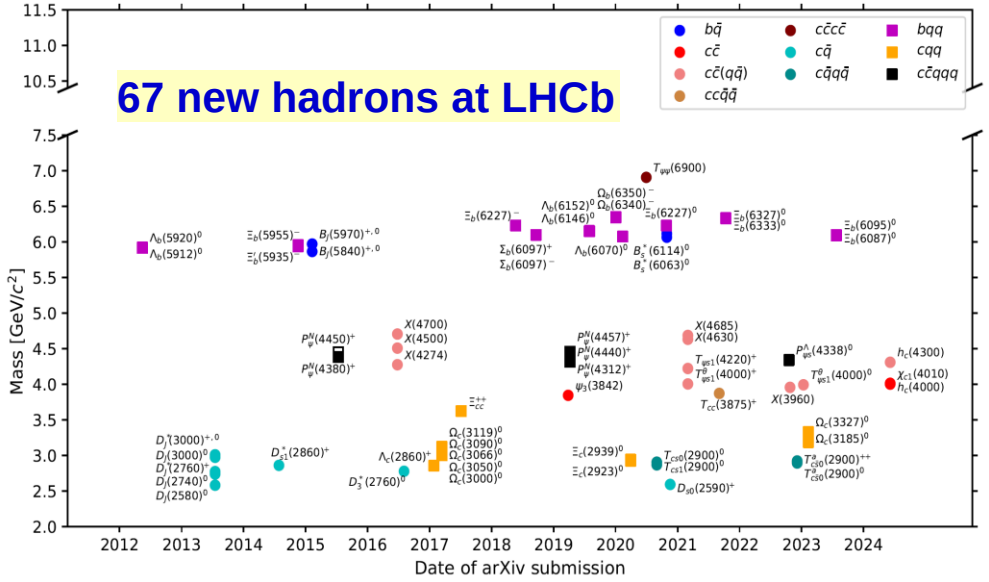


Δm_s



- Phys. Rev. Lett. 122 (2019) 211803
- JHEP 12 (2021) 141
- Nature Physics 18, (2022) 1-5

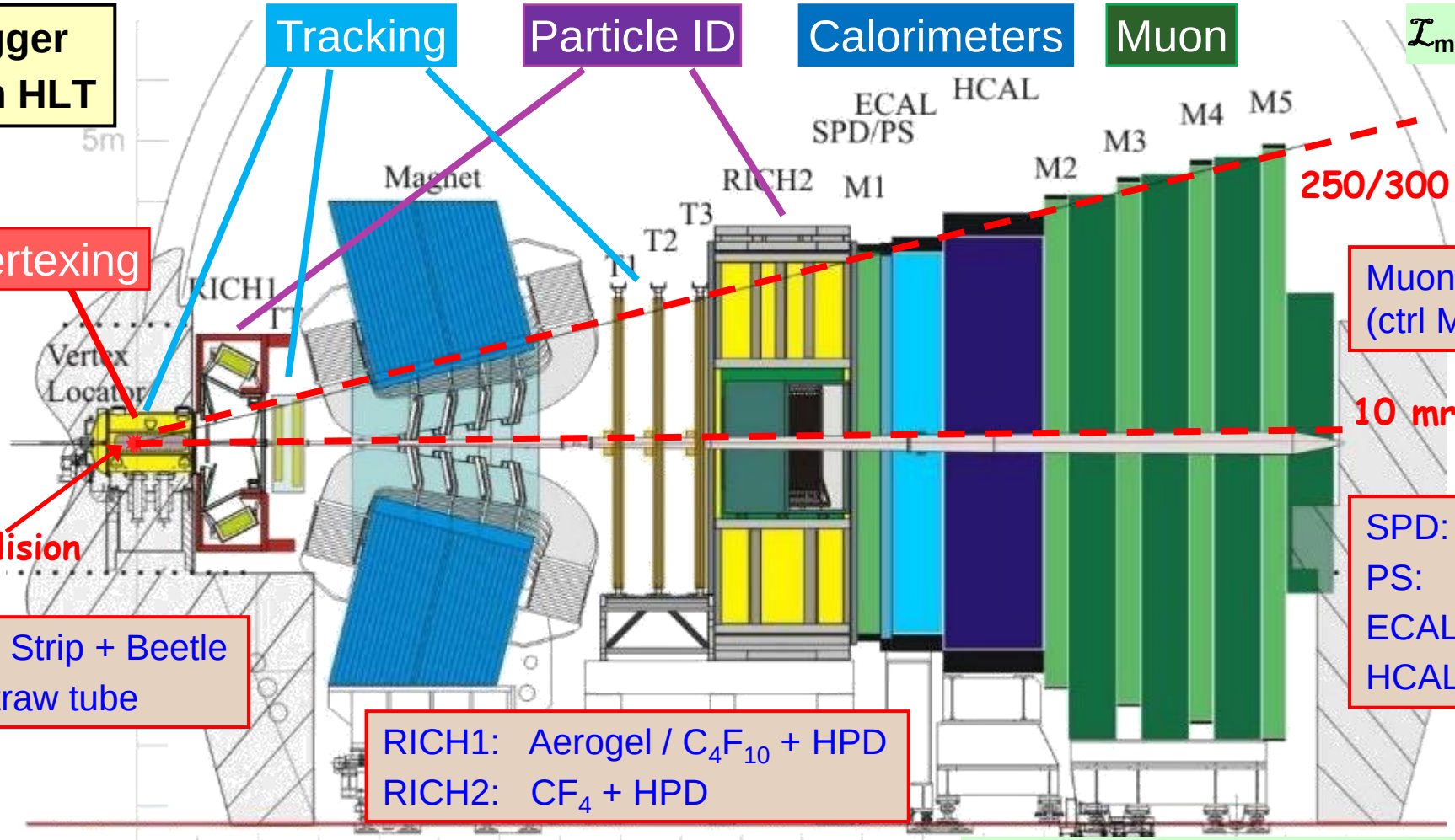
LHCb contributed a series of discoveries and precision measurements



LHCb Base Detector

Hardware trigger
Computer farm HLT

$\mathcal{L}_{max}$ ~ 4×10^{32} cm^{-2}s^{-1}

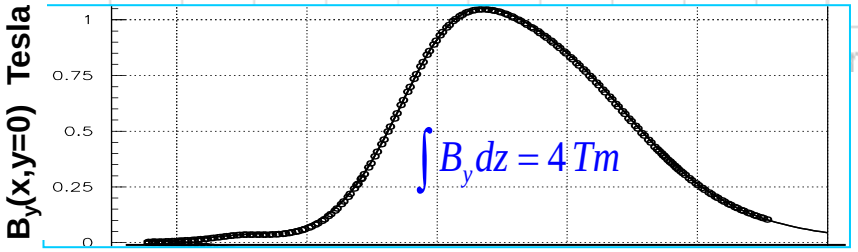


Muon: MWPC
(ctrl M1): Triple-GEM

SPD: PS+Pb+PMT
PS: PS+Pb+PMT
ECAL: PS+Pb+PMT
HCAL: PS+Fe+PMT

VeLo/TT/IT: Si Strip + Beetle
OT: Straw tube

RICH1: Aerogel / C_4F_{10} + HPD
RICH2: CF_4 + HPD



- $\Delta p/p = 0.5\%$ at <20 GeV, 1.0% at 200 GeV
- IP resolution ~ 15 + 29/p_T [GeV/c] μm
- Decay time resolution 45 fs (e.g. $B_s \to J/\psi\ \phi$)
- Kaon ID ~ 95% for 5% $\pi\to K$ mis-ID probability

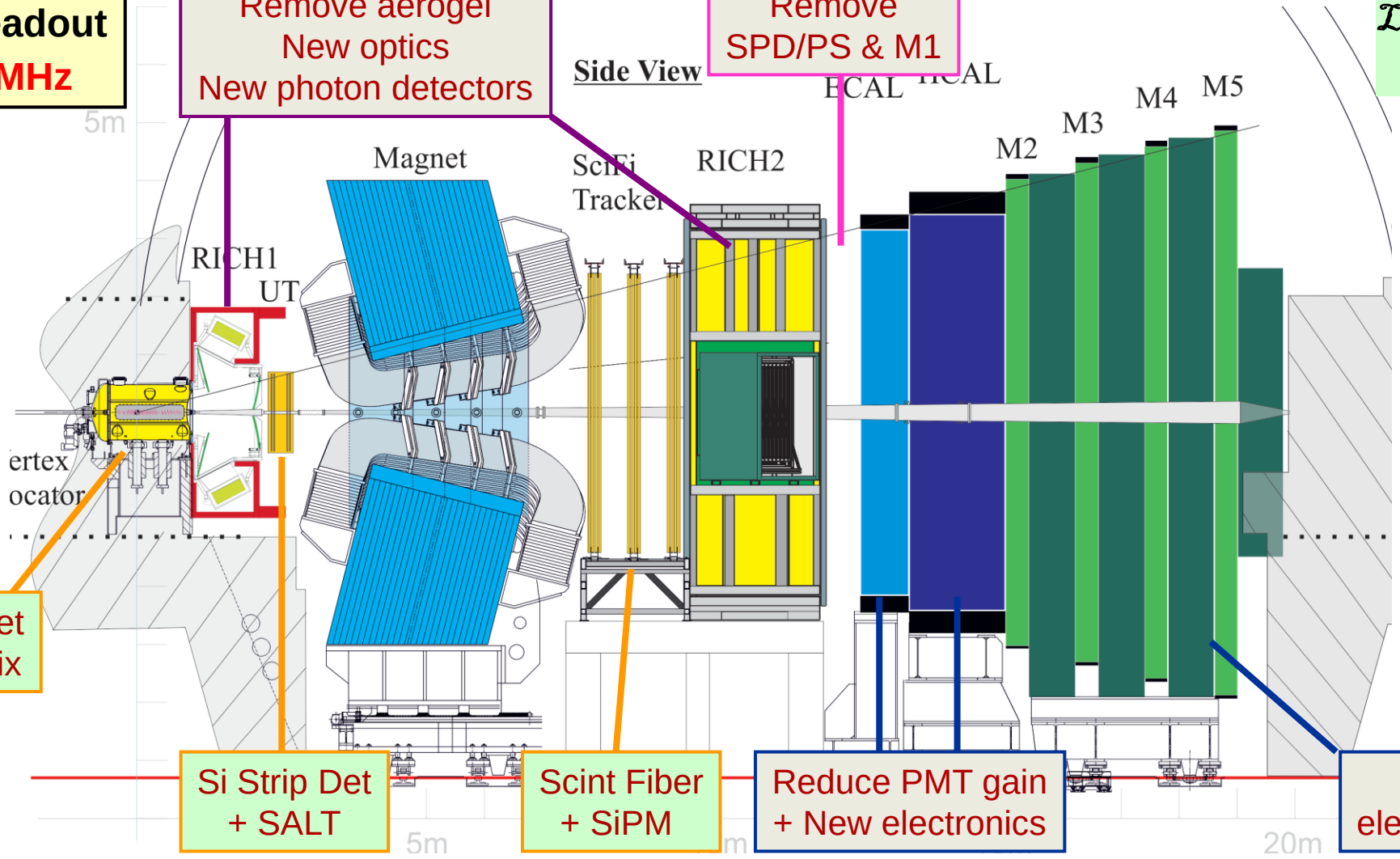
LHCb Phase I Upgrade

Trigger-less readout
1 MHz ⇒ 40 MHz

Remove aerogel
New optics
New photon detectors

Remove
SPD/PS & M1

$\mathcal{L}_{max}$ ~ 2×10^{33} cm^{-2}s^{-1}
(increase × 5)



Software,RTA…

中国组

Si Pix Det
+ VeloPix

Si Strip Det
+ SALT

Scint Fiber
+ SiPM

Reduce PMT gain
+ New electronics

New
electronics

中国组

中国组

LHCb Phase II Upgrade

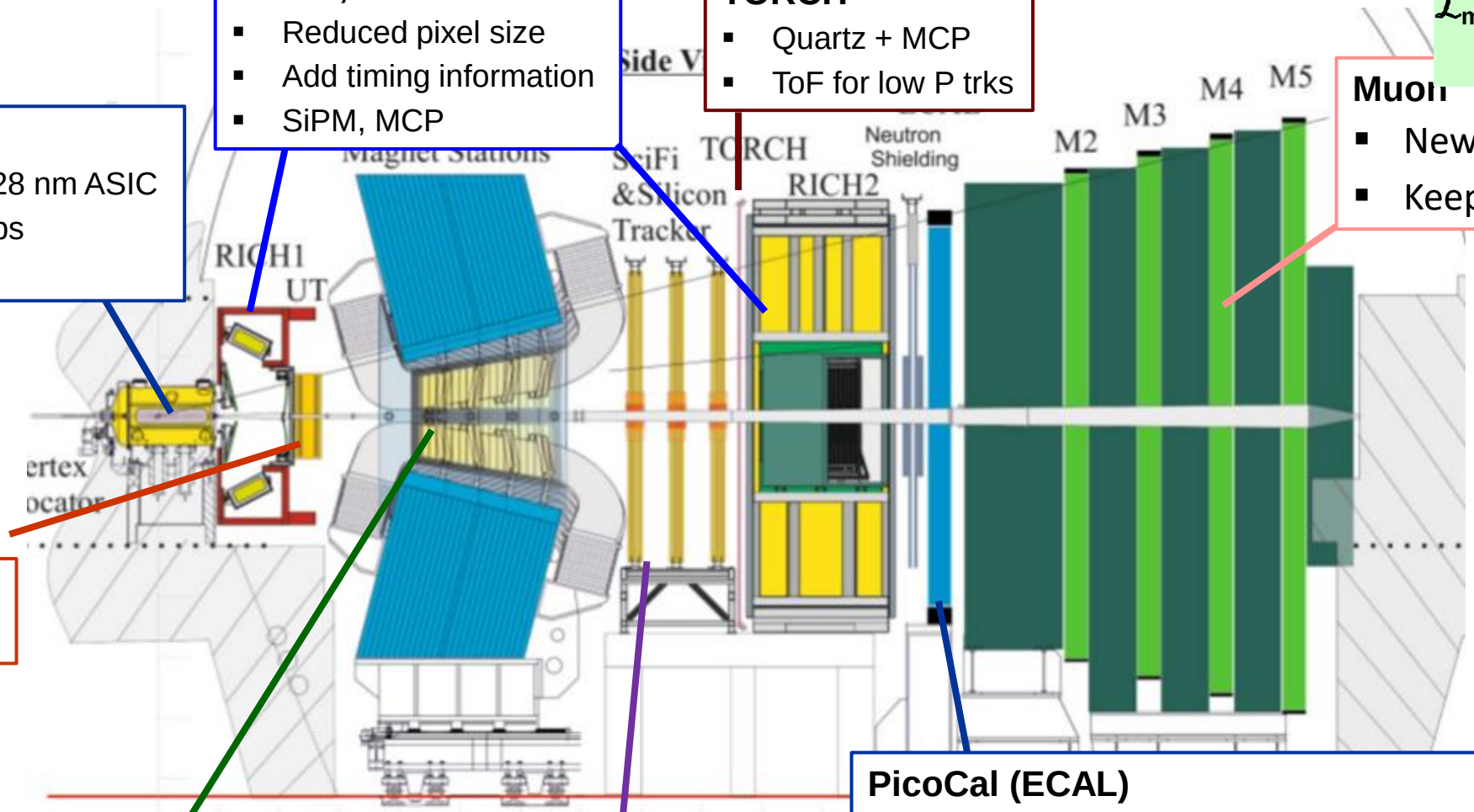
RICH1, RICH2
- Reduced pixel size
- Add timing information
- SiPM, MCP

TORCH
- Quartz + MCP
- ToF for low P trks

$\mathcal{L}_{max}$ ~ 1.5×10^{34} $cm^{-2}s^{-1}$
(increase × 7.5)

VELO → TV
- 3D Si Pixel, 28 nm ASIC
- Timing ~ 50 ps
- New RF-foil

Muon
- New μRWELL (inner)
- Keep MWPC (outer)



UT → UP
- MAPS pixel

中国组

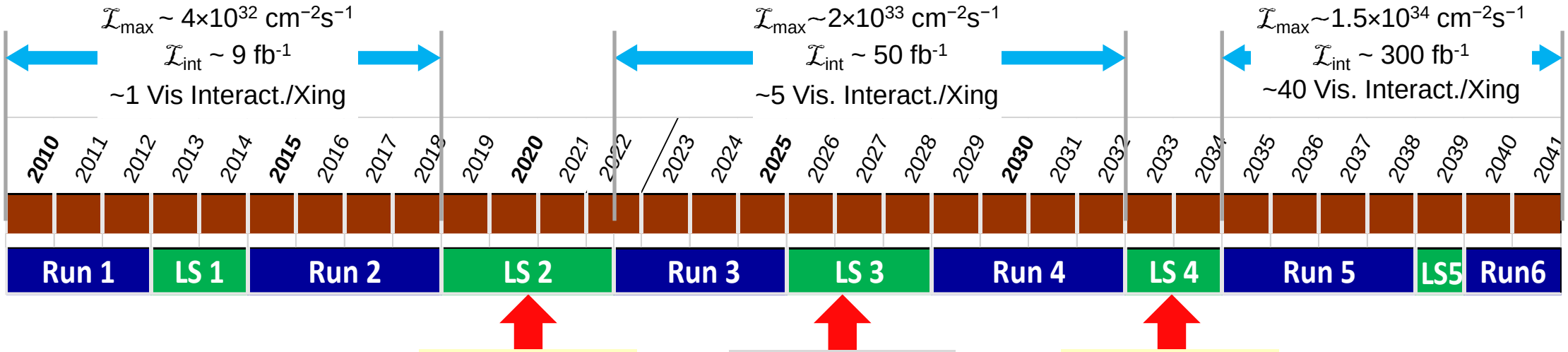
Magnet Stations (MS)
- Scintillating bar
- Low P particles

SciFi → MT
- MAPS pixel (inner)
- SciFi (outer)

PicoCal (ECAL)
- Timing, longitudinal segmentation
- SPACAL with radiation hard crystals
- Keep Shashlik for outer region

中国组

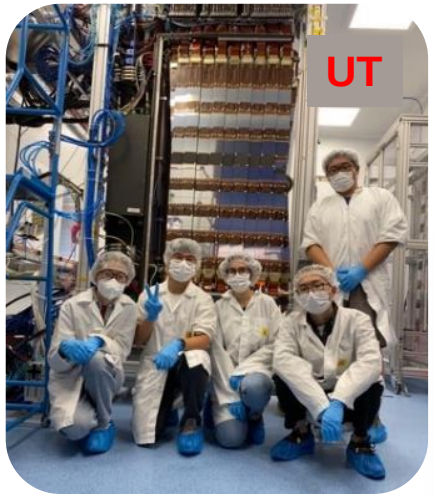
Timeline of LHCb Operation and Upgrade



U1 installation

Consolidations (U1.b)

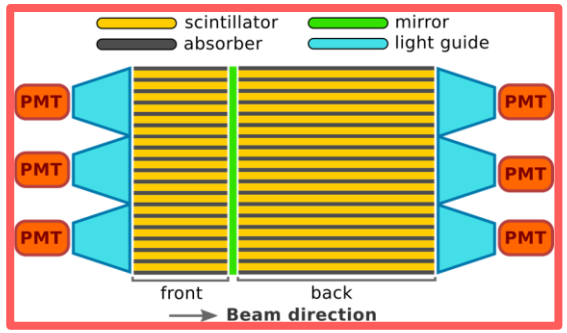
U2 installation



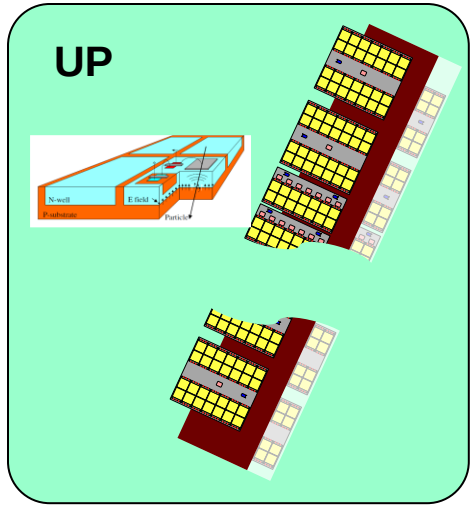
IHEP + (THU, CCNU, LZU, SCNU, UCAS)

THU

PicoCal / SPACAL



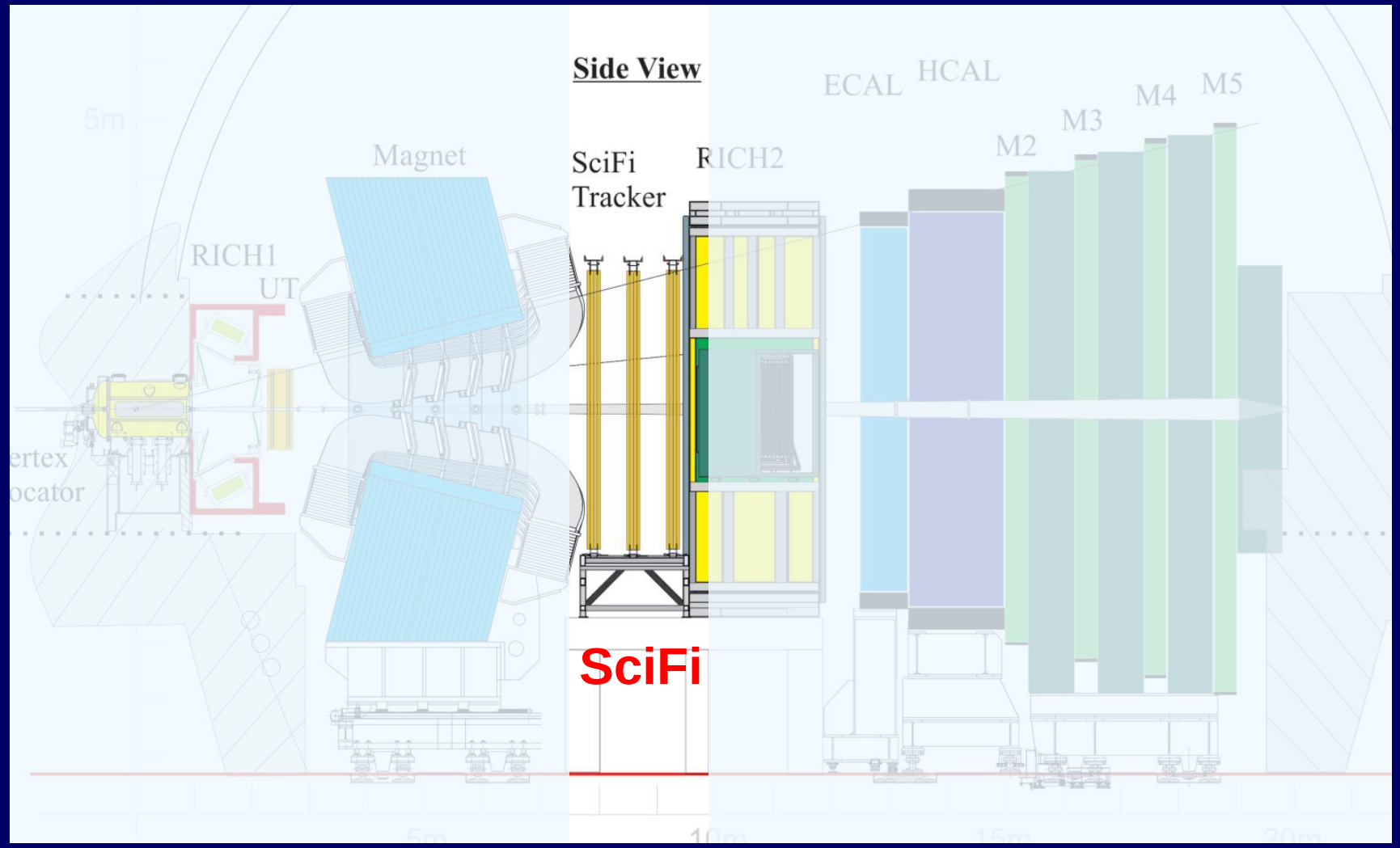
PKU, THU, WHU, SCNU + …



IHEP, CCNU, HNU, LZU, UCAS

+4 French Institutes

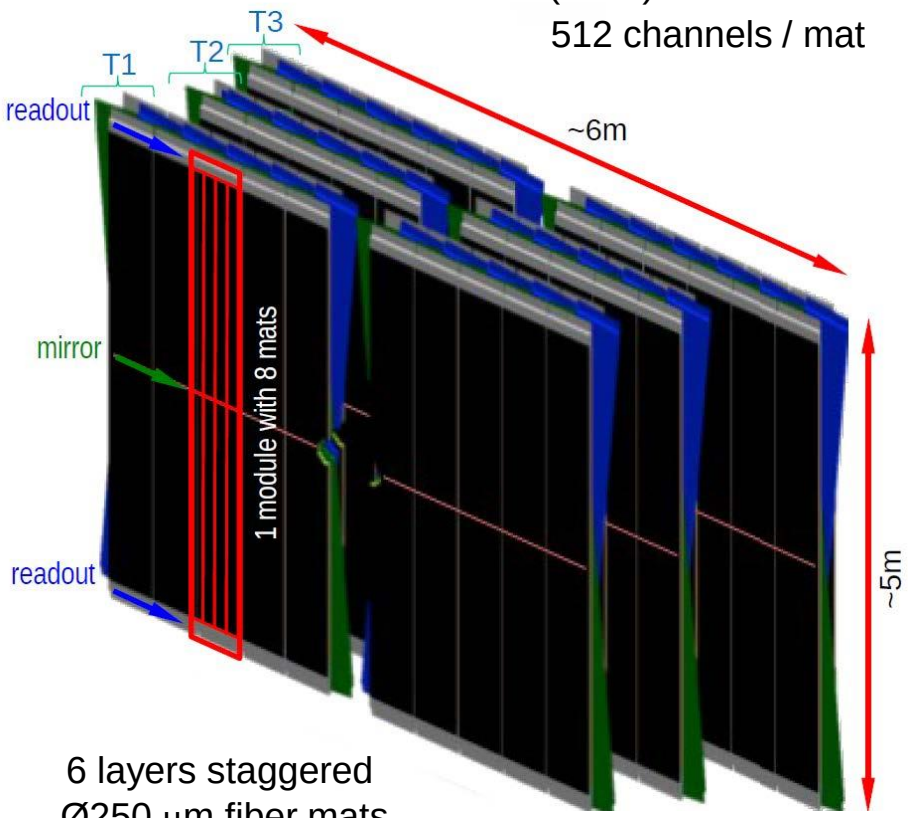
Phase I Upgrade: SciFi



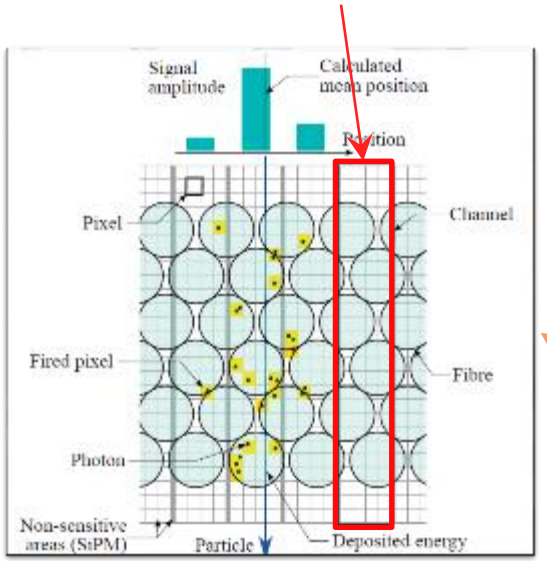
Scintillation Fiber Detector

- The tracking stations (straw tube & Si strip) are replaced by 3-station (12-layer) scintillation fiber detector.
- Read out with arrays of SiPMs, and custom made PACIFIC ASICs (64-ch, 130 nm CMOS). In total SciFi has ~0.52 M readout channels.
- Spatial resolution better is than 100 μm in X. The single hit efficiency reaches ~98% in operation.
- Chinese team mainly on FE electronics and commissioning

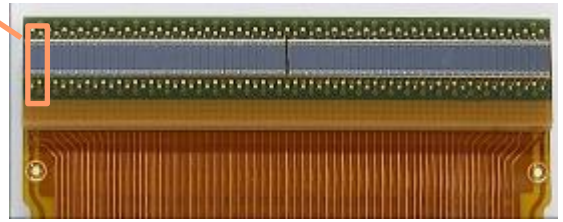
3 stations × 4 layers (XUVX)
10 (or 12) modules / layer
8 (4 × 2) mats / module
512 channels / mat



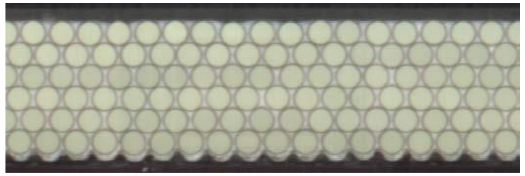
1 SiPM Channel



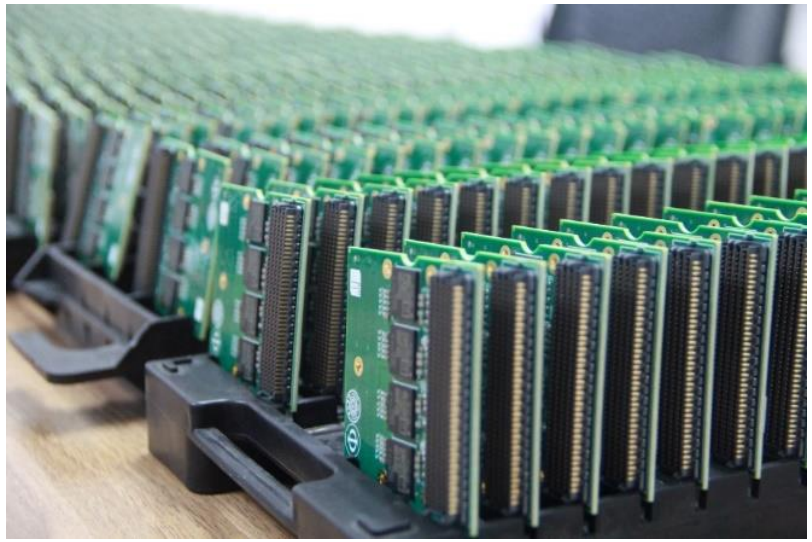
128-ch SiPM Array



6 layers staggered
Ø250 μm fiber mats

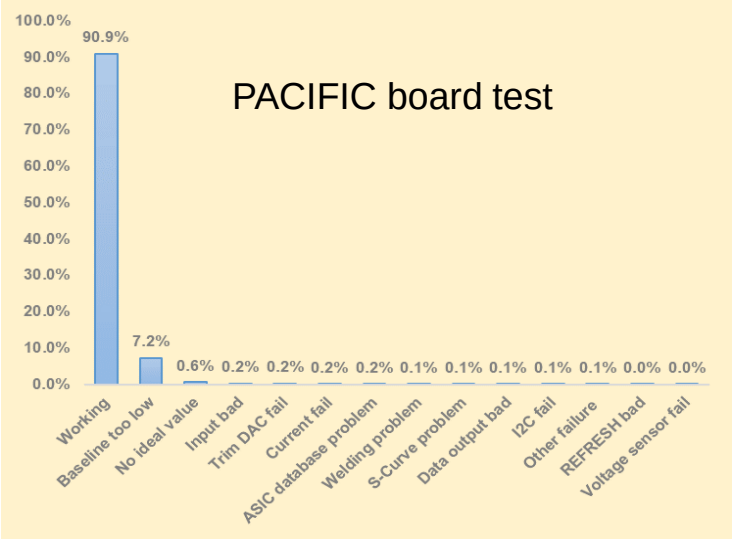


SciFi Front-end Board



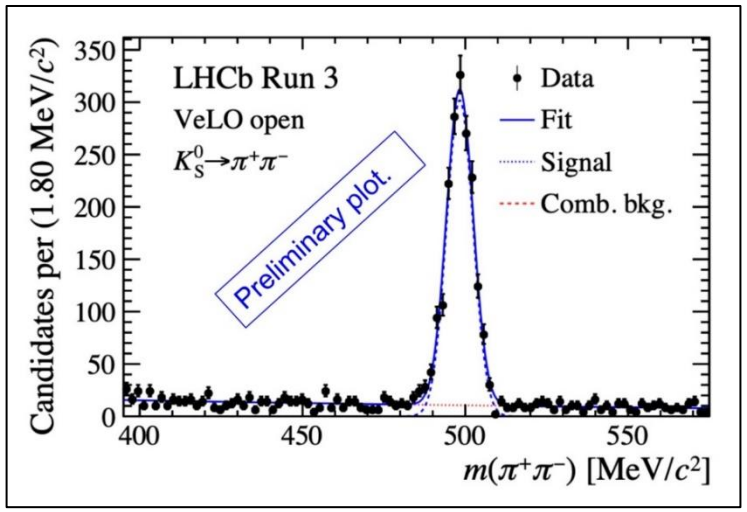
Contributions from the Chinese team (**THU**):

- Co-design the PACIFIC Frontend Board, with Heidelberg
- Manufacture all 2,528 boards (2,048 + spares)
- Test the PACIFIC boards (THU 50%, Valencia 50%)
- Produced quality assurance system for PACIFIC chip & boards, total 11 setups @ THU, Valencia, Barcelona & Heidelberg
- Build new software sequence for SciFi specific processing of testbeam data

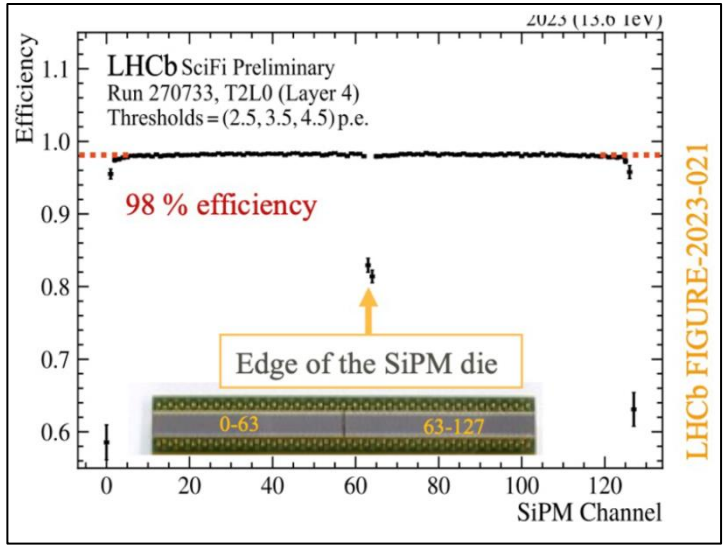


SciFi Operation

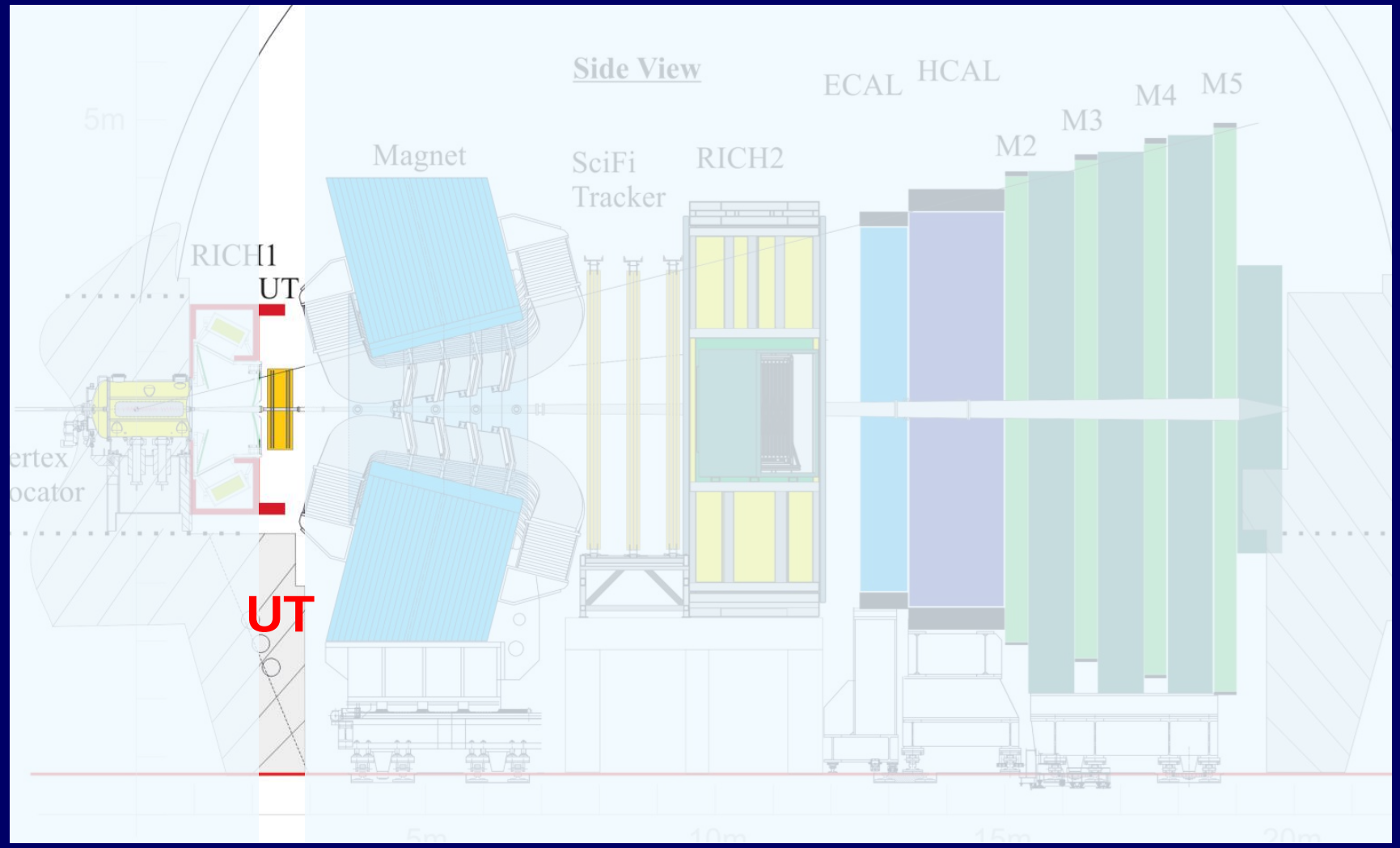
- THU group participated in the SciFi commissioning efforts
- The SciFi single hit efficiency reaches ~98% during operation in 2023
- The tracking system provides high quality measurements



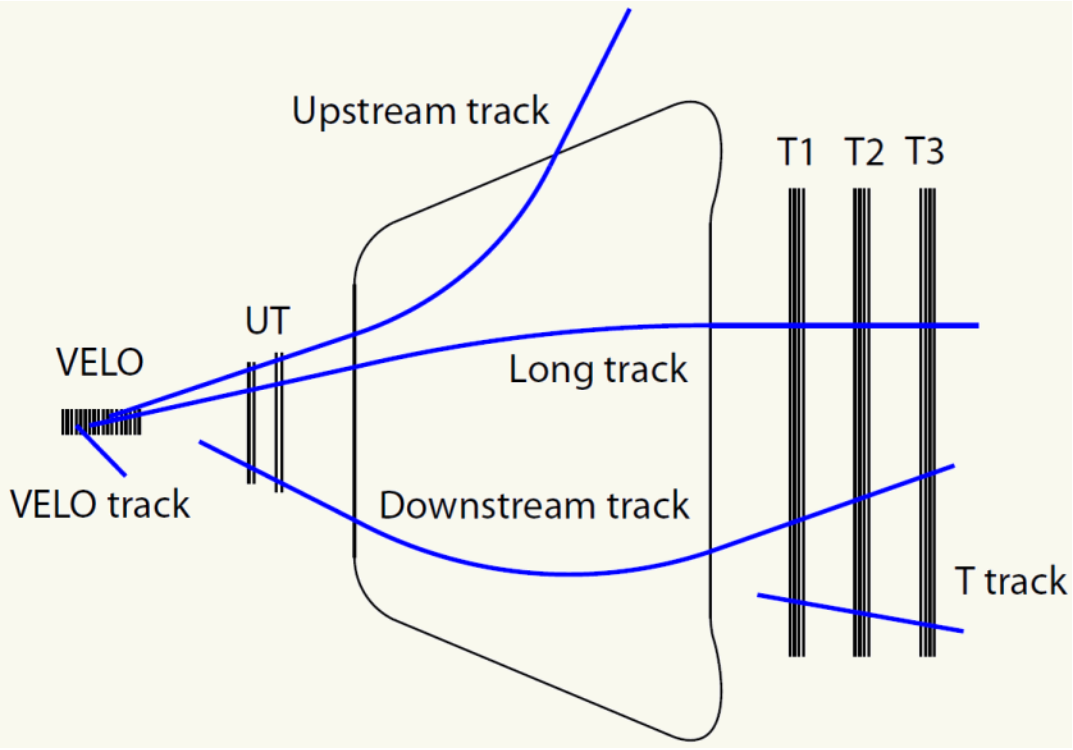
SiPM operates at -40°C

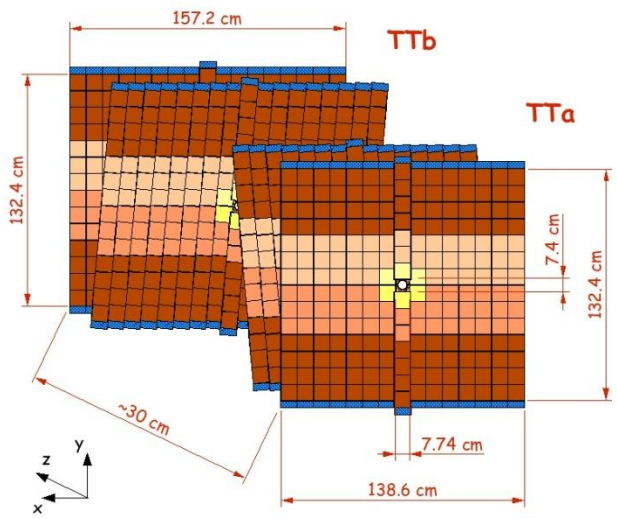


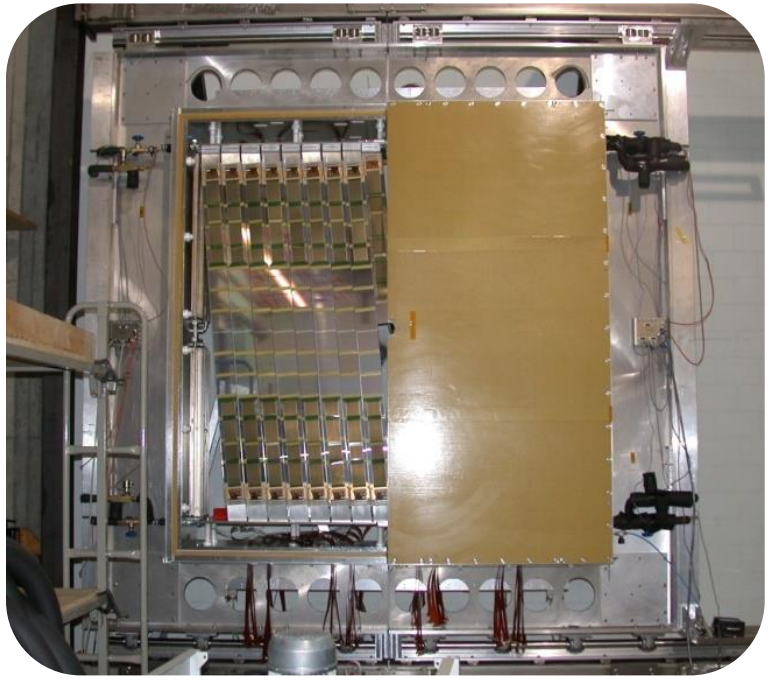
Phase I Upgrade: UT



UT Role in The Tracking System





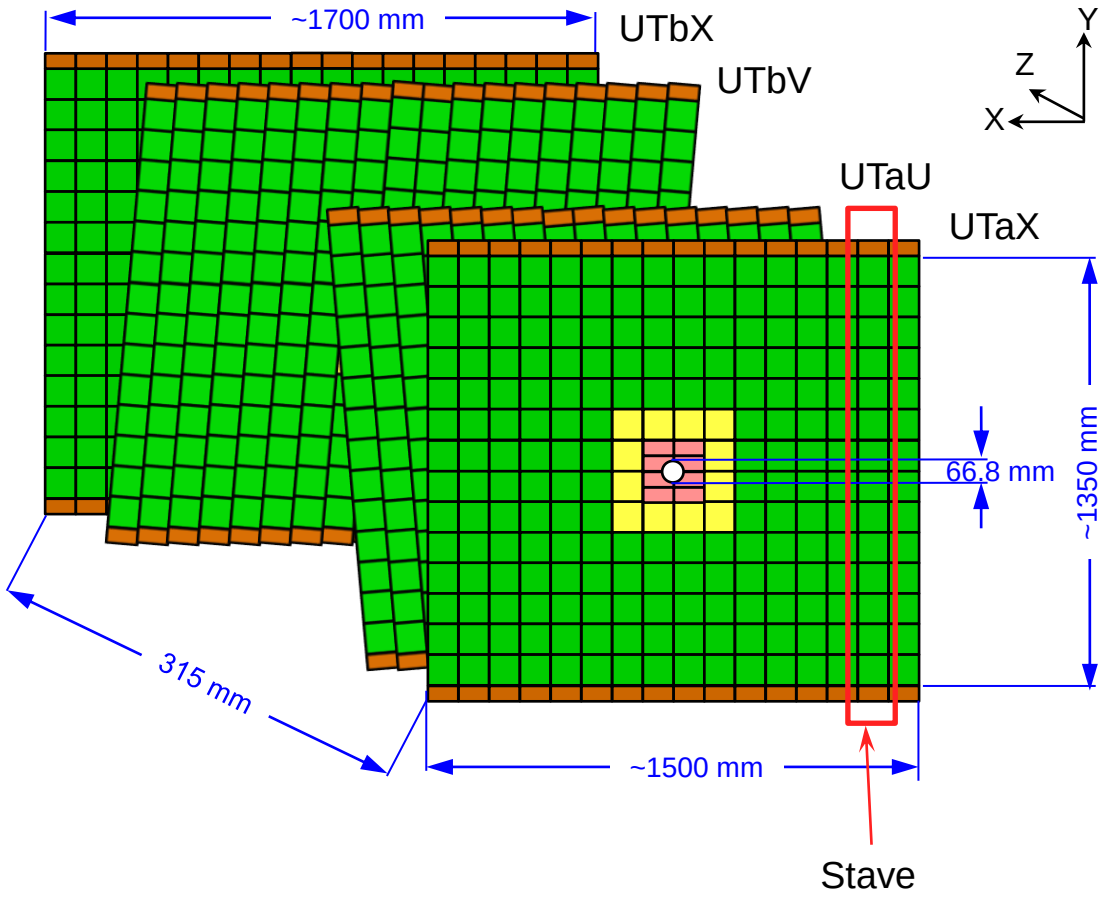


- The UT project was added later, when we realized that the trigger-less readout would be in jeopardy with the old TT
- Bridge between VELO and T tracks, reduce significantly the reconstruction time for software trigger
- Reduce ghost rate and improve momentum resolution
- Increase reconstruction efficiency of long lived particles, e.g. $K_s^0 \to \pi^+\pi^-,\ \Lambda \to p\pi^-$

Geometric Configuration of UT

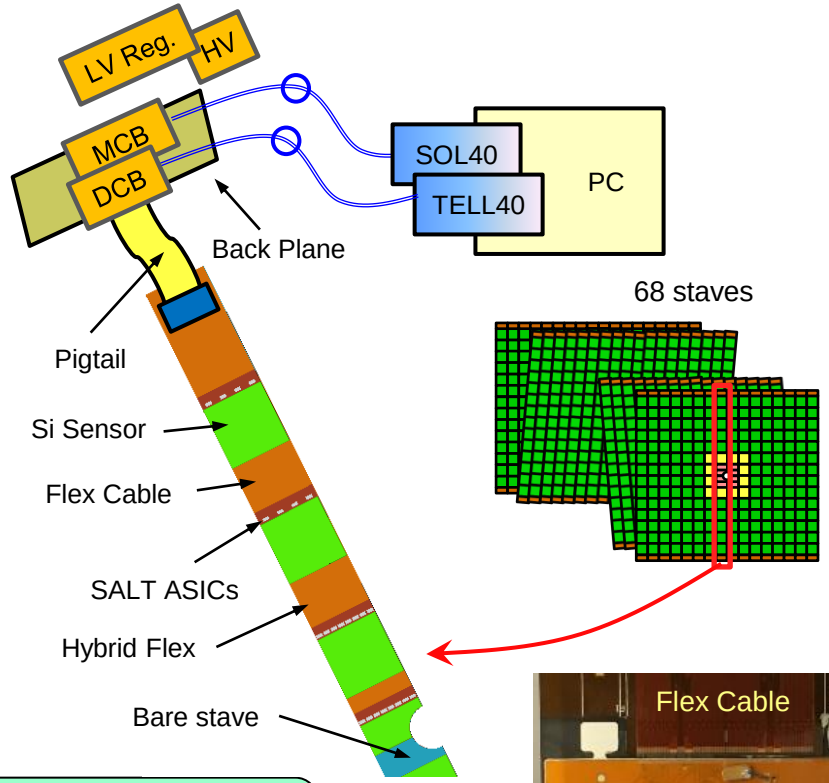
Sensor	A	B	C	D
Type	p-in-n	n-in-p	n-in-p	n-in-p
Thickness(μm)	320	250	250	250
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16

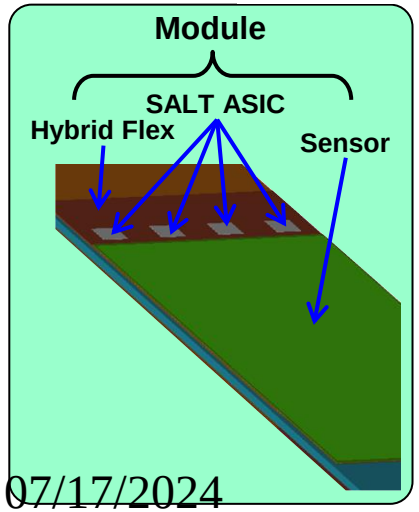
4 planes, 68 staves
968 sensors, 4192 ASICs

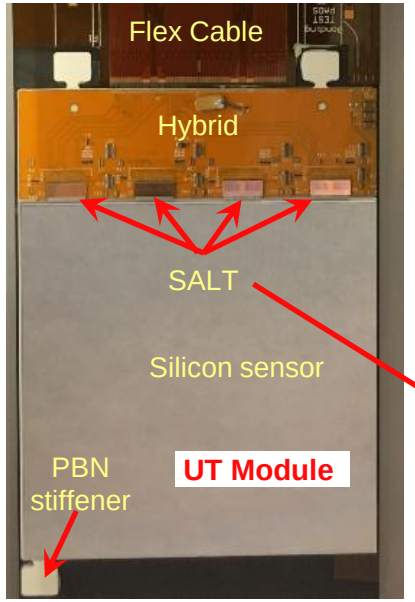


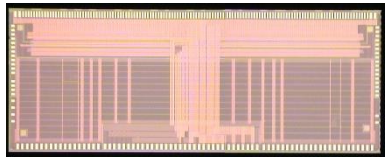
- Four planes of silicon strip detectors, readout ASICs at sensor proximity.
- Stave structure: modules on 2 sides for overlapping, readout at 2 ends.
- Higher segmentations near the center. The maximum occupancy ~1.4%.
- Sensor radiation resilience, Φ_{max}~5×10^{14} n_{eq}cm^{-2}

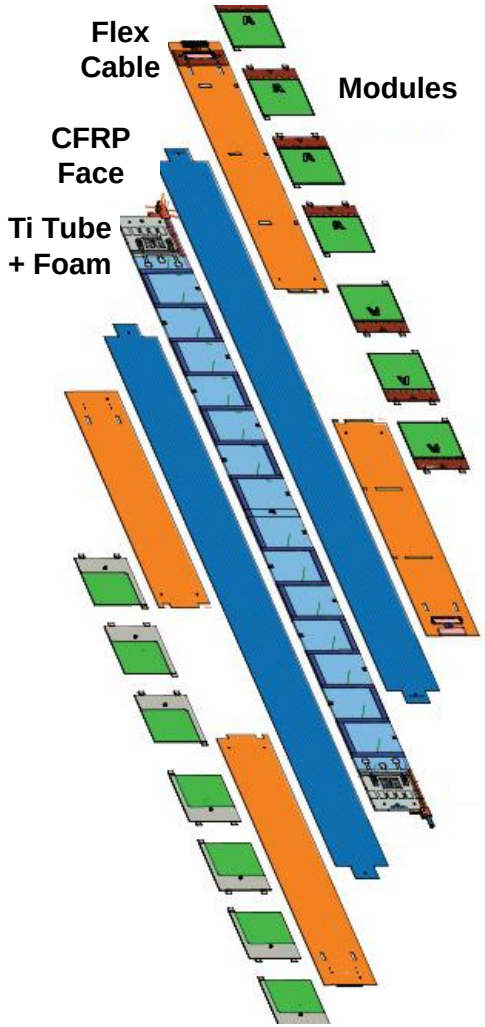
UT Stave Design



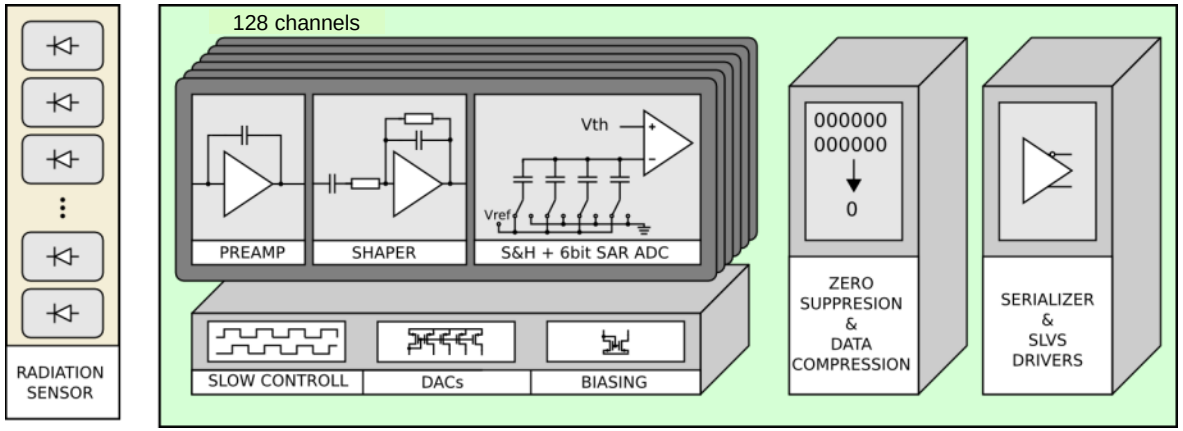




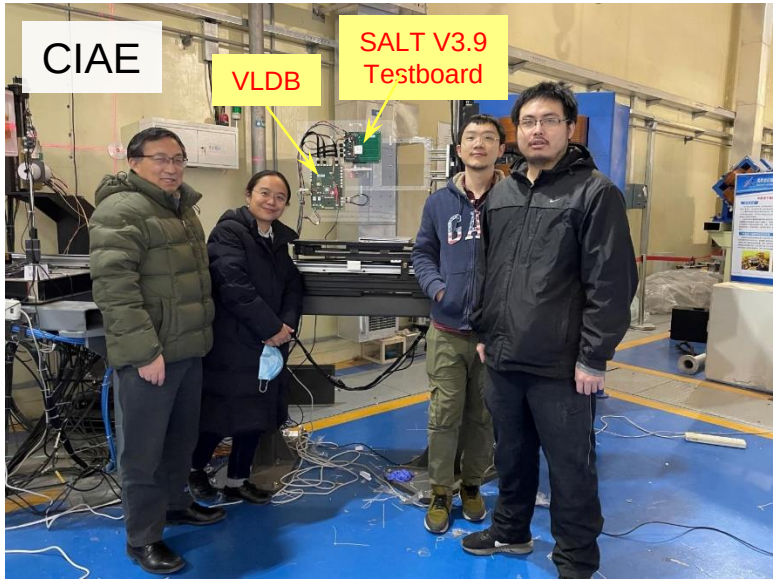




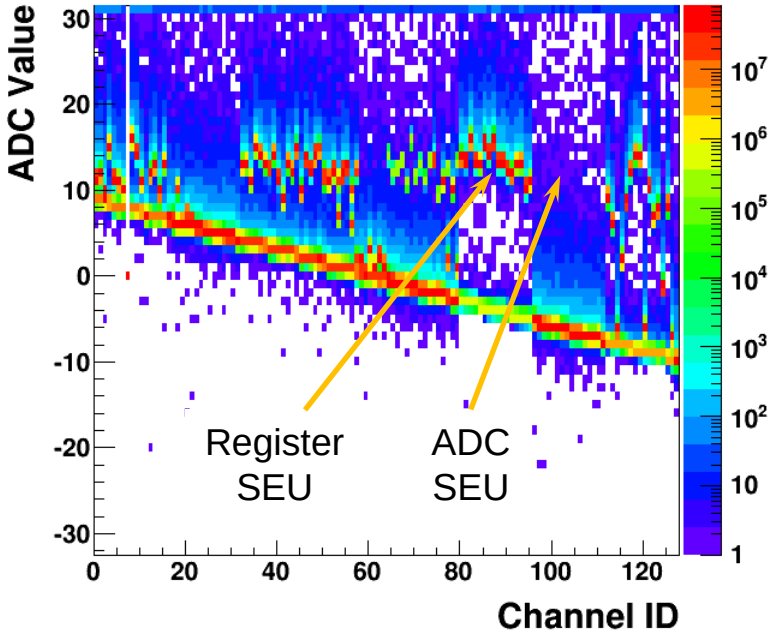
UT Front-End Readout ASIC - SALT



- CMOS 130 nm technology (IBM, TSMC)
- 40 MHz readout, digital data packet in ASIC
- 128 channels, per channel preamplifier & 6-bit ADC
- Sensor capacitance 2-12 pF, AC coupled
- Dynamic range ~ 30 ke, both input signal polarities
- Noise: ENC ~ 1000 e @ 10 pF + 50 e / pF
- T_{peak} < 25 ns, short tail ~5%@25ns+T_{peak}.
- Power consumption < 6 mW / channel.

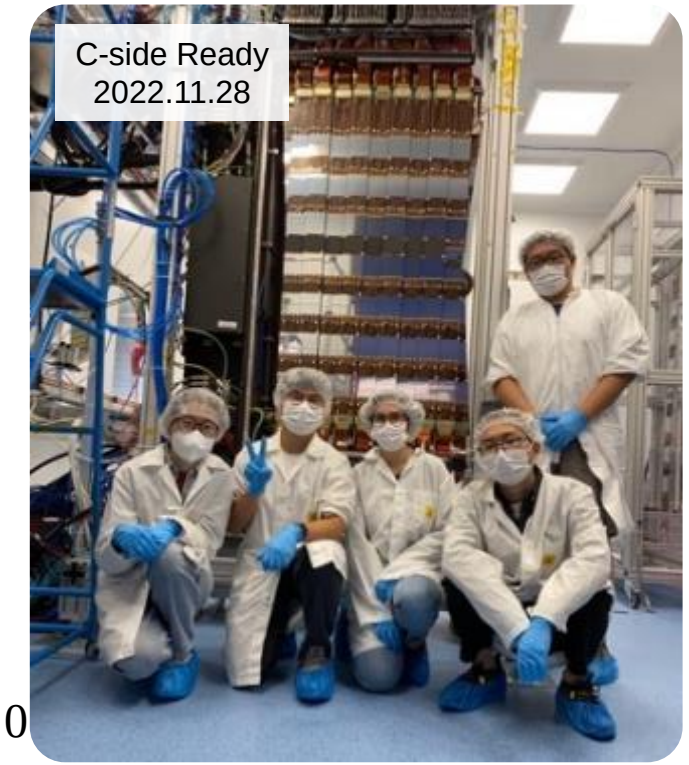


- Custom-designed SALT ASIC
- Validation of SALT functionalities by IHEP & Syracuse groups
- Radiation hardness is very crucial, a few studies at MGH, PSI, CIAE, and CSNS, led by IHEP group
- Few iterations for radiation hardened reinforcement, Mixed use in the final system due to tight schedule

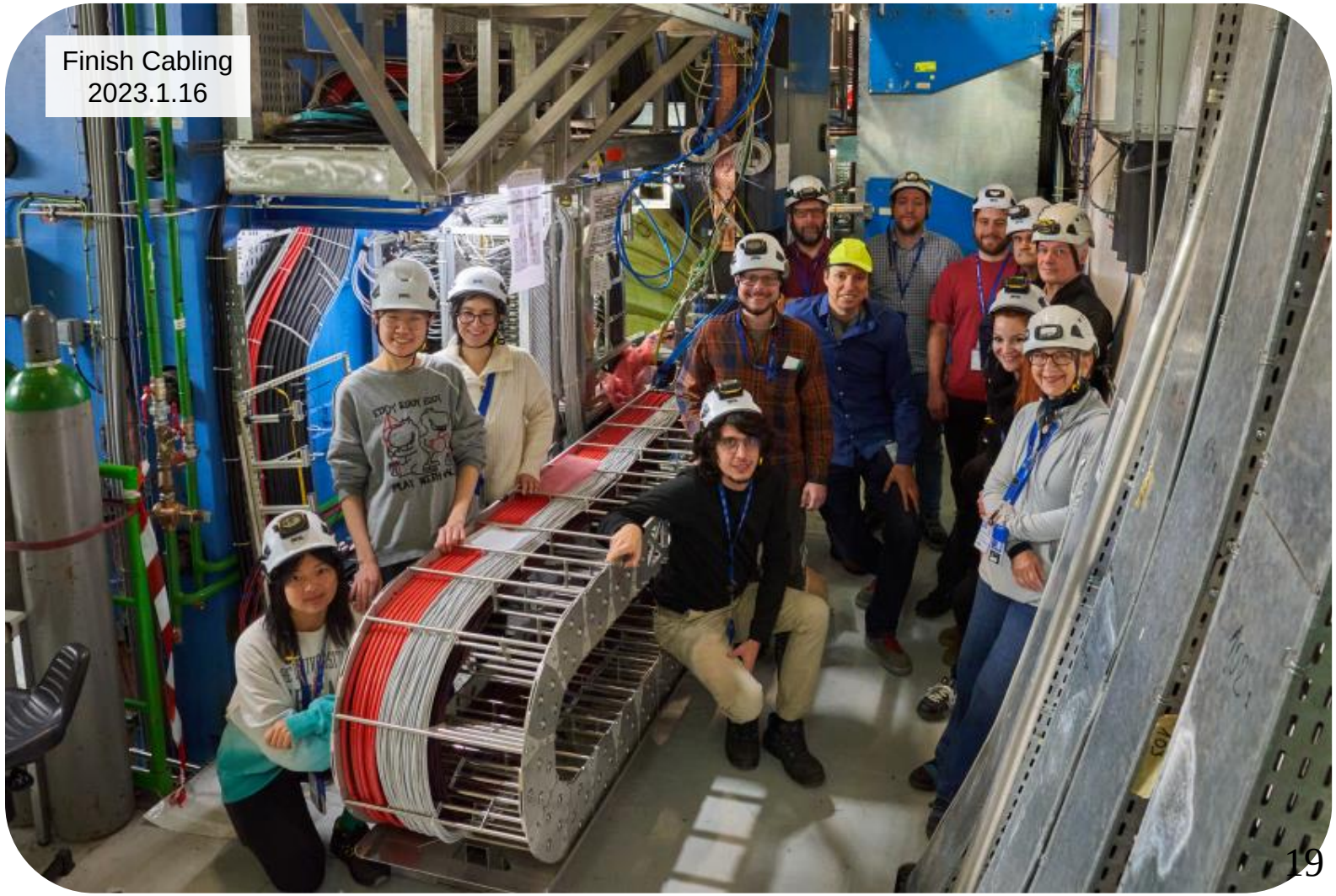


UT Installation Efforts


Start Slice Setup
2019.12.03

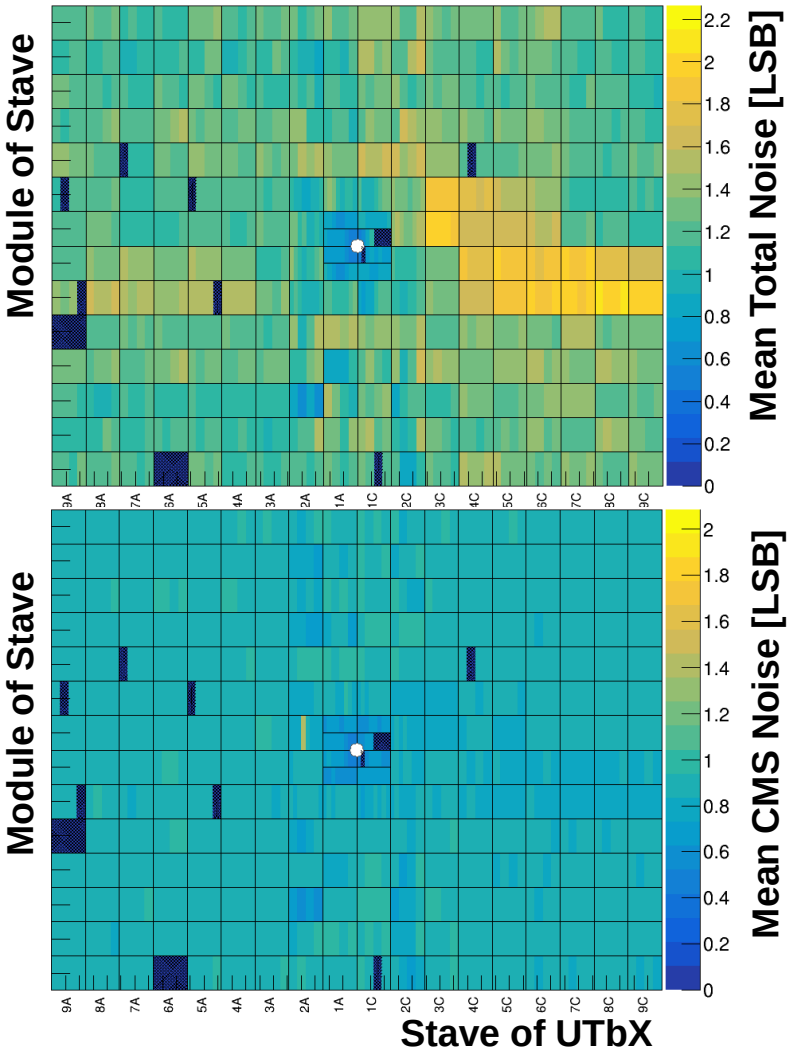

C-side Ready
2022.11.28

- The Chinese team played key role in the UT installation.
- Maintain sufficient human resource at CERN during the difficult time (IHEP, THU, HNU, CCNU, LZU, SCNU, UCAS)

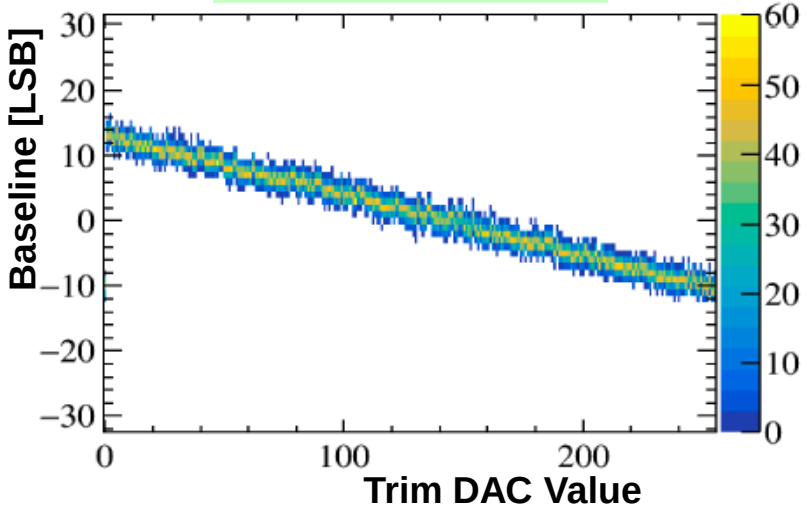

Finish Cabling
2023.1.16

UT Commissioning - Calibration

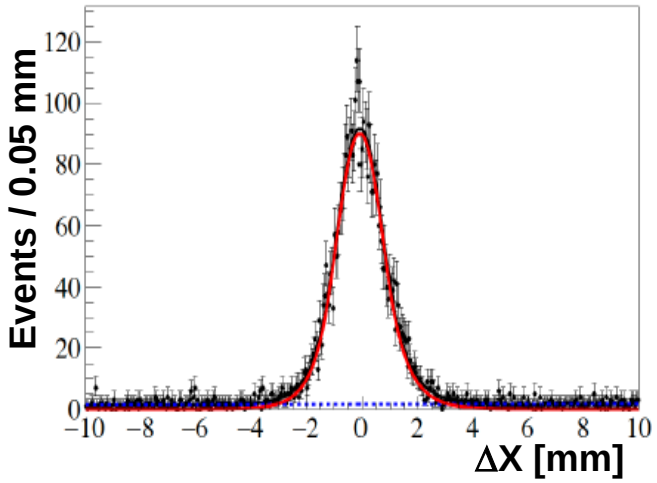
Pedestal and Noise Calibration



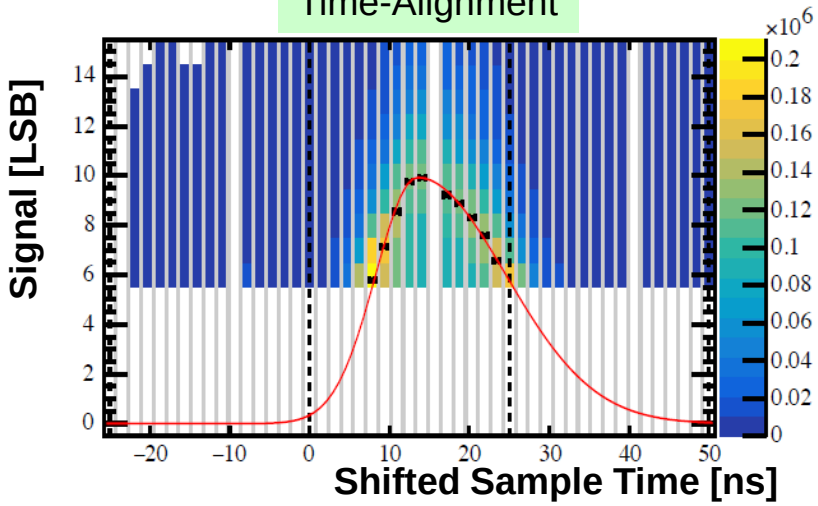
Baseline equalization

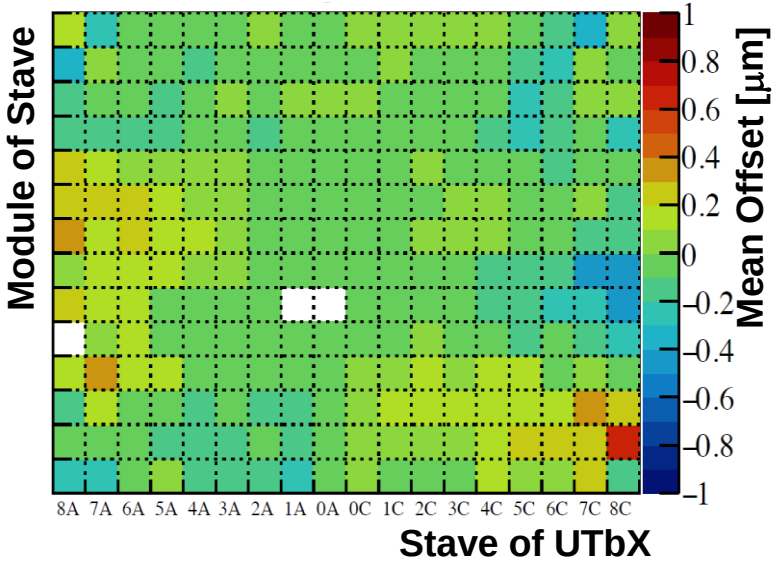


Unbiased Residual of one Module



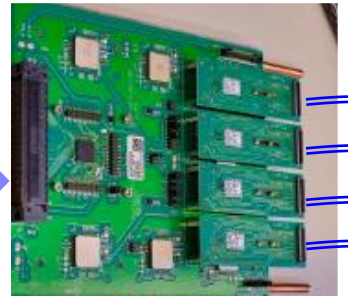
Time-Alignment

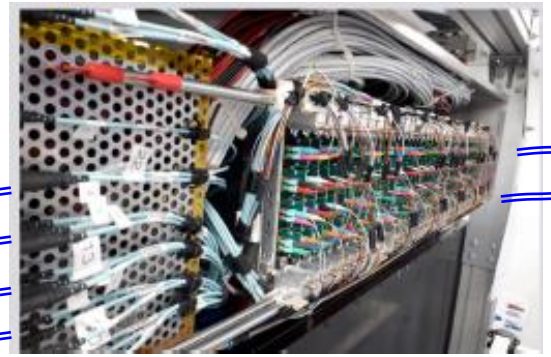


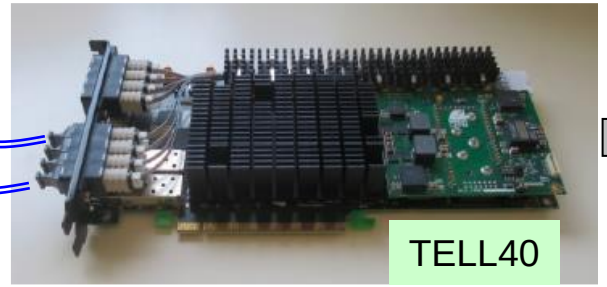


Majority of the UT FE ASICs behave normal now. The rest will be optimized individually.

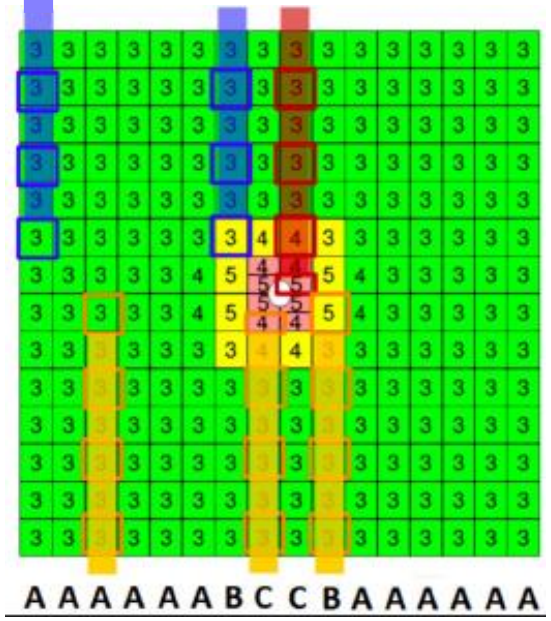
Data Flow Architecture and TELL40 Issue



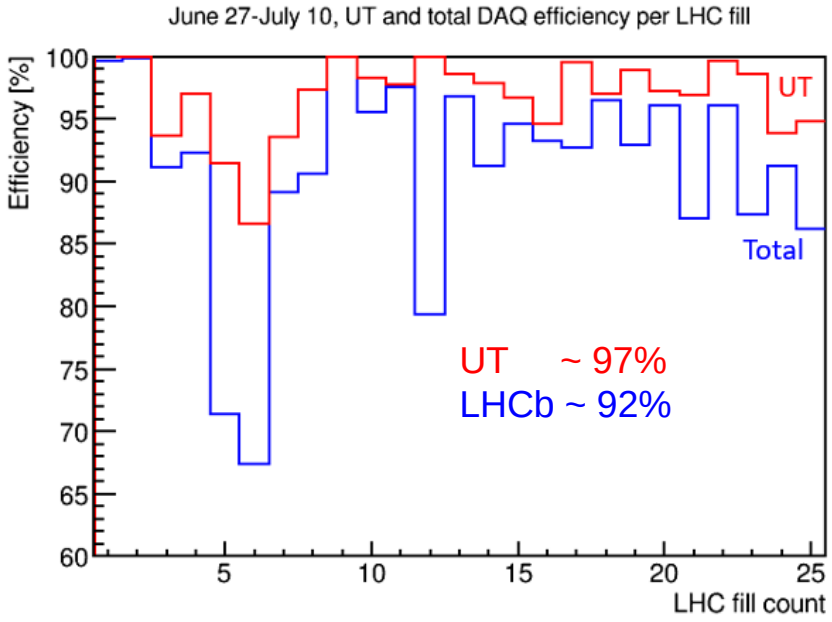




Computer Farm

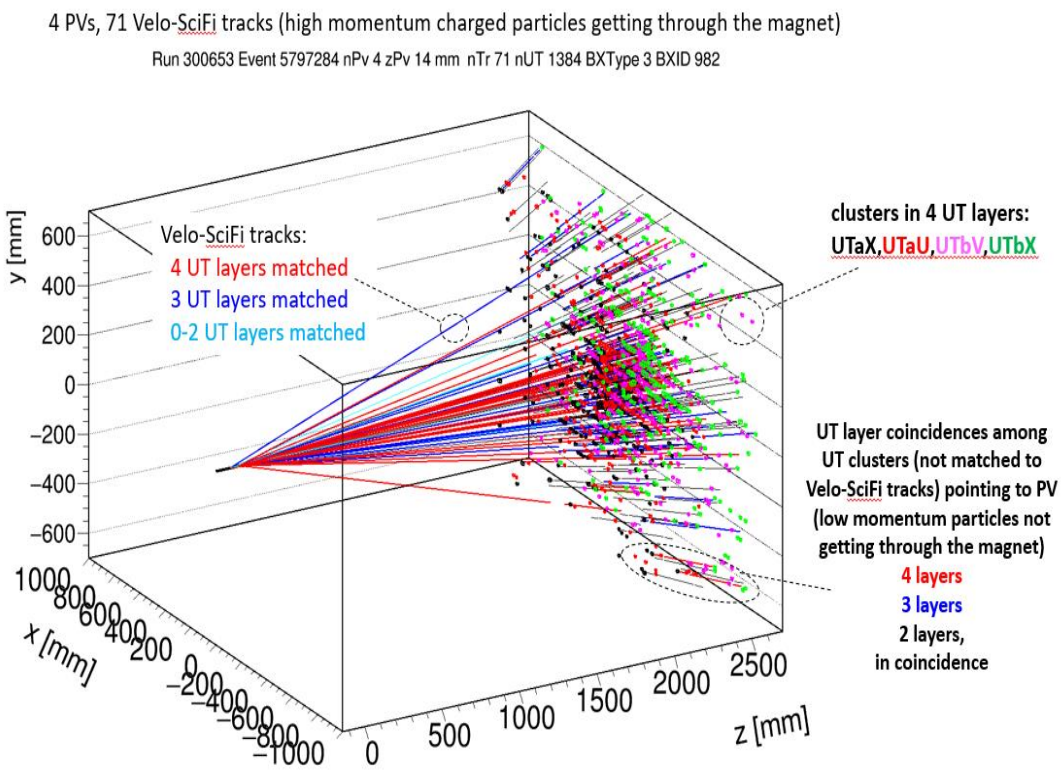


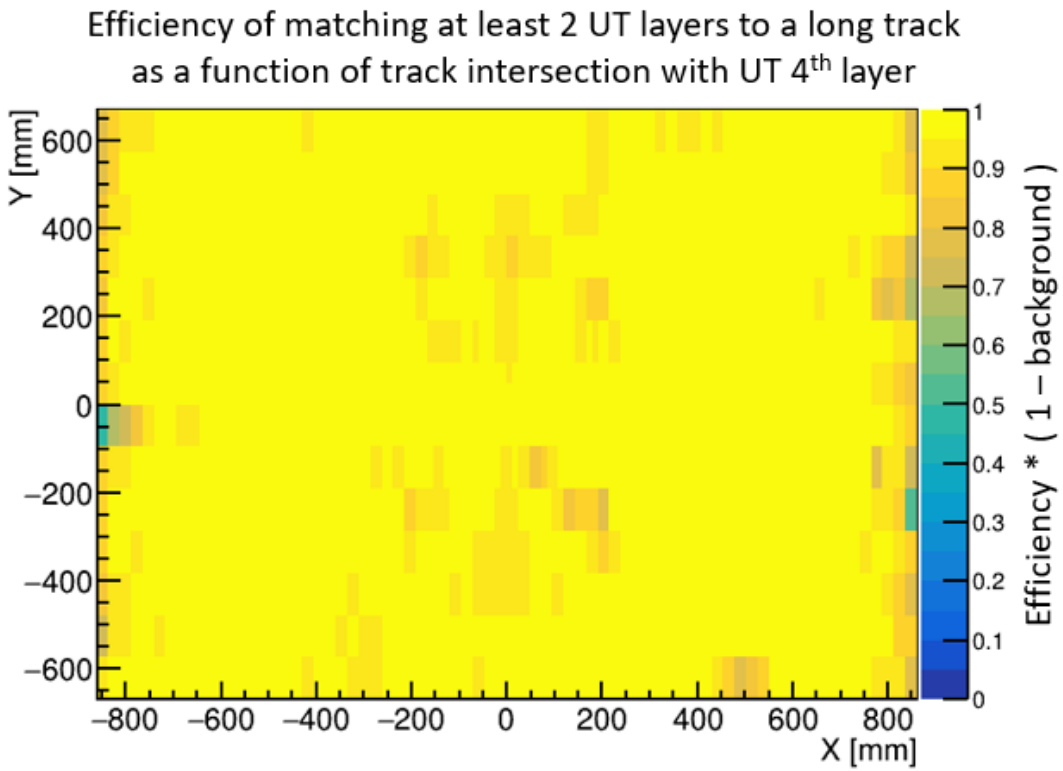
- A TELL40 concentrates data from up to 48 SALT ASICs in design
- FPGA on TELL40 has limited resource, and is difficult to handle large fluctuation
- When the overall system is not very stable yet, TELL40s often get clogged, causing DAQ to halt.
- After implementing extra protection, the TELL40s were able to operate at ~80% nominal luminosity
- The average luminosity data taking efficiency of UT is ~97%. The overall efficiency is ~92%.



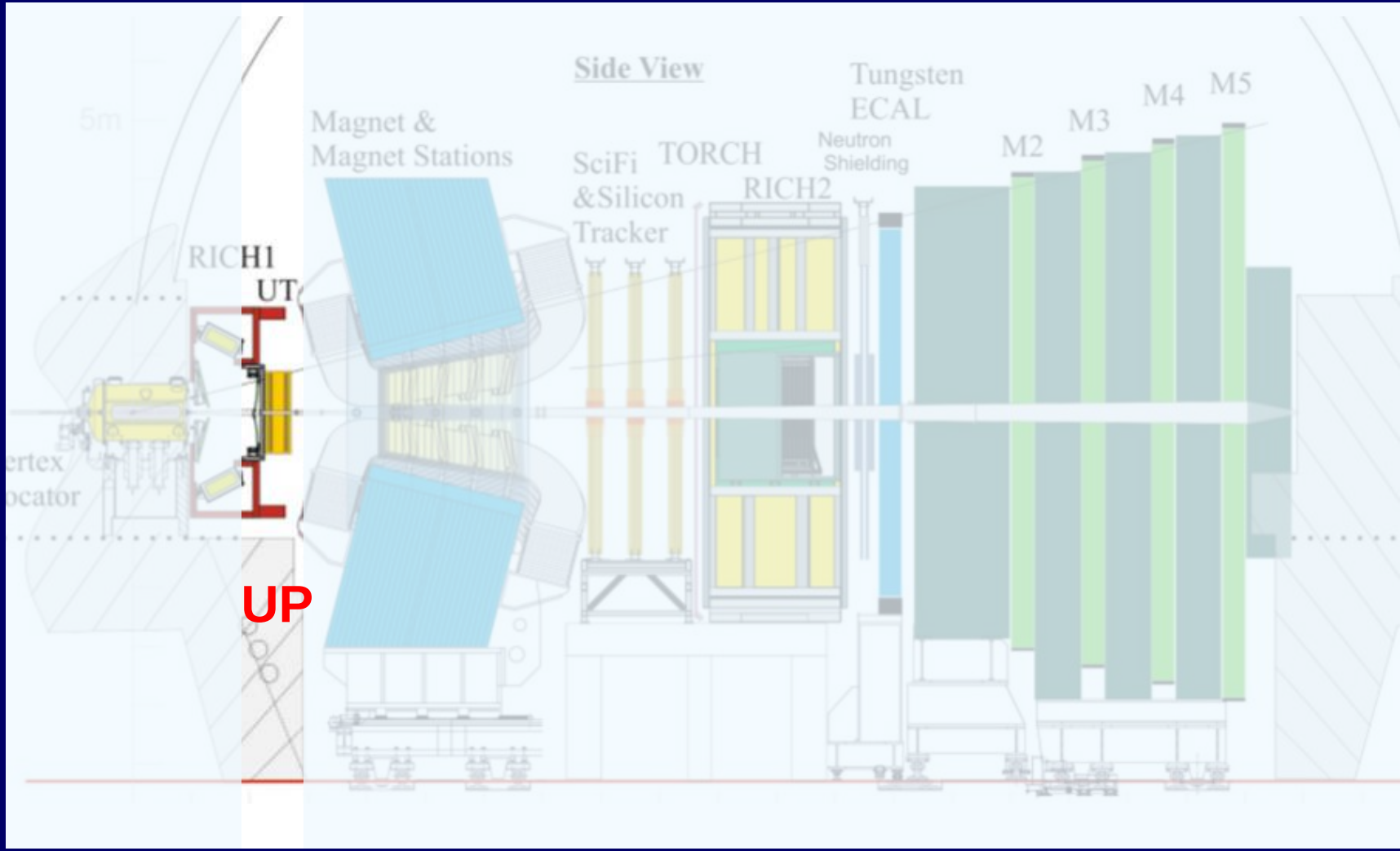
UT in Tracking System

- UT is powerful in rejecting wrong matching between VELO & SciFi track segments. Without UT the online event reconstruction is too slow to handle the high data rate.
- Currently UT still have ASICs to be recovered leaving holes in certain region. By requiring at least 3 out of 4 layers to have matched UT hits, the track efficiency is ~94%. It reaches ~99.5% when requiring only 2 UT hits.





Phase II Upgrade: UP



UT/UP Project Management Structure

PL: Jianchun Wang (IHEP, UT/UP) 2024.03 -

DPL: Tomasz Skwarnicki (Syracuse, UT), Stefano Panebianco (IRFU, UP)

UT Management Structure

Yiming Li / IHEP
Fabrice Guilloux / IRFU
Franck Gastaldi / LLR
Sensor chip design and characterization

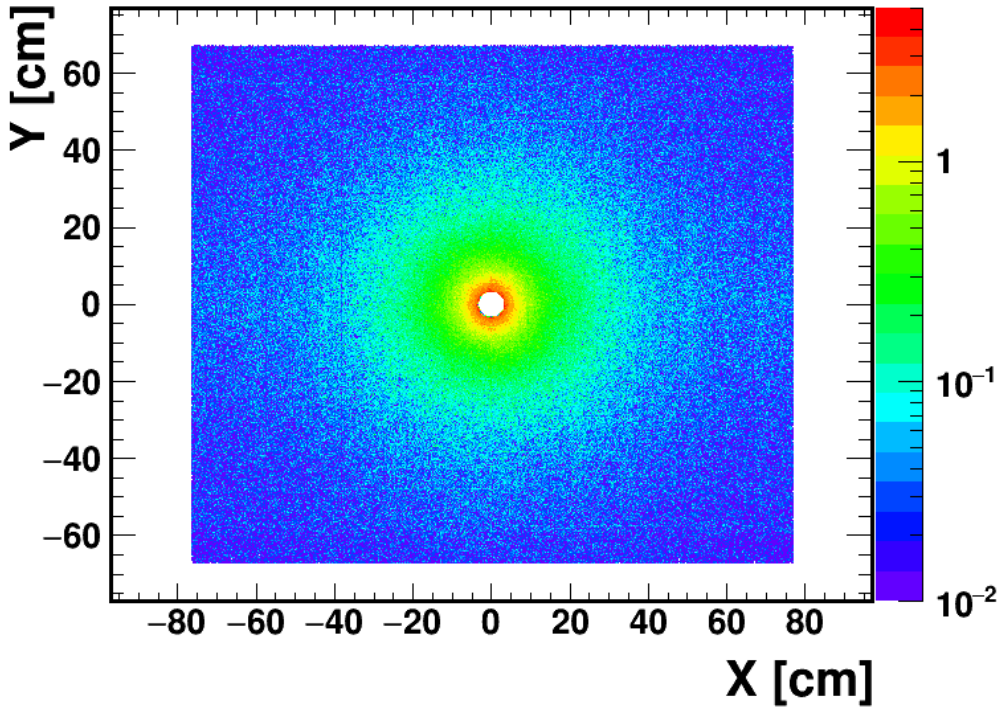
Charlotte Riccio / IRFU
Jiesheng Yu / HNU
Module stave and mechanical structure

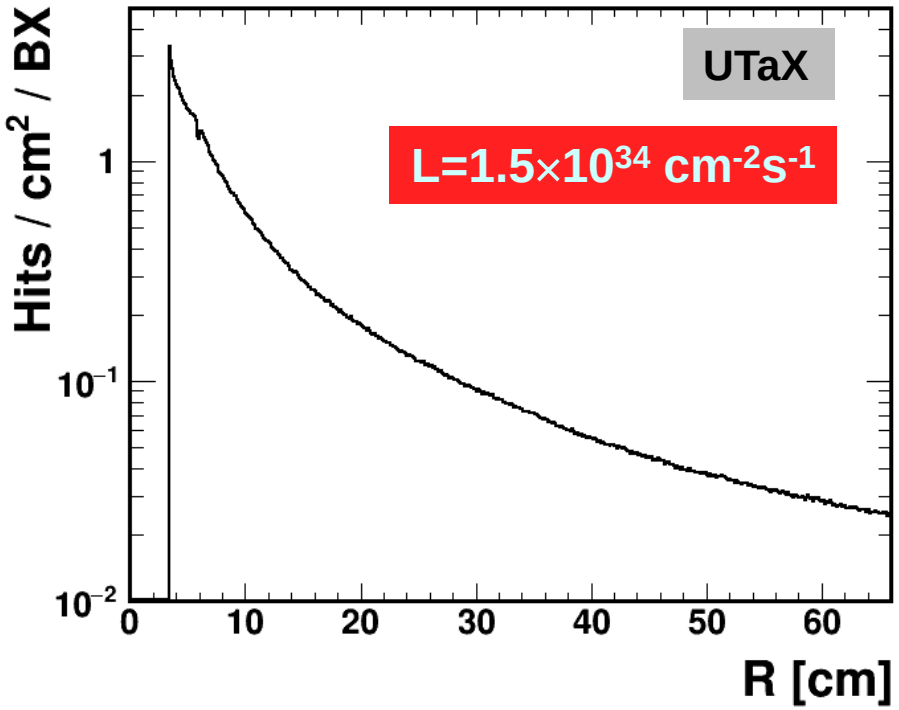
Benjamin Audurier / IRFU
Xuhao Yuan / IHEP
Simulation, reconstruction & performance

Manuel Guittiere / Subtech
Overall mechanics, integration & services

Kai Chen / CCNU
Readout scheme, DAQ firmware & software

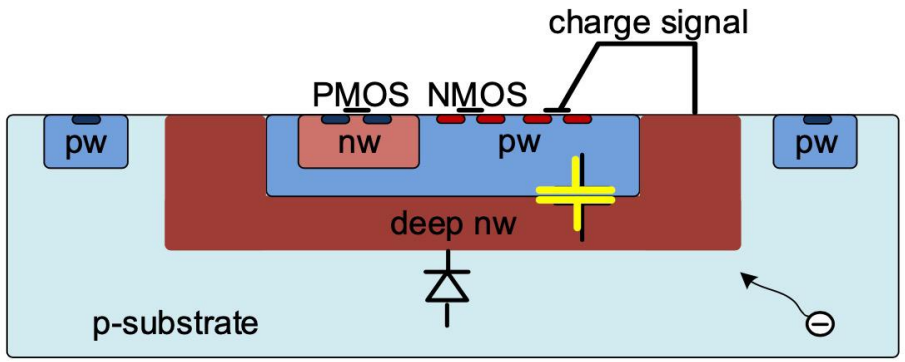
UT Needs Upgrade for Run 5/6

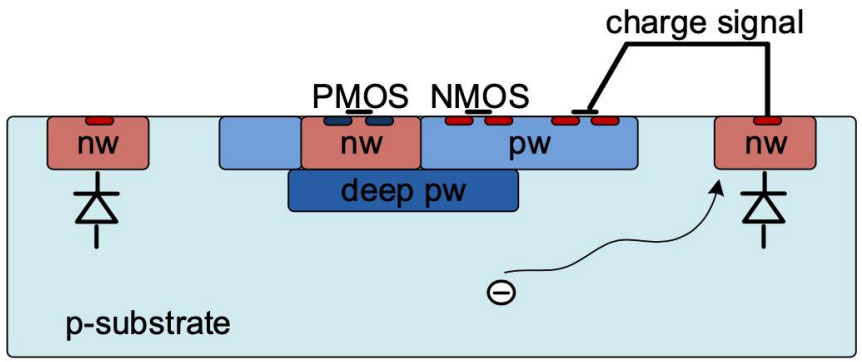




- Peak luminosity for pp ~1.5×10^{34} $cm^{-2}s^{-1}$. 2574 / 3564 beam-beam bunch crossing. The max hit density ~5.52 hits/cm^2/BX for beam-beam collisions, or 4.0 averaged over all bunch crossings
- Much increased track density requires a higher granularity, especially in the central area
- High data rate needs increased bandwidth
- It receives up to 3×10^{15} n_{eq}/cm^2, or 240 Mrad TID after 250 fb^{-1} operation. Si sensors for TT were not qualified for the high radiation dose.

MAPS Technologies





Large collection electrode

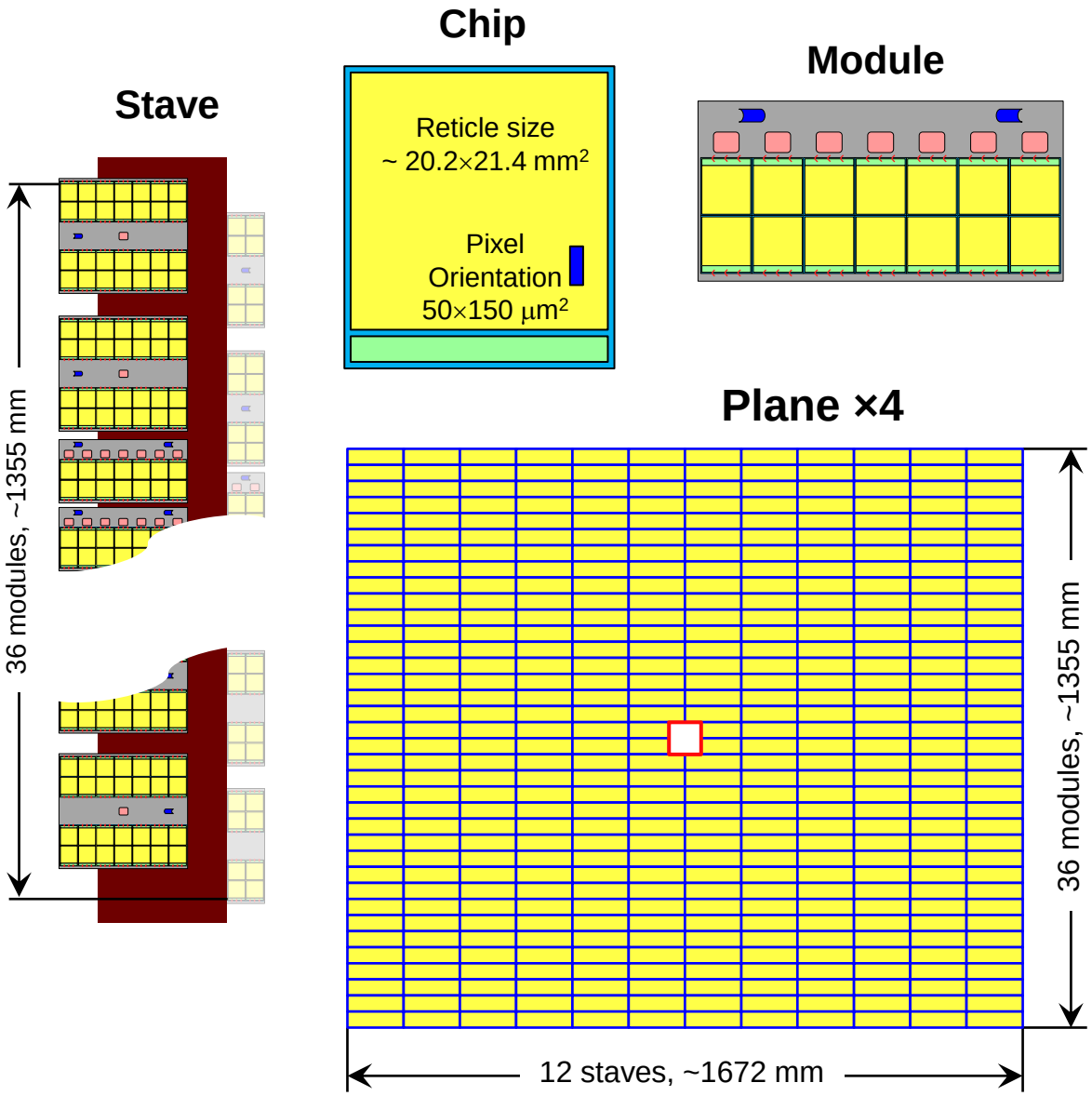
- Circuitry inside the charge collection well
- Large uniform electric field
- On average shorter drift path
- Better radiation hardness (less trapping)
- Very large sensor capacitance (both pw and dnw)

Small collection electrode

- Circuitry outside the charge collection well
- Optimization of little low-field regions
- On average longer drift path
- Radiation hardness needs process modifications
- Very small sensor capacitance

- UT requirements: radiation hardness 3×10^{15} n_{eq}/cm^2, and 240 Mrad TID; time resolution O(1) ns for BXID tagging with low power consumption 100-300 mW/cm^2
- Both solutions have pros and cons. We are reaching on both small electrode (e.g. MALTA, SPARC), and large electrode (e.g. AtlasPix, MightyPix, COFFEE)
- Need to converge for TDR in 2026

Conceptual UP Detector Design



- The current UT can not be kept for U2.
  - Much increased track density requires higher granularity, especially in the central area.
  - Bandwidth for high data rate
  - Radiation hardness
- A MAPS-based pixel detector UP
  - Small electrode: MALTA, SPARC, …
  - Large electrode (HV-CMOS): AtlasPix, MightyPix, COFFEE…
  - Other technologies are not excluded
- Certain features of the current UT may be kept, e.g. the stave structure, and strip / long pixel orientation.

Sensor Specification

Characteristics	LV-CMOS (Based on TJ)	HV-CMOS (Based on TSI / AMS)
Chip size	3.5×3.5 cm^2	2.0×2.0 cm^2
Pixel size	30×30 μm^2	50×150 μm^2
Chip thickness	~ 100 μm	
Position resolution	5-10 μm	15, 40 μm
Time resolution	O (1) ns	
Power consumption	100 – 300 mW/cm^2	
Radiation dose	3×10^{15} n_{eq}/cm^2, or 240 Mrad TID	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s

- ❑ Depends strongly on the desired time resolution
- ❑ Time resolution O(1) ns for BXID tagging

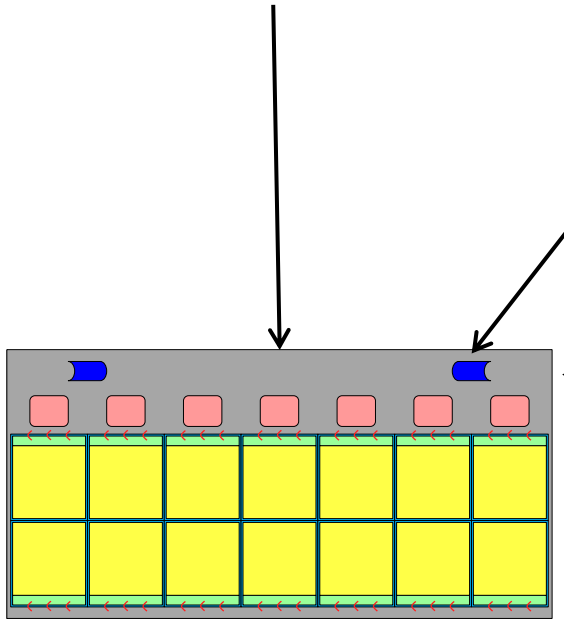
⇒ the cooling requirements

- ❑ The radiation hardness requirement is tougher than the MT
- ❑ HV-CMOS may be more radiation hard than LV-CMOS
- ❑ It may be possible to replace the inner-most modules beyond certain radiation dose

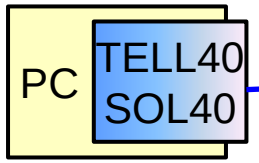
Readout Scheme

1 lpGBT provides 28×0.32, 14×0.64, or 7×1.28 Gbps **DATA** links

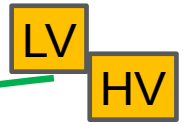
Designated lpGBTs for **ECS/TFC/CLK** as required.



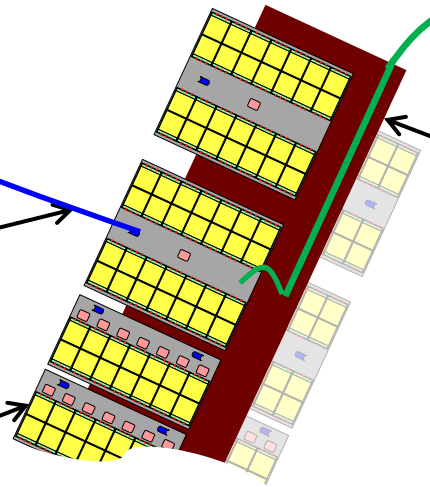
Data Center



Service Area



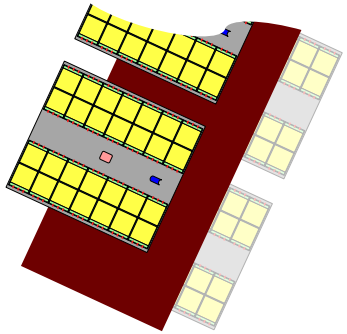
Detector



Flex Cable for LV/HV & return

4× 8.96 Gbps up-links
1× 2.56 Gbps down-link
per VTRx+

Multiple lpGBTs
& VTRx+
on a FE Module

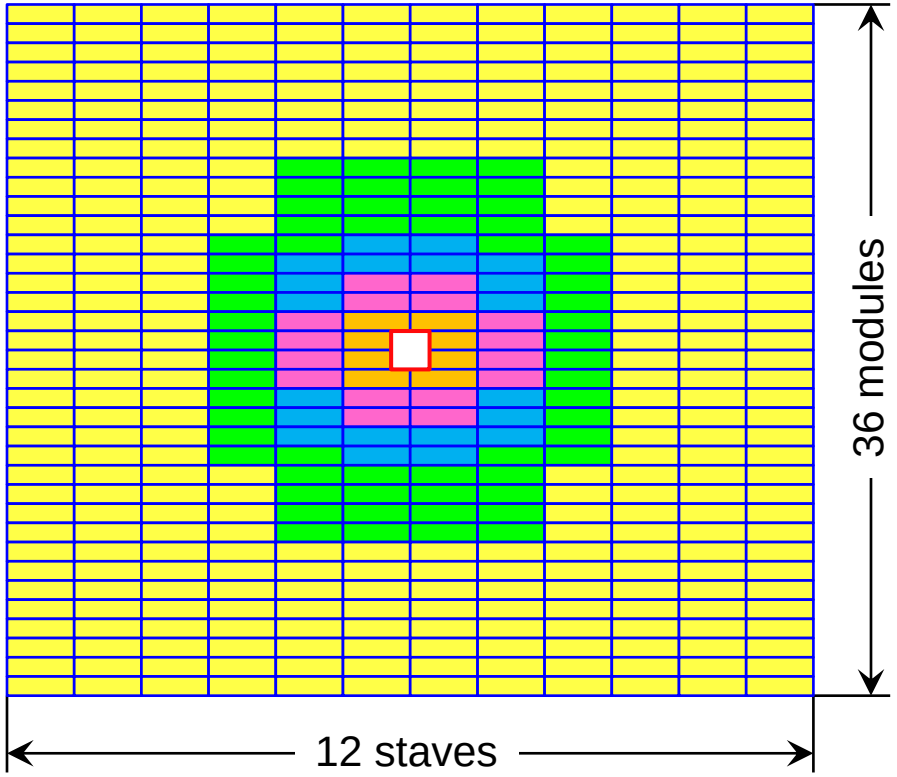


LV options:

1. Serial powering at FE
2. DC-DC convertors at FE
3. Individually regulated at SBC

Front End Data & Control Connections

A box corresponds a 7×2-Chip module



1888 lpGBTs (data)
1312 lpGBTs (control)
1312 VTRx+
4512 Optical fibers

PCIe400 boards

TELL400: 56 + 8(spare)
SOL400: 14 + 4(spare)

Ring	5	4	3	2	1	All
e-links / chip	1	1	1	1-3	2-7	
Gbps / e-link	0.32	0.64	1.28	1.28	1.28	
lpGBT / module	0.5	1	2	7	14/10	
Num of modules	1312	240	80	64	32	1728
Num of data lpGBTs	656	240	160	448	384	1888
Num of ctrl lpGBTs	656	240	80	192	144	1312

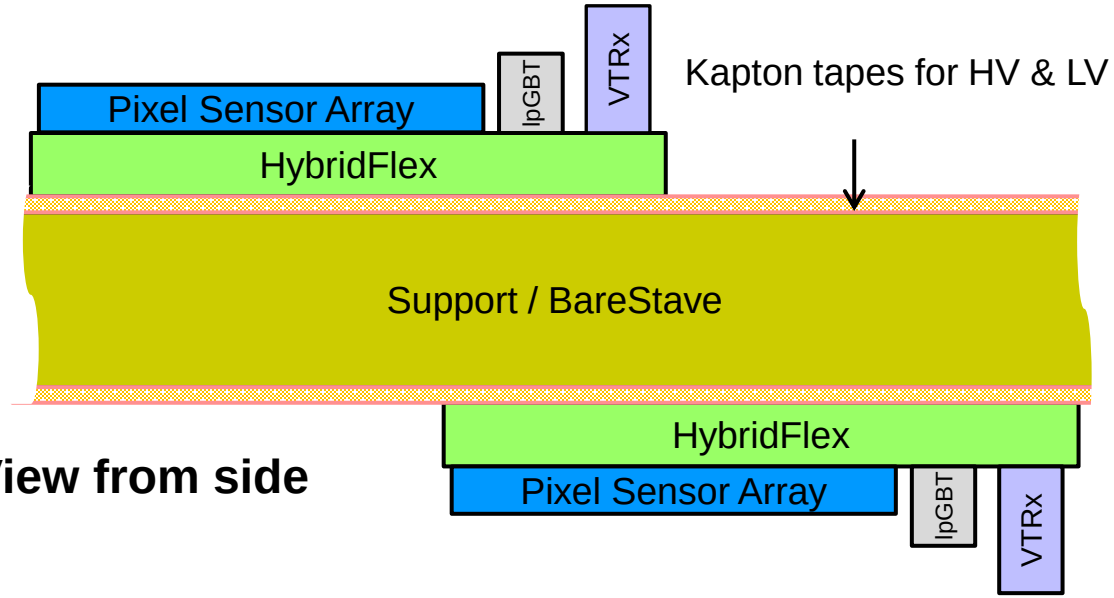
Dual-module

BXID	Column	Row	Parity
12b (0-3563)	9b (≤399)	6b (≤63)	1b

Assume 28 bits, without ToT or event packet

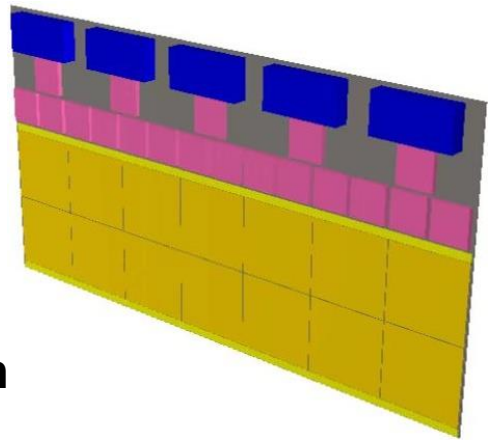
Module Type	A	B	C	D	E	F
Sensor Chips	28	14	14	14	14	10
lpGBT ASICs	2	2	3	10	19	14
VTRx+ units	1	1	1	3	5	4

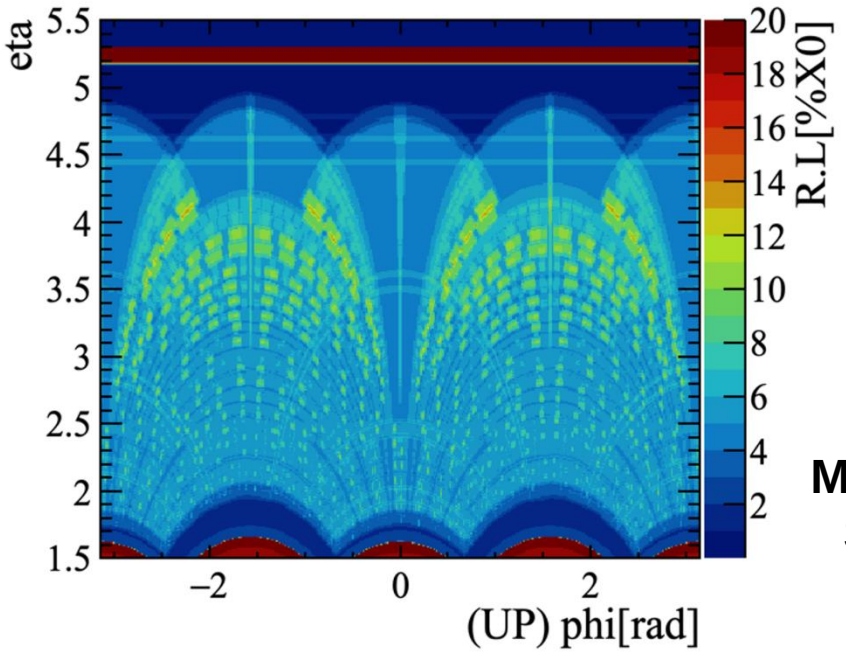
Conceptual Stave Design and Material Budget



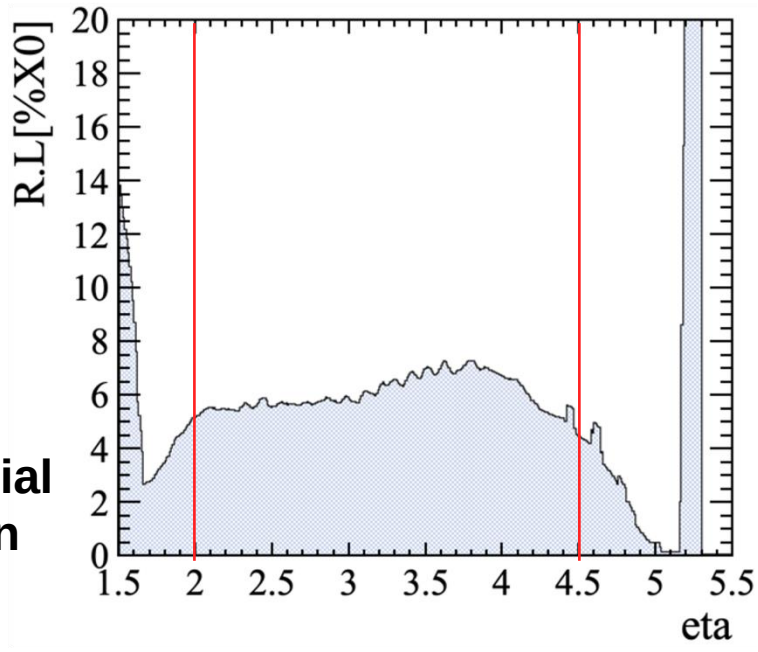
View from side

Detector description in MC simulation



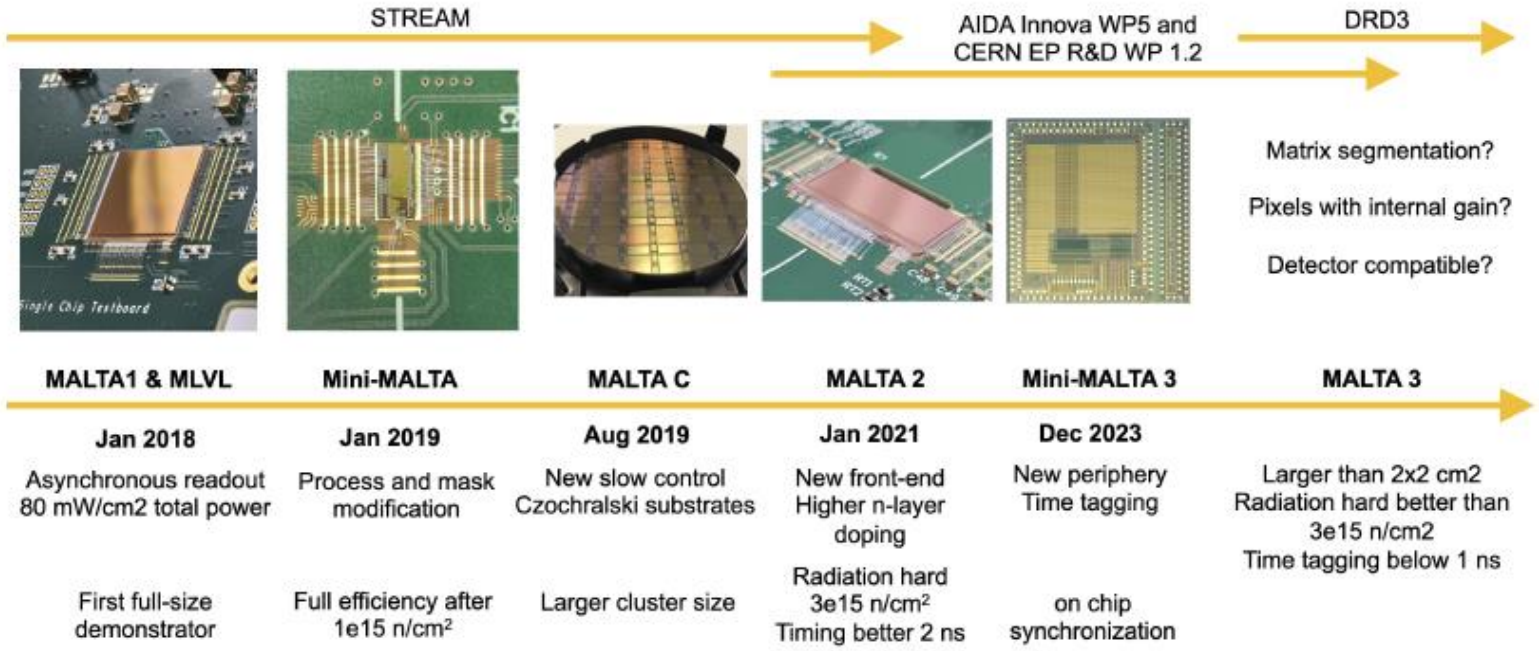


Material Scan

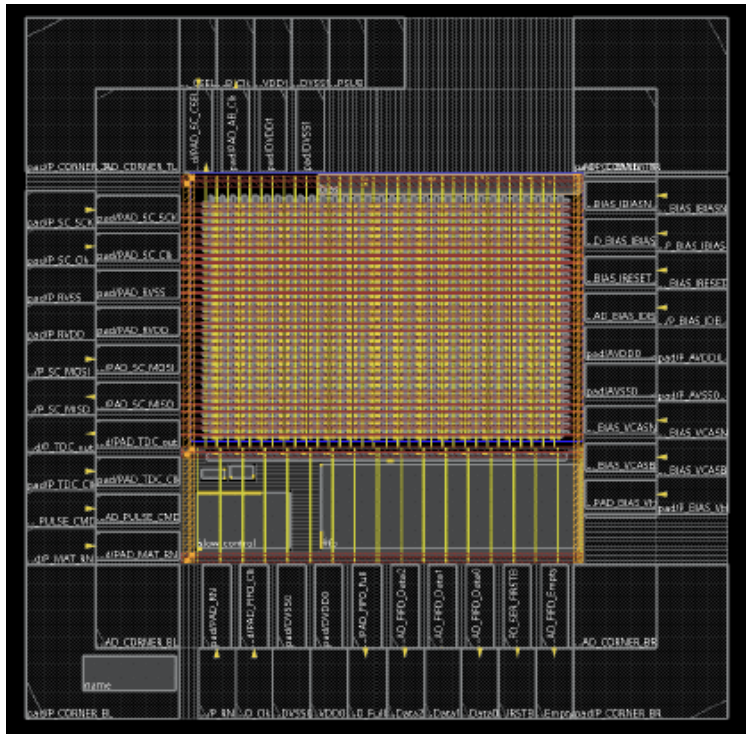


	Thickness [mm]	RL (2<h<4.5) [% X_0]
Pixel Sensor	0.200	0.24
lpGBT	1.250	0.07
VTRx+	4.000	0.13
HybridFlex	0.200	0.28
Kapton Tape	0.100	0.27
BareStave	4.000	0.21
One plane	**-**	**1.20**
UPBox	-	1.20
Air	-	0.01
Total	**-**	**6.01**

MALTA and SPARC



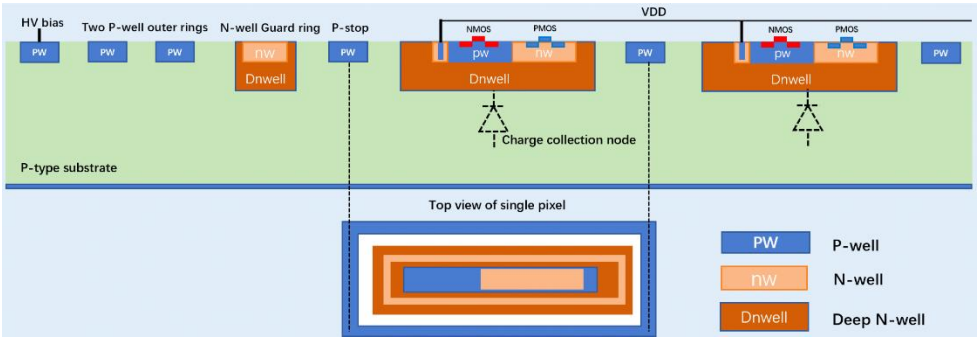
- IPHC, CERN, IRFU use TPSCo 65nm technology
- Chip of asynchronous versatile readout, 32×32 pixels (16×25 μm^2), available by Q4, 2024

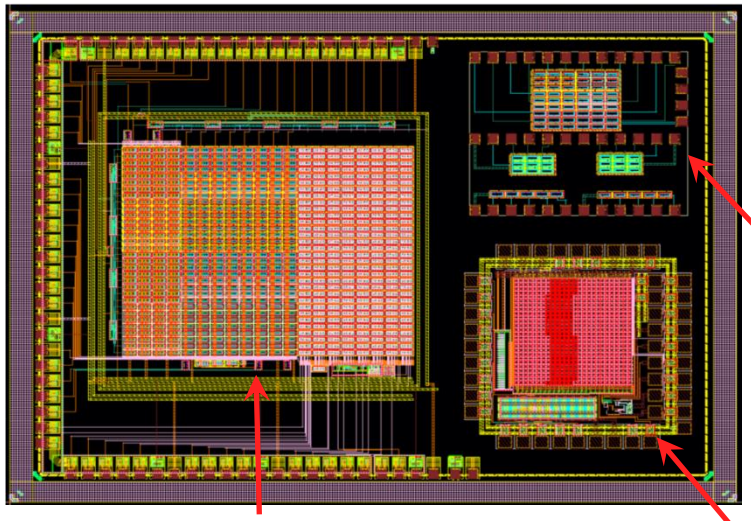


- MALTA2 chip is studied at CEA-IRFU.
- Threshold and noise were measured in room temperature.
- Common threshold set to ~60 e ⇒ dispersion ~13.7 e.
- Average noise ~12 e within expectation, homogenous over the whole matrix.

COFFEE Series

- Exploring alternative foundries (domestic especially), aiming for smaller feature size (180→55, 65 nm)
- COFFEE chip with SMIC 55nm process
  - HVCMOS process, with 1kΩ ·cm wafer
  - Next MPW submission ~ Oct 2024





COFFEE2 chip with SMIC 55 nm process

Zone 1

6×9 pixels, 80×40μm^2

Diodes of different charge collection

Zone 2

20×32 pixels, 72×36μm^2

Designs of charge collection & cell electronics

Zone 3

26×26 pixels, 25×25μm^2

Peripheral digital processing and communication

- Performed / ongoing studies on COFFEE2:
  - IV measurement, breakdown voltage
  - ISE-TCAD simulation study of V_{break}
  - CV measurement, depletion voltage
  - Radiation hardness
  - Readout and signal study with test board and a DAQ setup

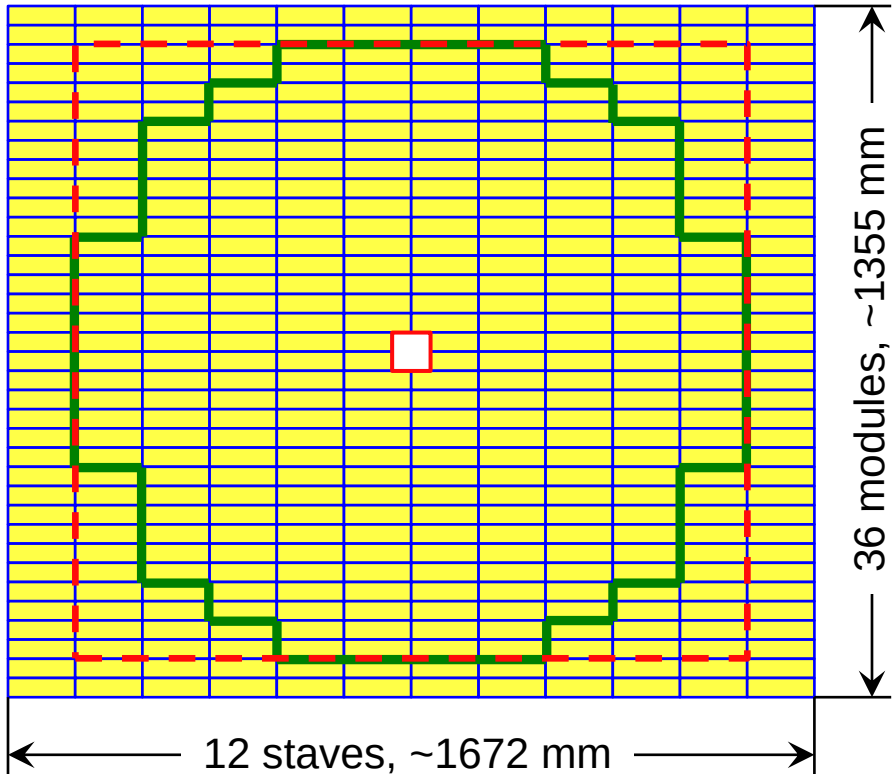
Karlsruher Institut für Technologie

UP Scoping Scenarios

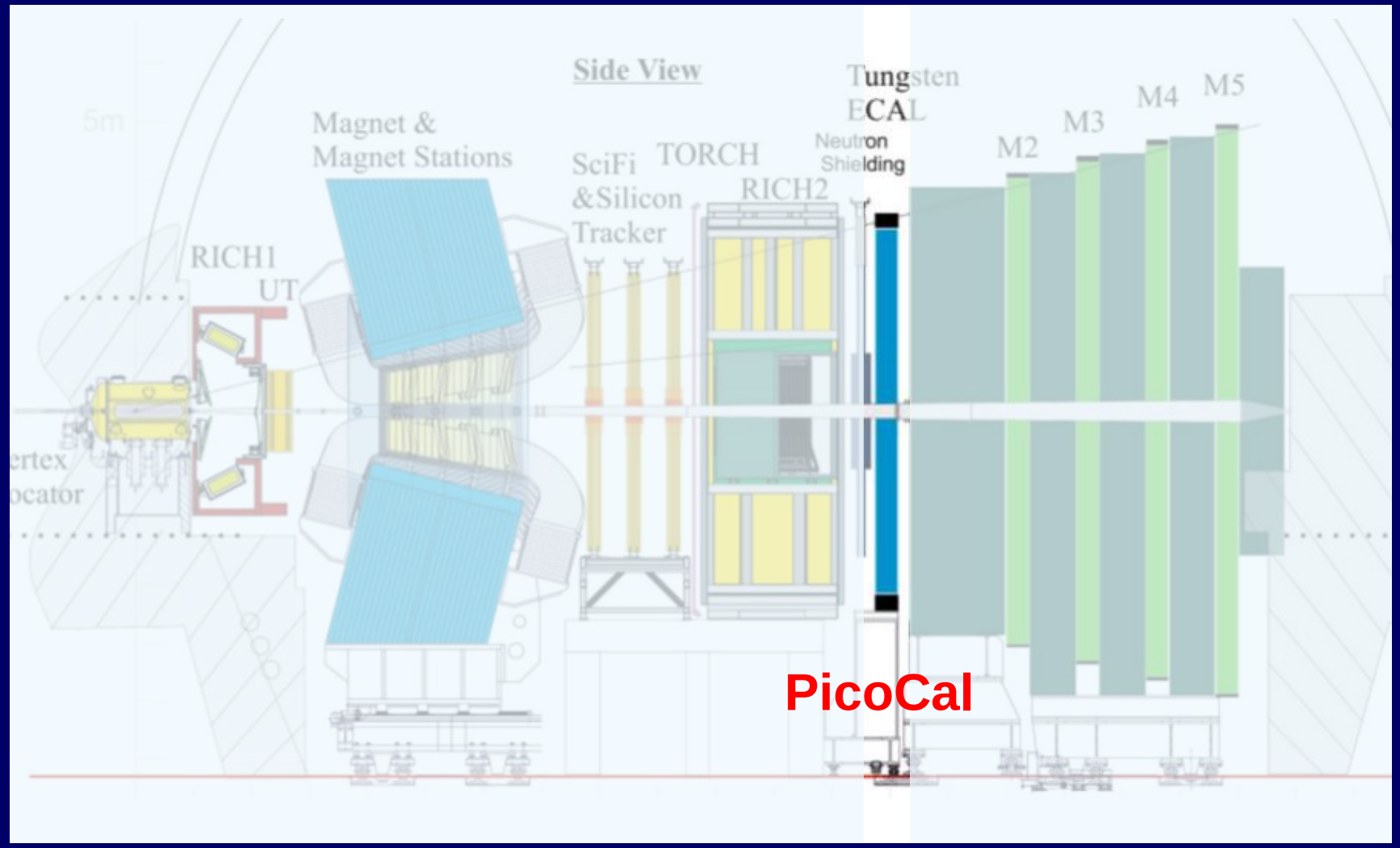
1) Reduced coverage: **(12→10)** staves × **(36→32)** modules
   - Reduce 26% detection area at the outer ring
   - The single track inefficiency ~5.5% in inclusive b events
   - The overall budget decreases from FTDR design by **~17%.** This is now considered as the new baseline design

2) Reduced peak luminosity (**1.5→1.3→1.0**)×10^{34} cm^{-2} s^{-1}
   - On top of the new baseline, this is considered medium plan
   - Designs of sensor chip & detector module are less difficult, even though the cost reduction is not very significant
   - Budget reduction from the new baseline: **1.8%** and **4.4%** for L = 1.3 and 1.0×10^{34} cm^{-2} s^{-1}, respectively

3) Further reduce the coverage (green line)
   - This is considered lower plan on top of L = 1.0×10^{34} cm^{-2} s^{-1}
   - Reduce 41% detection area over the original configuration, or 20% over new baseline.
   - The inclusive-b single track inefficiency ~9.3% over the original configuration, or 4.0% over new baseline
   - Budget reduction from the new baseline **~15%**



Phase II Upgrade: PicoCal / SPACAL



ECAL/PicoCal Management Structure

PL: Frederic Machefert (IJCLab)

DPL: Yuri Guz (PKU, ECAL), Rhilipp Roloff (CERN, PicoCal)

ECAL Management Structure

WP1: Absorbers
CERN, China
Hubert G. , Sergey K. & Liming Zhang (THU)

WP2: Optics assembly
UMD, Milano, & China*
Matteo S. & Zhenwei Yang (PKU)

WP4: PMT, HV & LED system
CERN, ICCUB, CSIC, UMD, Cincinnati, Bologna, Milano
Phoebe H., Yuri G. & Gonor H.

WP3: Organic & crystal fibers
UMD, & China*
Etiennette A. & Ming Zeng(THU)

WP5: Electronics
IJCLab, LPC, LAPP, ICCUB, CSIC, Syracuse
Patrick R. & Christophe B.

WP6: Infrastructure
CERN, LAPP, Imperial
Rolf L. & Andrei G.

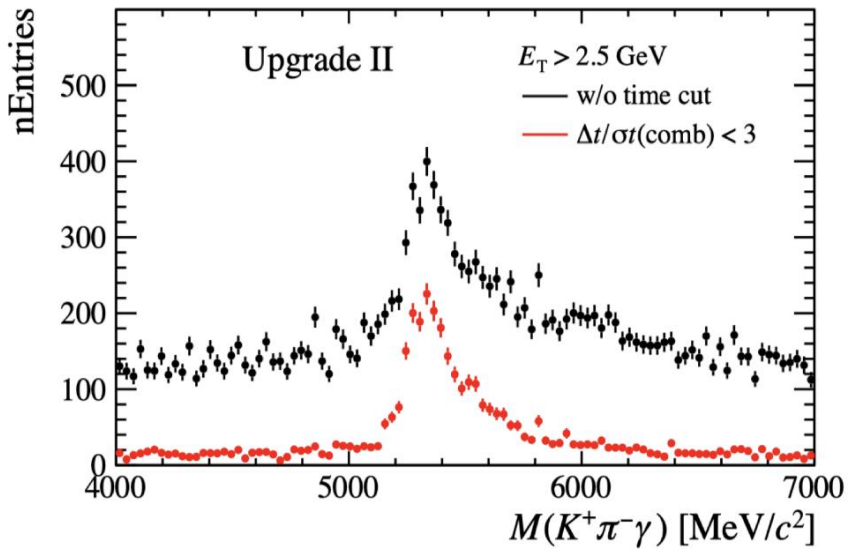
WP8: Testbeam coordination & analysis
CERN & All
Loris M. & Daniele M.

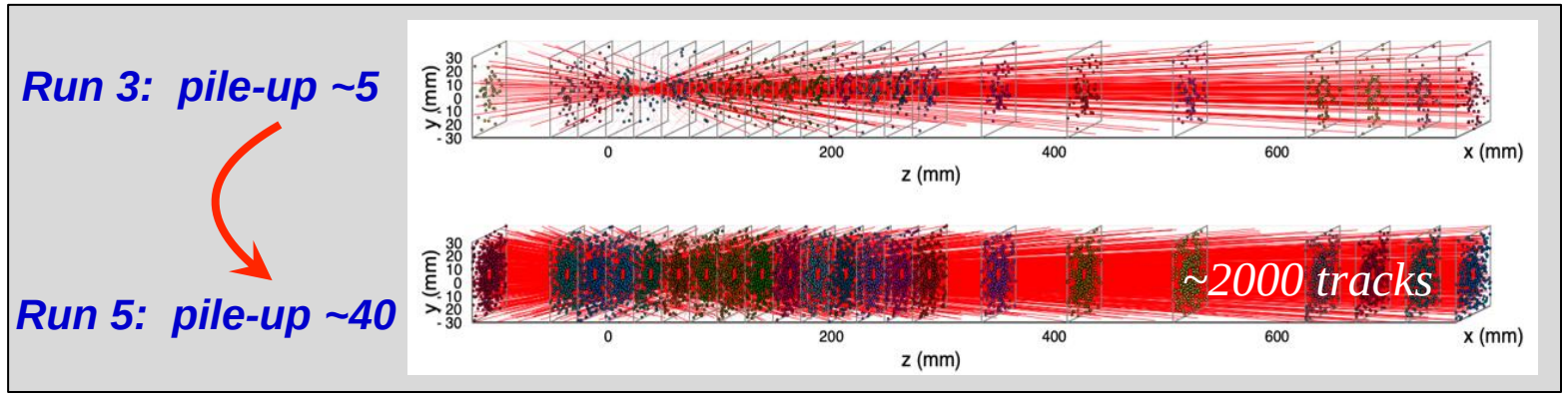
WP7: Detector Software
CERN, China*, La Salle, Padova, Milano-Bicocca, MIT, Syracuse
Marco P. & Liupan An (PKU)

PicoCal: Precise Time Measurement

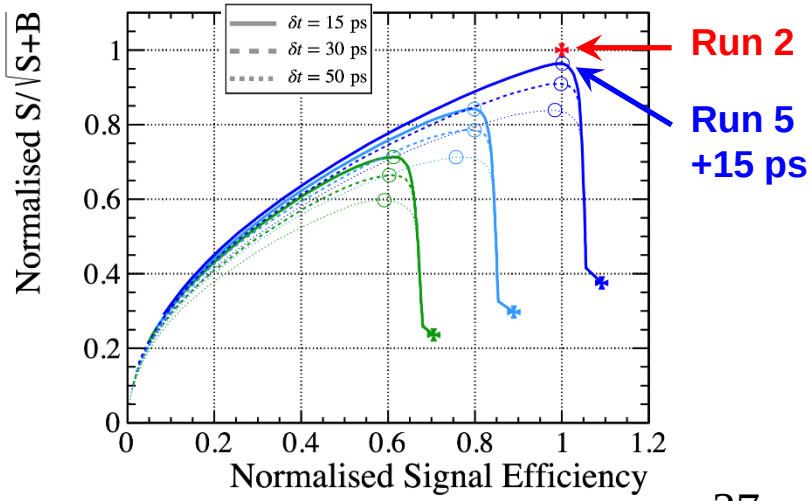
- To fight again large background due to pile-up, add time measurement in ECAL with a precision of 15 ps ➔ PicoCal
- Select cells with $|t_{ECAL} - t_{PV}| < 3\,\sigma(t)$
  - t_{PV} : collision time measured by other detectors
  - t_{ECAL}: time measured by ECAL cell, ToF corrected
  - $\sigma(t)$: ECAL time resolution

Effect of timing cut on invariant mass for B→ K*γ



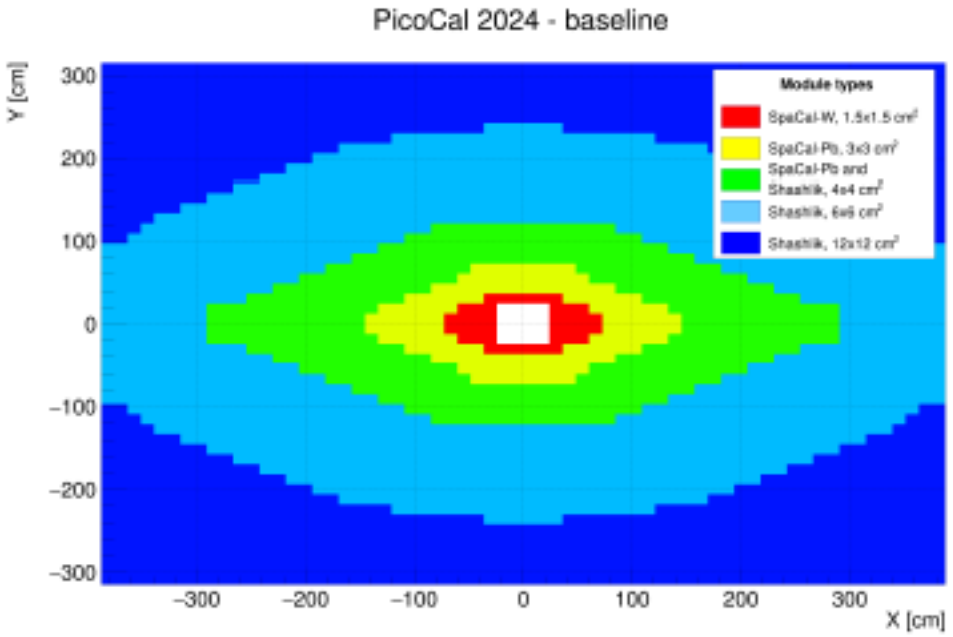


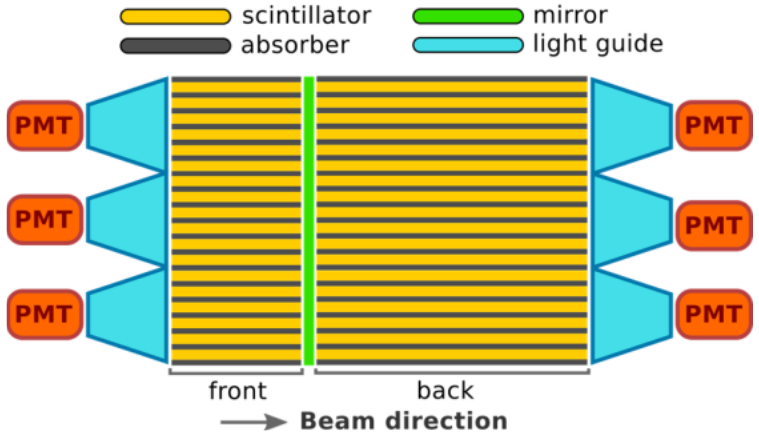
Signal $B^0 \to K^{*0}\,\gamma$ with pile-up



ECAL Upgrade (PicoCal): Granularity

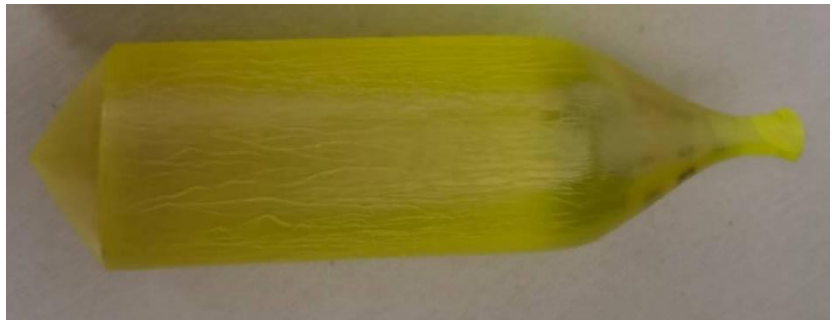
- Improve efficiently the performance at high luminosity
- Re-organize ECAL zones to follow the radiation and occupancy map
- Five zones with cells of different sizes: (1 module = 1 bloc of 12×12 cm^2)
  - **1.5x1.5 cm^2**: 32 modules (type SpaCal-W) – 2048 cells
  - **3x3 cm^2**: 144 modules (type SpaCal-Pb) – 2304 cells
  - **4x4 cm^2**: 448 modules (type Shashlik) – 4032 cells
  - **6x6 cm^2**: 1344 modules (type Shashlik) – 5376 cells
  - **12x12 cm^2**: 1344 modules (type Shashlik) – 1344 cells
- **Baseline option:** add longitudinal segmentation at shower maximum in all cells to separate e/h
- One cell = 2 channels for readout, 1 front and 1 back, total 30208 channels
- **Descoped option:** No longitudinal segmentation in outer modules (4x4 cm^2, 6x6 cm^2, 12x12 cm^2)



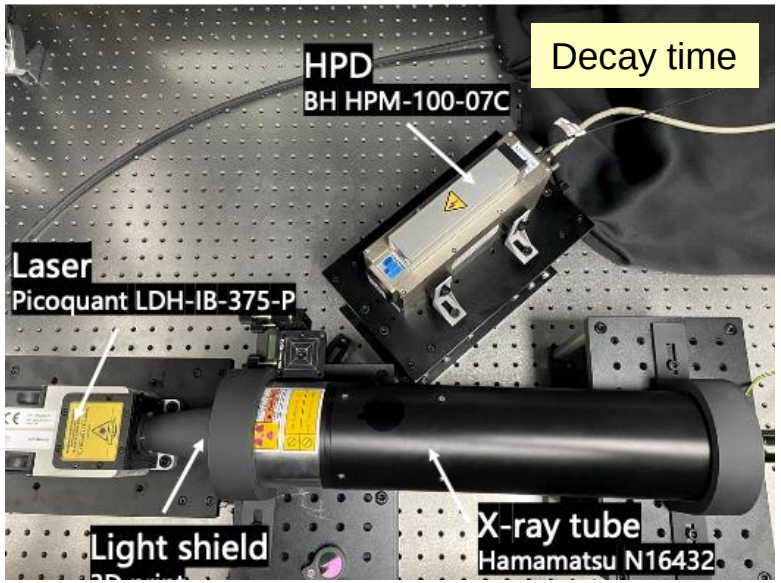


Chinese team works mainly on **SPACAL**

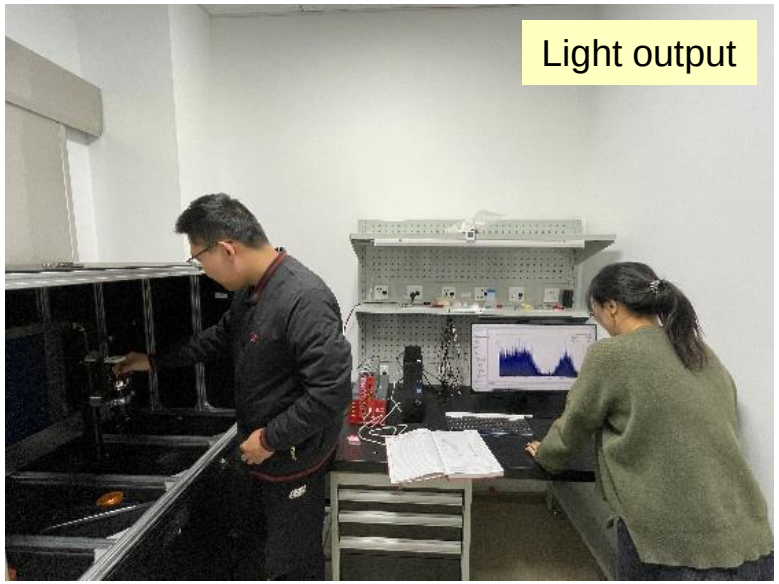
GAGG Scintillator Fiber



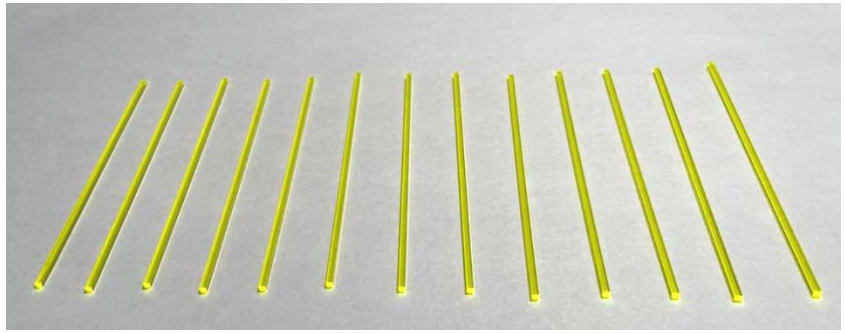
PKU



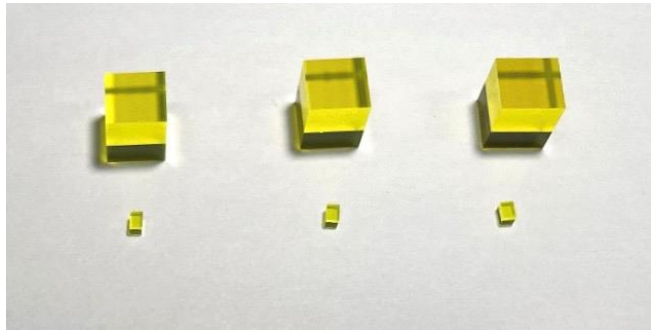
- GAGG scintillator for SPACAL: radiation-hard, high density, high light output, and fast decay time.
- Commercial available GAGG has decay time ~50 ns, desirable ~5 ns.
- Collaborate with电科芯片技术研究院, decay time was reduced to ~20 ns,



Fibers for prototype SPACAL [1x1mm^2]



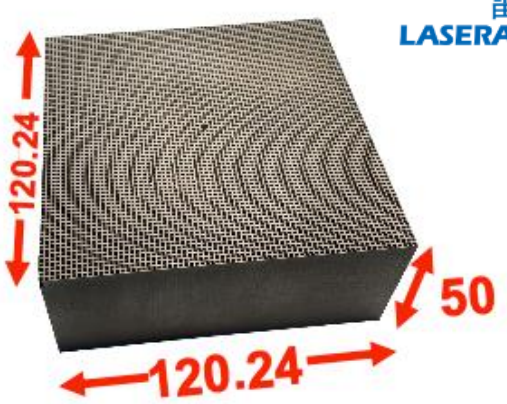
Test samples



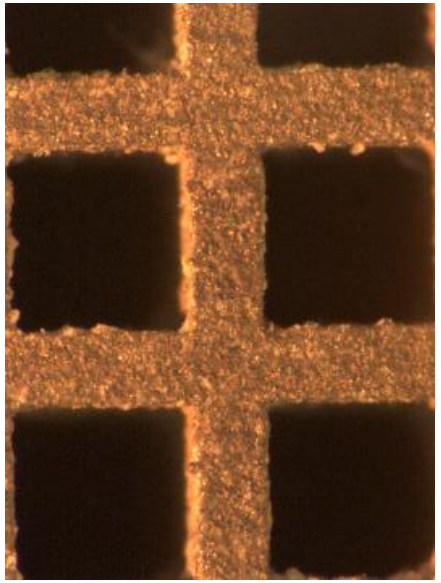
3D-Printing Tungsten (W) Absorber

- W has smaller radiation length and small Moliere radius
- Collaboration with LaserAdd to produce W absorber
  - High density, 18.9 g/cm^3, in comparison to 19.3 of pure W
  - Good roughness Ra ≈ 4 μm was achieved, can smoothly insert fibers
  - Good samples obtained for prototype detector

Unit: mm

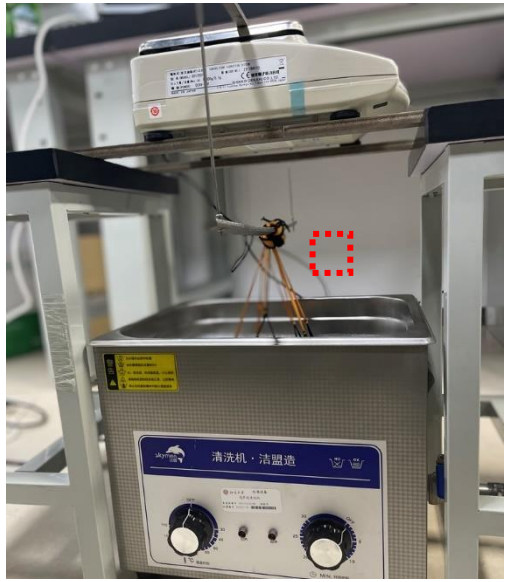


THU

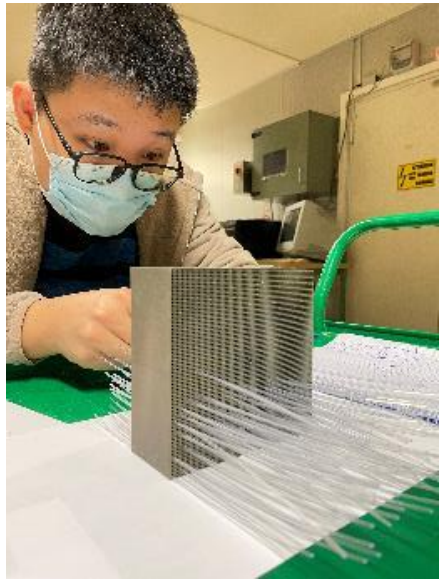


显微镜照片

测量表面粗糙度

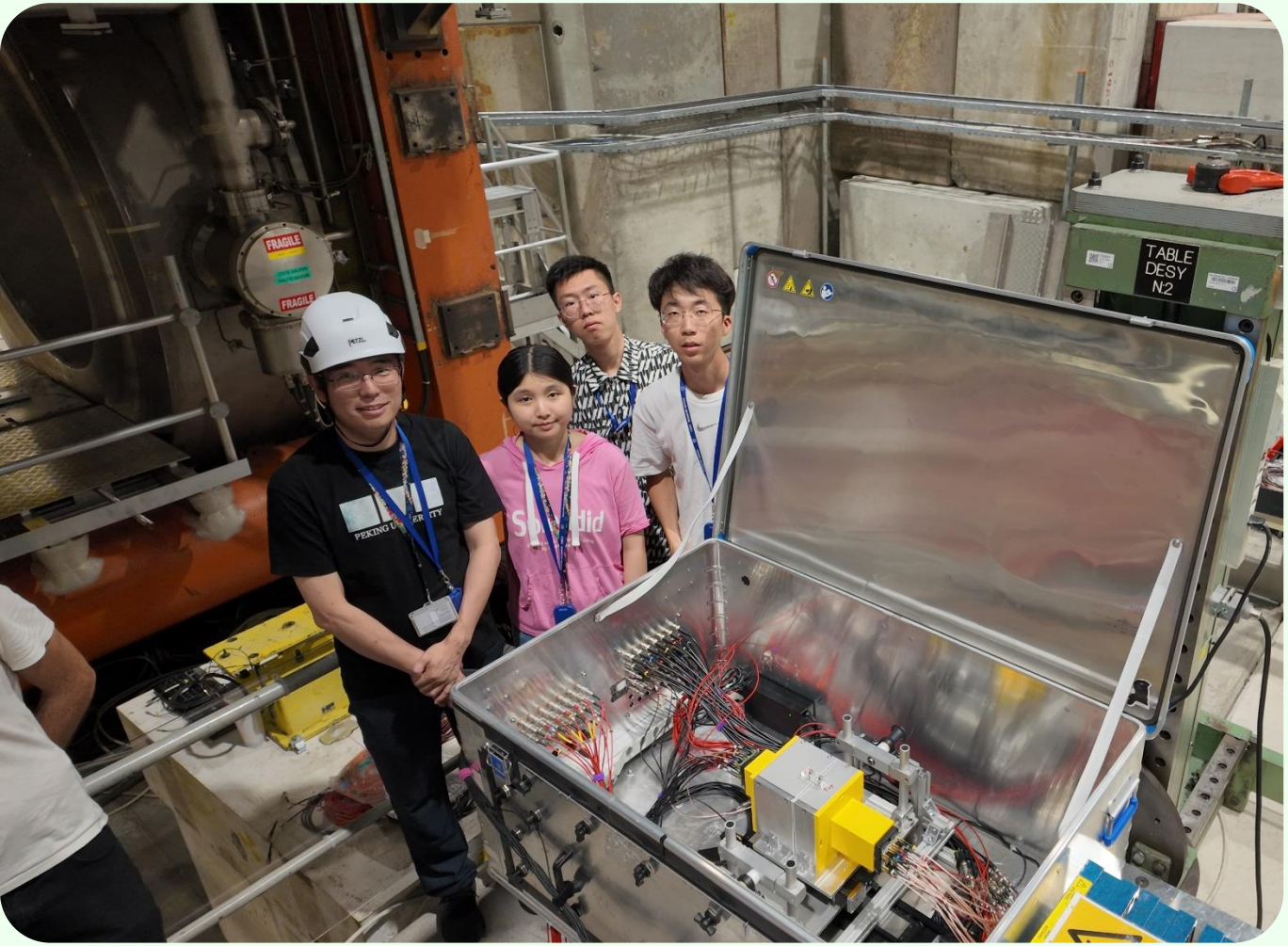


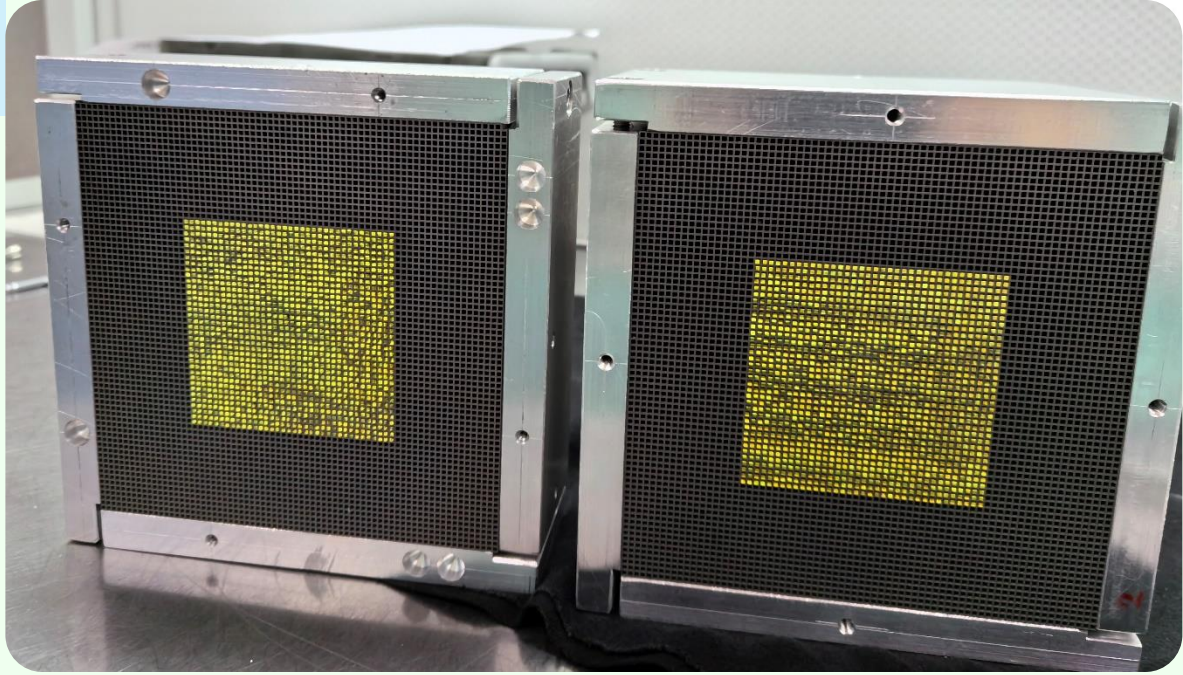
测量体积、密度

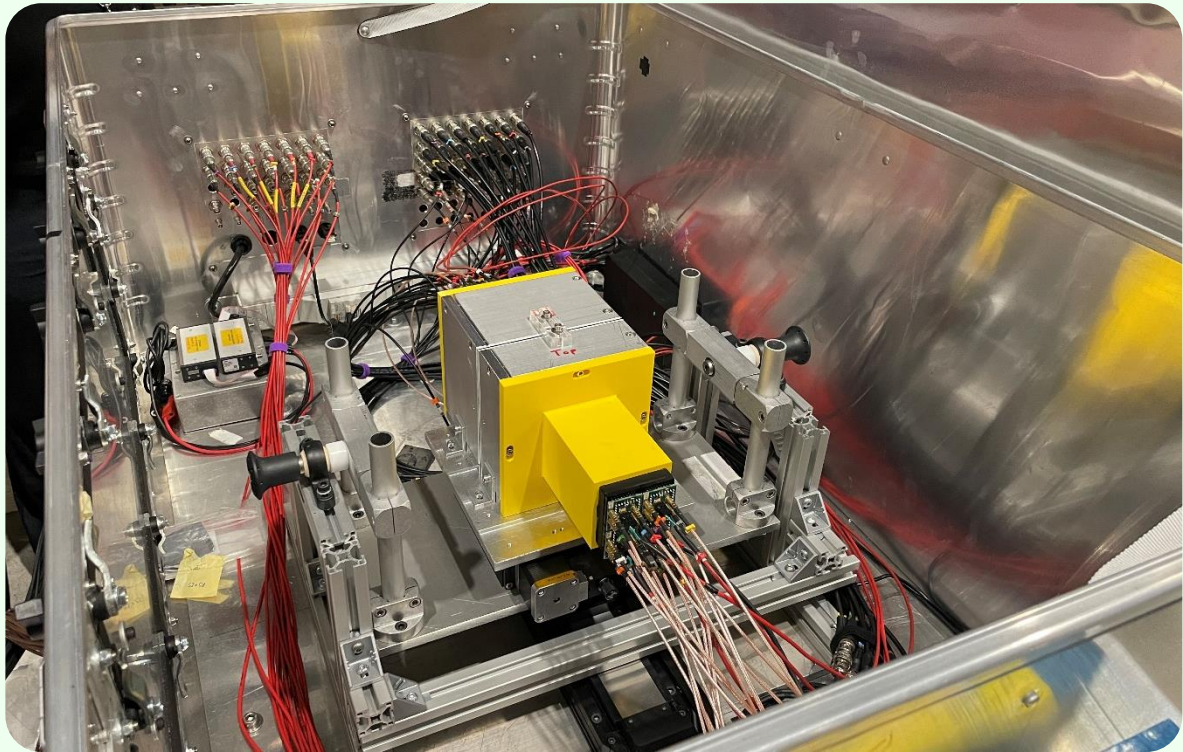


光纤插入测试

Testbeam of Prototype SPACAL







Testbeam of a prototype SPACAL at CERN 2024.07

07/17/2024

小结

- LHCb中国团队近年来不断发展壮大，除在物理分析研究、软件开发、实时数据分析等方面取得重要成果外，在探测器研制方面有非常大的进步，在合作组内已占有举足轻重的地位。
- 在一期升级中，中国团队在 闪烁光纤探测器 和上游硅微条径迹探测器 两个项目中做出显著贡献，也锻炼了队伍。
- 在二期升级中，中国团队已开展 上游硅像素径迹探测器 和 电磁量能器核心SPACAL量能器的研发，并将主导两个项目的发展。

非常感谢！