大型粒子物理实验中的电子学系统发展趋势及初步考虑

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青岛，核电子学与探测技术学术年会

下一代（基于加速器的）大型粒子物理实验探测器系统

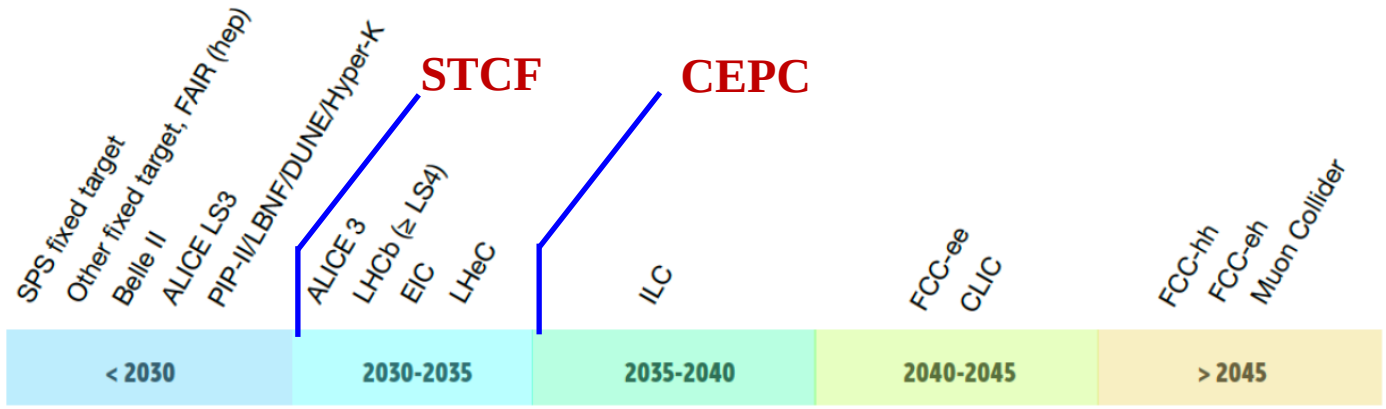
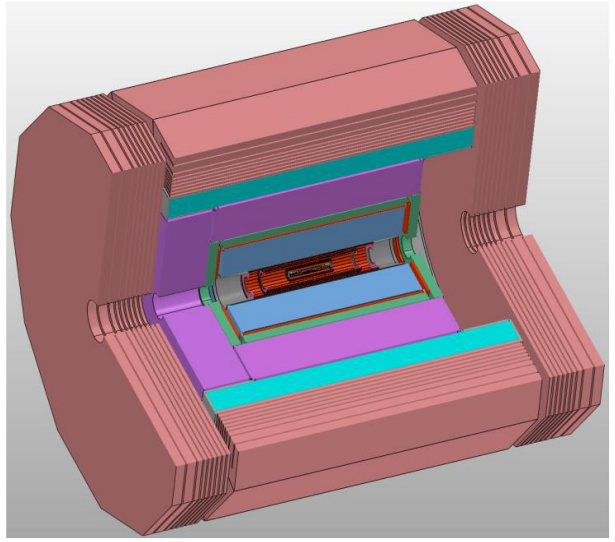
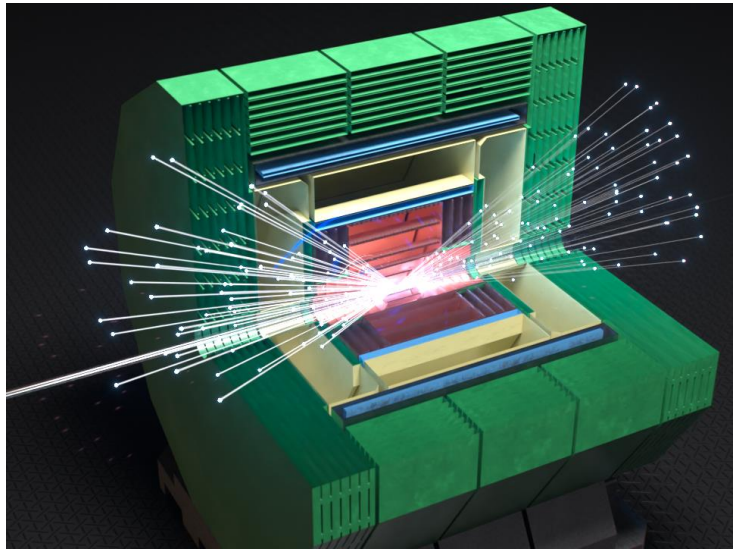


Figure 3: Large Accelerator Based Facility/Experiment Earliest Feasible Start Dates.

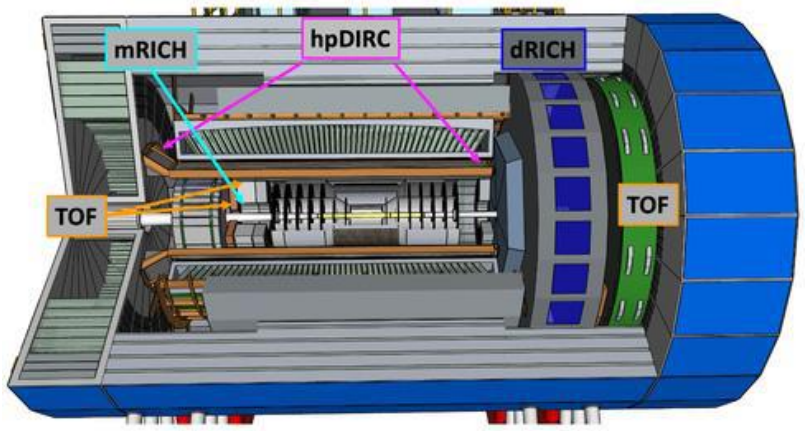
from European Committee for Future Accelerator (ECFA) Roadmap `21



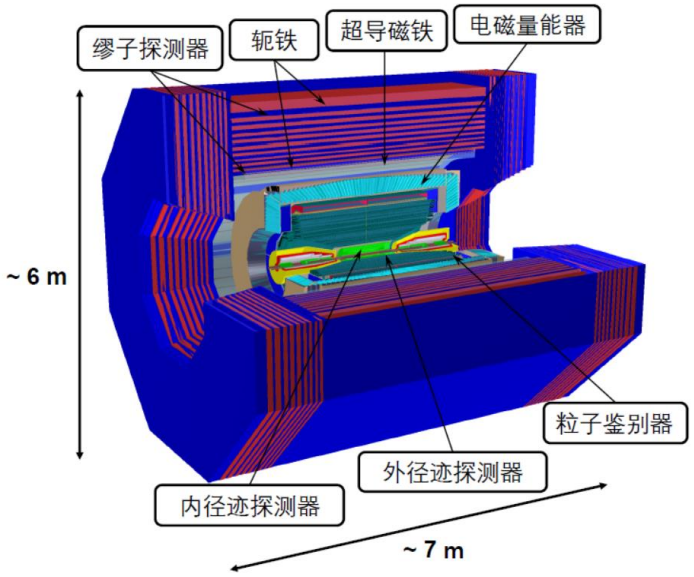
CEPC



FCC-ee



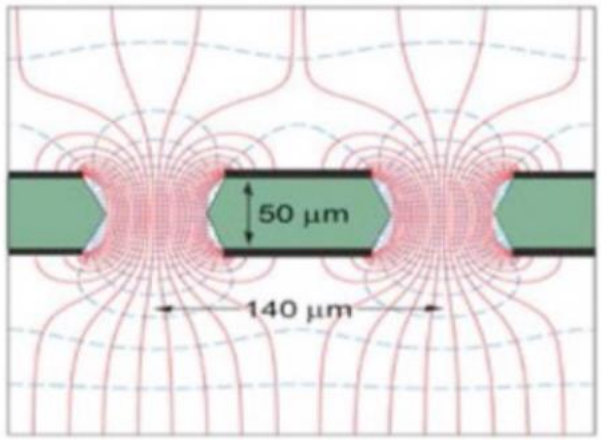
EIC



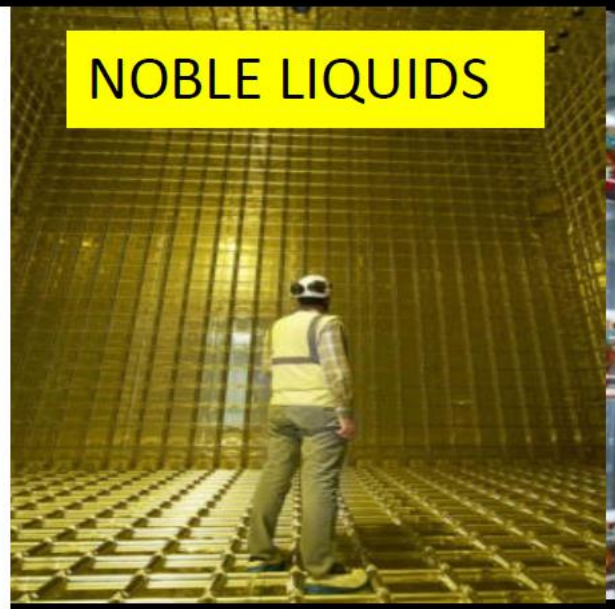
STCF

Technology Classification for the ECFA R&D Roadmap

GASEOUS



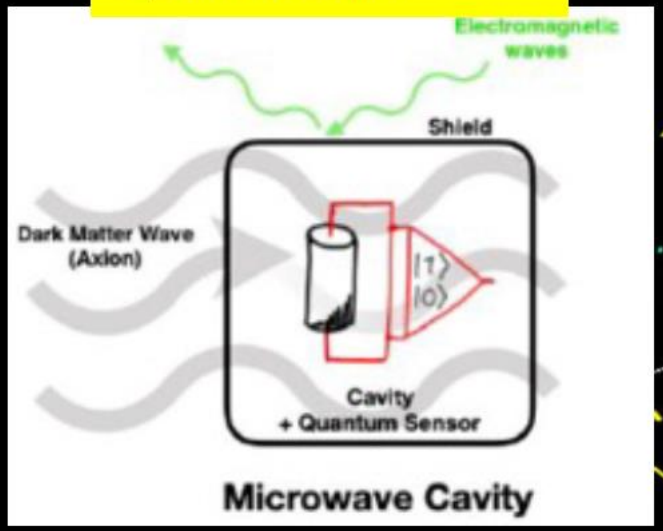
NOBLE LIQUIDS



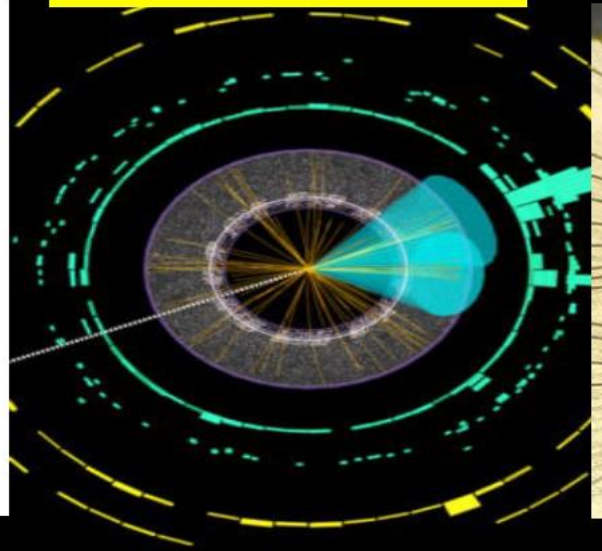
SOLID STATE

PHOTODETECTORS

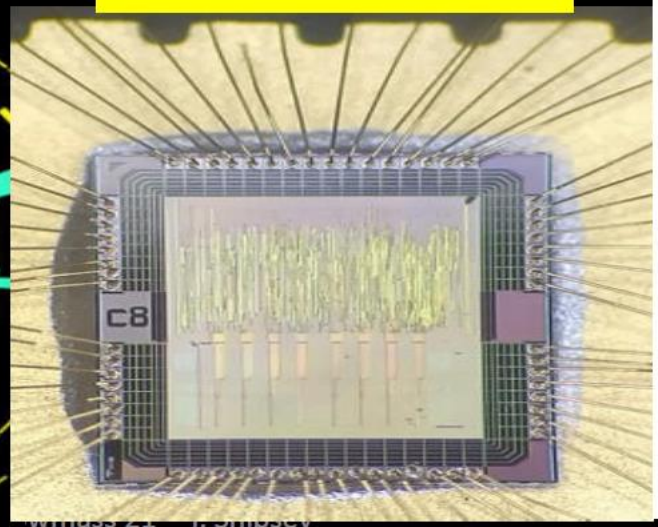
QUANTUM



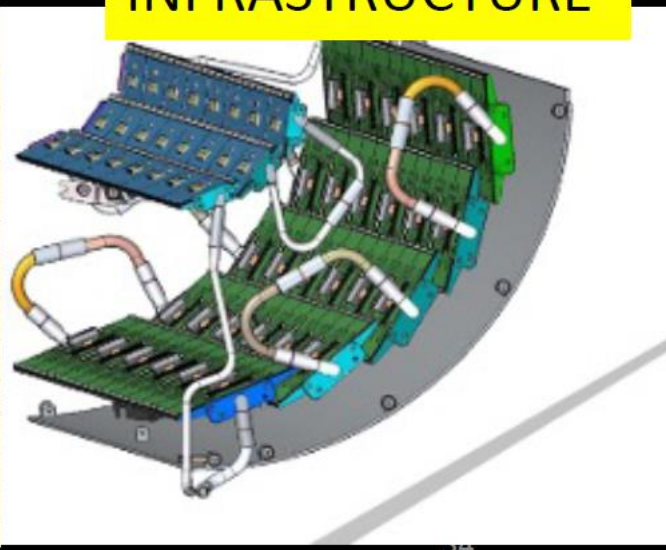
CALORIMETER



ELECTRONICS



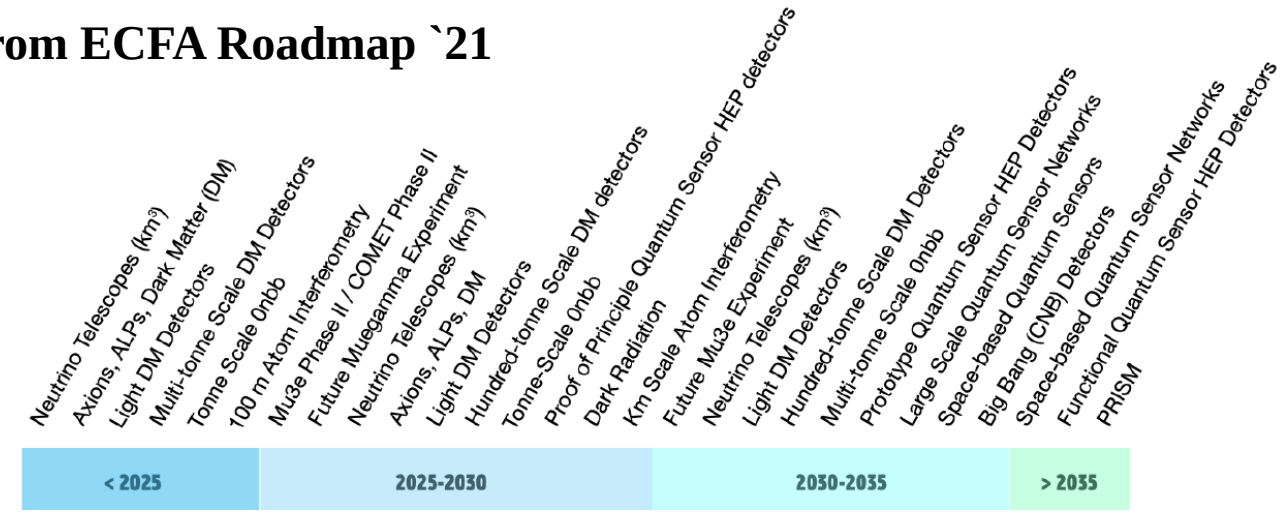
INFRASTRUCTURE



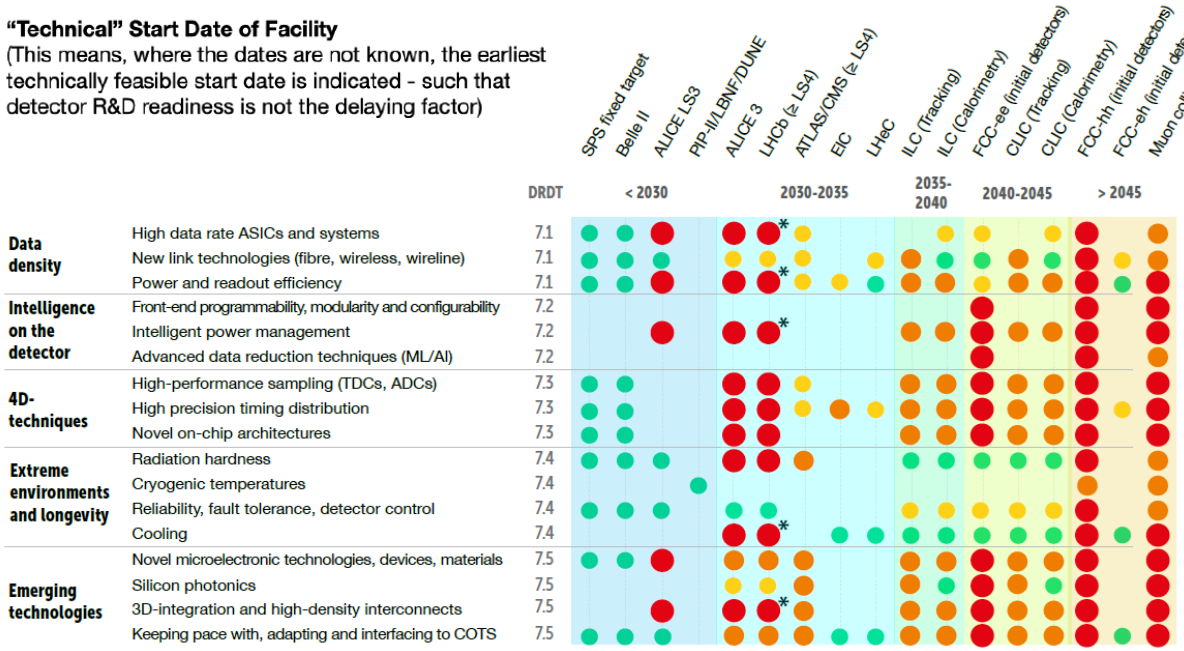
from ECFA Roadmap Snowmass 21 -- I. Shipsey

相关规划——欧洲ECFA探测器发展路线图

from ECFA Roadmap `21

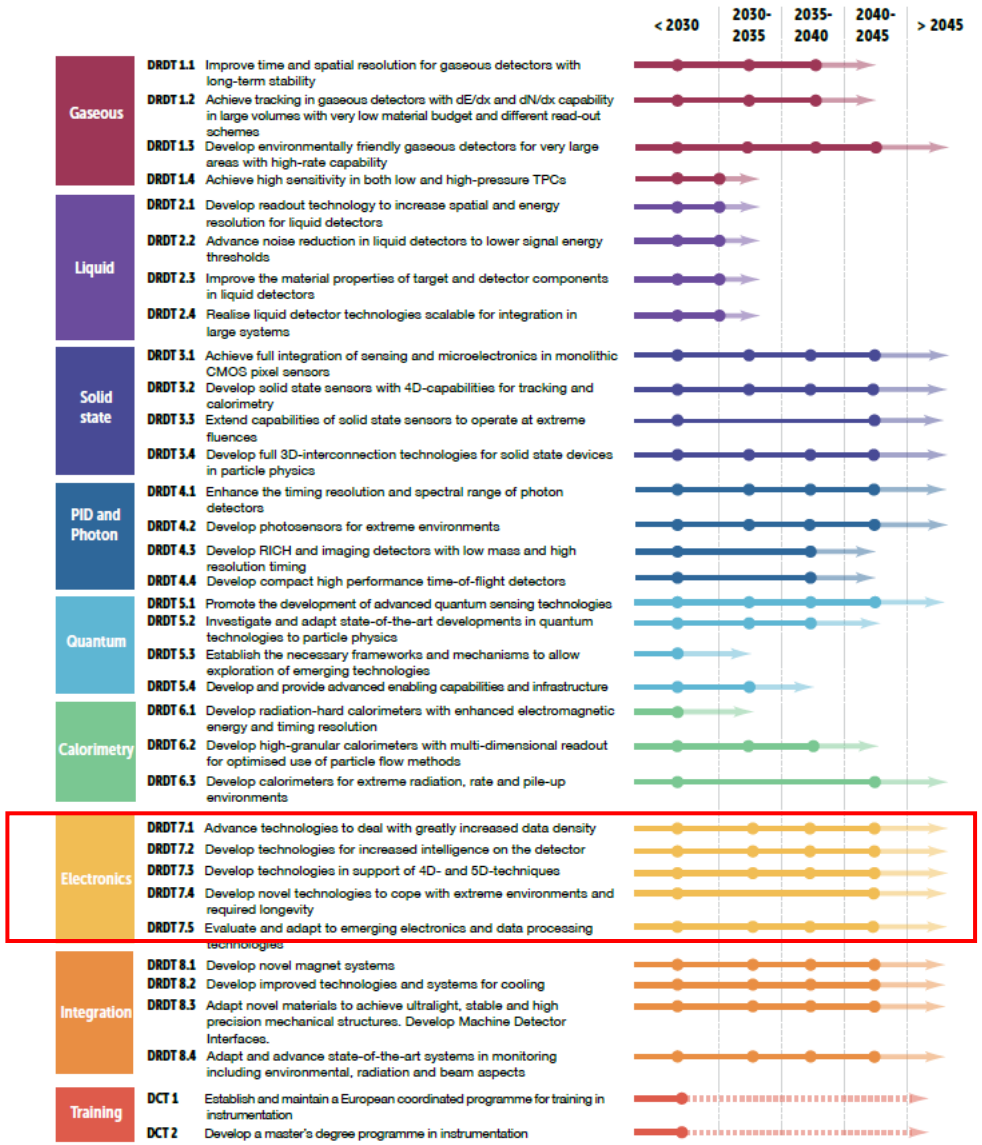


"Technical" Start Date of Facility
(This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)

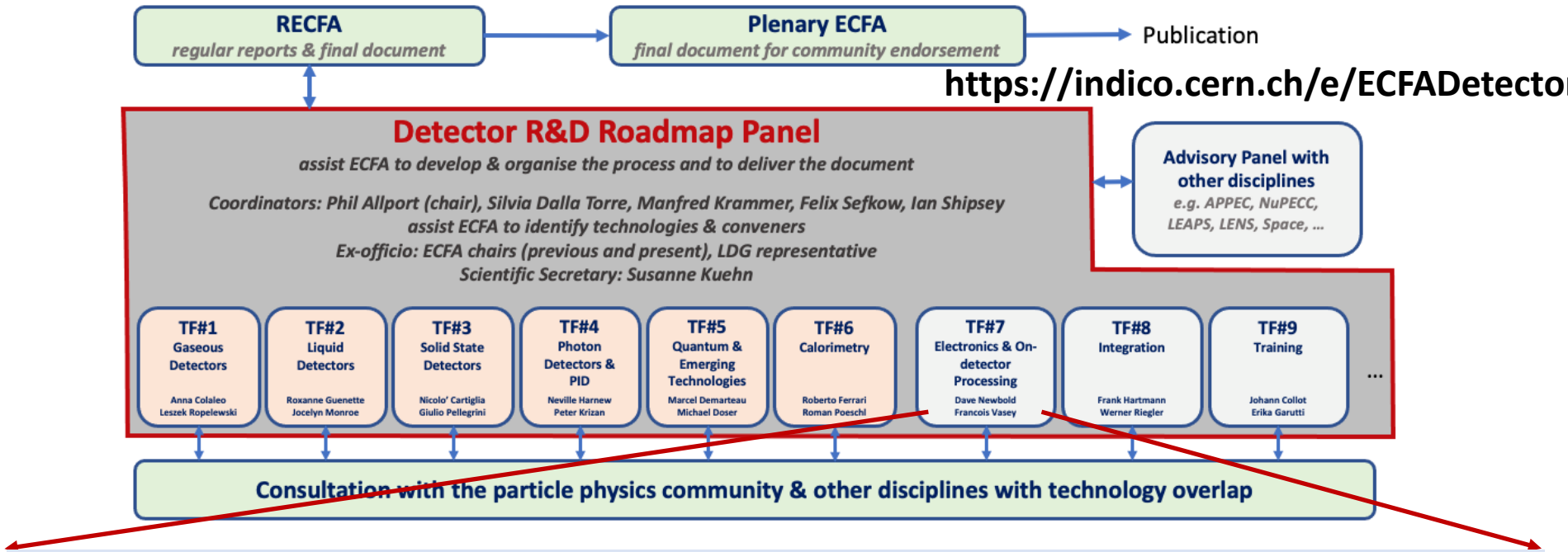


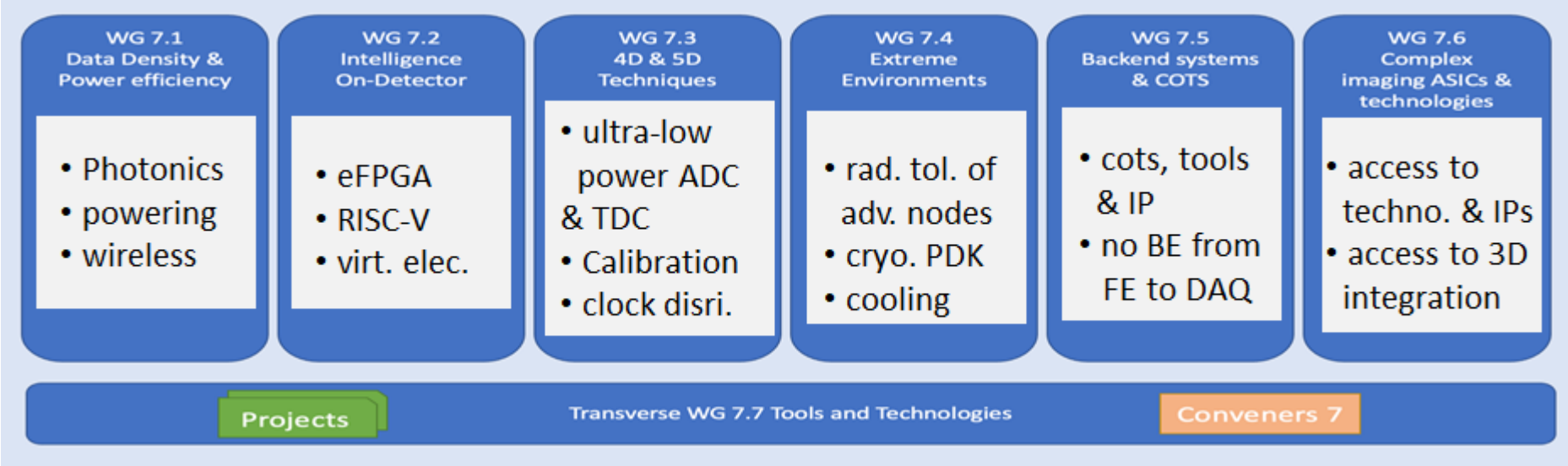
Must happen or main physics goals cannot be met
Important to meet several physics goals
Desirable to enhance physics reach
R&D needs being met

DETECTOR RESEARCH AND DEVELOPMENT THEMES (DRDTs) & DETECTOR COMMUNITY THEMES (DCTs)



相关规划——DRD7 for Electronics

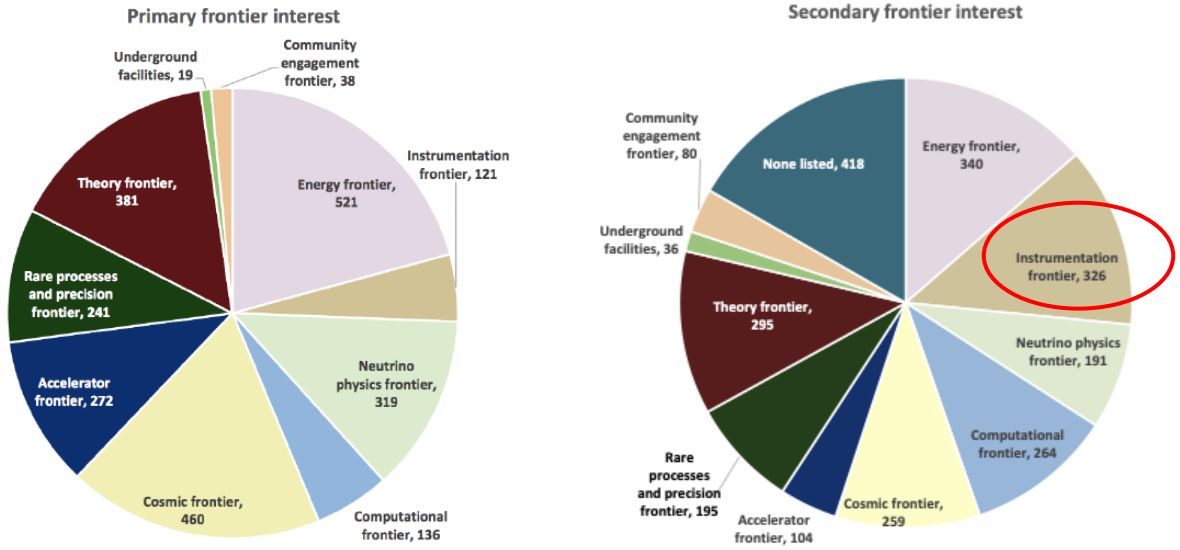




相关规划——美国SNOWMASS Instrumentation Frontier

10 Frontiers	80 Topical Groups
Energy Frontier	Higgs Boson properties and couplings, Higgs Boson as a portal to new physics, Heavy flavor and top quark physics, EW Precision Phys. & constraining new phys., Precision QCD, Hadronic structure and forward QCD, Heavy Ions, Model specific explorations, More general explorations, Dark Matter at colliders
Frontiers in Neutrino Physics	Neutrino Oscillations, Sterile Neutrinos, Beyond the SM, Neutrinos from Natural Sources, Neutrino Properties, Neutrino Cross Sections, Nuclear Safeguards and Other Applications, Theory of Neutrino Physics, Artificial Neutrino Sources, Neutrino Detectors
Frontiers in Rare Processes & Precision Measurements	Weak Decays of b and c, Strange and Light Quarks, Fundamental Ph… …eriments. Baryon and Lepton Number Violation, Charged Lepton Flavor Violation … …es, Hadron spectroscopy
Cosmic Frontier	Dark Matter: Particle-like, Dark Matter: Wave-lik… …Energy & Cosmic Acceleration: The Modern Universe, Dark … …mic Dawn & Before, Dark Energy & Cosmic Acceleration: Complement…
Theory Frontier	String theory, quantum gr… …ry techniques, CFT and formal QFT, Scattering amplitudes, Lattice … …precision physics, Collider phenomenology, BSM model building, Astro… …uantum information science, Theory of Neutrino Physics
Accelerator Frontier	Be… …on, Accelerators for Neutrinos, Accelerators for Electroweak and Higgs …elerators for Physics Beyond Colliders & Rare Processes, Advanced …elerator Technology R&D: RF, Magnets, Targets/Sources
Instrumentati…	…s, Photon Detectors, Solid State Detectors & Tracking, Trigger and DAQ, Micro Pattern Gas …Calorimetry, Electronics/ASICS, Noble Elements, Cross Cutting and System Integration, Radio …ction
Computational …	Experimental Algorithm Parallelization, Theoretical Calculations and Simulation, Machine Learning, Storage and processing resource access (Facility and Infrastructure R&D), End user analysis
Underground Facilities and Infrastructure Frontier	Underground Facilities for Neutrinos, Underground Facilities for Cosmic Frontier, Underground Detectors
Community Engagement Frontier	Applications & Industry, Career Pipeline & Development, Diversity & Inclusion, Physics Education, Public Education & Outreach, Public Policy & Government Engagement

30 Frontier conveners, ~250 Topical Group conveners,
>40 Inter-Frontier Liaisons, ~25 Early Career Liaisons

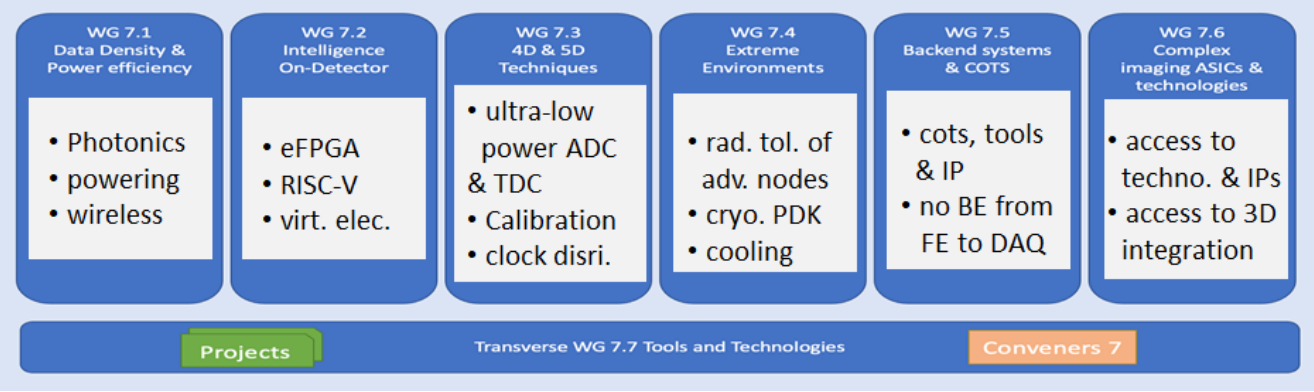


在前沿关注方面列居领域第三

- **IF07 White Papers – ASICs and Electronics**
  - **Calorimeter Readout Electronics**
  - **Electronics for Fast Timing**
  - **Optical Links**
  - **Smart Sensors Using AI**
  - **Cryogenics Readout**
  - **RF Electronics**

US Snowmass'21 process and perspectives, Tor Raubenheimer
https://arxiv.org/pdf/2209.15519

国外主要发展规划的共性趋势——关键词



DRD7

Data density	High data rate ASICs and systems
	New link technologies (fibre, wireless, wireline)
	Power and readout efficiency
Intelligence on the detector	Front-end programmability, modularity and configurability
	Intelligent power management
	Advanced data reduction techniques (ML/AI)
4D-techniques	High-performance sampling (TDCs, ADCs)
	High precision timing distribution
	Novel on-chip architectures
Extreme environments and longevity	Radiation hardness
	Cryogenic temperatures
	Reliability, fault tolerance, detector control
	Cooling
Emerging technologies	Novel microelectronic technologies, devices, materials
	Silicon photonics
	3D-integration and high-density interconnects
	Keeping pace with, adapting and interfacing to COTS

ECFA

- **IF07 White Papers– ASICs and Electronics**
  - **Calorimeter Readout Electronics**
  - **Electronics for Fast Timing**
  - **Optical Links**
  - **Smart Sensors Using Artificial Intelligence**
  - **Cryogenics Readout**
  - **RF Electronics**

- **侧重点&区别：**
  - **ECFA & DRD7的技术驱动性更明显**
  - **SNOWMASS IF7的应用针对性更明显**
- **一些共性关键词：**
  - **ASIC**
  - **Timing**
  - **Link**
  - **Intelligence**
  - **Cryogenic**
  - **……**

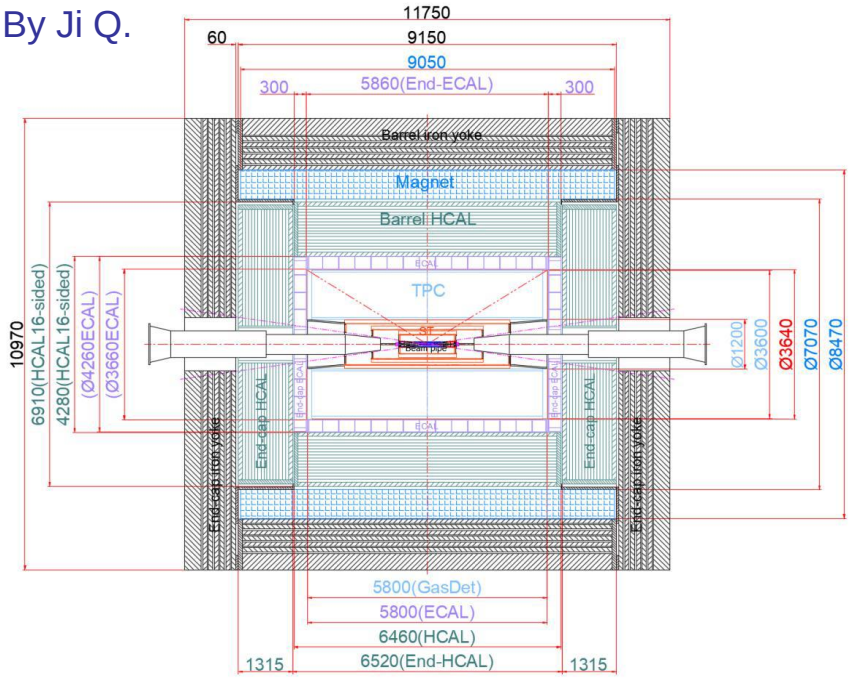
我们需要怎样的下一代电子学系统？——以CEPC为例

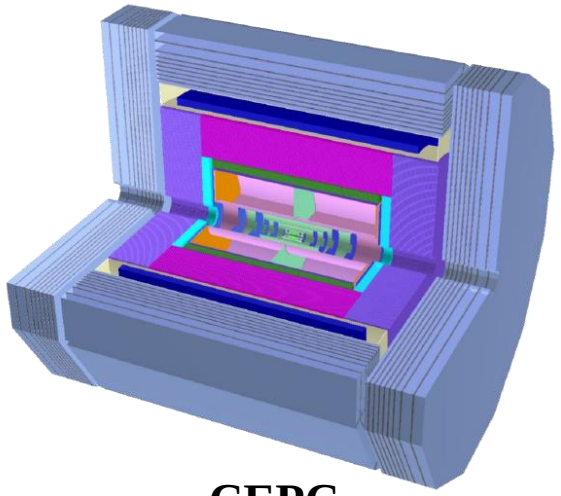
System	Technologies		
Vertex	CMOS Pixel	CMOS+Stitching	SOI
Tracker & PID	SPD ITrk		
	Pixelated TPC	PID Drift Chamber	
	AC-LGAD OTrk	SSD OTrk	SPD OTrk
		LGAD ToF	
ECAL	4D Crystal Bar	Stereo Crystal Bar	
	GS+SiPM	PS+SiPM+W	SiDet+W
HCAL	GS+SiPM+Fe	PS+SiPM+Fe	RPC+Fe
Magnet	LTS	HTS	
Muon	PS Bar+SiPM	RPC	
TDAQ	Conventional	Software Trigger	
BE electr.	Common	Independent	

R

Baseline　For Comparison　To Be Decided

By Ji Q.

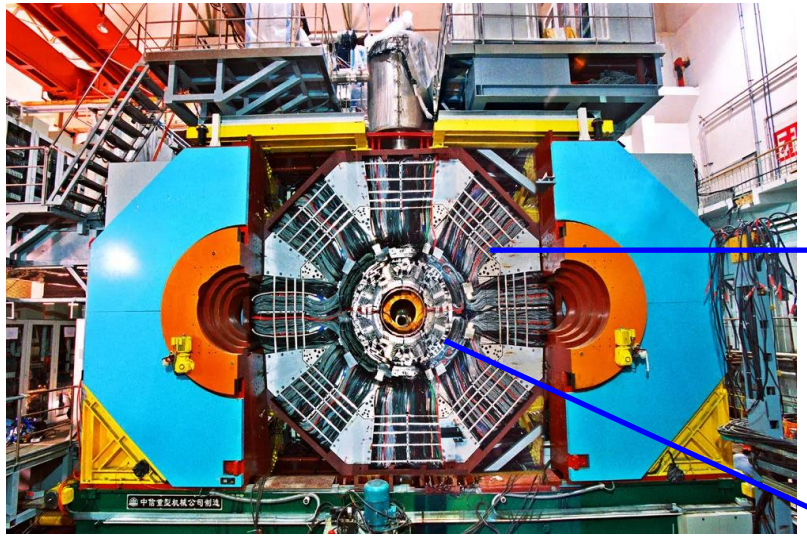


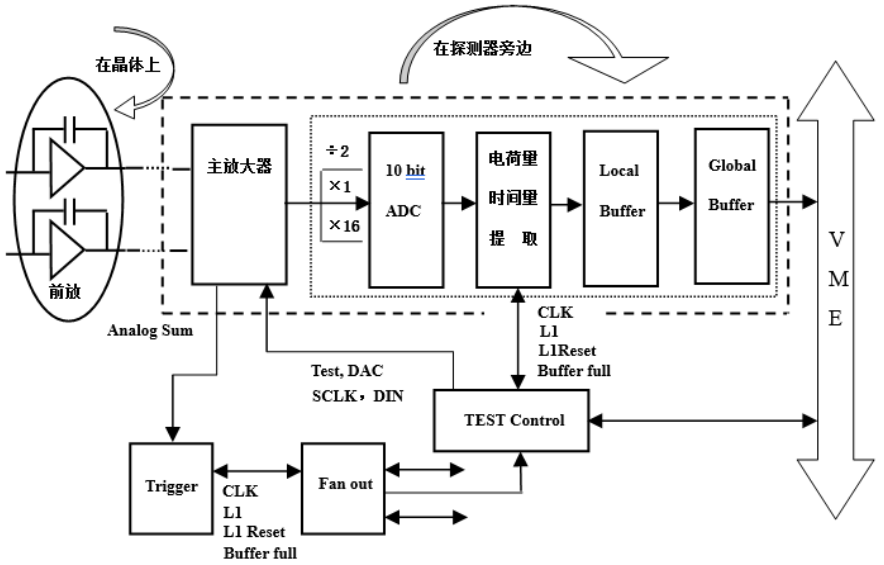


CEPC

- 我们正准备参考性探测器的技术设计报告（Ref-TDR）
- 将继续开展各项探测器关键技术R&D

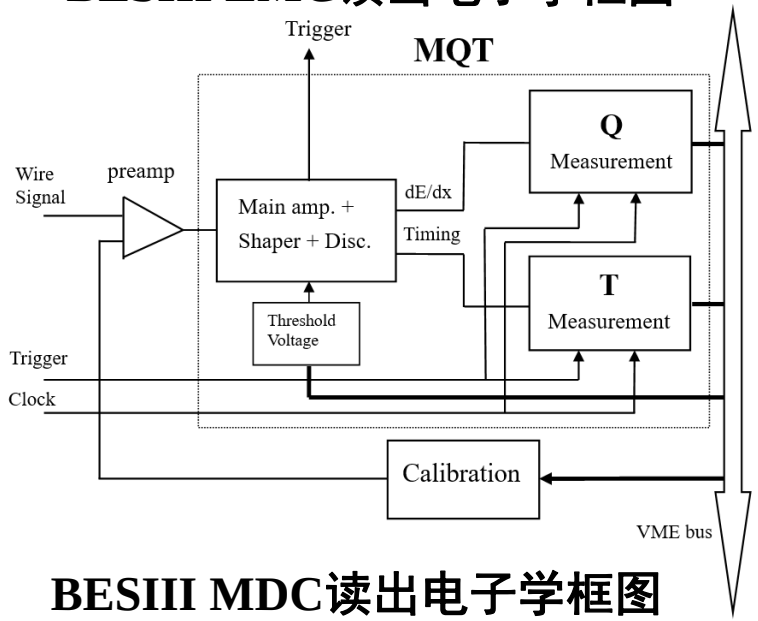
此前…





BESIII EMC读出电子学框图

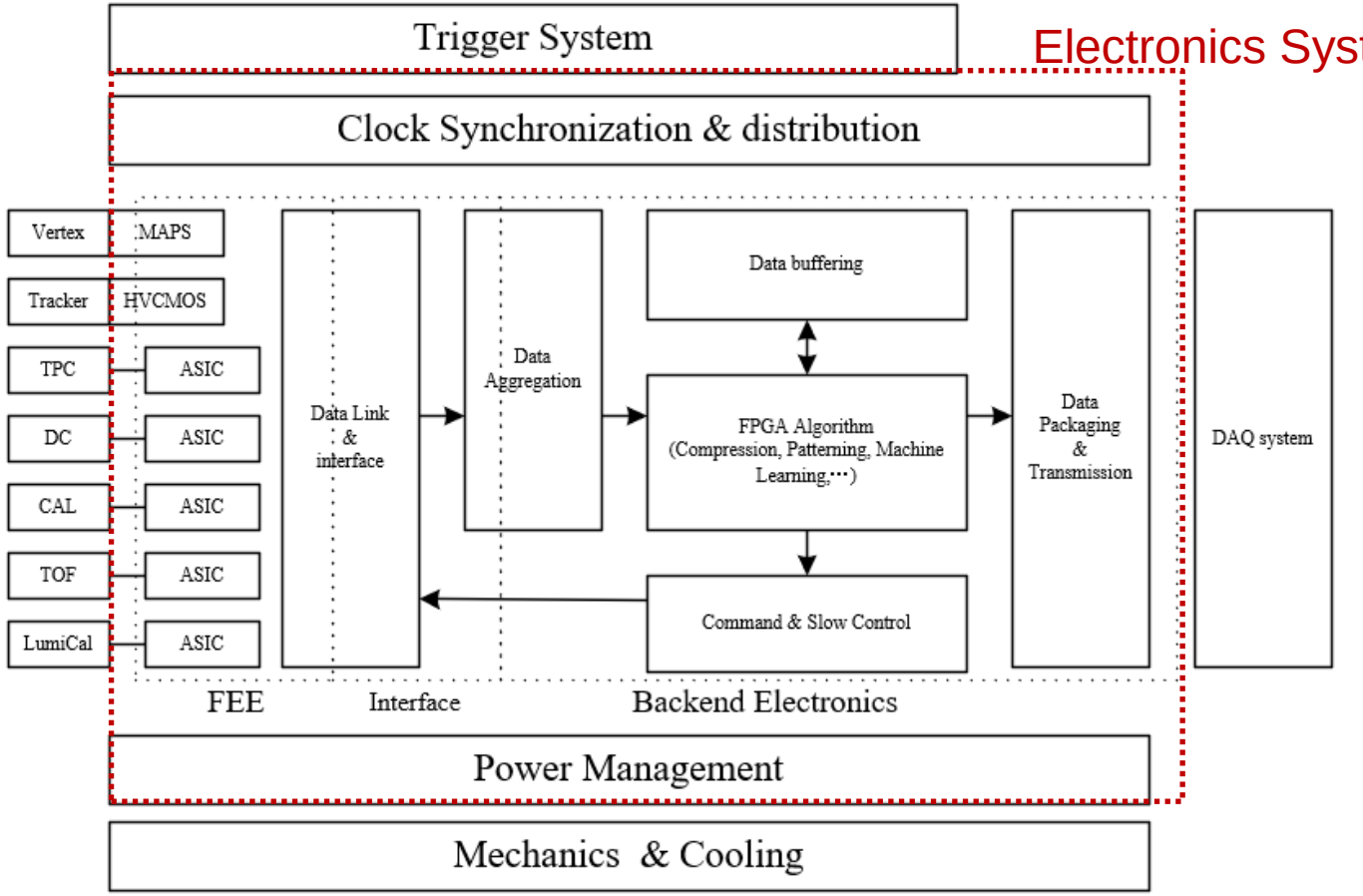
- 历史经验：
  - 一定程度的全局标准化：统一了系统接口（VME……）
  - 成熟商用器件的使用：加快了设计速度、提高了设计可靠性（FPGA、HPTDC、ADC……）
- Lessons learned：
  - 本质上各系统均为完全的定制化设计，一些通用设计重复劳动
  - 各系统独立设计，并未实现彻底的统一标准，系统联调效率不高（如DAQ接口）
  - 整体升级可能性有限（如BIIU升级）



BESIII MDC读出电子学框图

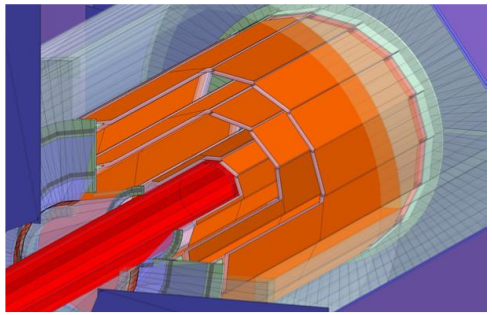
Ref. 北京正负电子对撞机重大改造工程初步设计

未来，或许我们应该...

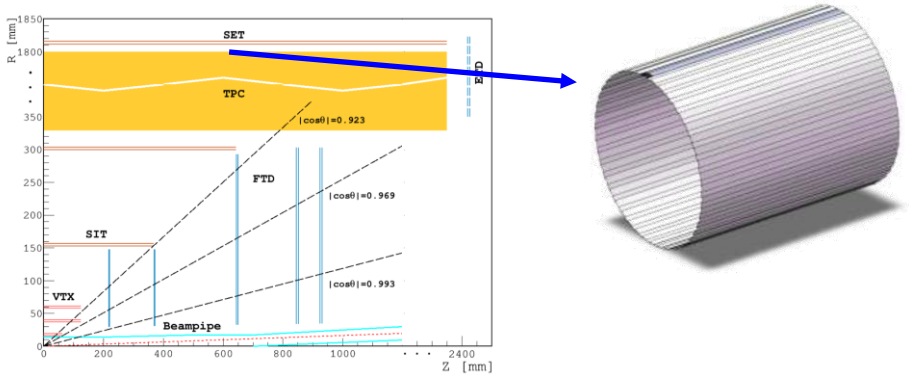


- **各系统统一的设计风格**：基于全ASIC的On-Detector抗辐照电子学
- **各系统统一的设计框架**：全FEE Triggerless / 全On-Det AI Trigger、前端数据汇总框架……
- **各系统统一的接口**：全光纤的数据传输框架、统一协议的前端控制、统一协议的时钟分配……
- **尽可能的通用设计**、最大可升级可扩展性：通用后端电子学、通用触发板、成熟商用器件COTS

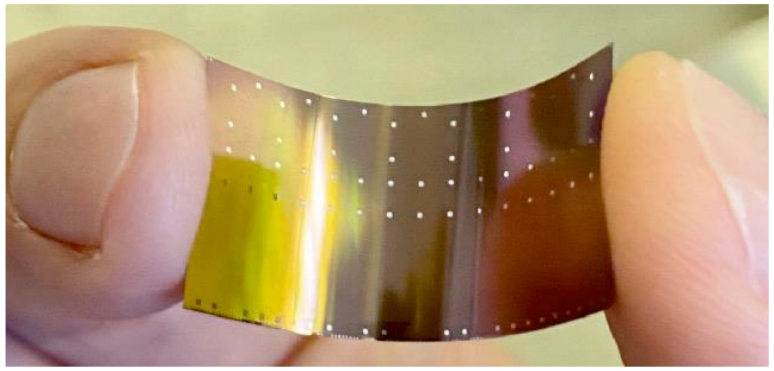
我们面临的挑战——一些例子



VTX：Hit rate 40MHz/cm^2



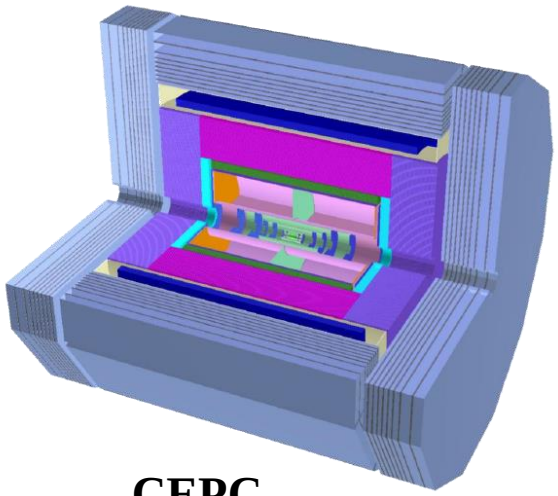
LGAD TOF：时间分辨 30ps



Stitching工艺

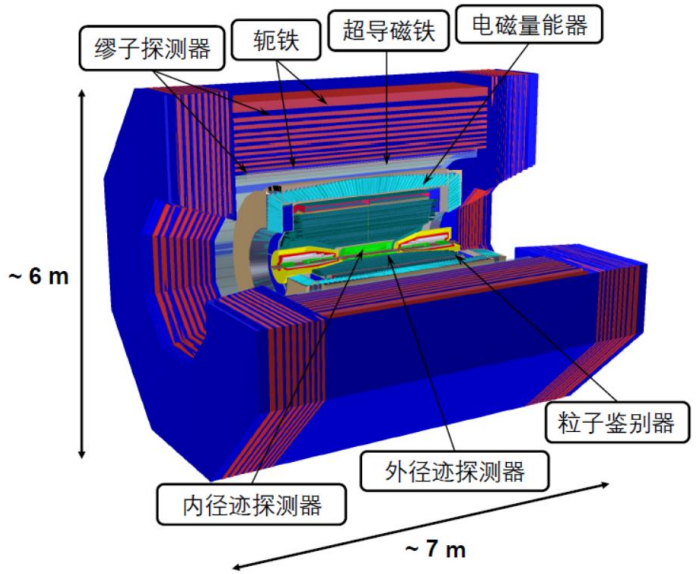
- 高计数率vs潜在新物理
  - 近束流管——VTX数据率 ~6Gbps/Chip@Z
  - On-Det AI vs 高速数据传输
- 高精度时间分辨 & 4D
  - CEPC全部探测器均有时间测量要求，4D everywhere
  - PID & TOF——时间分辨30ps
  - 高粒度量能器——动态范围~10^5 + 时间分辨 ~400ps
  - 高精度TDC
  - 高精度时钟分配
- 高亮度Higgs工厂
  - 极端环境——抗辐照5Mrad/y
  - 低物质量0.15%X_0——低功耗、先进工艺
- 与ECFA的关键词不谋而合！

共性聚焦问题和国内外现状对比——ASIC



CEPC

TaichuPix@VTX
COFFEE@ITK
TEPIX@Pixel TPC
LGAD TOF ROC
SiPM ROC@CAL &Muon
GBTx-like Series
Data Aggregation
DC-DC Controller
……



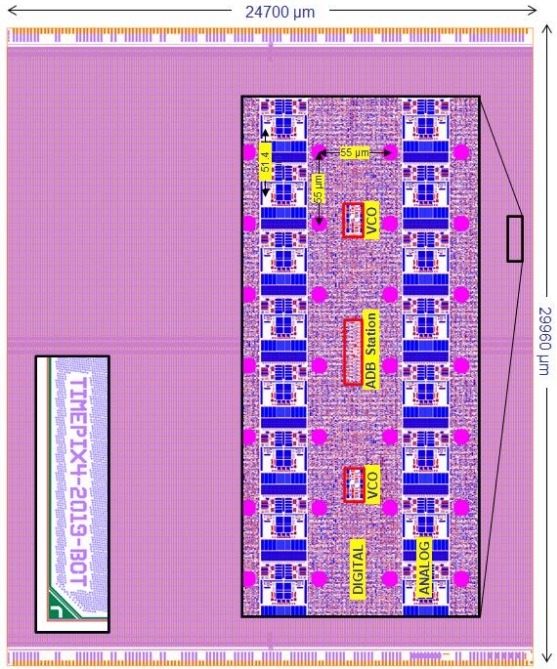
STCF

MAPS ASIC@ITK
MPGD ASIC@ITK
MDC ASIC
RICH ASIC for PID
DTOF ASIC for PID
EMC readout ASIC
Muon readout ASIC
Data Transmission
……

- 今天，ASIC的必要性已无需赘述
- 国内发展阶段
  - 前端FEE设计能力已相对成熟，可基本满足各种探测器需求
  - 一批芯片批量应用于大科学工程
    - 散裂、LHAASO、JUNO、HEPS
  - 但主要研究还仍集中在模拟前端
    - 高复杂度数字设计：无、少
    - 复杂模拟IP：有、但不标准
    - D-on-T等先进设计体系：无、少
    - 平台型芯片设计：无、少
    - 工业界合作设计：无、少
  - 主要工艺：130nm、180nm、65nm
    - 28nm等先进工艺：无、少

Ref. STCF探测谱仪研究进展，刘建北，2024

国外现状、规划——ASIC

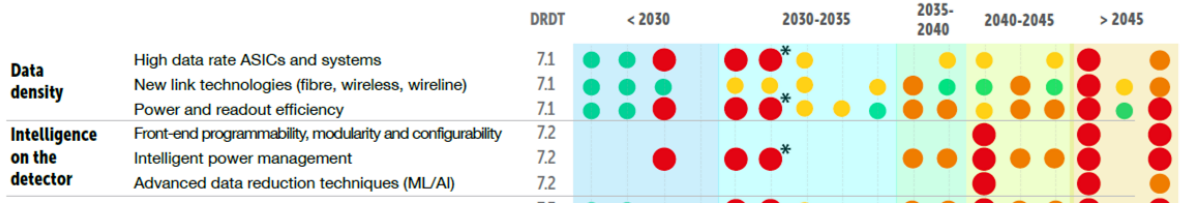


Pixel size	55 x 55 µm
Array	512 x 448
Pixels	229376
aPLL	19
aDLL	16
10.24 Gbps serializers (Nikhef)	16
On-pixel VCO (Nikhef)	28672
dDLL Columns	448
Biasing DACs	13
ADC (IFAE)	1
Transistors in pixel	~6000
Transistors in chip	~1.5 bn

Timepix4以及模块构成

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable [8.3% dead area] 256 x 256	4-side buttable [0.5% dead area] 512 x 448	3.5x
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	33%
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	8x
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	6x
TOT energy resolution			< 2KeV	**< 1Kev**	2x
Time resolution			1.56ns	**195.3125ps**	8x
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	≤163.84 Gbps (16x @10.24 Gbps)	32x
Target global minimum threshold			<500 e^-	<500 e^-	

- 关键定语：High Data rate ASIC
  - 数据暴涨将导致体系、框架、方法的革新
- 以Timepix4芯片为例
- 设计体系
  - Digital-on-Top Flow广泛采用
  - 海量数字逻辑
  - PLL、DLL等复杂模拟IP大量采用，数量>>1
  - 海量数据产生 160Gbps/Chip
  - 真实需求驱动：更高计数率 & 时间分辨
- 主要工艺：65nm、130nm
  - 28nm已有大量R&D开展，成为下一个节点共识

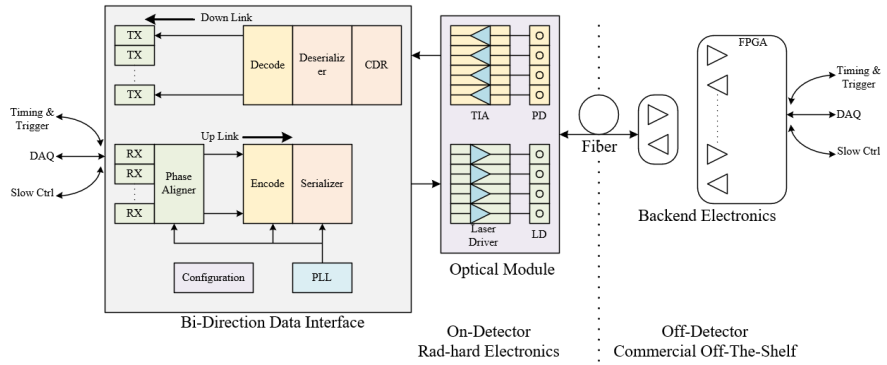


规划和思考——ASIC

from Cadence.com

	A	A/d	A/D	D/A	D/a	D
Methodology	Analog on Top (AoT)		Mixed-Signal on Top (MSoT)		Digital on Top (DoT)	
Design Flow	Schematic-Driven		Netlist-Driven			
Top level Connectivity	Schematic		Verilog		Verilog	
Design Characteristics	• Top level is analog • Standard cell digital designed in a digital flow		Analog blocks and standard cell digital mixed at the top level		• Top level is digital • Analog designed in an analog flow	
Floorplanning	Virtuoso floorplanner and Virtuoso Digital Implementation		Virtuoso floorplanner and Innovus		Innovus	
Analog Content	Main and Top Level		Co-Designed		Separate Hierarchy	
Digital Content	Separate Hierarchy		Co-Designed		Main and Top Level	
Routing	• VSR for top level and analog • NR for routing within the digital blocks		• VSR for analog blocks and NR for digital blocks • Top level uses VSR for analog and NR for digital		• Top level is digital • Analog designed in an analog flow	
Chip Integration	Virtuoso		Innovus		Innovus	
Signoff	MSPS		Tempus		Tempus	
Chip Finishing	Virtuoso		Virtuoso		Virtuoso/Innovus	

Analog-on-Top vs Digital-on-Top Design Flow

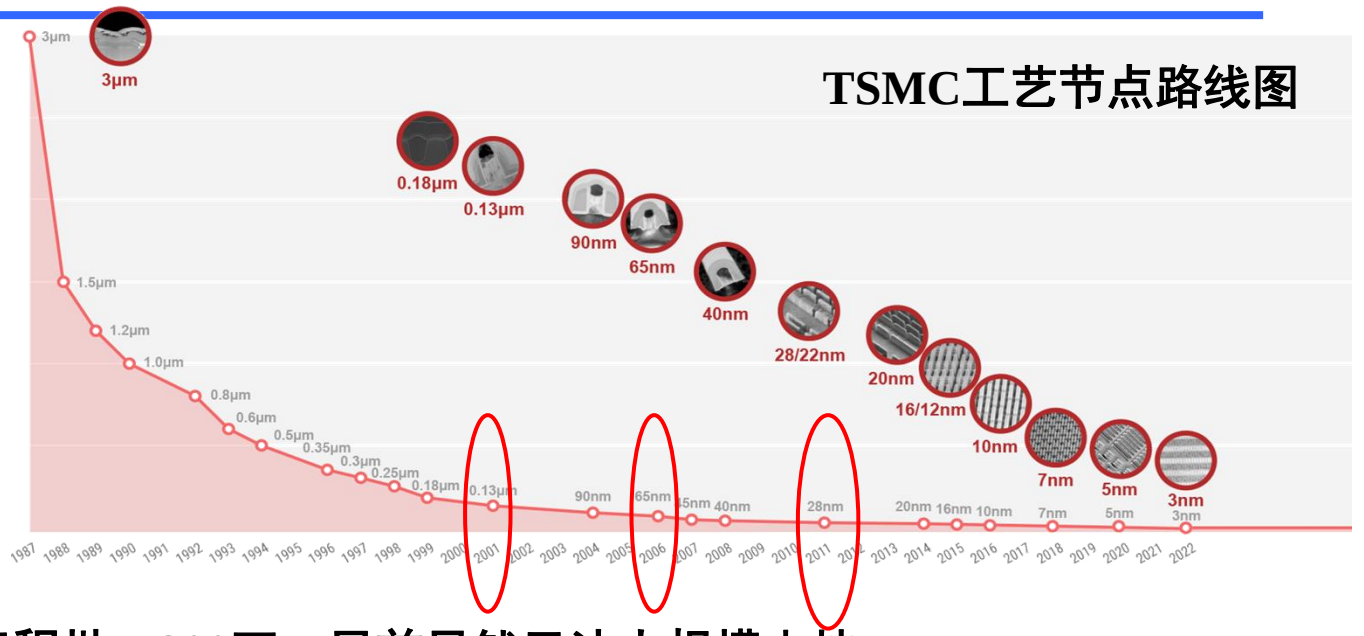


GBTx-like芯片组

- ASIC当前能力判断
  - 满足大型实验探测器需求：可
  - 实现先进电子学体系：难
  - 主要发展目标：提升整体设计体系
- 对等发展目标
  - D-on-T设计Flow：必要且紧迫
    - ➢添加全局数字功能的必需，大型芯片全局设计优化（时序、电源）的必需
  - 复杂模拟IP（PLL、SER）：已有核心设计，提高标准性，实现平台化设计
    - ➢业界标准协议、标准接口
  - 海量数字逻辑：仍由需求驱动
    - ➢优点：芯片功能、性能的提升
    - ➢问题：设计复杂度提高、迭代周期增加

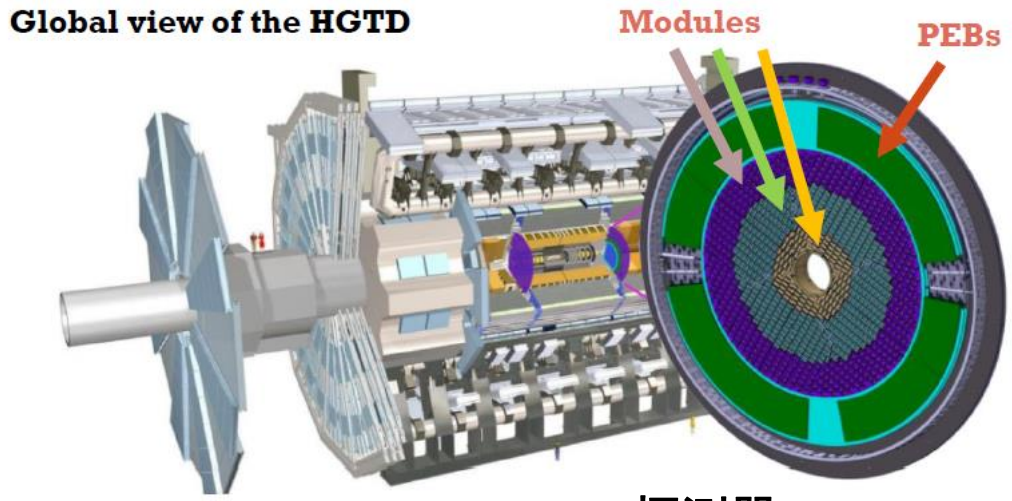
我们是否需要28nm？

- 粒子物理ASIC是远离摩尔定律的领域，特点源自需求
  - 应按自身特点发展，避免盲目追赶
- 采用28nm的好处
  - 速度：Timing、Data Link、数据汇总，其他领域暂未看到
  - 集成度：除非VTX@28nm CIS，有限时间尺度内可能性低，可暂不考虑

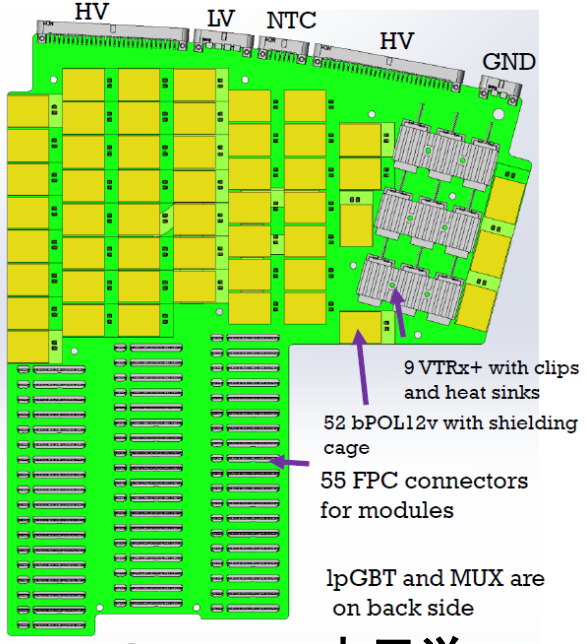


- 采用28nm的代价
  - 成本显著增加：（经询价）MPW~100万，工程批~1200万，目前显然无法大规模支持
    - CERN形成了大客户效应，多有免费流片机会（与国内的显著区别）
  - 系统集成困难：SOC前端设计也需绑定28nm同种工艺，设计难度显著增加
  - 功耗？：电源电压0.9V☺，但漏电流增加☹
- 国外的实际考虑 Ref. ASICs and front-end electronics, CdlT, 2021
  - 建议保留28nm和65nm两个节点，并非全面过渡：高端高成本 & 普通低成本
- 个人观点
  - 在特定领域保持R&D追踪，但大规模推进不符合国情（可组团MPW流片）
  - 首要任务：以65nm为下个立足点，对标ASIC整体设计体系和理念

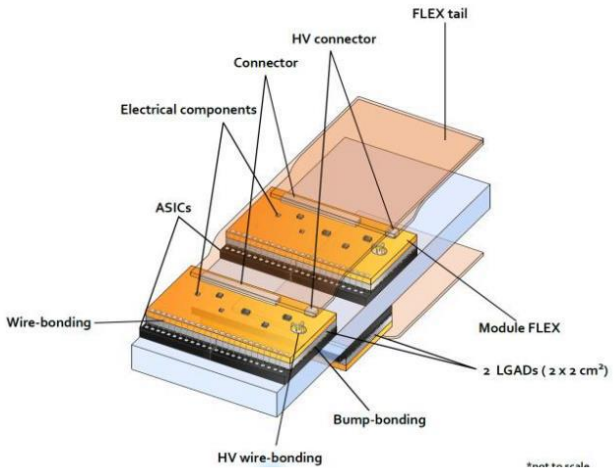
共性聚焦问题和国内外现状对比——Timing



ATLAS HGTD探测器



HGTD PEB电子学

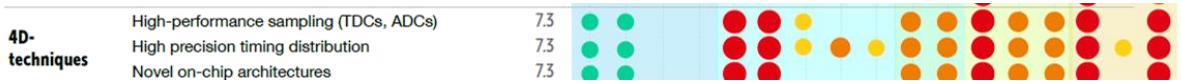


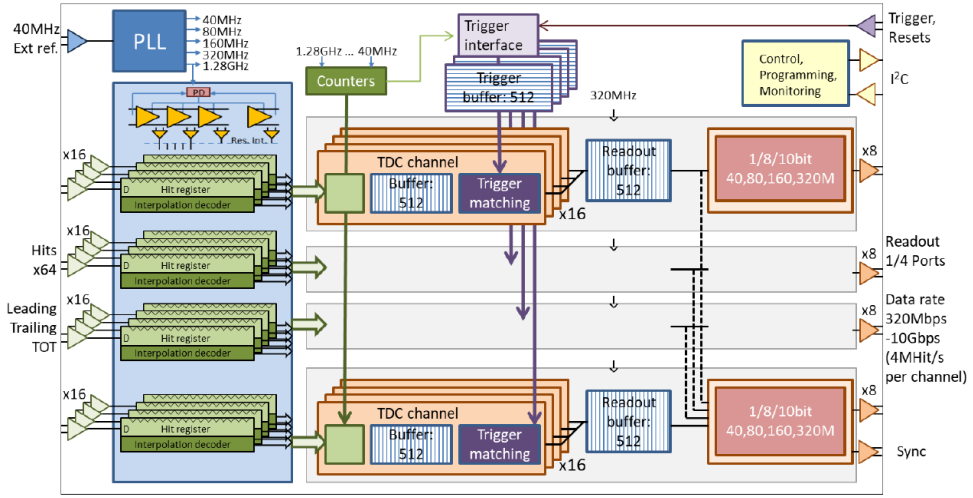
HGTD 探测器模块

- ATLAS HGTD vs. CEPC OTK ~30ps
- 4D = 3D+T / 2D+A+T
- 从物理需求上，国内外已达相同目标
  - 原始驱动已具备，必要性毋庸置疑
- 国内现状
  - 工程级别-HGTD
    - 全面参加Sensor、电子学、测试刻度等工作
    - 端盖外围读出板PEB的主要设计单位
    - 不足：ALTIROC芯片仅有限参与设计
  - 高精度时间分辨电子学
    - On-FPGA：已有多年研究历史，技术成熟
    - On-ASIC：
      - 以高精度TDC、波形采样SCA研究居多
      - 高速前端+TDC研究较少
      - 期待工程应用

Ref. ATLAS HGTD电子学进展，张杰，2024

国外现状、规划——Timing





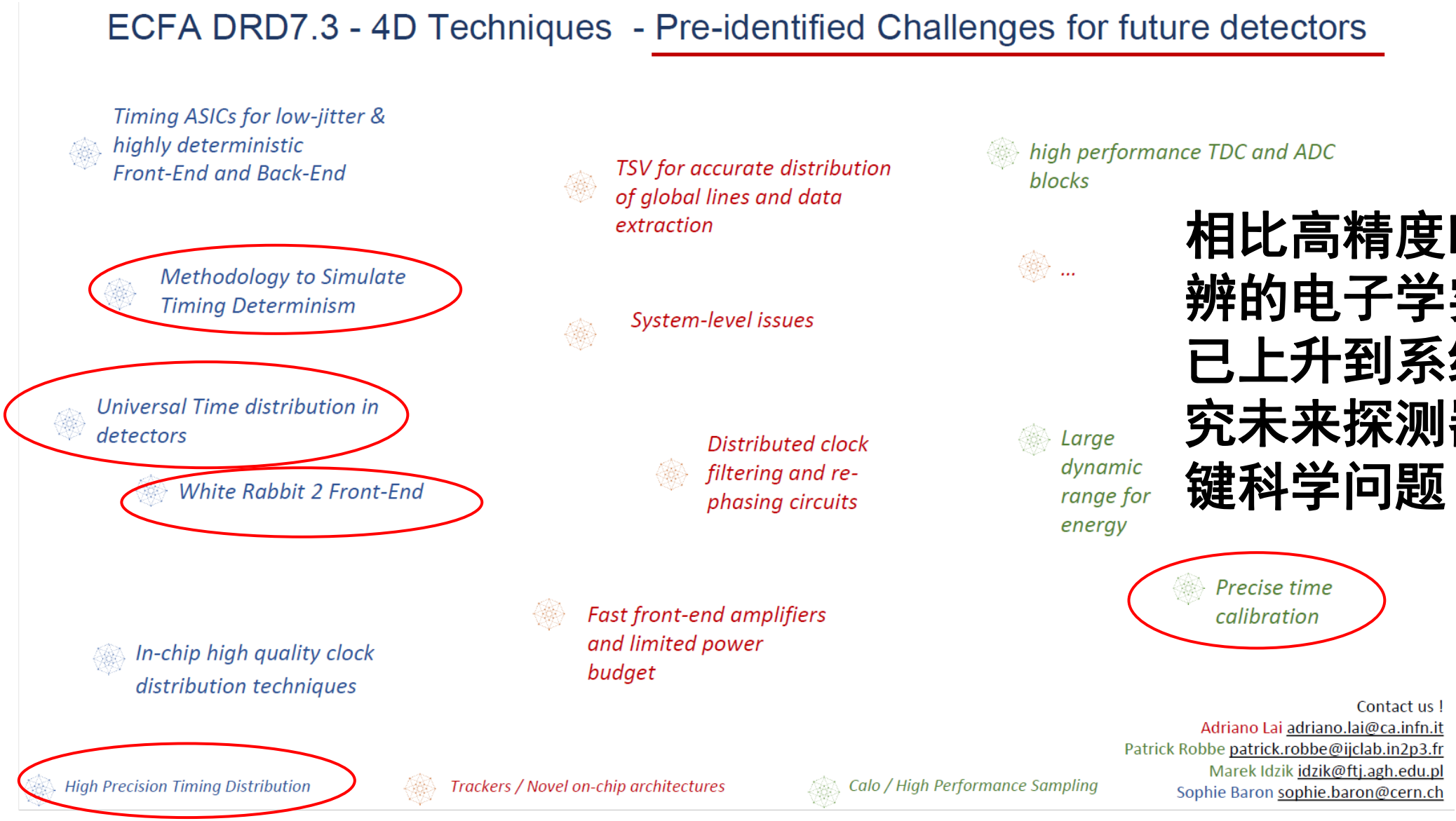
picoTDC：https://picotdc.web.cern.ch/

Going 4D: Timing Requirements Challenges	*Sophie Baron*	
222/R-001, CERN	15:30 - 15:40	
Going 4D: High Precision Timing: Detector Simulation Challenges - an ATLAS HGTD perspective	*Louis D'Eramo*	
222/R-001, CERN	15:40 - 15:50	
4D for Trackers Challenges: an overview	*Adriano Lai*	
222/R-001, CERN	15:50 - 16:00	
4D for Trackers Challenges: focus on the LHCb Velo Upgrade	*Martin Van Beuzekom*	
222/R-001, CERN	16:00 - 16:15	
4D for Calo Challenges: an overview	*Marek Idzik*	
222/R-001, CERN	16:15 - 16:25	
4D for Calo Challenges: focus on LHCb ECAL Upgrade	*Dominique Robert Breton*	
222/R-001, CERN	16:25 - 16:40	
Discussion		
222/R-001, CERN	16:40 - 17:00	

Implementing DRD7: an R&D Collaboration on Electronics and On-detector Processing. 1st workshop：4D Session

- 在ECFA中归在4D发展目标中
  - 主要解决未来的4D Tracker、4D Calo问题
- 当前设计水平
  - Ultra-fast 前端ASIC已有大量设计及工程应用
    - ➢NINO →Timepix4、Timespot @100ps/pixel
  - 高精度TDC
    - ➢HPTDC → picoTDC ~3ps rms 64Chn
- 公认的28nm最合适应用领域之一
- 高精度时钟分配问题被专门提出

4D & Timing的关键问题@ECFA Workshop

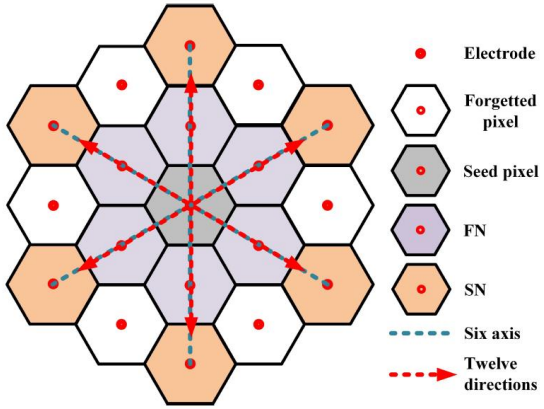


相比高精度时间分辨的电子学实现，已上升到系统性研究未来探测器的关键科学问题

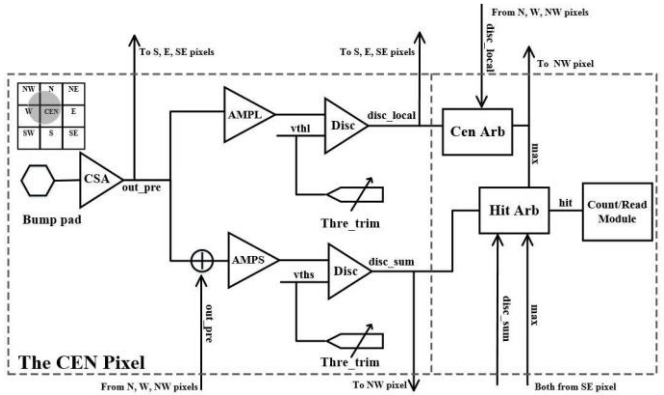
我们应该如何发展Timing技术？

- 当前能力判断
  - ASIC：
    - 一些关键技术普遍研发中，接近整体突破
    - 主要均为TDC等模块级研发，芯片整体框架性考虑不足
  - 系统电子学：
    - 依赖lpGBT等LHC信号链芯片技术，已有工程经验，但核心芯片应用受限
    - 不依赖上述芯片，仅有BESIII TOF-U时期的设计体系
      - 无法满足CEPC高辐照环境下的应用（FPGA无法前端使用）
- 个人观点：明确自身步调，首先满足自身物理需求，伺机赶超
  - ASIC：尽快完善高精度时间分辨ASIC设计体系
    - Ultra Fast 前端：依据物理目标开展R&D，完成工程检验
    - High Precision TDC：首先完成成熟化和IP化，进一步优化，实现多通道和可扩展性
      - 可暂定~128Chn 条形电极 & 256*256像素阵列两个典型应用目标
  - 系统级：
    - 配合GBTx平台性芯片研发，实现基于国内芯片环境的高精度时钟分配系统
    - 探索高精度时间刻度方案，可有重要国际贡献

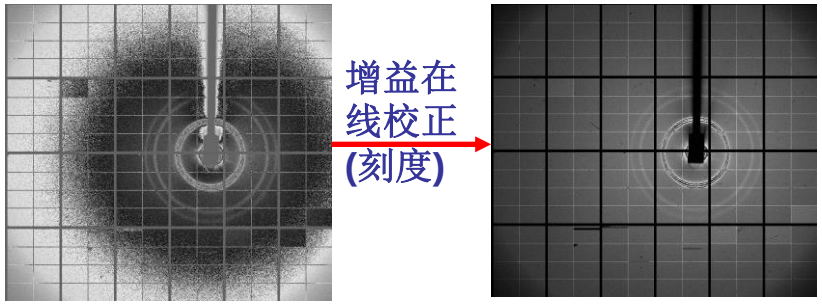
共性聚焦问题和国内外现状对比——AI

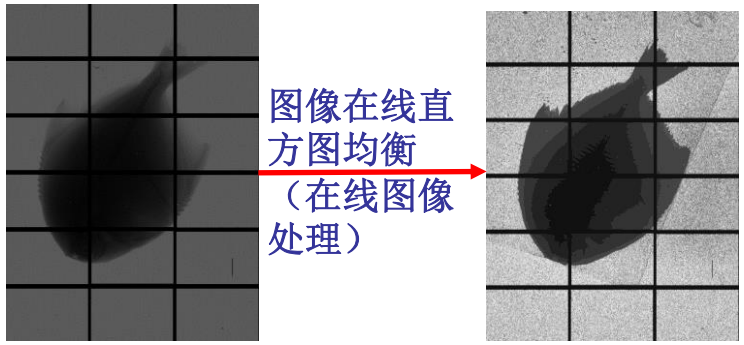


Ref. 面向背景粒子筛除的智能化CMOS像素探测器研发，赵瑞光，2023



Ref.一种小尺寸像素探测器读出芯片的设计与改进，崔珊珊，2022

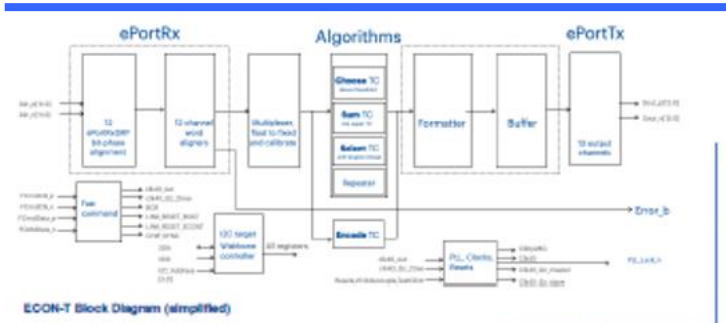




基于FPGA加速卡的在线计算平台建设，张杰、江晓山等

- 来自探测器的数据暴涨是真实的
  - 智能数据压缩是必要的，有原始驱动的
  - 无论此轮AI浪潮是否持久
- 国内发展现状
  - On ASIC
    - 有少量研究开展，均待成熟
  - On FPGA
    - 有大量算法研究开展，已有一些束流实验级检验
    - 实现技术已非常成熟
    - 在线计算平台的建设核心仍在算力
      - 电子学：高性能FPGA加速卡
      - TDAQ及其他：GPU/CPU等
  - 但工程量级的电子学系统应用暂无
    - 定义为大型神经网络级
    - 主要因需求因素导致

国外现状、规划——AI



- 4 selectable trigger data compression algorithms: variable and fixed-latency options.
- Includes formatter and smart buffer.
- PLL and 1.28GHz phase-aligners from lpGBT.


ECON-T Layout

128 pin packaged ECON-T.


HGCAL Readout Architecture

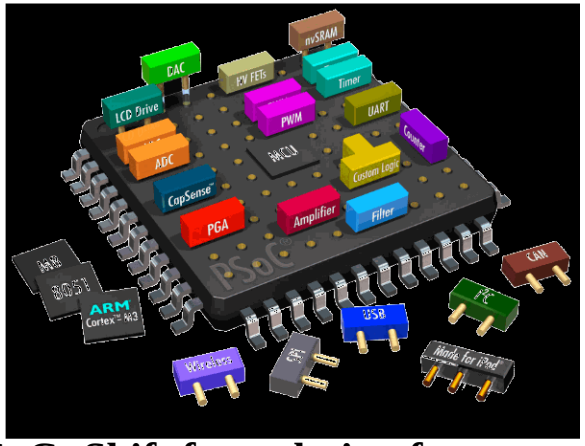
AI on Chip: **Reconfigurable Encoder**

- Quantization Aware Training of Encoder algorithm based on LHC simulation.
- Optimization of CNN architecture for physics performance and area and power requirements.
- Reconfigurable weights and biases via I²C.
- Full triplication of clocks, logic, and resets for I²C configuration.

FERMILAB-POSTER-22-214-PPD

Design and first test results of the CMS HGCAL on-detector ECON-T ASIC with a reconfigurable encoder algorithm for data compression

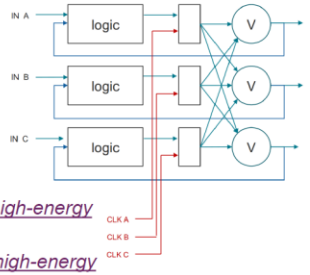
- **先进数据压缩（ML/AI）**
  - 国外领域也几乎无成熟的AI ASIC应用
  - 在系统级，主要关注算法研究，与之在设计技术及体系上并无太大差距
- **前端可编程、模块化**
  - 相关讨论均基于RISC-V架构，本质上属软件设计，**并非前端ASIC的可编程化**
  - **最大挑战：可编程器件的辐照环境应用**
    - ➢ 类比FPGA在前端辐照环境应用的困境
    - ➢ 三模冗余 vs 资源巨大开销



SoC: Shift from design for an application to design for resources

The most robust approach to harden a processor is **Triple Modular Redundancy (TMR)**: combinational logic, registers and clocks are triplicated and majority voted at the output.

- Simple to understand
- Maximum SEU protection
- Can be automatized
- Very large area and power overhead (> 3x)
- Can be difficult to implement correctly (depending on RTL and physical constraints)

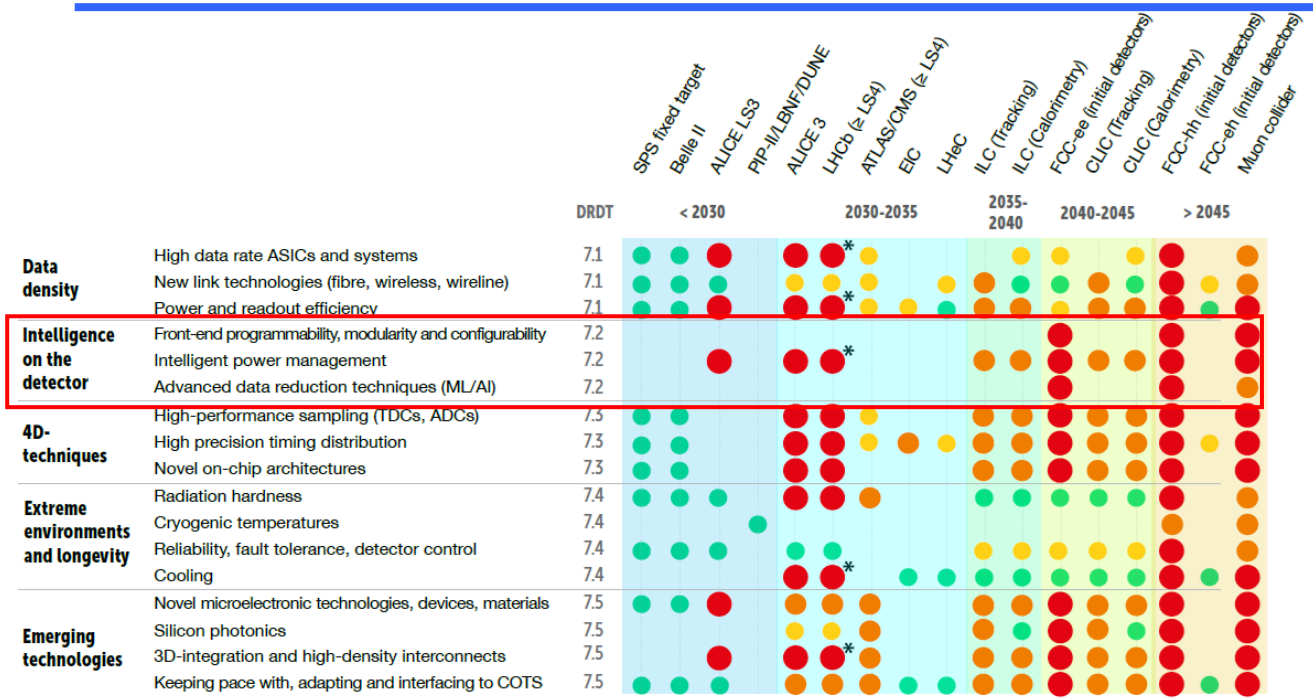


Examples of works using TMR:

- A. Walsemann et al., *STRV — a radiation hard RISC-V microprocessor for high-energy physics applications*, 2023, JINST 18
- M. Andorno et al., *Rad-hard RISC-V SoC and ASIP ecosystems studies for high-energy physics applications*, 2023, JINST 18
- A. E. Wilson and M. Wirthlin, *Neutron Radiation Testing of Fault Tolerant RISC-V Soft Processor on Xilinx SRAM-based FPGAs*, 2019, IEEE SCC

Ref. DRDT 7.2: Front-end programmability, M. Andorno, 2023

国外规划与“谜雾”



More intelligence can be included in the front end ASICs to allow for data reduction and possibly an overall system power reduction, though there is a trade-off with the needs of software event reconstruction. As with today's trigger systems, complex processing having an irrevocable effect on the recorded data must be adaptable to changing experimental conditions. Ideally the ASICs would be programmable, and either "FPGA-like" or "CPU-like". Such programmability and configurability will ultimately enable the community to develop fewer ASICs of higher complexity and flexibility.

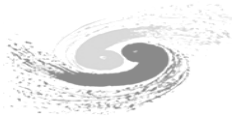
Development of specialised AI and ML hardware in academia and industry is extremely rapid, and it is not clear how this can be reconciled with the extended development cycles for large detector systems. Standardisation and modularisation of front-end electronics and interfaces may offer a solution. It is unlikely that COTS components will be suitable for use in the detector without adaptation, due to power, robustness and radiation hardness constraints. The long-term radiation tolerance of any candidate novel processing technologies must be established.

- **ECFA规划显示出该方向近期并无确定性计划?**
- **思考：高能物理vs硬件AI的矛盾点**
  - **高能物理环境是变化的（老化、辐照）**

    基于硬件加速要求对象是不变的
  - **探测器系统需多轮迭代周期**

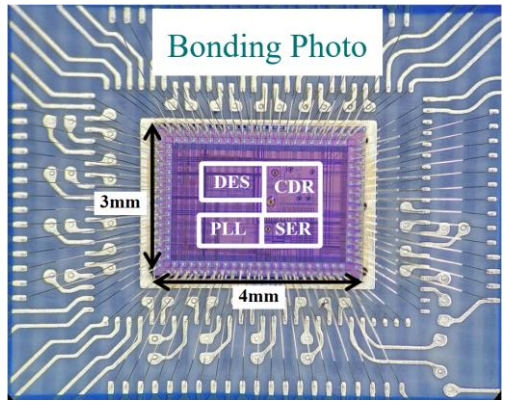
    算法训练需真实物理数据，仅能等待探测器运行后再行部署
    - **或为表中跳过前置R&D直接对应2040 FCC-ee初始探测器节点的由来**

我们应该如何发展硬件AI技术？

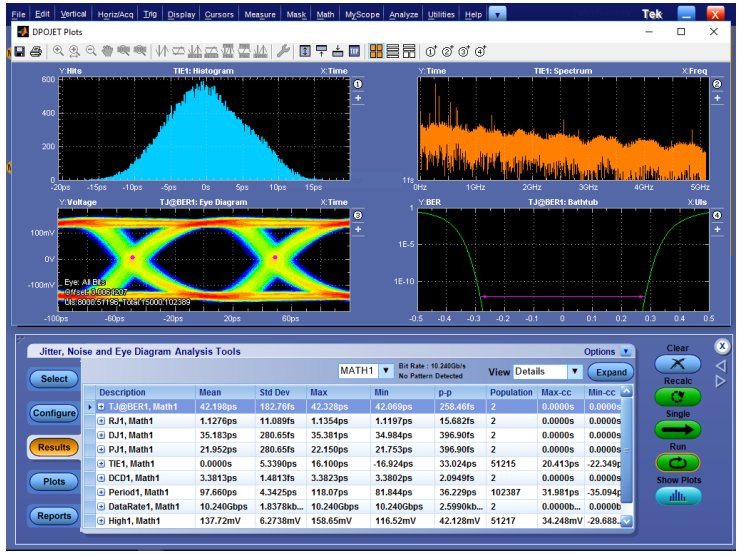


- 不应讨论是否发展ML/AI（大势所趋），而应讨论AI on Where
- 发展ML/AI，国内环境与国外环境的本质区别
  - 我们没有真正ASIC时代的对撞机，即没有真实物理数据，所有数据均为仿真假设
  - 但ML/AI的原理在于数据训练
- 当前能力判断
  - 虽然设计技术、原理、体系均无障碍，但真实应用对象不存在
- 个人观点
  - ASIC迭代周期长，成本高，只适合算法固化，不适合算法验证
  - FPGA算法可在线更新，迭代快，适合方法研究
  - 初步判断：
    - ML/AI算法均需等待真实探测器建成后再部署验证，因此仅存AI-on-FPGA一种可能性
    - 且新物理的本质驱动，决定了AI算法或需不断更新，AI-on-ASIC亦不可能
      - AI-on-ASIC并非不重要，建议可考虑场景更为固定应用的硬件加速
  - 引申讨论：(Smart) Trigger-on-FEE vs Trigger-on-BEE (=FEE Triggerless)
    - 在FEE ASIC上部署AI，均面临相同困境
    - FEE-Triggerless看起来是更具性价比的选择——ASIC不涉及算法，亦可迅速定型

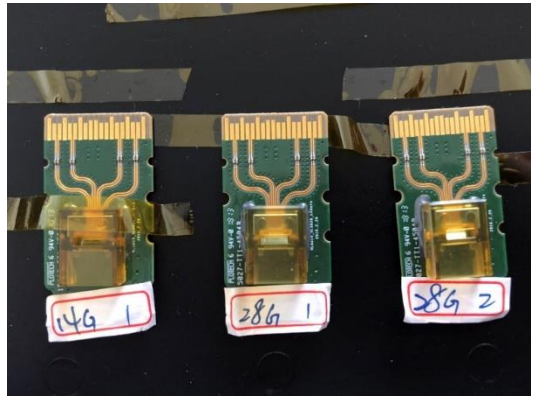
共性聚焦问题和国内外现状对比——Link



双向数据接口芯片
输出的10.24 Gbps眼图
Total Jitter = 42.19 ps
RMS Jitter = 1.13 ps

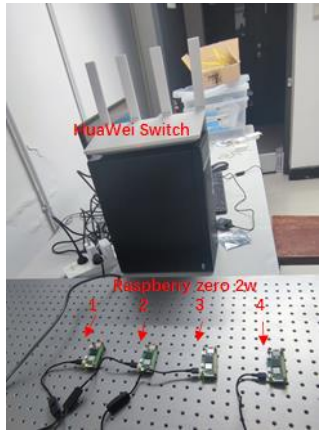


- **High Data rate下必要性毋庸置疑**
- **国内发展现状**
  - **高速串行链路**
    - **各单位均普遍开展研究**
    - **主要核心模块均已有相当基础**
  - **Optical Link**
    - **华师 & SMU**
    - **已有模组化设计，尺寸满足应用需求**
  - **Wireless Communication**
    - **已对几种主要技术开展R&D**

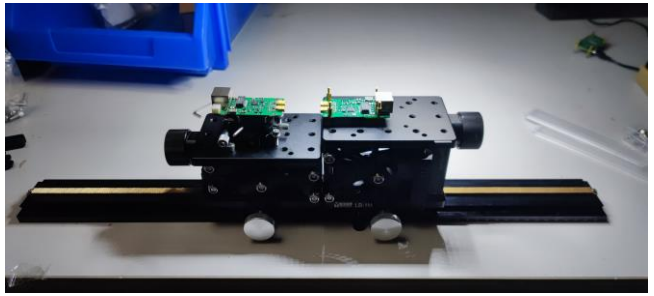


四通道阵列式光发送模块

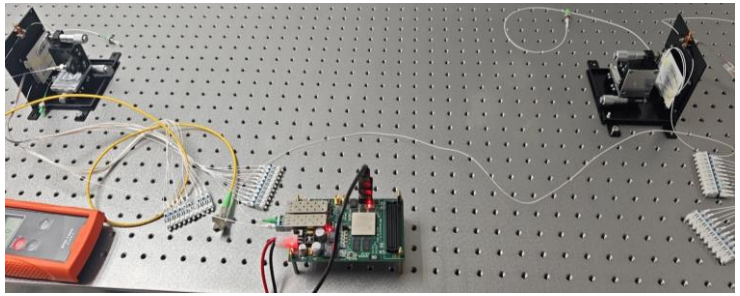
By 郭迪@CCNU



On Wifi



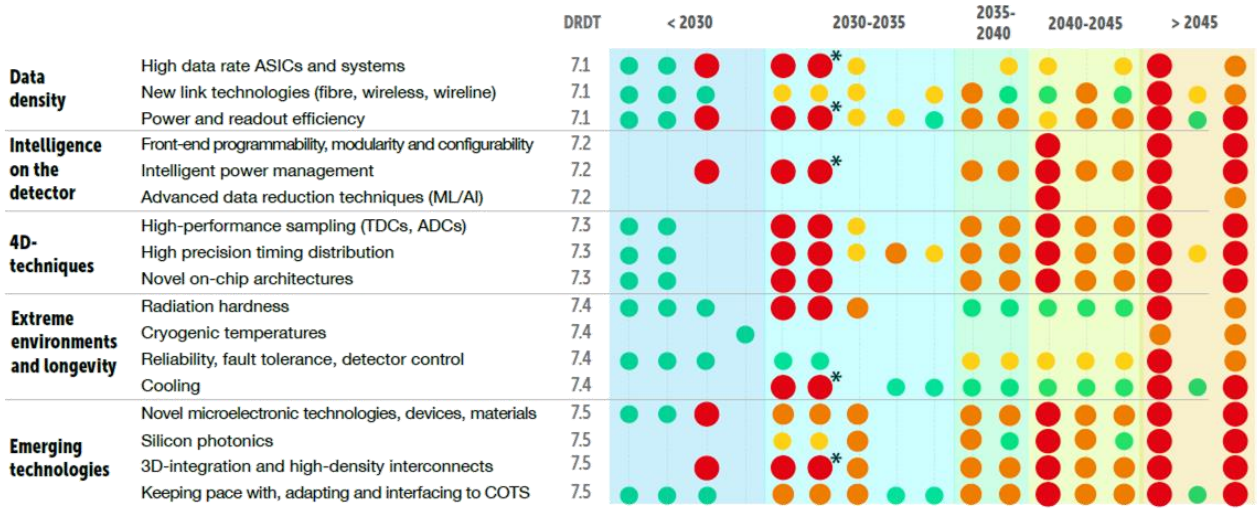
On mm-Wave

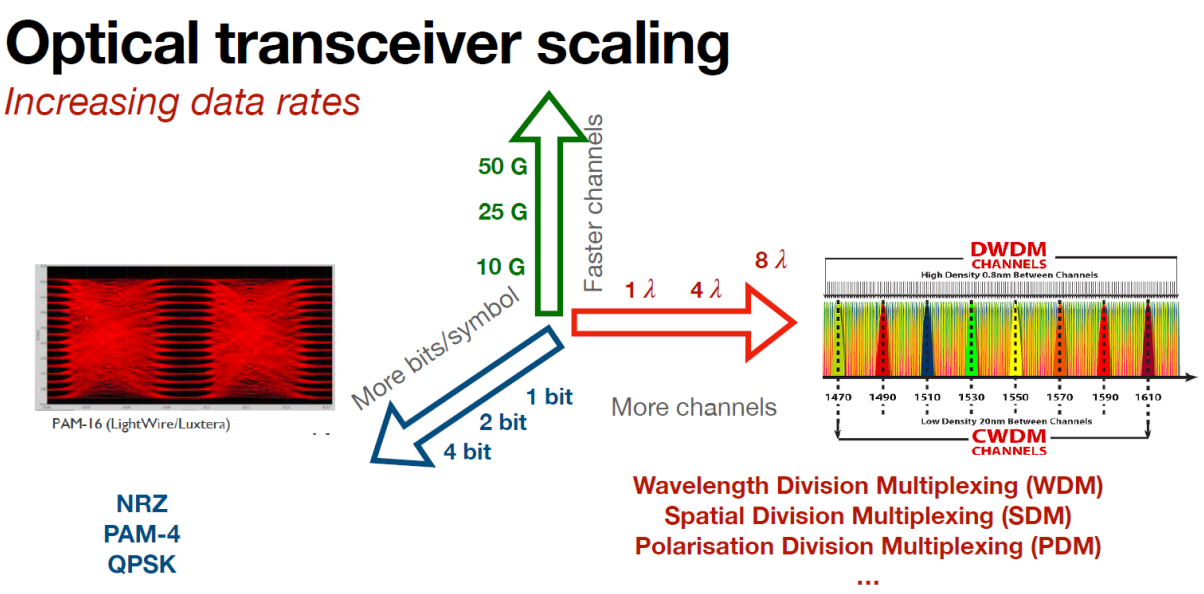


On Free-Space Optical

By 胡俊@IHEP

国外现状、规划——Link



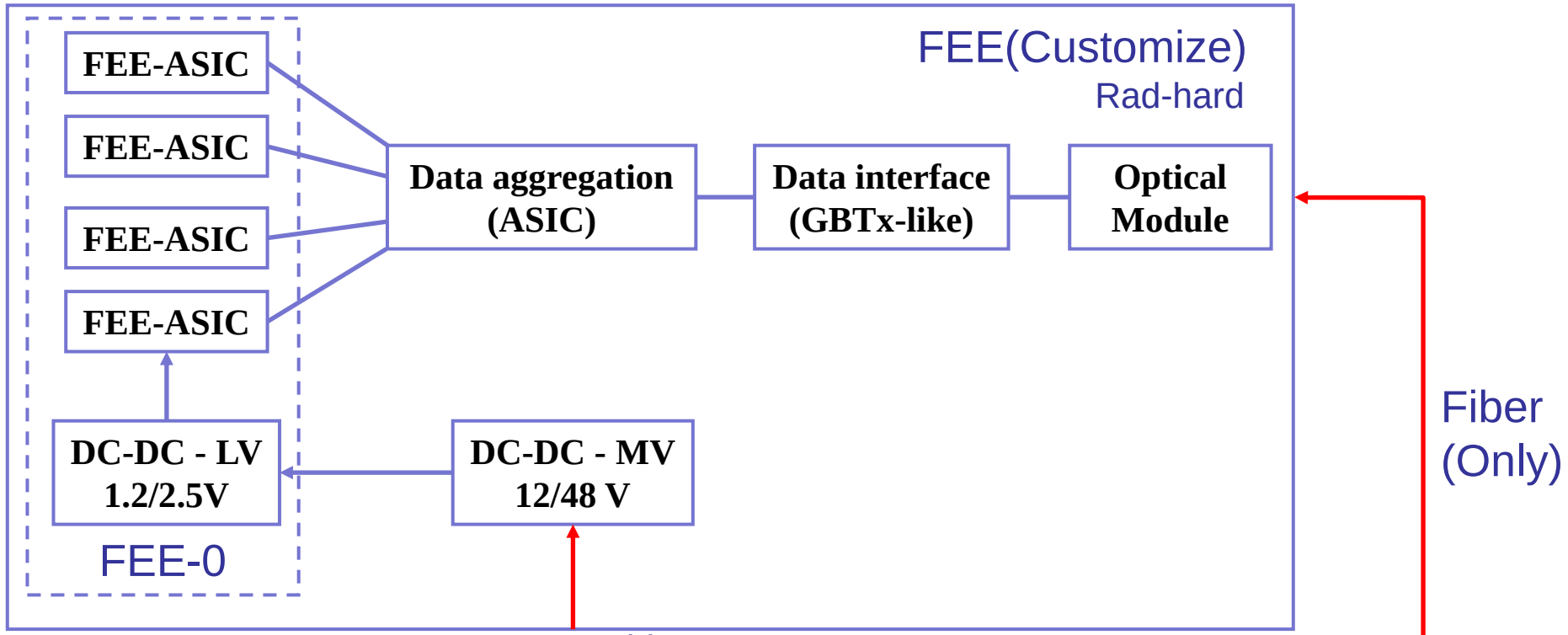


- lpGBT经过几代发展，已成为LHC实验的平台型芯片
  - 但我们无法大规模使用
- 两种主要链接方式
  - 电连接（up to 1.28Gbps）
  - 光连接– VCSEL/PD-based （ 2.56 – 10.24 Gbps）
- 28nm毫无争议的主攻方向
- 规划突出了New Link Tech
  - 除Wireless着眼物质量外，主要目标仍是提升传输速度
  - Silicon Photonics为主要R&D方向

我们应该如何发展Link技术？

- 当前能力判断
  - 实现lpGBT的核心模块设计不存在显著障碍
- 个人观点
  - 由于lpGBT的应用限制，实现国内自主的平台性传输芯片设计成为未来实验的关键点
  - 应结合物理实验驱动，尽快完成GBTx芯片（组）的成熟化和通用化，满足实验需求
    - 类lpGBT的通用协议及芯片架构是下一步的关键点
  - 未来技术发展
    - 与国外目标是一致的
    - 应开展相应R&D（如PAM4等），跟踪国外研究进展
    - Si Photonics为工业界标准，或可寻求工业界帮助
  - 无线传输技术
    - 我们在认真推动
    - 期望形成自身特色方案

以CEPC为例-电子学触发系统架构-A Proposal



- 前端Triggerless方案 = 后端/软件触发
- 定制前端ASIC+通用平台电子学系统
  - 统一风格的前端-汇总-光电-后端系统
- 全光纤数据链路&模块化设计，提高系统可靠性和可升级性
- 最大化通用设计，子系统可以Scaling方式设计
- On-Det全ASIC架构，最大化抗辐照性能

不一而足，未深入讨论的关键点……

- 高亮度、高数据率 vs 先进On-Det电源及分配系统
  - 相比(BESIII)传统方案，抗辐照、提升效率成为必要
  - 基于GaN的高效率DC-DC电源方案
  - 国内研究完全欠缺，我们需要补课——另一重要的平台性芯片/系统
- 极端环境
  - Cryo在目前的谱仪设计中目前或不关键，应首先解决高辐照本底问题
  - 当前国内研究不成体系，缺少相应设计工具（SEU），我们需要补课
- 先进工艺（Integration on DRDT8）
  - TSV（3D）、微流道冷却、Stitching……
  - 非电子学但关系紧密，必须协同设计
  - 已同国内工业界建立良好合作关系，或是赶超的好时机
- 商用器件COTS & IP
  - 不要忘记寻求工业界的合作
  - JUNO的良好例子

合作倡议

- 实验规模越来越大，所需资源越来越多
  - 研发经费、设计人力、测试、验证……
- 没有任何人能独立完成任务
- 共性问题越来越凸显，难度越来越大
- 个人倡议
  - 从分别解决相似问题、设计相同模块→分工合作，实现整个电子学设计体系、理念提升
  - 避免重复造车轮，提炼领域内共性问题（Link、Power等）
  - 尽快实现平台性芯片设计，推动设计体系、新框架提升
  - 广泛寻求工业界合作，优势互补
    - HEPer，解决领域内特色问题
    - EE/CSer，提供工业标准设计、通用设计（ADC、Si Photonics、Wireless Module等）
    - 双方均不可能替代对方角色

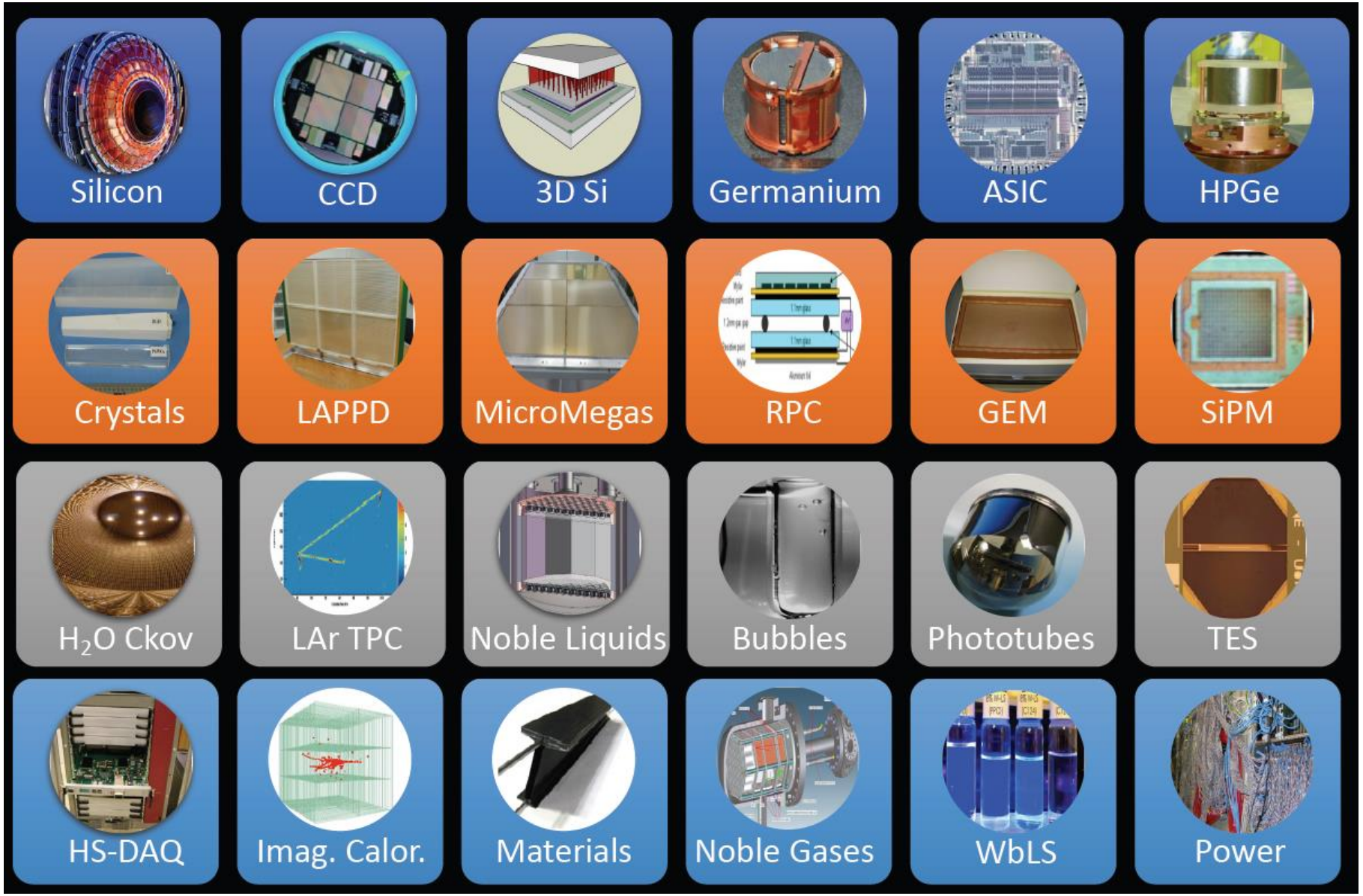
谢谢大家！

观点非常主观，抛砖引玉

欢迎批评、指正、争吵

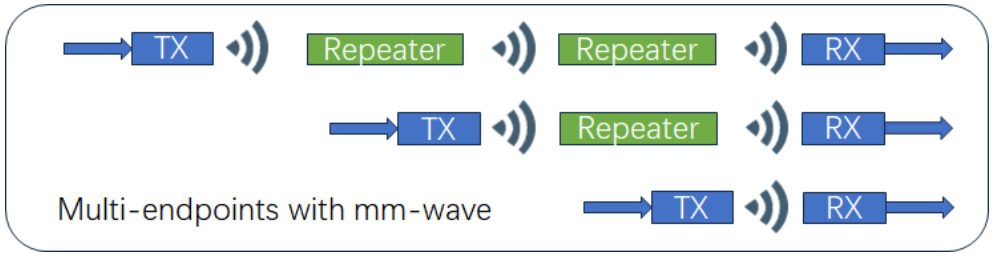
Backup

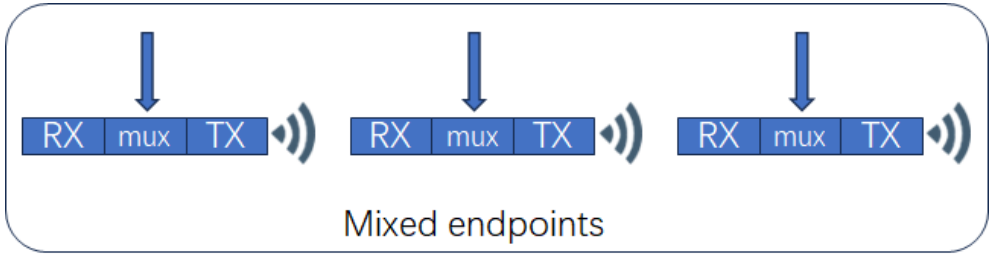
粒子物理领域相关探测器技术



from ECFA Roadmap Snowmass 21 -- I. Shipsey

Wireless Comm. backup scheme for CEPC Ref-TDR





- **Proposed several schemes for different readout architecture:**
  - **Radial direction for multi-layer detector (Inner Trk)**
    - **Via repeaters**
  - **Axial direction for long stave (OTK, CAL)**
    - **Via cascaded endpoints**
  - **Radial direction for endcaps**
    - **Via cascaded endpoints**
- **Fiber links & cost can be greatly reduced, but major challenges have to be solved**
  - **Detector interference, alignment, mechanical…**
- **Suggested to make clear the application target:**
  - **On detector readout: mm-Wave based**
  - **On accelerator timing: Free Space Optical based**

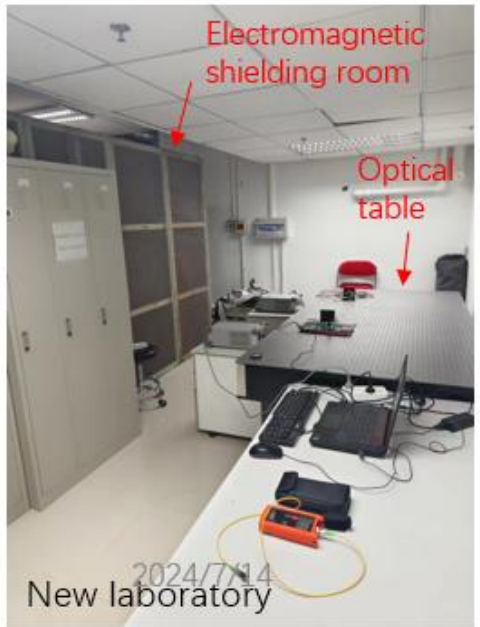
Plan

- 2023.1.1 - 2023.4.30
- 2024.1.1-2024.8.31
- 2025.9.1-2025.12.31

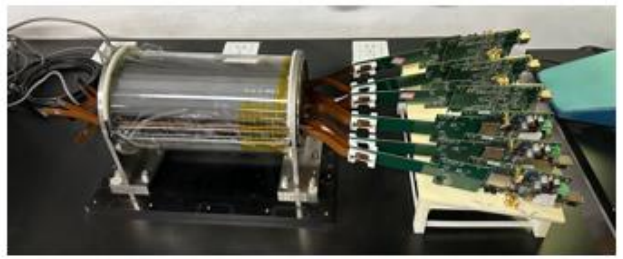
Now

Technique investigate	Built the Test setup with commerical components for different scheme	Intergration test with dectetors and determine the scheme	Built the prototype toward to the realuse	Final test

- 2023.5.1 - 2023.12.31
- 2024.9.1-2025.8.31

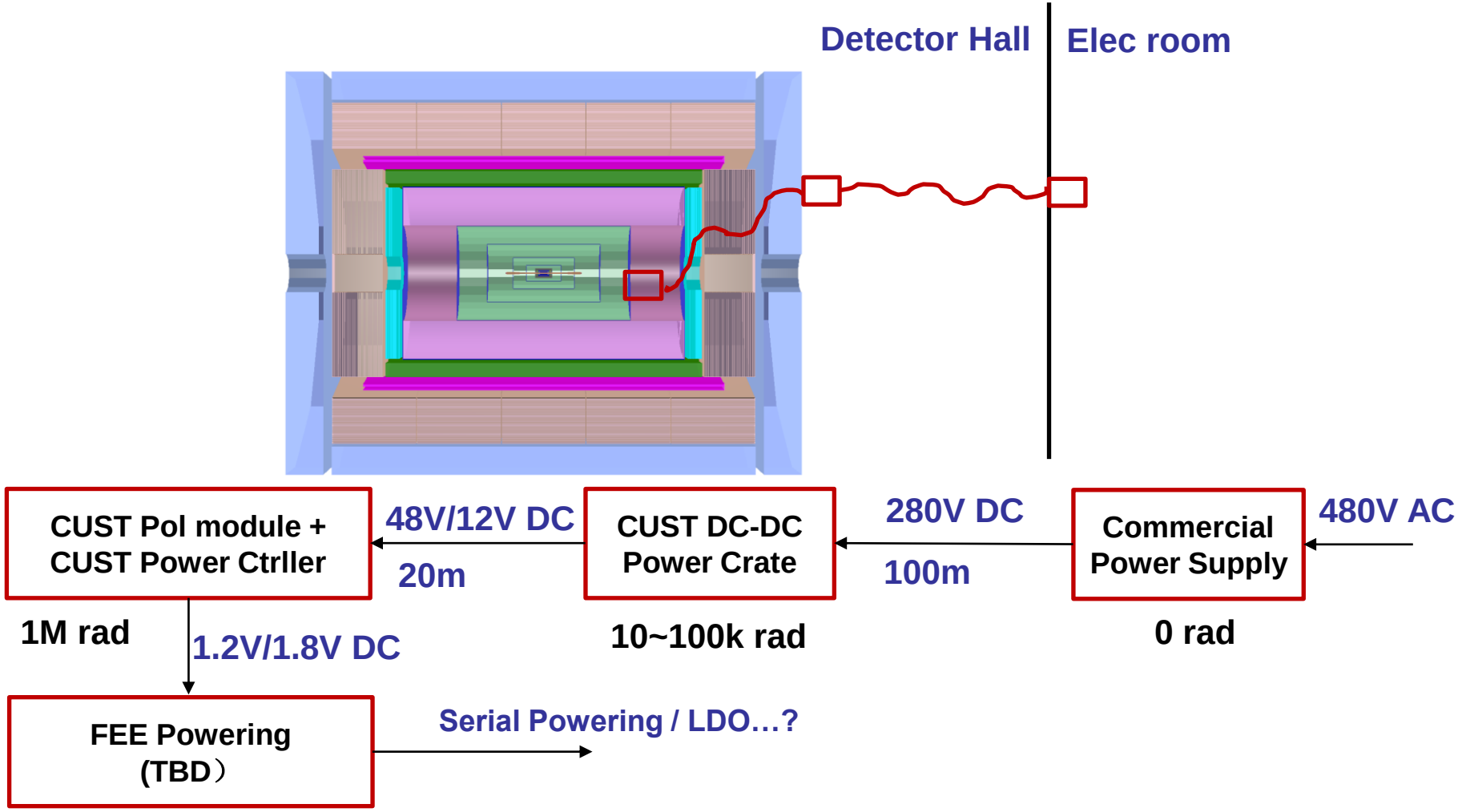


New laboratory



- Proof concept demonstrator with commercial components
  - Muli-channel cross talk test
  - Wireless noise to the detector module
- Develop the core transceiver / driver custom chips for radiation hard

Common framework on Power



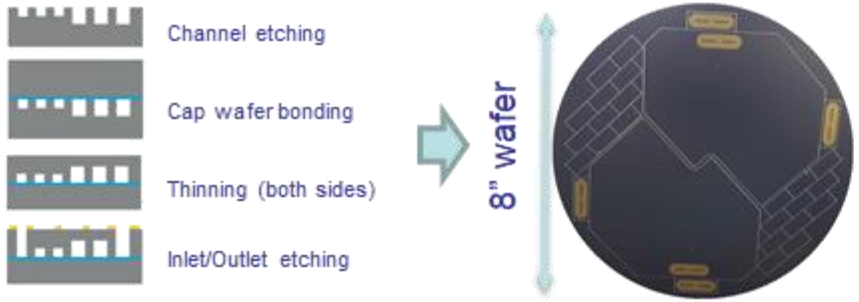
- Propose to develop a rad-hard power module series as the common platform for all sub-det
- Module height & size are constrained from some key detectors (Vertex & CAL)

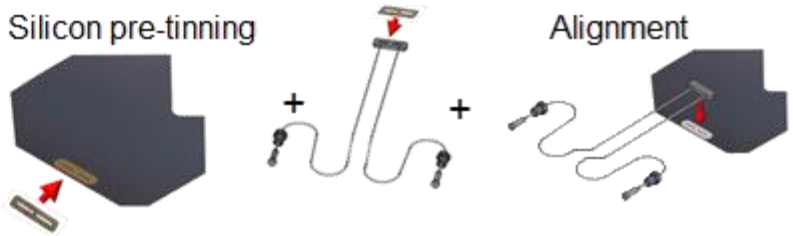
Preliminary consideration on common BEE

	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory(Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

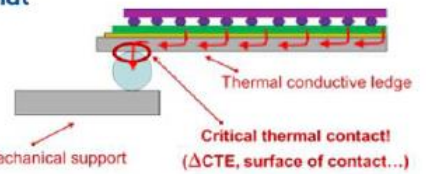
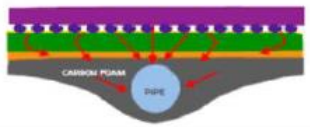
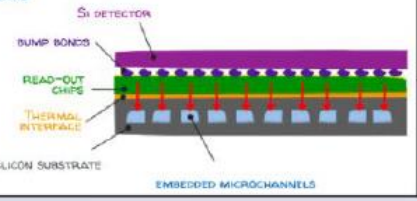
- **A common station for fibers from FEE**
- **Providing data buffers till trigger comes**
- **Possible calculation resource needed for trigger algorithm**
- **Number of IOs, port rate & the cost are the major concerns**

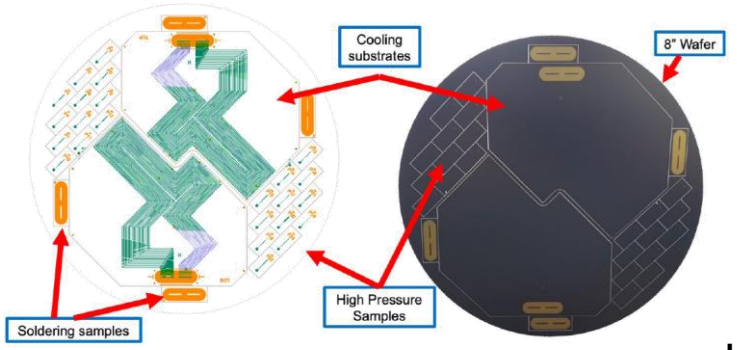
共性技术挑战——功耗及散热

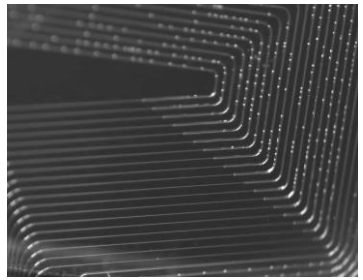




$$TFM = \frac{(\Delta T \text{ fluid - sensor})}{\text{power density}}$$

approach	TFM
conventional 	20
integrated 	12
microchannels 	5-8 liquid 3 bi-phase





Liquid CO_2 flows in μ-Chan

- 海量数据 = 巨额功耗
  - VeloPix @ LHCb: 1W/cm^2
- 先进光源通常还有真空使用的需求
- 必须采用高效散热设计
  - 传统散热方式逐渐无法满足需求——散热新架构
- 微沟道前端水冷散热？

- Paula Collins, The LHCb VELO Upgrade Programme, IHEP Seminar, 2022
- Kazu Akiba, Upgrades of the LHCb Vertex Locator, HSTD 2019

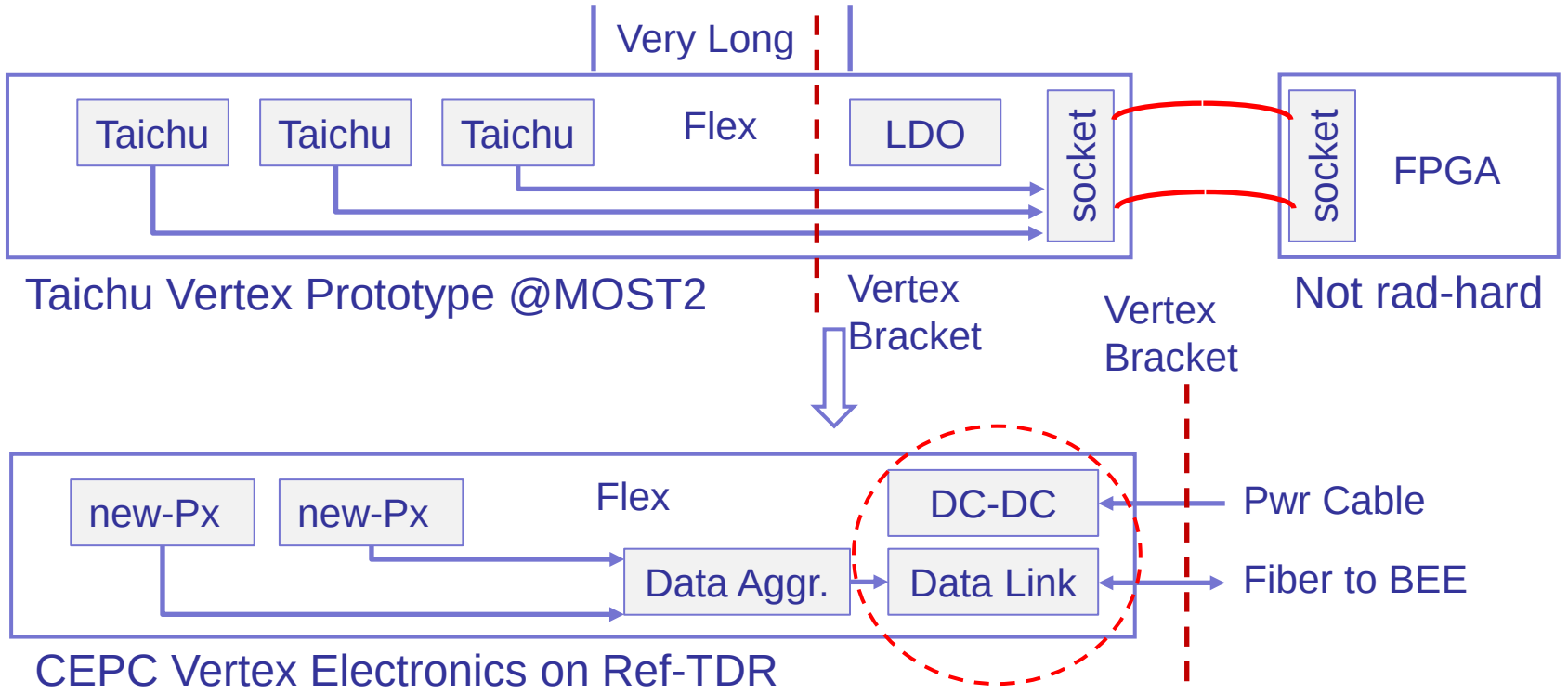
Renew of the detector key requirements

	Vertex	Pix Tracker	TOF	Si Strip	TPC	DC	CAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT
Channels per chip	500k Pixelized	50k Pixelized	128	128	128	-	16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	ADC + TDC / TOT+TOA	Discri.	ADC + BX ID	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC
Main challenge for FEE	• Small pixel size • Fast readout • Low power	• Large area • Cost effective • Low power	• ~50ps timing • Power		• Low power • High density integration	• Ultra fast PA • Ultra fast ADC	• ~10^5 dynamic range • ~400ps timing • Huge channel Low power
Data rate for FEE	1Gbps/chip@ Triggerless Innermost	~30Mbps/chip Innermost	<kHz/chip	<kHz/chip	~70Mbps/module Innermost	~500Mbps/module /a sector	<100MHz/module

- **We are still working on the data rate between the FEE and the BEE, esp. for the endcaps**
- **We aim for a data-stream mode (FEE triggerless) for all subsystems.**
- **We are preparing a review by experts in our field about the electronics and TDAQ.**

Thanks for the inputs from colleagues working on the detector

Elec scheme – Vertex for the CEPC Ref-TDR



- **Trying to be also triggerless readout**
  - **1st step: Triggerless, low power for Low LumiZ for 1st 10y**
  - **2nd step: major upgrade for the ultimate high LumiZ**
- **Stitching technology is proposed to be the baseline scheme**

Specification calculation- from hit density

		Hit density (Hits/cm^2/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm^2)	Hit Pix rate (M Px/cm^2)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	0.017
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	3.6
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

- TDR raw hit density: Higgs 0.54，Z 0.3；Safety factor: TDR 1.5, CDR 10;
- Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)
- Area: 1.28cm*2.56cm=3.27cm^2 (@pixel size 25um*25um)
- Word length: 32bit/event (@Taichu's scale, 512*1024 array)
- Trigger rate：20kHz@CDR，120kHz@Z, 10Hz@Higgs, 2kHz@W TDR
  - Trigger latency: 3us(very likely not enough), Error window: 7 bins
  - FIFO depth: @3us * hit rate/chip
  - Data rate=pixel/bunch*trigger rate*32bit*error window